Qualcomm Technologies, Inc.

MSM8909/MSM8209/MSM8208/MSM8905 (SDM205)

Device Specification

80-NP408-1 Rev. N

May 11, 2018

For additional information or to submit technical questions go to https://createpoint.qti.qualcomm.com

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Revision history

Revision	Date	Description
A	August 2014	Initial release
B	October 2014	■ Global: □ Updated the chipset configuration support from WTR2955 to WTR4905 □ Added MSM8209 variant and related information ■ Updated Table 1-2: □ Updated the display resolution support to 720p HD (MSM8909) and qHD (MSM8208) ■ Updated Table 1-3: □ Updated the display resolution support to 720p HD (MSM8909) and qHD (MSM8208) □ Updated the graphics performance (up to 400MHz) for MSM8909 ■ Updated Table 2-12: □ Added pin U25 and associated details ■ Added Section 3.3: □ PDN maximum impedance specification added ■ Updated Chapter 4: □ Corrected Figure 4-1 to remove pin G22 □ Added device part marking information and the device identification code details in Section 4.2
C	January 2015	■ Global: Added support for PM8916-1 and QFE4301/QFE4303/BST3215/BST3218 and WCN3660B ■ Updated Table 1-1: □ Updated title of Software Interface document to Hardware Register Description document for OEMs. □ Updated titles of MSM8909/MSM8209/MSM8208 Pin Assignment Spreadsheet and MSM8909/MSM8209/MSM8208 GPIO Configuration Spreadsheet to include APQ8009. □ Updated the DCN for Chipset Layout Guidelines document. ■ Updated Table 2-10: □ Updated pad characteristics for GPIO_93. ■ Updated Section 3.3, Power delivery network specification □ In Table 3-5 updated the lumped VDD_CORE + VDD_APC PDN specification to separate PDN specification for VDD_CORE and VDD_APC. □ In Table 3-6 updated the PDN specification for VDD_P1. ■ Added Section 3.6, Digital-logic characteristics ■ Updated Table 4-1: □ Updated assembly site code

Revision	Date	Description
C (cont.)	January 2015	■ Added Table 4-2, QFPROM_CORR_JTAG_ID_LSB register definition for FEATURE_ID and JTAG_ID ■ Updated Section 4.3: □ Updated Table 4-3 with ES2 sample and device identification code information
D	March 2015	■ Global: Added MSM8609 variant and PM8208 related information ■ Table 1-3, Summary of MSM8x0x features: Updated details for 4-lane MIPI CSI support ■ Table 2-3, Pin descriptions – multimedia functions: Updated pin mapping details for 4-lane MIPI CSI support ■ Chapter 3, Electrical Specifications: Added the following sections: □ Section 3.1, Absolute maximum ratings □ Section 3.2, Operating conditions □ Section 3.4, DC power characteristics □ Section 3.5, Power sequencing □ Section 3.7, Timing characteristics to Section 3.12, RF and power management interfaces □ Updated PDN spec for VDD_P1 in Table 3-6, Power distribution network impedance vs. frequency ■ Updated MSM8609 variant details, date code and CS information in Table 4-3, Device identification code details. ■ Added Section 4.4, Device moisture-sensitivity level and Section 4.5, Thermal characteristics ■ Added the following chapters: □ Chapter 5, Carrier, Storage, & Handling Information □ Chapter 6, PCB Mounting Guidelines □ Chapter 7, Part Reliability
E	May 2015	■ Updated APC and GPU frequencies for MSM8909-AA variants in Table 1-3, Summary of MSM8x0x features ■ Added Section 3.4.2, Dhrystone and rock bottom maximum power ■ Updated Section 3.12.1, RF front-end (RFFE): □ Added Figure 3-18, Clock driver output waveform □ Added footnotes for Table 3-32, RFFE data □ Added Figure 3-19, Setup and hold timing waveform □ Added Figure 3-20, Tx data output delay with respect to rising edge of clock ■ Updated MSM8909-AA variant details in Table 4-3, Device identification code details ■ Added an example for MSM8909-AA variant in Figure 4-3, Device identification code ■ Figure 5-1, Carrier tape drawing with part orientation Updated orientation of individual parts as laid out on carrier tape ■ Updated the link to board level reliability 504 NSP (BR80-NP526-1) in Section 6.4, Board-level reliability ■ Added reliability data from Global Foundry in Section 7.1.2, MSM8x0x reliability evaluation report for device from GF

Revision	Date	Description
F	June 2015	■ Table 1-1, Primary MSM8x0x documentation: Updated the document title of 80-NP408-2x ■ Section 3.3.1, PDN specification (PCB only): Updated text to emphasize that given PDN spec is applicable for all MSM8x0x variants. ■ Table 3-7, Dhrystone and rock bottom power specifications: Added Dhrystone and rock bottom power specification for 1.267 GHz part. ■ Table 3-35, Supported SPMI standards and exceptions: Removed max specification for setup and hold time. ■ Figure 4-2, MSM8x0x device marking (top view, not to scale) and Table 4-1, MSM8x0x device marking line definitions: Replaced “Additional line” with “Line E” in the part marking diagram and part marking table.
G	August 2015	■ Table 4-3 (Device identification code details): □ Added CS date code information for MSM8909-AA variants □ Added note for service key provisioning support ■ Section 5.4, Barcode label and packing for shipment: Added identification details for MSM parts supporting service key provisioning.
H	November 2015	■ Global: □ Updated the exact Fmax for ARM Cortex A7 core. □ Removed MSM8609 variant information. ■ Table 4-3, Device identification code details: Removed MSM8909-3-VV, MSM8909-3-AA, and MSM8609-0-VV variants.
J	January 2016	■ Table 4-1, MSM8x0x device marking line definitions: Added SMIC fab information. ■ Table 4-4, Source configuration codes – MSM8909/MSM8209/MSM8208: Added SMIC information. ■ Section 5.4, Barcode label and packing for shipment: Modified details on service key provisioning support. ■ Section 7.1.3, MSM8x0x reliability evaluation report for device from SMIC: Added new section for SMIC fab information. ■ Section 7.2, Qualification sample description: Added SMIC fab information.
K	January 2017	■ Global: □ Updated the document with the MSM8905 (SDM205) – feature phone variant information □ Updated the Qualcomm CreatePoint references throughout the document ■ Section 1.2, MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) introduction: Updated with the MSM8905 feature information ■ Figure 1-1, MSM8909/MSM8209/MSM8208 functional block diagram and example application: Removed the NFC block from the figure since QCA1990 is now obsolete ■ Figure 1-2, MSM8905 functional block diagram and example application: Added a block diagram for MSM8905 ■ Table 1-2, MSM8x0x variants: Added information for the MSM8905 chipset ■ Section 1.3.2, Summary of MSM8905 features: Added a new table with MSM8905 features ■ Figure 4-3, Device identification code details: Updated the table with MSM8905 variant information

Revision	Date	Description
L	December 2017	Table 4-3 Device identification code details: Updated the device identification code details for p code value = 3
M	February 2018	■ Table 2-4 Pin descriptions – connectivity functions: □ Updated the Audio MI2S interface #1 to Audio speaker I2S interface □ Updated the functional description for the pins AA28, AA29, Y28, Y29, W28, J26, J27, J28, J29, and AD28 □ Changed the pin type to DO for AA28, AA29, J26, and J29 □ Updated the functional description for the pins AF28 and AE27 ■ Table 2-10 Pin descriptions – general-purpose input/output ports □ Updated the configurable functions information for the range GPIO_59 to GPIO_63 and GPIO_94 to GPIO_96, & also for GPIO_98 and GPIO_110 □ Changed the pad characteristics type as DO for GPIO_62, GPIO_63, GPIO_95, and GPIO_96
N	May 2018	■ Section 3.3.1 MSM8x0x PDN specification (PCB only) except MSM8905: Updated the title ■ Section 3.3.2 MSM8905 PDN Specification (PCB only): Added new section for MSM8905 PDN Specification ■ Table 1-4 *Summary of MSM8905 features:* Updated the value from 1.094 GHz to 1.267 GHz for Application processor. ■ Table 4-3 *Device identification code details:* Added MSM8905 (SDM205) variant and related information.

1 Introduction

1.1 Documentation overview

This device specification defines MSM™ devices, MSM8909, MSM8209, and MSM8208 and the MSM8905 (SDM205) device. Throughout this document, the devices are referred to as the MSM8x0x when material presented applies to all of them. The main differences between the variants are their supported air interface standards, microprocessor (dual or quad core), and multimedia capabilities, as summarized in Section 1.2.1.

Technical information for these devices is primarily covered by the documents listed in Table 1-1. All documents should be studied for a thorough understanding of the device and its applications. Released MSM8x0x documents are available for download at createpoint.qti.qualcomm.com.

Table 1-1 Primary MSM8x0x documentation

Document number	Title/description
80-NP408-1 (this document)	*MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) Device Specification* Provides all MSM8x0x electrical specifications and mechanical information. Additional material includes pin assignments; shipping, storage, and handling instructions; Printed circuit board (PCB) mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-NP408-1A	*MSM8909/MSM8209/MSM8208/APQ8009/MSM8905 (SDM205) Pin Assignment Spreadsheet* A Microsoft Excel spreadsheet listing all MSM8x0x pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions. This information can be used to help build the IC's CAD library symbol, or for quick reference for a particular pad's functional assignment.
80-NP408-1B	*MSM8909/MSM8209/MSM8208/APQ8009/MSM8905 (SDM205) GPIO Configuration Spreadsheet* A Microsoft Excel spreadsheet listing all MSM8x0x GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations. This information can be used to help designers define their products' GPIO assignments.
80-NP408-2X	*MSM8909/MSM8609/MSM8209/MSM8208/APQ8009 Hardware Register Description Document for OEMs* Provides detailed information about the MSM8x0x software interface and its clocks, security, user interface, and registers.
80-NP408-3A	*MSM8909/MSM8905 (SDM205) Chipset Layout Guidelines* ■ Key layout guidelines for the chipset are illustrated and explained.
80-NP408-4	*MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) Device Revision Guide* Provides a history of MSM8x0x revisions, explains how to identify the various device revisions, and discusses known issues (or bugs) for each revision and how to work around them.

Table 1-1 Primary MSM8x0x documentation (cont.)

Document number	Title/description
80-NP408-5B	*MSM8909/MSM8609/MSM8209/MSM8208/APQ8009/MSM8905 (SDM205) Digital Baseband Design Guidelines/Training Slides* ■ Detailed descriptions of MSM8x0x functions ■ Detailed interface descriptions for the MSM™ in various applications ■ Key design guidelines for the chipset are illustrated and explained, including: □ Technology overviews □ DC power distribution □ Interface schematic details □ PCB layout guidelines □ External-component recommendations □ Ground and shielding recommendations

This document is organized as follows:

Chapter 1 Provides an overview of the MSM8x0x documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical performance specifications, including absolute maximum ratings and operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of the MSM8x0x.

Chapter 6 Presents procedures and specifications for mounting the MSM8x0x onto PCBs.

Chapter 7 Presents MSM8x0x reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) introduction

The MSM8x0x (Figure 1-1) maintains the mobile device features while drastically reducing cost and board space. Its ARM Cortex-A7 application processors helps expand mass-market chipset capabilities by making 3G and 4G high-speed data and rich multimedia features accessible to more consumers worldwide.

This multimode solution supports the latest air interface standards including 1xEV-DOrA, 1x Advanced, DC-HSPA+, TD-SCDMA, and LTE, plus dual SIM dual standby (DSDS) and Single Radio LTE (SRLTE) operation.

The MSM8905 (SDM205) variant, designed for 4G enabled feature phones, supports DC-HSPA+, and LTE, plus dual SIM dual standby (DSDS) and Single Radio LTE (SRLTE) operation.

The MSM8x0x leverages Qualcomm Technologies, Inc. (QTI) airlink and multimedia technology leadership to significantly lower the cost of high-performance mobile devices.

The MSM8x0x has a high level of integration that reduces the bill-of-material (BOM) and board area. The cost and time-to-market advantages of this IC will help drive wireless broadband adoption in mass markets around the world.

Wireless products based on the MSM8x0x may include:

- Voice and data phones (smartphones and feature phones)
- Music player-enabled devices and applications
- Camera phones
- Multimedia phones with gaming, streaming video, and videoconferencing features
- GPS, Galileo, GLONASS, and BeiDou for global location-based service
- Wireless connectivity – Bluetooth, WLAN, and FM receiver

The MSM8x0x benefits are applied to each of these product types and include:

- Higher integration to reduce PCB surface area, time-to-market, and BOM costs while adding capabilities and processing power
- Integrated application processors and hardware cores eliminate multimedia coprocessors, providing superior image quality and resolution for mobile devices while extending application times
  - Higher computing power for high-end applications, and DC power savings for longer run times
- Position location and navigation systems are supported via the WTR's global navigation satellite system (GNSS) receiver
  - The MSM8x0x supports Gen 8C operation
- Single platform that provides dedicated support for all market-leading codecs and other multimedia formats to support carrier deployments around the world
- DC power reduction using innovative techniques

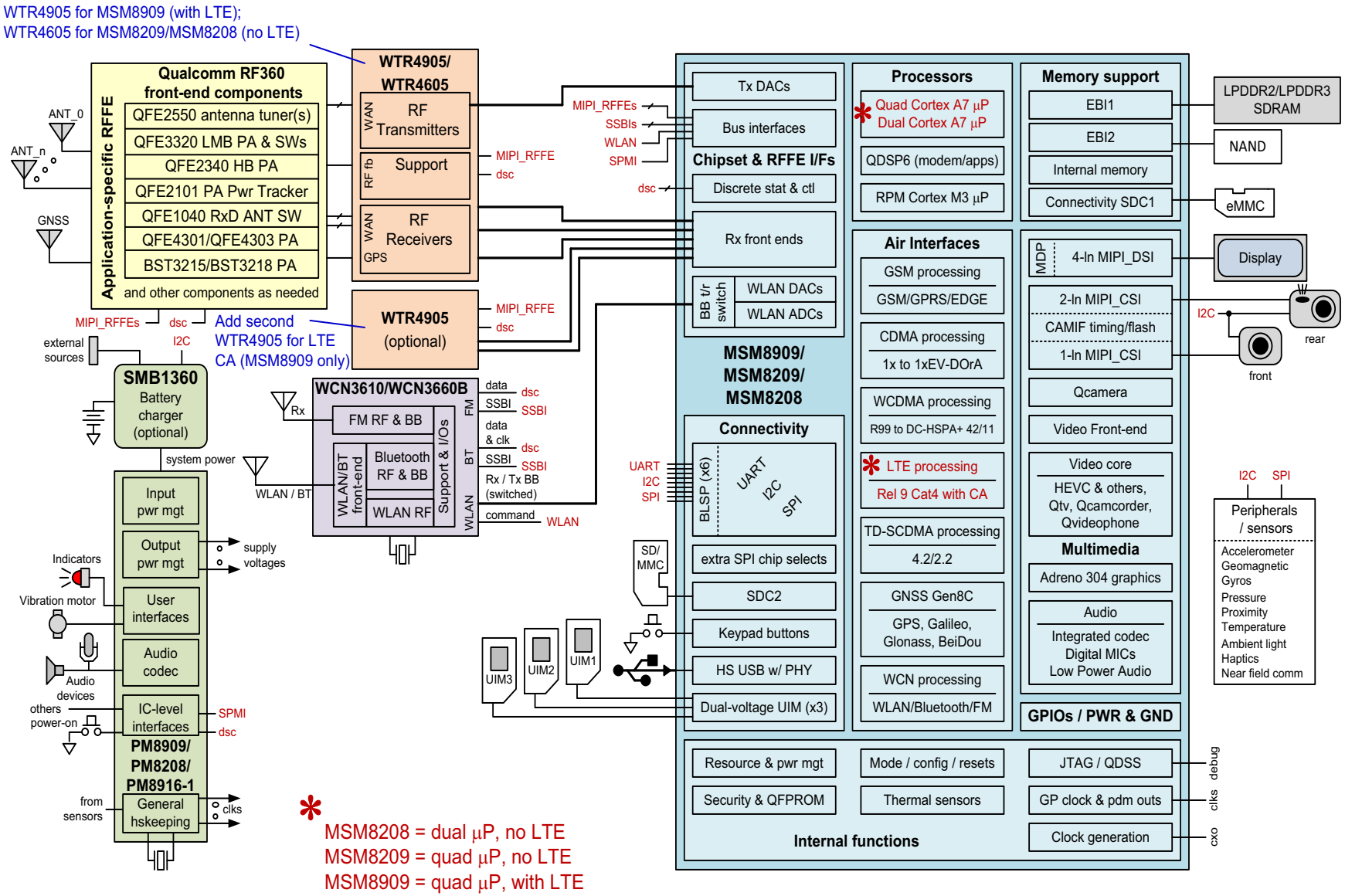


Figure 1-1 MSM8909/MSM8209/MSM8208 functional block diagram and example application

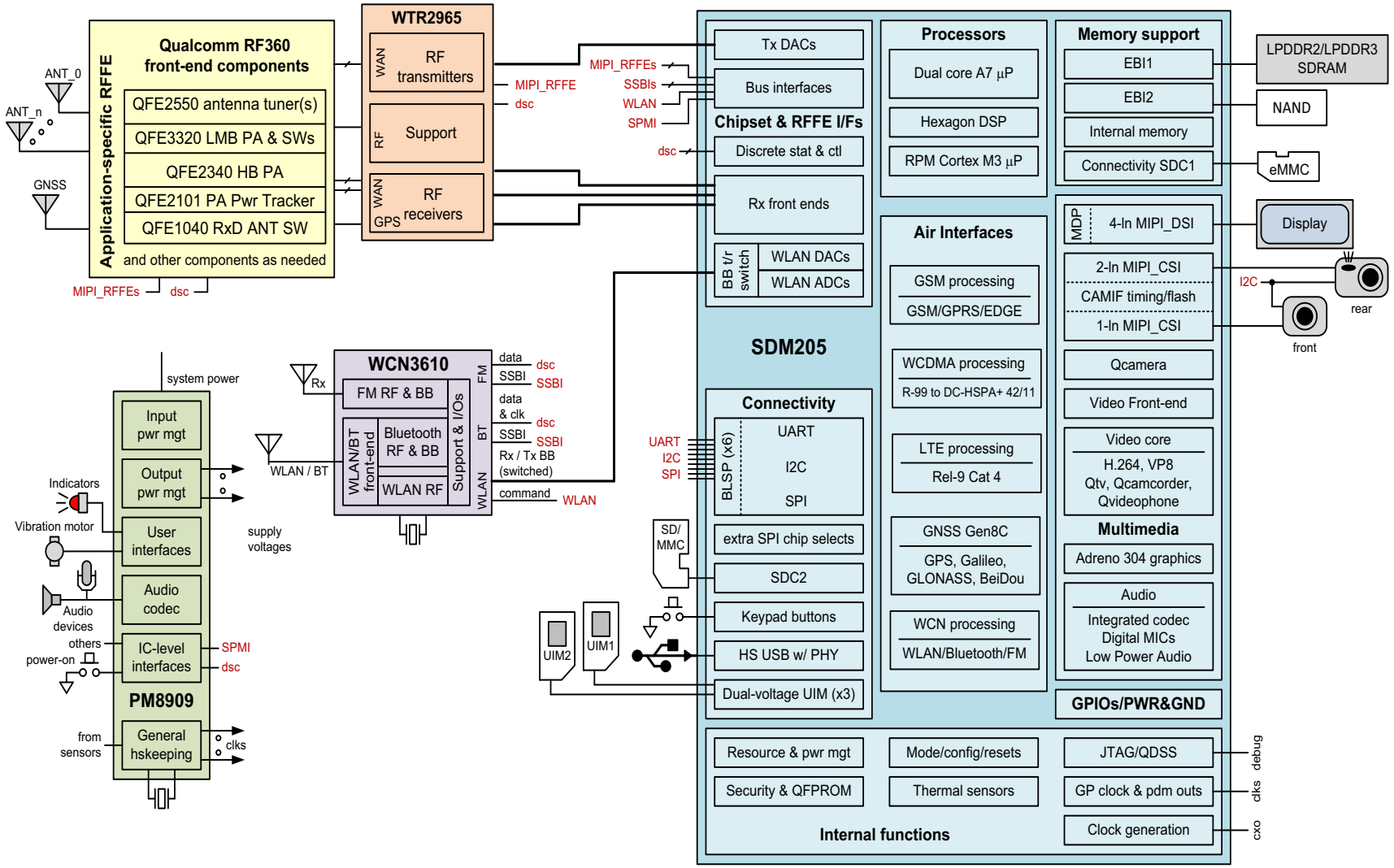


Figure 1-2 MSM8905 functional block diagram and example application

The MSM8x0x is fabricated using the advanced 28 nm LP CMOS process, and is available in the 504 NSP; 11.1 × 12.0 × 0.96 mm package with many ground pins for improved electrical grounding, mechanical strength, and thermal continuity.

The MSM8909/MSM8209/MSM8208 supports high-performance applications worldwide using various wireless networks:

- GSM/GPRS/EDGE
- CDMA2000 1X, 1x Advanced, and 1xEV-DOrA
- WCDMA Rel-99 to Rel-9 DC-HSPA+ (42 Mbps)
- TD-SCDMA with 4.2 Mbps DL and 2.2 Mbps UL option
- LTE Cat 4, including 2 × 10 MHz carrier aggregation (MSM8909 only, two WTR4905 ICs)

Complementary ICs within the MSM8909/MSM8209/MSM8208 chipset include:

- Power management:
  - PM8909 (80-NP409-x documents) or
  - PM8916-1 (80-NK808-x documents)
- Wafer-level RFIC
  - WTR4905/WTR4605 (80-NL713-x documents)
- RF front-end ICs:
  - QFE2550 antenna tuner IC (80-NL733-x documents)
  - QFE3320 LMB PA IC (80-NJ121-x documents)
  - QFE2340 HB PA IC (80-NF232-x documents)
  - QFE1040 RxD antenna switch IC (80-NJ120-x documents)
  - QFE2101 PA power tracker IC (80-NL893-x documents)
  - QFE4301/QFE4303 PA IC (80-NT565-x/80-NT566-x documents)
  - BST3215/BST3218 PA IC (80-NT032-x/80-NT033-x documents)
- Wireless connectivity: WCN3610/WCN3660B for WLAN, Bluetooth, and FM (80-WL008-x/80-WL007-x documents)

MSM8905 features

- GSM/GPRS/EDGE
- WCDMA Rel-99 to Rel-9 DC-HSPA+ (42 Mbps)
- LTE Cat 4 (paired with WTR2965 IC)

Complementary ICs within theMSM8905 chipset include:

- Power management:
  - PM8909 (80-NP409-x documents)
- Wafer-level RFIC
  - WTR2965 (80-NP237-x documents)
- RF front-end ICs:
  - QFE2550 antenna tuner IC (80-NL733-x documents)
  - QFE3320 LMB PA IC (80-NJ121-x documents)
  - QFE2340 HB PA IC (80-NF232-x documents)
  - QFE1040 RxD antenna switch IC (80-NJ120-x documents)
  - QFE2101 PA power tracker IC (80-NL893-x documents)
- Wireless connectivity: WCN3610 for WLAN, Bluetooth, and FM (80-WL008-x documents)

The MSM8x0x chipset and system software solution supports the Convergence Platform for mobile applications by leveraging QTI's years of systems expertise and field experience with CDMA, WCDMA, GSM, TD-SCDMA, LTE, and GNSS technologies. QTI works with its partners to develop products that meet the exact needs of the growing wireless market, providing its customers with complete, verifiable solutions, including fully segmented product families, systems software, testing, and support.

Since the MSM8x0x includes so many diverse functions, its operation is more easily understood by considering major functional blocks individually. Therefore, the MSM8x0x document set is organized according to the following block partitioning:

- Architecture and baseband processors
- Memory support
- Air interfaces
- Multimedia
- Connectivity
- Internal functions
- Interfaces to other functions (including the other ICs within the chipset)
- Configurable general-purpose input/output (GPIO) ports

Most of the information contained in this device specification is organized accordingly – including the circuit groupings within its functional block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3).

1.2.1 Device variants

The differences between MSM8x0x variants are summarized in Table 1-2.

Table 1-2 MSM8x0x variants

Device	Supported airlink technologies					A7 μP core	Multimedia		
	GSM	WCDMA	TD-SCDMA	LTE	CDMA		Camera	Video decode	Display
MSM8909	to EDGE	to DC-HSPA+	4.2/2.2 Mbps	to Cat 4 with CA	to DOrA	quad	8 MP	1080p	HD (720p)
MSM8209	to EDGE	to DC-HSPA+	4.2/2.2 Mbps	—	—	quad	8 MP	1080p	HD (720p)
MSM8208	to EDGE	to DC-HSPA+	4.2/2.2 Mbps	—	—	dual	5 MP	720p	qHD
MSM8905	to EDGE	to DC-HSPA+	—	to Cat 4	—	dual	3 MP (with 512 MB) 2 MP (with 256 MB)	720p	VGA (with 512 MB) QVGA (with 256 MB)

1.3 MSM8x0x features

NOTE: Some of the hardware features integrated within the MSM8x0x must be enabled by software. To identify the enabled MSM8x0x features, refer to the latest version of the applicable software release notes.

1.3.1 Summary of MSM8909/MSM8209/MSM8208 features

Table 1-3 Summary of MSM8909/MSM8209/MSM8208 features

Feature	MSM8909/MSM8209/MSM8208 capability
Processors	
Applications	ARM Cortex-A7 microprocessor [operating at a maximum frequency of 1.094 GHz or 1.267 GHz (-AA variants)]. ■ 32-bit processor, 512 kB L2 cache ■ Multiple cores □ Quad core ~ MSM8209/MSM8909 □ Dual core ~ MSM8208 ■ Primary boot processor
Modem system	Q6 v5 core at up to 691.2 MHz ■ 768 kB L2 caches ■ See Table 1-2 for supported airlink technologies, and Section 1.3.3 for performance details. ■ Advanced techniques □ Dual SIM dual standby (DSDS) □ Support for Single Radio LTE (SRLTE) ~ MSM8909 only □ LTE 2 x 10 MHz carrier aggregation (CA) ~ MSM8909 only

Table 1-3 Summary of MSM8909/MSM8209/MSM8208 features (cont.)

Feature	MSM8909/MSM8209/MSM8208 capability
RPM system	Cortex M3 MPM coordinates shutdown/wakeup, clock rates, and VDDs
Memory support	
System memory via EBI1	Non-PoP LPDDR2, LPDDR3 SDRAM; 32-bit wide; up to 533 MHz (MSM8909/MSM8209); up to 400 MHz (MSM8208)
Flash memory via EBI2	8-bit NAND interface
Graphics internal memory	96 kB unified SRAM pool on-chip memory (GMEM)
External memory via SDC1	eMMC v4.5/SD flash devices
RF support	
RF operating bands	As defined by QFE and WTR device support
WAN air interfaces GSM CDMA WCDMA TD-SCDMA LTE	See summary in Table 1-2 and details in Section 1.3.3. Yes Yes ~ MSM8909 Yes Yes Yes ~ MSM8909 only
GNSS – Qualcomm® IZat™ engine	Gen 8C; support for three bands ***concurrently***: ■ GPS, Beidou, and **GLONASS** or ■ GPS, Beidou, and **Galileo**
Multimedia	
Display interfaces Resolution MIPI_DSI	 HD (720p) at 60 fps ~ MSM8909/MSM8209 qHD(960 x 540) at 60 fps ~ MSM8208 four lanes, 1.5 Gbps each
Camera interfaces Resolution Number of CSIs CSI configurations Configurations supported General camera features	Qcamera 8 MP ~ MSM8909/MSM8209 5 MP ~ MSM8208 Two; 1.5 Gbps per lane 2-lane rear camera and 1-lane front camera or 4-lane rear camera only (secondary camera not supported) Pixel manipulations, camera modes, image effects, and postprocessing techniques, including defective pixel correction I^2C controls
Mobile display processor	MDP 3.05 for display processing

Table 1-3 Summary of MSM8909/MSM8209/MSM8208 features (cont.)

Feature	MSM8909/MSM8209/MSM8208 capability
Video applications performance	
Encode	H.264 BP/MP – 720p, 30 fps MPEG-4 SP / H.263 P0 – WVGA, 30 fps VP8 – WVGA, 30 fps
Decode □ RES = 1080p ~ MSM8909/MSM8209 □ RES = 720p ~ MSM8208	H.264 BP/MP/HP – RES, 30 fps MPEG-4 SP/ASP – RES, 30 fps DivX 4x/5x/6x – RES, 30 fps H.263 P0 – WVGA, 30 fps VP8 – RES, 30 fps (HEVC) H.265 MP 8-bit – RES, 30 fps
Graphics	Qualcomm® Adreno™ 304; 3D graphics accelerator Up to 456 MHz ~ MSM8909 -AA variants Up to 409.6 MHz ~ MSM8909/MSM8209 Up to 307.2 MHz ~ MSM8208
Audio Low-power audio Voice codec support Audio codec support Enhanced audio Synthesizer	PM8909/PM8208/PM8916-1 audio required Low-power audio for MP3 and AAC playback; surround sound Versatile – many audio playback & voice modes; encoders for audio & FM recording; many concurrency modes G711; raw PCM; QCELP; EVRC, EVRC-B, EVRC-WB; AMR-NB, AMR-WB; GSM-EFR, GSM-FR, GSM-HR MP3; aacPlus, eAAC; AMR-NB, AMR-WB, G.711, WMA 9/10 Pro Dolby Digital Plus and DTS-HD surround sound Fluence™ Noise Cancellation QAudioFX™/Qconcert™/QEnsemble 128-voice polyphony wavetable
Web technologies	V8 JavaScript Engine optimizations WebKit browser JPEG hardware decode acceleration Networking Stack IP and HTTP tuning Flash 10.x & video processor decode optimization
Messaging	Text messages; text encoding for SMS Multimedia messaging services – combined video (MPEG-4), still image (JPEG), voice tag (AMR), text sent as message
Connectivity	
BLSP ports UART I^2C SPI (master only)	Six BLSP ports, 4-bits each; multiplexed serial interface functions Yes – up to 4 Mbps Yes – cameras, sensors, near field communicator (NFC), SMB charger, and so on Yes – cameras, sensors, and so on
UIM	Three ports – dual voltage (1.8 V/2.85 V)
USB	One USB 2.0 high speed
Secure digital interfaces	Up to two ports, both dual-voltage One 8-bit and one 4-bit SD 3.0; SD/MMC card; eMMC v4.5

Table 1-3 Summary of MSM8909/MSM8209/MSM8208 features (cont.)

Feature	MSM8909/MSM8209/MSM8208 capability
Wireless connectivity	With WCN3610/WCN3660B
WLAN	802.11 b/g/n for WCN3610
	802.11 a/b/g/n for WCN3660B
Bluetooth	Bluetooth 4.0 LE and earlier
FM radio	Rx only
NFC	QCA1990
Touchscreen support	Capacitive panels via external IC (I^2C, SPI, & interrupts)
Audio interfaces	
DMIC	One port for digital mic application
MI^2S	Up to two ports (primary and secondary ports)
CDC PDM port	Interface between MSM8x0x and PM8909/PM8208/PM8916-1 for analog transducer I/Os
Configurable GPIOs	
Number of GPIO ports	113 GPIOs – GPIO_0 to GPIO_112
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
Secure boot	ROM based or eFuses based tamper-proof root of trust
	Multiple root certificates
Secure debug	Software unlock using chip-unique certificate
Hardware crypto engine	General-purpose crypto engine in hardware
	Hardware Random number generator
QFPROM eFuses	Available OTP bits for OEM use in QFPROM
Secure Execution Environment	Based on ARM TrustZone
	Includes secure memory and secure file system
PLLs and clocks	Multiple clock regimes; watchdog & sleep timers
	19.2 MHz CXO master clock input
	General-purpose outputs: M/N counter, PDM
Resource and power manager	Fundamental to power management
	Key blocks: RPM core, Cortex M3, security controller, MPM
	Improved efficiency via clock control, split-rail power collapse & voltage scaling; several low-power sleep modes
Debug	JTAG, QDSS
Others	Thermal sensors; modes & resets; peripheral subsystem

Table 1-3 Summary of MSM8909/MSM8209/MSM8208 features (cont.)

Feature	MSM8909/MSM8209/MSM8208 capability
Chipset and RF front-end (RFFE) interface features	
WTR RFICs	WTR4905 (one or two, MSM8909 only); WTR4605 (one, MSM8209/MSM8208)
WAN baseband data GNSS baseband data Status & control	Four Rx (CH0, CH1, CH2, CH3) & One Tx (DAC0) analog interfaces Rx (GNSS) analog interface MIPI_RFFEs and discrete signals as needed via GPIOs
Power management	PM8909/PM8208/PM8916-1 2-line SPMI; dedicated clock & reset lines; plus other GPIOs as needed
WCN wireless connectivity WLAN baseband data WLAN status & control Bluetooth FM radio	WCN3610/WCN3660B Multiplexed Rx/Tx analog interface Proprietary 5-line interface 2-line data interface plus SSBI 1-line data interface plus SSBI
Near field communicator	Via QCA1990; I^2C plus other GPIOs as needed
Qualcomm RF360™ QFE devices	MIPI_RFFEs
Power amplifiers & RF switches	MIPI_RFFEs and discrete control lines
Fabrication technology and package	
Digital die	28 nm LP CMOS
Small, thermally efficient package	504 NSP: 11.1 × 12.0 × 0.96 mm; 0.4 mm pitch

1.3.2 Summary of MSM8905 features

Table 1-4 Summary of MSM8905 features

Feature	MSM8905 capability
Processors	
Applications	ARM Cortex-A7 microprocessor (operating at a maximum frequency of 1.267 GHz). ■ 32-bit processor, 512 KB L2 cache ■ Dual core ■ Primary boot processor
Modem system	Q6 v5 core at up to 691.2 MHz ■ 768 kB L2 caches ■ See Table 1-2 for supported airlink technologies, and Section 1.3.3 for performance details. ■ Advanced techniques □ Dual SIM dual standby (DSDS) □ LTE
RPM system	Cortex M3 MPM coordinates shutdown/wakeup, clock rates, and VDDs
Memory support	
System memory via EBI1	Non-PoP LPDDR2, LPDDR3 SDRAM; 32-bit wide; up to 384 MHz
Flash memory via EBI2	8-bit NAND interface
Graphics internal memory	96 kB unified SRAM pool on-chip memory (GMEM)
External memory via SDC1	eMMC v4.5/SD flash devices
RF support	
RF operating bands	As defined by QFE and WTR device support
WAN air interfaces GSM WCDMA LTE	See summary in Table 1-2 and details in Section 1.3.3. Yes Yes Yes
GNSS – Qualcomm® IZat™ engine	Gen 8C Lite; support for three bands ***concurrently***: ■ GPS, Beidou, and **GLONASS** or ■ GPS, Beidou, and **Galileo**
Multimedia	
Display interfaces Resolution MIPI_DSI	 VGA (with 512 MB) and QVGA (with 256 MB) Four lanes, 1.5 Gbps each
Camera interfaces Resolution Number of CSIs CSI configurations Configurations supported General camera features	Qcamera 3 MP (with 512 MB) and 2 MP (with 256 MB) Two; 1.5 Gbps per lane 2-lane rear camera and 1-lane front camera Pixel manipulations, camera modes, image effects, and postprocessing techniques, including defective pixel correction I^2C controls

Table 1-4 Summary of MSM8905 features (cont.)

Feature	MSM8905 capability
Mobile display processor	MDP 3.05 for display processing
Video applications performance	
Encode	H.264 BP/MP – 480p, 30 fps
	VP8 – 480p, 30 fps
	H.264 BP/MP/HP – 720p, 30 fps
Decode	VP8 – 720p, 30 fps
Graphics	Adreno 304; 3D graphics accelerator
	Up to 307.2 MHz
Audio	PM8909 audio required
Low-power audio	Low-power audio for mp3 and AAC playback; surround sound
Voice codec support	Versatile – many audio playback and voice modes; encoders for audio & FM recording; many concurrency modes
Audio codec support	G711; raw PCM; QCELP; EVRC, EVRC-B, EVRC-WB; AMR-NB, AMR-WB; GSM-EFR, GSM-FR, GSM-HR
Enhanced audio	MP3; aacPlus, eAAC; AMR-NB, AMR-WB, G.711, WMA 9/10 Pro
Synthesizer	Dolby Digital Plus and DTS-HD surround sound
	Fluence noise cancellation
	QAudioFX/Qconcert/QEnsemble
	128-voice polyphony wavetable
Web technologies	V8 JavaScript Engine optimizations
	WebKit browser JPEG hardware decode acceleration
	Networking Stack IP and HTTP tuning
	Flash 10.x and video processor decode optimization
Messaging	Text messages; text encoding for SMS
	Multimedia messaging services – combined video (MPEG-4), still image (JPEG), voice tag (AMR), and text sent as message
Connectivity	
BLSP ports	Six BLSP ports, 4-bits each; multiplexed serial interface functions
UART	Yes
I^2C	Yes
SPI (master only)	Yes
UIM	Three ports – dual voltage (1.8 V/2.85 V)
USB	One USB 2.0 high-speed
Secure digital interfaces	Up to two ports, both dual-voltage
	One 8-bit and one 4-bit
	SD 3.0; SD/MMC card; eMMC v4.5
Wireless connectivity	With WCN3610
WLAN	802.11 b/g/n
Bluetooth	Bluetooth 4.1 LE and earlier
FM radio	Rx only

Table 1-4 Summary of MSM8905 features (cont.)

Feature	MSM8905 capability
Audio interfaces	
DMIC	One port for digital mic application
MI^{2}S	Up to two ports (primary and secondary ports)
CDC PDM port	Interface between MSM8905 and PM8909 for analog transducer I/Os
Configurable GPIOs	
Number of GPIO ports	113 GPIOs – GPIO_0 to GPIO_112
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security	
Secure boot	ROM based or eFuses based tamper-proof root of trust
	Multiple root certificates
Secure debug	Software unlock using chip-unique certificate
Hardware crypto engine	General-purpose crypto engine in hardware
	Hardware Random number generator
QFPROM eFuses	Available OTP bits for OEM use in QFPROM
Qualcomm® Secure Execution Environment	Based on ARM TrustZone
	Includes secure memory and secure file system
PLLs and clocks	Multiple clock regimes; watchdog & sleep timers
	19.2 MHz CXO master clock input
	General-purpose outputs: M/N counter and PDM
Resource and power manager	Fundamental to power management
	Key blocks: RPM core, Cortex M3, security controller, MPM
	Improved efficiency via clock control, split-rail power collapse & voltage scaling; several low-power sleep modes
Debug	JTAG and QDSS
Others	Thermal sensors, modes and resets; peripheral subsystem
Chipset and RF front-end (RFFE) interface features	
WTR RFICs	WTR2965
WAN baseband data	Four Rx (CH0, CH1, CH2, CH3) and one Tx (DAC0) analog interfaces
GNSS baseband data	Rx (GNSS) analog interface
Status and control	MIPI_RFFEs and discrete signals as needed via GPIOs
Power management	PM8909
	2-line SPMI; dedicated clock & reset lines, plus other GPIOs as needed

Table 1-4 Summary of MSM8905 features (cont.)

Feature	MSM8905 capability
WCN wireless connectivity WLAN baseband data WLAN status & control Bluetooth FM radio	WCN3610 Multiplexed Rx/Tx analog interface Proprietary 5-line interface 2-line data interface plus SSBI 1-line data interface plus SSBI
Qualcomm RF360 QFE devices	MIPI_RFFEs
Power amplifiers & RF switches	MIPI_RFFEs and discrete control lines
Fabrication technology and package	
Digital die	28 nm LP CMOS
Small, thermally efficient package	504 NSP: 11.1 × 12.0 × 0.96 mm; 0.4 mm pitch

1.3.3 Air interface features

This information will be included in future revisions of this document.

1.4 Terms and acronyms

Table 1-5 defines terms and acronyms commonly used throughout this document.

Table 1-5 Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
AGC	Automatic gain control
BER	Bit error rate
bps	Bits per second
CDMA	Code division multiple access
CRC	Cyclic redundancy code
CSI	Camera serial interface
DAC	Digital-to-analog converter
DDR	Double data rate
DRM	Digital Rights Management
DSDA	Dual SIM dual active
DSDS	Dual SIM dual standby
DSI	Display serial interface
DSP	Digital signal processor
EBI	External bus interface
EDGE	Enhanced data rates for GSM evolution

Table 1-5 Terms and acronyms (cont.)

Term	Definition
ETB	Embedded trace buffer
EV-DO	Evolution data optimized
FDD	Frequency division duplex
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General packet radio services
GPS	Global positioning system
GPU	Graphics processing unit
GRFC	General RF control
GSM	Global system for mobile communications
HSPA+	High-speed packet access
I^2C	Interintegrated circuit
ISP	Image signal processing
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1760)
kbps	kilobits per second
LCD	Liquid crystal display
LPA	Low-power audio
LPASS	Low-power audio subsystem
LPDDR	Low-power DDR
LPM	LPASS memory
LSB	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
MDP	Mobile display processor
MIPI	Mobile industry processor interface
MMC	Multimedia card
MPM	Modem power management
MSB	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
NSP	Nanoscale package
OMA	Open Mobile Alliance
PA	Power amplifier
PDM	Pulse-density modulation
PM	Power management
QDSS	Qualcomm debug subsystem

Table 1-5 Terms and acronyms (cont.)

Term	Definition
QFPROM	Qualcomm fuse programmable read-only memory
QLIC	Quasi-linear interference cancellation
QTI	Qualcomm Technologies, Inc.
QUP	Qualcomm Unified Peripheral
RBDS	Radio broadcast data system
RDS	Radio data system
RLP	Radio link protocol
RPM	Resource power manager
SBI	Serial bus interface
SD	Secure digital
SDC	Secure digital controller
SFS	Secure file system
SIM	Subscriber identity module
SMT	Surface mount technology
SPI	Serial peripheral interface
sps	Symbols per second (or samples per second)
SPSS	Smart peripheral subsystem
SSBI	Single-wire SBI
TAP	Test access port
TCXO	Temperature-compensated crystal oscillator
TDD	Time division duplexing
TSTS	Triple SIM Triple Standby
UART	Universal asynchronous receiver transmitter
UIM	User identity module
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
USIM	UMTS subscriber identity module
WCDMA	Wideband code division multiple access
WCN	Wireless connectivity network
WLAN	Wireless local area network
WTR	Wafer-scale RF transceiver
XO	Crystal oscillator
ZIF	Zero intermediate frequency

1.5 Special marks

Table 1-6 defines special marks used in this document.

Table 1-6 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number (for example, 0x0000). All numbers are decimal (base 10) unless otherwise specified. Nonobvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).
|	A blue vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

2 Pin definitions

The MSM8x0x is available in the 504 NSP – see Chapter 4 for package details. A high-level view of all pin assignments is shown in Figure 2-2. The pins are colored to indicate which function type they support, as defined in Figure 2-1.

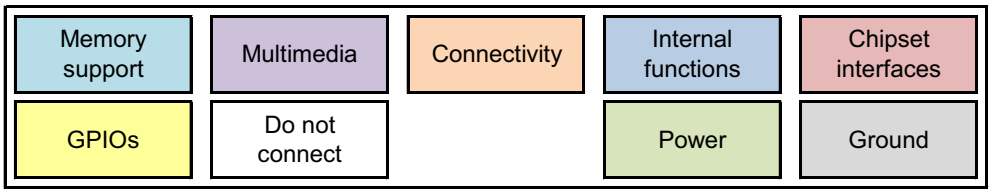


Figure 2-1 MSM8x0x pin assignments – legend

Since the text within Figure 2-2 is difficult to read when viewing an 8½" by 11" hard copy, other viewing options are available:

- Print that one page on a 11" by 17" sheet.
- View the graphic soft copy and zoom in – the resolution is sufficient for comfortable reading.
- Download the *MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) Pin Assignment Spreadsheet* (80-NP408-1A) – this Microsoft Excel spreadsheet lists all MSM8x0x pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

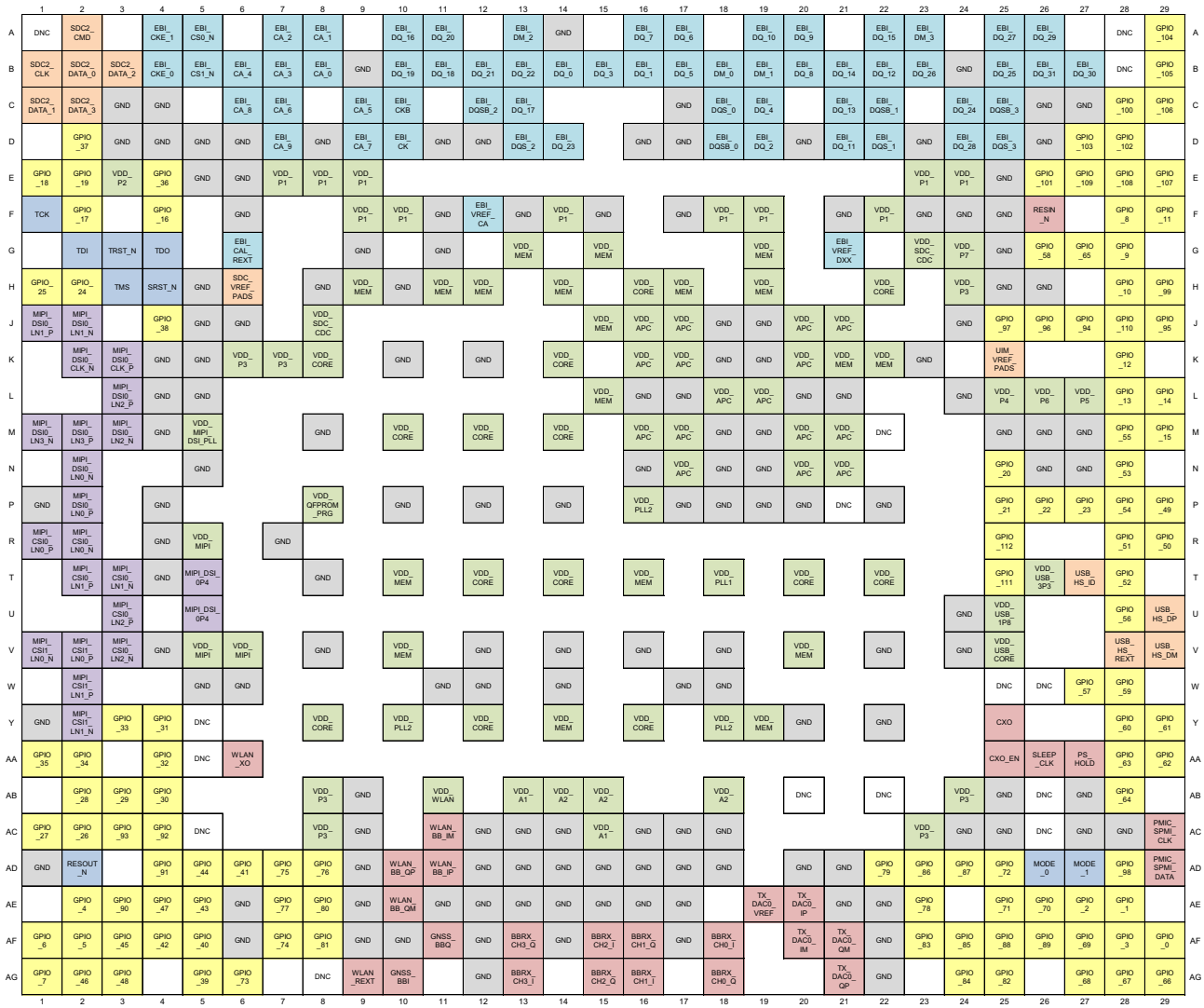
NOTE: Click the link below to download the pin assignment spreadsheet (80-NP408-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-NP408-1A

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	
A	DNC	SDC2_CMD		EBI_CKE_1	EBI_CS0_N		EBI_CA_2	EBI_CA_1		EBI_DQ_16	EBI_DQ_20		EBI_DM_2	GND		EBI_DQ_7	EBI_DQ_6		EBI_DQ_10	EBI_DQ_9		EBI_DQ_15	EBI_DM_3		EBI_DQ_27	EBI_DQ_29		DNC	GPIO_104	A
B	SDC2_CLK	SDC2_DATA_0	SDC2_DATA_2	EBI_CKE_0	EBI_CS1_N	EBI_CA_4	EBI_CA_3	EBI_CA_0	GND	EBI_DQ_19	EBI_DQ_18	EBI_DQ_21	EBI_DQ_22	EBI_DQ_0	EBI_DQ_3	EBI_DQ_1	EBI_DQ_5	EBI_DM_0	EBI_DM_1	EBI_DQ_8	EBI_DQ_14	EBI_DQ_12	EBI_DQ_26	GND	EBI_DQ_25	EBI_DQ_31	EBI_DQ_30	DNC	GPIO_105	B
C	SDC2_DATA_1	SDC2_DATA_3	GND	GND		EBI_CA_8	EBI_CA_6		EBI_CA_5	EBI_CKB		EBI_DQSB_2	EBI_DQ_17				GND	EBI_DQS_0	EBI_DQ_4		EBI_DQ_13	EBI_DQSB_1		EBI_DQ_24	EBI_DQSB_3	GND	GND	GPIO_100	GPIO_106	C
D		GPIO_37	GND	GND	GND	GND	EBI_CA_9	GND	EBI_CA_7	EBI_CK	GND	GND	EBI_DQS_2	EBI_DQ_23		GND	GND	EBI_DQSB_0	EBI_DQ_2	GND	EBI_DQ_11	EBI_DQS_1	GND	EBI_DQ_28	EBI_DQS_3	GND	GPIO_103	GPIO_102		D
E	GPIO_18	GPIO_19	VDD_P2	GPIO_36	GND	GND	VDD_P1	VDD_P1	VDD_P1														VDD_P1	VDD_P1	GND	GPIO_101	GPIO_109	GPIO_108	GPIO_107	E
F	TCK	GPIO_17		GPIO_16		GND			VDD_P1	VDD_P1	GND	EBI_VREF_CA	GND	VDD_P1	GND		GND	VDD_P1	VDD_P1		GND	VDD_P1	GND	GND	GND	RESIN_N		GPIO_8	GPIO_11	F
G		TDI	TRST_N	TDO		EBI_CAL_REXT			GND		GND		VDD_MEM		VDD_MEM				VDD_MEM		EBI_VREF_DXX		VDD_SDC_CDC	VDD_P7	GND	GPIO_58	GPIO_65	GPIO_9		G
H	GPIO_25	GPIO_24	TMS	SRST_N	GND	SDC_VREF_PADS		GND	VDD_MEM	GND	VDD_MEM	VDD_MEM		VDD_MEM		VDD_CORE	VDD_MEM		VDD_MEM			VDD_CORE		VDD_P3	GND	GND		GPIO_10	GPIO_99	H
J	MIPI_DSI0_LN1_P	MIPI_DSI0_LN1_N		GPIO_38	GND	GND		VDD_SDC_CDC							VDD_MEM	VDD_APC	VDD_APC	GND	GND	VDD_APC	VDD_APC			GND	GPIO_97	GPIO_96	GPIO_94	GPIO_110	GPIO_95	J
K		MIPI_DSI0_CLK_N	MIPI_DSI0_CLK_P	GND	GND	VDD_P3	VDD_P3	VDD_CORE		GND		GND		VDD_CORE		VDD_APC	VDD_APC	GND	GND	VDD_APC	VDD_MEM	VDD_MEM	GND		UIM_VREF_PADS			GPIO_12		K
L			MIPI_DSI0_LN2_P	GND	GND										VDD_MEM	GND	GND	VDD_APC	VDD_APC	GND	GND			GND	VDD_P4	VDD_P6	VDD_P5	GPIO_13	GPIO_14	L
M	MIPI_DSI0_LN3_N	MIPI_DSI0_LN3_P	MIPI_DSI0_LN2_N	GND	VDD_MIPI_DSI_PLL			GND		VDD_CORE		VDD_CORE		VDD_CORE		VDD_APC	VDD_APC	GND	GND	VDD_APC	VDD_APC	DNC			GND	GND	GND	GPIO_55	GPIO_15	M
N		MIPI_DSI0_LN0_N			GND											GND	VDD_APC	GND	GND	VDD_APC	VDD_APC				GPIO_20	GND	GND	GPIO_53		N
P	GND	MIPI_DSI0_LN0_P		GND				VDD_QFPROM_PRG		GND		GND		GND		VDD_PLL2	GND	GND	GND	GND	DNC	GND			GPIO_21	GPIO_22	GPIO_23	GPIO_54	GPIO_49	P
R	MIPI_CSI0_LN0_P	MIPI_CSI0_LN0_N		GND	VDD_MIPI		GND																		GPIO_112			GPIO_51	GPIO_50	R
T		MIPI_CSI0_LN1_P	MIPI_CSI0_LN1_N	GND	MIPI_DSI_0P4			GND		VDD_MEM		VDD_CORE		VDD_CORE		VDD_MEM		VDD_PLL1		VDD_CORE		VDD_CORE			GPIO_111	VDD_USB_3P3	USB_HS_ID	GPIO_52		T
U			MIPI_CSI0_LN2_P		MIPI_DSI_0P4																			GND	VDD_USB_1P8			GPIO_56	USB_HS_DP	U
V	MIPI_CSI1_LN0_N	MIPI_CSI1_LN0_P	MIPI_CSI0_LN2_N	GND	VDD_MIPI	VDD_MIPI		GND		VDD_MEM		GND		GND		GND		GND		VDD_MEM		GND		GND	VDD_USB_CORE			USB_HS_REXT	USB_HS_DM	V
W		MIPI_CSI1_LN1_P			GND	GND					GND	GND		GND			GND	GND							DNC	DNC	GPIO_57	GPIO_59		W
Y	GND	MIPI_CSI1_LN1_N	GPIO_33	GPIO_31	DNC			VDD_CORE		VDD_PLL2		VDD_CORE		VDD_MEM		VDD_CORE		VDD_PLL2	VDD_MEM	GND		GND			CXO			GPIO_60	GPIO_61	Y
AA	GPIO_35	GPIO_34		GPIO_32	DNC	WLAN_XO																			CXO_EN	SLEEP_CLK	PS_HOLD	GPIO_63	GPIO_62	AA
AB		GPIO_28	GPIO_29	GPIO_30				VDD_P3	GND		VDD_WLAN		VDD_A1	VDD_A2	VDD_A2			VDD_A2		DNC		DNC		VDD_P3	GND	DNC	GND	GPIO_64		AB
AC	GPIO_27	GPIO_26	GPIO_93	GPIO_92	DNC			VDD_P3	GND		WLAN_BB_IM	GND	GND	GND	VDD_A1	GND	GND	GND						VDD_P3	GND	GND	DNC	GND	GND	PMIC_SPMI_CLK	AC
AD	GND	RESOUT_N		GPIO_91	GPIO_44	GPIO_41	GPIO_75	GPIO_76	GND	WLAN_BB_QP	WLAN_BB_IP	GND	GND	GND	GND	GND	GND	GND		GND	GND	GPIO_79	GPIO_86	GPIO_87	GPIO_72	MODE_0	MODE_1	GPIO_98	PMIC_SPMI_DATA	AD
AE		GPIO_4	GPIO_90	GPIO_47	GPIO_43	GND	GPIO_77	GPIO_80	GND	WLAN_BB_QM	GND	GND	GND	GND	GND	GND	GND		TX_DAC0_VREF	TX_DAC0_IP	GND	GND	GPIO_78		GPIO_71	GPIO_70	GPIO_2	GPIO_1		AE
AF	GPIO_6	GPIO_5	GPIO_45	GPIO_42	GPIO_40	GND	GPIO_74	GPIO_81	GND	GND	GNSS_BBQ	GND	BBRX_CH3_Q	GND	BBRX_CH2_I	BBRX_CH1_Q	GND	BBRX_CH0_I		TX_DAC0_IM	TX_DAC0_QM	GND	GPIO_83	GPIO_85	GPIO_88	GPIO_89	GPIO_69	GPIO_3	GPIO_0	AF
AG	GPIO_7	GPIO_46	GPIO_48		GPIO_39	GPIO_73		DNC	WLAN_REXT	GNSS_BBI		GND	BBRX_CH3_I		BBRX_CH2_Q	BBRX_CH1_I		BBRX_CH0_Q			TX_DAC0_QP	GND		GPIO_84	GPIO_82		GPIO_68	GPIO_67	GPIO_66	AG
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-2 High-level view of MSM8x0x pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: ■ NP: pdpukp = default no-pull with programmable options following the colon (:) ■ PD: nppukp = default pulldown with programmable options following the colon (:) ■ PU: nppdkp = default pullup with programmable options following the colon (:) ■ KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pullup device
PD	Contains an internal pulldown device
Pad voltage groupings for baseband circuits	
P1	EBI Pad group 1 (EBI for LPDDR2/LPDDR3 memory); tied to VDD_P1 pins (1.2 V only)
P2	Pad group 2 (SDC2); tied to VDD_P2 pins (1.80 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.80 V only)
P4	Pad group 4 (UIM3); tied to VDD_P4 pins (1.80 V or 2.95 V)
P5	Pad group 5 (UIM1); tied to VDD_P5 pins (1.80 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDD_P6 pins (1.80 V or 2.95 V)
P7	Pad group 7 (SDC1); tied to VDD_P7 pins (1.80 V)
CSI	Supply voltage for MIPI_CSI circuits; tied to VDD_MIPI (1.2 V only)
DSI	Supply voltage for MIPI_DSI circuits; tied to VDD_MIPI (1.2 V only)
Output current drive strength	
EBI pads	Pads for EBI are tailored for 1.2 V interfaces and are source terminated; additional details will be given in future revisions of this document.
3.0 V (H) pads	Programmable drive strength, 2 to 8 mA, in 2 mA steps
Others [1]	Programmable drive strength, 2 to 16 mA, in 2 mA steps

1. Digital pads other than EBI pads or high-voltage tolerant pads.

2.1.1 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2: Memory support functions

Table 2-3: Multimedia functions

Table 2-4: Connectivity functions

Table 2-6: Internal functions

Table 2-8: Chipset interface functions

Table 2-9: RF front-end interface functions

Table 2-10: General-purpose input/output ports

Table 2-11: No connection, do not connect, and reserved pins

Table 2-12: Power supply pins

Table 2-13: Ground pins

Table 2-2 Pin descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
D7	EBI_CA_9		P1	DO	LPDDR command/address bit 9
C6	EBI_CA_8		P1	DO	LPDDR command/address bit 8
D9	EBI_CA_7		P1	DO	LPDDR command/address bit 7
C7	EBI_CA_6		P1	DO	LPDDR command/address bit 6
C9	EBI_CA_5		P1	DO	LPDDR command/address bit 5
B6	EBI_CA_4		P1	DO	LPDDR command/address bit 4
B7	EBI_CA_3		P1	DO	LPDDR command/address bit 3
A7	EBI_CA_2		P1	DO	LPDDR command/address bit 2
A8	EBI_CA_1		P1	DO	LPDDR command/address bit 1
B8	EBI_CA_0		P1	DO	LPDDR command/address bit 0
B26	EBI_DQ_31		P1	B	LPDDR data bit 31
B27	EBI_DQ_30		P1	B	LPDDR data bit 30
A26	EBI_DQ_29		P1	B	LPDDR data bit 29
D24	EBI_DQ_28		P1	B	LPDDR data bit 28
A25	EBI_DQ_27		P1	B	LPDDR data bit 27
B23	EBI_DQ_26		P1	B	LPDDR data bit 26
B25	EBI_DQ_25		P1	B	LPDDR data bit 25
C24	EBI_DQ_24		P1	B	LPDDR data bit 24
D14	EBI_DQ_23		P1	B	LPDDR data bit 23
B13	EBI_DQ_22		P1	B	LPDDR data bit 22

Table 2-2 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
B12	EBI_DQ_21		P1	B	LPDDR data bit 21
A11	EBI_DQ_20		P1	B	LPDDR data bit 20
B10	EBI_DQ_19		P1	B	LPDDR data bit 19
B11	EBI_DQ_18		P1	B	LPDDR data bit 18
C13	EBI_DQ_17		P1	B	LPDDR data bit 17
A10	EBI_DQ_16		P1	B	LPDDR data bit 16
A22	EBI_DQ_15		P1	B	LPDDR data bit 15
B21	EBI_DQ_14		P1	B	LPDDR data bit 14
C21	EBI_DQ_13		P1	B	LPDDR data bit 13
B22	EBI_DQ_12		P1	B	LPDDR data bit 12
D21	EBI_DQ_11		P1	B	LPDDR data bit 11
A19	EBI_DQ_10		P1	B	LPDDR data bit 10
A20	EBI_DQ_9		P1	B	LPDDR data bit 9
B20	EBI_DQ_8		P1	B	LPDDR data bit 8
A16	EBI_DQ_7		P1	B	LPDDR data bit 7
A17	EBI_DQ_6		P1	B	LPDDR data bit 6
B17	EBI_DQ_5		P1	B	LPDDR data bit 5
C19	EBI_DQ_4		P1	B	LPDDR data bit 4
B15	EBI_DQ_3		P1	B	LPDDR data bit 3
D19	EBI_DQ_2		P1	B	LPDDR data bit 2
B16	EBI_DQ_1		P1	B	LPDDR data bit 1
B14	EBI_DQ_0		P1	B	LPDDR data bit 0
D10	EBI_CK		P1	DO	LPDDR differential clock – positive
C10	EBI_CKB		P1	DO	LPDDR differential clock – negative
A4	EBI_CKE_1		P1	DO	LPDDR clock enable 1
B4	EBI_CKE_0		P1	DO	LPDDR clock enable 0
B5	EBI_CS1_N		P1	DO	LPDDR chip select 1
A5	EBI_CS0_N		P1	DO	LPDDR chip select 0
A23	EBI_DM_3		P1	DO	LPDDR data mask for byte 3
A13	EBI_DM_2		P1	DO	LPDDR data mask for byte 2
B19	EBI_DM_1		P1	DO	LPDDR data mask for byte 1
B18	EBI_DM_0		P1	DO	LPDDR data mask for byte 0
D25	EBI_DQS_3		P1	B	LPDDR differential data strobe for byte 3 – positive
C25	EBI_DQSB_3		P1	B	LPDDR differential data strobe for byte 3 – negative
D13	EBI_DQS_2		P1	B	LPDDR differential data strobe for byte 2 – positive
C12	EBI_DQSB_2		P1	B	LPDDR differential data strobe for byte 2 – negative
D22	EBI_DQS_1		P1	B	LPDDR differential data strobe for byte 1 – positive

Table 2-2 Pin descriptions – memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
C22	EBI_DQSB_1		P1	B	LPDDR differential data strobe for byte 1 – negative
C18	EBI_DQS_0		P1	B	LPDDR differential data strobe for byte 0 – positive
D18	EBI_DQSB_0		P1	B	LPDDR differential data strobe for byte 0 – negative
F12	EBI_VREF_CA		–	AI	LPDDR CA reference voltage
G21	EBI_VREF_DXX		–	AI	LPDDR D0, D1, D2, and D3 reference
G6	EBI_CAL_REXT		–	AI	LPDDR calibration resistor

1. See to Table 2-1 for parameter and acronym definitions.

Table 2-3 Pin descriptions – multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Primary camera serial interface – 2-lane MIPI_CSI0					
V3	MIPI_CSI0_LN2_N		CSI	AI, AO	MIPI camera serial interface 0 lane 2 – negative
U3	MIPI_CSI0_LN2_P		CSI	AI, AO	MIPI camera serial interface 0 lane 2 – positive
T3	MIPI_CSI0_LN1_N	MIPI_CSI0_CLK_N	CSI	AI, AO AI	MIPI camera serial interface 0 lane 1 – negative MIPI camera serial interface 0 clock – negative
T2	MIPI_CSI0_LN1_P	MIPI_CSI0_CLK_P	CSI	AI, AO AI	MIPI camera serial interface 0 lane 1 – positive MIPI camera serial interface 0 clock – positive
R2	MIPI_CSI0_LN0_N		CSI	AI, AO	MIPI camera serial interface 0 lane 0 – negative
R1	MIPI_CSI0_LN0_P		CSI	AI, AO	MIPI camera serial interface 0 lane 0 – positive
Secondary camera serial interface – 1-lane MIPI_CSI1					
Y2	MIPI_CSI1_LN1_N	MIPI_CSI1_CLK_N	CSI	AI, AO AI	MIPI camera serial interface 1 lane 1 – negative MIPI camera serial interface 1 clock – negative
W2	MIPI_CSI1_LN1_P	MIPI_CSI1_CLK_P	CSI	AI, AO AI	MIPI camera serial interface 1 lane 1 – positive MIPI camera serial interface 1 clock – positive
V1	MIPI_CSI1_LN0_N		CSI	AI, AO	MIPI camera serial interface 1 lane 0 – negative
V2	MIPI_CSI1_LN0_P		CSI	AI, AO	MIPI camera serial interface 1 lane 0 – positive
Primary camera serial interface - 4-lane[1] MIPI_CSI					
V3	MIPI_CSI0_LN2_N	MIPI_CSI_LN1_N	CSI	AI, AO	MIPI camera serial interface lane 1 – negative
U3	MIPI_CSI0_LN2_P	MIPI_CSI_LN1_P	CSI	AI, AO	MIPI camera serial interface lane 1 – positive
T3	MIPI_CSI0_LN1_N	MIPI_CSI_CLK_N	CSI	AI, AO AI	Camera serial interface clock – negative
T2	MIPI_CSI0_LN1_P	MIPI_CSI_CLK_P	CSI	AI, AO AI	Camera serial interface clock – positive
R2	MIPI_CSI0_LN0_N	MIPI_CSI_LN0_N	CSI	AI, AO	MIPI camera serial interface lane 0 – negative

Table 2-3 Pin descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
R1	MIPI_CSI0_LN0_P	MIPI_CSI_LN0_P	CSI	AI, AO	MIPI camera serial interface lane 0 – positive
Y2	MIPI_CSI1_LN1_N	MIPI_CSI_LN2_N	CSI	AI, AO AI	MIPI camera serial interface lane 2 – negative MIPI
W2	MIPI_CSI1_LN1_P	MIPI_CSI_LN2_P	CSI	AI, AO AI	MIPI camera serial interface lane 2– positive MIPI
V1	MIPI_CSI1_LN0_N	MIPI_CSI_LN3_N	CSI	AI, AO	MIPI camera serial interface lane 3– negative
V2	MIPI_CSI1_LN0_P	MIPI_CSI_LN3_P	CSI	AI, AO	MIPI camera serial interface lane 3– positive
Camera-related timing signals					
AC1	CAM_MCLK1	GPIO_27	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
AC2	CAM_MCLK0	GPIO_26	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
J4	CCI_TIMER2	GPIO_38	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/O
AA4	CCI_TIMER1	GPIO_32	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/O
Y4	CCI_TIMER0	GPIO_31	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/O
Y3	CCI_ASYNC0	GPIO_33	P3	DI B-PD:nppukp	Camera control interface async 0 Configurable I/O
AB2	WEBCAM_RST_N	GPIO_28	P3	DO B-PD:nppukp	Webcam reset Configurable I/O
AA2	CAM1_STANDBY_N	GPIO_34	P3	DO B-PD:nppukp	Camera 1 standby Configurable I/O
AA1	CAM1_RST_N	GPIO_35	P3	DO B-PD:nppukp	Camera 1 reset Configurable I/O
Display serial interface – 4-lane MIPI_DSI0					
M1	MIPI_DSI0_LN3_N		DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
M2	MIPI_DSI0_LN3_P		DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
M3	MIPI_DSI0_LN2_N		DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
L3	MIPI_DSI0_LN2_P		DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
J2	MIPI_DSI0_LN1_N		DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
J1	MIPI_DSI0_LN1_P		DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
N2	MIPI_DSI0_LN0_N		DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
P2	MIPI_DSI0_LN0_P		DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
K2	MIPI_DSI0_CLK_N		DSI	AO	MIPI display serial interface 0 clock – negative
K3	MIPI_DSI0_CLK_P		DSI	AO	MIPI display serial interface 0 clock – positive
T5, U5	MIPI_DSI_0p4		DSI	AI, AO	MIPI DSIPHY internal supply
H1	DSI_RST	GPIO_25	P3	DO B-PD:nppukp	Display reset Configurable I/O
D2	BACKLIGHT_EN	GPIO_37	P3	DO B-PD:nppukp	Backlight enable Configurable I/O

Table 2-3 Pin descriptions – multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Mobile display processor (MDP) vertical sync					
H2	MDP_VSYNC_P	GPIO_24	P3	DI B-PD:nppukp	MDP vertical sync – primary Configurable I/O
H1	MDP_VSYNC_S	GPIO_25	P3	DI B-PD:nppukp	MDP vertical sync – secondary Configurable I/O

1. If the design uses 4-lane primary camera serial interface, then a secondary camera cannot not be supported
2. See to Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See to Table 2-10 for a list of all supported functions for each GPIO.

Table 2-4 Pin descriptions – connectivity functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
High-speed USB 2.0					
V29	USB_HS_DM		–	AI, AO	USB HS data minus
U29	USB_HS_DP		–	AI, AO	USB HS data plus
T27	USB_HS_ID		–	AI	USB HS ID
V28	USB_HS_REXT		–	AI	USB HS external resistor
Secure digital controller 1 (SDC1) interface – supports eMMC					
C28	SDC1_CLK	GPIO_100	P7	B B-NP:pdpukp	Secure digital controller 1 clock Configurable I/O
E27	SDC1_CMD	GPIO_109	P7	B B-PD:nppukp	Secure digital controller 1 command Configurable I/O
E26	SDC1_DATA_7	GPIO_101	P7	B B-PD:nppukp	Secure digital controller 1 data bit 7 Configurable I/O
D28	SDC1_DATA_6	GPIO_102	P7	B B-PD:nppukp	Secure digital controller 1 data bit 6 Configurable I/O
D27	SDC1_DATA_5	GPIO_103	P7	B B-PD:nppukp	Secure digital controller 1 data bit 5 Configurable I/O
A29	SDC1_DATA_4	GPIO_104	P7	B B-PD:nppukp	Secure digital controller 1 data bit 4 Configurable I/O
B29	SDC1_DATA_3	GPIO_105	P7	B B-PD:nppukp	Secure digital controller 1 data bit 3 Configurable I/O
C29	SDC1_DATA_2	GPIO_106	P7	B B-PD:nppukp	Secure digital controller 1 data bit 2 Configurable I/O
E29	SDC1_DATA_1	GPIO_107	P7	B B-PD:nppukp	Secure digital controller 1 data bit 1 Configurable I/O
E28	SDC1_DATA_0	GPIO_108	P7	B B-PD:nppukp	Secure digital controller 1 data bit 0 Configurable I/O
Secure digital controller 2 (SDC2) interface – supports dual-voltage SD i/f					
B1	SDC2_CLK		P2	BH-NP:pdpukp	Secure digital controller 2 clock
A2	SDC2_CMD		P2	BH-PD:nppukp	Secure digital controller 2 command
C2	SDC2_DATA_3		P2	BH-PD:nppukp	Secure digital controller 2 data bit 3
B3	SDC2_DATA_2		P2	BH-PD:nppukp	Secure digital controller 2 data bit 2
C1	SDC2_DATA_1		P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
B2	SDC2_DATA_0		P2	BH-PD:nppukp	Secure digital controller 2 data bit 0
J4	SD_CARD_DET_N	GPIO_38	P3	DI PD:nppukp	Secure digital card detection Configurable I/O
H29	SD_WRITE_PROTECT	GPIO_99	P3	DI B-PD:nppukp	Secure digital card write protection Configurable I/O
SDC pad reference – common to all SDCs					
H6	SDC_VREF_PADS		–	AI	Reference for secure digital I/O pads

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
8-bit NAND interface					
F29	EBI2_NAND_CS_N	GPIO_11	P3	DO B-PD:nppukp	EBI2 chip select for NAND Configurable I/O
H28	EBI2_A_D[0]	GPIO_10	P3	B B-PD:nppukp	EBI2 address data bit 0 Configurable I/O
G28	EBI2_A_D[1]	GPIO_9	P3	B B-PD:nppukp	EBI2 address data bit 1 Configurable I/O
F28	EBI2_A_D[2]	GPIO_8	P3	B B-PD:nppukp	EBI2 address data bit 2 Configurable I/O
E29	EBI2_A_D[3]	GPIO_107	P7	B B-PD:nppukp	EBI2 address data bit 3 Configurable I/O
D27	EBI2_A_D[4]	GPIO_103	P7	B B-PD:nppukp	EBI2 address data bit 4 Configurable I/O
A29	EBI2_A_D[5]	GPIO_104	P7	B B-PD:nppukp	EBI2 address data bit 5 Configurable I/O
C29	EBI2_A_D[6]	GPIO_106	P7	B B-PD:nppukp	EBI2 address data bit 6 Configurable I/O
B29	EBI2_A_D[7]	GPIO_105	P7	B B-PD:nppukp	EBI2 address data bit 7 Configurable I/O
C28	EBI2_OE_N	GPIO_100	P7	DO B-NP:pdpukp	EBI2 Output Enable Configurable I/O
E28	EBI2_WE_N	GPIO_108	P7	DO B-PD:nppukp	EBI2 Write Enable Configurable I/O
E26	EBI2_ALE_N	GPIO_101	P7	DO B-PD:nppukp	EBI2 address latch enable Configurable I/O
D28	EBI2_CLE_N	GPIO_102	P7	DO B-PD:nppukp	EBI2 command latch enable Configurable I/O
E27	EBI2_BUSY_N	GPIO_109	P7	DI B-PD:nppukp	EBI2 busy signal for NAND Configurable I/O
Dual-voltage UIM1 interface					
N28	UIM1_DATA	GPIO_53	P5	B BH-PD:nppukp	UIM1 data Configurable I/O
P28	UIM1_CLK	GPIO_54	P5	DO BH-PD:nppukp	UIM1 clock Configurable I/O
M28	UIM1_RESET	GPIO_55	P5	DO BH-PD:nppukp	UIM1 reset Configurable I/O
U28	UIM1_PRESENT	GPIO_56	P3	DI B-PD:nppukp	UIM1 presence detection Configurable I/O
Dual-voltage UIM2 interface					
P29	UIM2_DATA	GPIO_49	P6	B BH-PD:nppukp	UIM2 data Configurable I/O
R29	UIM2_CLK	GPIO_50	P6	DO BH-PD:nppukp	UIM2 clock Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
R28	UIM2_RESET	GPIO_51	P6	DO BH-PD:nppukp	UIM2 reset Configurable I/O
T28	UIM2_PRESENT	GPIO_52	P3	DI B-PD:nppukp	UIM2 presence detection Configurable I/O
Dual-voltage UIM3 interface					
N25	UIM3_DATA	GPIO_20	P4	B BH-PD:nppukp	UIM3 data Configurable I/O
P27	UIM3_CLK	GPIO_23	P4	DO BH-PD:nppukp	UIM3 clock Configurable I/O
P26	UIM3_RESET	GPIO_22	P4	DO BH-PD:nppukp	UIM3 reset Configurable I/O
P25	UIM3_PRESENT	GPIO_21	P3	DI B-PD:nppukp	UIM3 presence detection Configurable I/O
Other UIM signals					
K25	UIM_VREF_PADS		–	AI	Reference for UIM I/O pads
W27	UIM_BATT_ALARM	GPIO_57	P3	DI B-PD:nppukp	UIM battery alarm Configurable I/O
Sensor and charger interrupts					
J27	ALSP_INT	GPIO_94	P3	DI B-PD:nppukp	Ambient light sensor interrupt Configurable I/O
J26	GYRO_ACCEL_INT_N	GPIO_96	P3	DI B-PD:nppukp	Gyro/accelerator interrupt Configurable I/O
G27	MAG_INT	GPIO_65	P3	DI B-PD:nppukp	Magnometer interrupt Configurable I/O
G26	SMB_INT	GPIO_58	P3	DO B-PD:nppukp	SMB charger interrupt Configurable I/O
Keypad button sensors					
AE3	KYPD_SNS0	GPIO_90	P3	DI B-PD:nppukp	Keypad sense bit 0 Configurable I/O
AD4	KYPD_SNS1	GPIO_91	P3	DI B-PD:nppukp	Keypad sense bit 1 Configurable I/O
AC4	KYPD_SNS2	GPIO_92	P3	DI B-PD:nppukp	Keypad sense bit 2 Configurable I/O
BAM-based low-speed peripheral interface 1 – see Table 2-5 for BLSP bit assignments					
AE2	BLSP1_3	GPIO_4	P3	B B-PD:nppukp	BLSP #1, bit 3; SPI, UART Configurable I/O
AF2	BLSP1_2	GPIO_5	P3	B B-PD:nppukp	BLSP #1, bit 2; SPI, UART Configurable I/O
AF1	BLSP1_1	GPIO_6	P3	B B-PD:nppukp	BLSP #1, bit 1; SPI, UART, or I^2C Configurable I/O
AG1	BLSP1_0	GPIO_7	P3	B B-PD:nppukp	BLSP #1, bit 0; SPI, UART, or I^2C Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
BAM-based low-speed peripheral interface 2 – see Table 2-5 for BLSP bit assignments					
N25	BLSP2_3	GPIO_20	P4	B BH-PD:nppukp	BLSP #2, bit 3; SPI, UART Configurable I/O
P25	BLSP2_2	GPIO_21	P3	B B-PD:nppukp	BLSP #2, bit 2; SPI, UART Configurable I/O
T25	BLSP2_1	GPIO_111	P3	B B-PD:nppukp	BLSP #2, bit 1; SPI, UART, or I^2C Configurable I/O
R25	BLSP2_0	GPIO_112	P3	B B-PD:nppukp	BLSP #2, bit 0; SPI, UART, or I^2C Configurable I/O
BAM-based low-speed peripheral interface 3 – see Table 2-5 for BLSP bit assignments					
AF29	BLSP3_3	GPIO_0	P3	B B-PD:nppukp	BLSP #3, bit 3; SPI only Configurable I/O
AE28	BLSP3_2	GPIO_1	P3	B B-PD:nppukp	BLSP #3, bit 2; SPI only Configurable I/O
AB3	BLSP3_3	GPIO_29	P3	B B-PD:nppukp	BLSP #3, bit 3; I^2C only Configurable I/O
AB4	BLSP3_2	GPIO_30	P3	B B-PD:nppukp	BLSP #3, bit 2; I^2C only Configurable I/O
AE27	BLSP3_1	GPIO_2	P3	B B-PD:nppukp	BLSP #3, bit 1; SPI only Configurable I/O
AF28	BLSP3_0	GPIO_3	P3	B B-PD:nppukp	BLSP #3, bit 0; SPI only Configurable I/O
BAM-based low-speed peripheral interface 4 – see Table 2-5 for BLSP bit assignments					
K28	BLSP4_3	GPIO_12	P3	B B-PD:nppukp	BLSP #4, bit 3; SPI only Configurable I/O
L28	BLSP4_2	GPIO_13	P3	B B-PD:nppukp	BLSP #4, bit 2; SPI only Configurable I/O
L29	BLSP4_1	GPIO_14	P3	B B-PD:nppukp	BLSP #4, bit 1; SPI or I^2C Configurable I/O
M29	BLSP4_0	GPIO_15	P3	B B-PD:nppukp	BLSP #4, bit 0; SPI or I^2C Configurable I/O
BAM-based low-speed peripheral interface 5 – see Table 2-5 for BLSP bit assignments					
F4	BLSP5_3	GPIO_16	P3	B B-PD:nppukp	BLSP #5, bit 3; SPI only Configurable I/O
F2	BLSP5_2	GPIO_17	P3	B B-PD:nppukp	BLSP #5, bit 2; SPI only Configurable I/O
E1	BLSP5_1	GPIO_18	P3	B B-PD:nppukp	BLSP #5, bit 1; SPI or I^2C Configurable I/O
E2	BLSP5_0	GPIO_19	P3	B B-PD:nppukp	BLSP #5, bit 0; SPI or I^2C Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
BAM-based low-speed peripheral interface 6 – see Table 2-5 for BLSP bit assignments					
F28	BLSP6_3	GPIO_8	P3	B B-PD:nppukp	BLSP #6, bit 3; SPI only Configurable I/O
G28	BLSP6_2	GPIO_9	P3	B B-PD:nppukp	BLSP #6, bit 2; SPI only Configurable I/O
H28	BLSP6_1	GPIO_10	P3	B B-PD:nppukp	BLSP #6, bit 1; SPI or I^{2}C Configurable I/O
F29	BLSP6_0	GPIO_11	P3	B B-PD:nppukp	BLSP #6, bit 0; SPI or I^{2}C Configurable I/O
Serial peripheral interface (SPI) extra chip selects (supplements BLSP ports configured for SPI protocol)					
J25	BLSP1_SPI_CSI1_N	GPIO_97	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP1 Configurable I/O
D2	BLSP1_SPI_CS2_N	GPIO_37	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP1 Configurable I/O
G27	BLSP1_SPI_CS3_N	GPIO_65	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP1 Configurable I/O
AD28	BLSP2_SPI_CS1_N	GPIO_98	P3	DO-Z B-PD:nppukp	Chip select 1for SPI on BLSP2 Configurable I/O
F2	BLSP2_SPI_CS2_N	GPIO_17	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP2 Configurable I/O
AF2	BLSP2_SPI_CS3_N	GPIO_5	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP2 Configurable I/O
J29	BLSP3_SPI_CS1_N	GPIO_95	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP3 Configurable I/O
G27	BLSP3_SPI_CS2_N	GPIO_65	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP3 Configurable I/O
AE2	BLSP3_SPI_CS3_N	GPIO_4	P3	DO-Z B-PD:nppukp	Chip select 3 for SPI on BLSP3 Configurable I/O
Audio Speaker I^{2}S interface [1]					
AA28	SPKR_MI^{2}S_1_D1_A	GPIO_63	P3	DO B-PD:nppukp	Speaker I^{2}S data output channel 1 A Configurable I/O
AA29	SPKR_MI^{2}S_1_D0_A	GPIO_62	P3	DO B-PD:nppukp	Speaker I^{2}S data output channel 0 A Configurable I/O
Y28	SPKR_MI^{2}S_1_SCK_A	GPIO_60	P3	B B-PD:nppukp	Speaker I^{2}S bit clock A Configurable I/O
Y29	SPKR_MI^{2}S_1_WS_A	GPIO_61	P3	B B-PD:nppukp	Speaker I^{2}S word select (L/R) A Configurable I/O
W28	SPKR_MI^{2}S_1_MCLK_A	GPIO_59	P3	B B-PD:nppukp	Speaker I^{2}S master clock A Configurable I/O
J26	SPKR_MI^{2}S_1_D1_B	GPIO_96	P3	DO B-PD:nppukp	Speaker I^{2}S data output channel 1 B Configurable I/O

Table 2-4 Pin descriptions – connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
J29	SPKR_MI2S_1_D0_B	GPIO_95	P3	DO B-PD:nppukp	Speaker I2S data output channel 0 B Configurable I/O
J27	SPKR_MI2S_1_SCK_B	GPIO_94	P3	B B-PD:nppukp	Speaker I2S bit clock B Configurable I/O
J28	SPKR_MI2S_1_WS_B	GPIO_110	P3	B B-PD:nppukp	Speaker I2S word select (L/R) B Configurable I/O
AD28	SPKR_MI2S_1_MCLK_B	GPIO_98	P3	B B-PD:nppukp	Speaker I2S master clock B Configurable I/O
Audio MI2S interface #2					
AF28	MI2S_2_D1	GPIO_3	P3	B B-PD:nppukp	MI2S #2 serial data input/output channel 1 Configurable I/O
AE27	MI2S_2_D0	GPIO_2	P3	B B-PD:nppukp	MI2S #2 serial data input/output channel 0 Configurable I/O
AE28	MI2S_2_SCK	GPIO_1	P3	B B-PD:nppukp	MI2S #2 bit clock Configurable I/O
AF29	MI2S_2_WS	GPIO_0	P3	DO B-PD:nppukp	MI2S #2 word select (L/R) Configurable I/O
AD28	MI2S_2_MCLK	GPIO_98	P3	B B-PD:nppukp	MI2S #2 master clock Configurable I/O
Audio codec interface					
AB28	CDC_PDM0_RX2	GPIO_64	P3	DO B-PD:nppukp	Audio codec PDM 0 receive 2 Configurable I/O
AA28	CDC_PDM0_RX1	GPIO_63	P3	DO B-PD:nppukp	Audio codec PDM 0 receive 1 Configurable I/O
AA29	CDC_PDM0_RX0	GPIO_62	P3	DO B-PD:nppukp	Audio codec PDM 0 receive 0 Configurable I/O
Y29	CDC_PDM0_TX0	GPIO_61	P3	DI B-PD:nppukp	Audio codec PDM 0 transmit 0 Configurable I/O
Y28	CDC_PDM0_SYNC	GPIO_60	P3	DO B-PD:nppukp	Audio codec PDM 0 sync Configurable I/O
W28	CDC_PDM0_CLK	GPIO_59	P3	DO B-PD:nppukp	Audio codec PDM 0 clock Configurable I/O
Audio headset					
J25	HDSET_DET	GPIO_97	P3	DI B-PD:nppukp	Headset detection Configurable I/O
Digital MIC interface					
AE2	DMIC0_CLK	GPIO_4	P3	DO B-PD:nppukp	Digital MIC0 clock Configurable I/O
AF2	DMIC0_DATA	GPIO_5	P3	DI B-PD:nppukp	Digital MIC0 data Configurable I/O

1. GPIO ‘A/B’ multiplexing is explained in Figure 2-3.
2. See to Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. See to Table 2-10 for a list of all supported functions for each GPIO.

BAM-enabled low-speed peripheral (BLSP) interfaces

Six 4-pin sets of GPIOs (six ports) are available as BLSP interfaces that can be configured to support various interface combinations. As shown in Table 2-5, 4-pin SPI is supported by all six ports, while the others (UART, UIM, and I^2C) are only supported by specific BLSPs.

Table 2-5 BLSP bit assignments

BLSP		GPIO #	BLSP assignment			Non-BLSP use options
#	bit		SPI	UART	I^2C	
1	3	4	MOSI	TX	—	BLSP3 SPI CS3, DMIC0_CLK, GP
	2	5	MISO	RX	—	BLSP2 SPI CS3, DMIC0_DATA, GP
	1	6	CS_N	CTS_N	SDA	GP
	0	7	CLK	RFR_N	SCL	GP
2	3	20	MOSI	TX	—	UIM3_DATA, GP PDM_0A, GP
	2	21	MISO	RX	—	UIM3_PRESENT, GP PDM_1A,, GP
	1	111	CS_N	CTS_N	SDA	GP
	0	112	CLK	RFR_N	SCL	GP
3	3	0 29	MOSI —	— —	— SDA	MI^2S_WS #2, GP GP
	2	1 30	MISO —	— —	— SCL	MI^2S_SCK #2, GP GP
	1	2	CS_N	—	—	MI^2S_D0 #2, GP
	0	3	CLK	—	—	MI^2S_D1 #2, GP
4	3	12	MOSI	—	—	GP CLK_2B, GP
	2	13	MISO	—	—	GP CLK_3B, GP
	1	14	CS_N	—	SDA	GP CLK_1B, GP
	0	15	CLK	—	SCL	GP
5	3	16	MOSI	—	—	GP
	2	17	MISO	—	—	BLSP2 SPI CS2, GP
	1	18	CS_N	—	SDA	GP
	0	19	CLK	—	SCL	GP
6	3	8	MOSI	—	—	EBI2_A_D[2], GP
	2	9	MISO	—	—	EBI2_A_D[1], GP
	1	10	CS_N	—	SDA	EBI2_A_D[0], GP
	0	11	CLK	—	SCL	EBI2_NAND_CS_N, GP

As noted throughout the pin definition tables, GPIO assignments must be done carefully to avoid conflicts, and to ensure that the desired functionality is achieved. For GPIOs that can be used as BLSPs, additional factors should be considered when making functional assignments:

1. Extra chip selects are available when certain BLSPs are used for SPI:
   - BLSP1 has extra CS1, CS2, and CS3 for its SPI.
   - BLSP2 has extra CS1, CS2, and CS3 for its SPI.
   - BLSP3 has extra CS1, CS2, and CS3 for its SPI.
2. SPI is only supported via BLSP, and each BLSPs supports a different SPI.
3. UART is only supported via BLSP, and only at BLSP1 and BLSP2.
4. I^2C is supported by each BLSP. All BLSPs except BLSP3 use bits [1:0] for I^2C, whereas BLSP3 uses bits [3:2].
5. EBI2 signals are multiplexed with BLSP6.

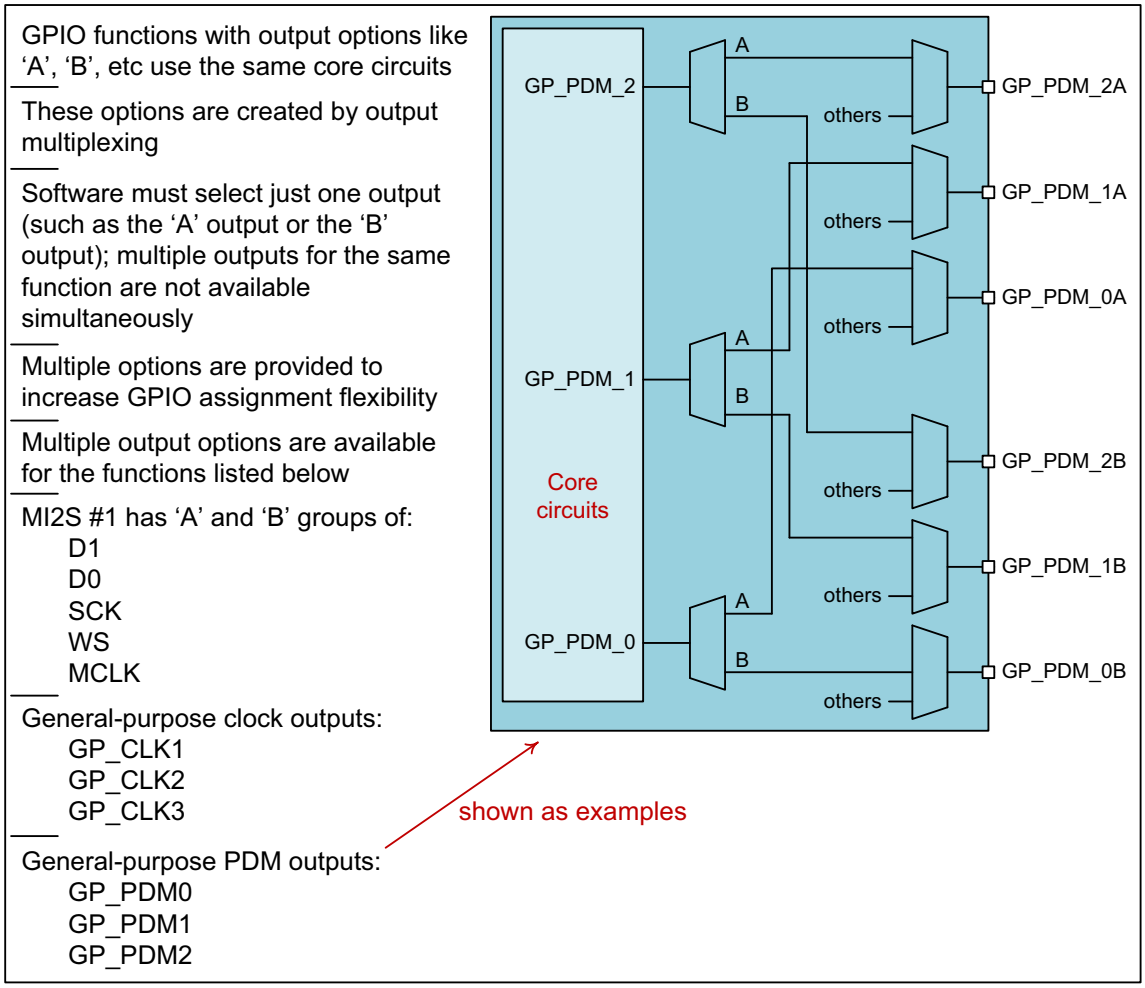


Figure 2-3 GPIO 'A/B' multiplexing

Table 2-6 Pin descriptions – internal functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
JTAG interface					
H4	SRST_N		P3	PU	JTAG reset for debug
F1	TCK		P3	PU	JTAG clock input
G2	TDI		P3	PU:nppdkp	JTAG data input
G4	TDO		P3	DO-Z	JTAG data output
H3	TMS		P3	PU:nppdkp	JTAG mode-select input
G3	TRST_N		P3	PD	JTAG reset
General Purpose Clocks, PDM, and related signals [1]					
J26	GP_MN	GPIO_96	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
Y4	GP_CLK0	GPIO_31	P3	DO B-PD:nppukp	General-purpose clock 0 Configurable I/O
AA4	GP_CLK1	GPIO_32	P3	DO B-PD:nppukp	General-purpose clock 1 Configurable I/O
N25	GP_PDM_0A	GPIO_20	P4	DO BH-PD:nppukp	General-purpose PDM output 0A Configurable I/O
AC2	GP_PDM_0B	GPIO_26	P3	DO B-PD:nppukp	General-purpose PDM output 0B Configurable I/O
P25	GP_PDM_1A	GPIO_21	P3	DO B-PD:nppukp	General-purpose PDM output 1A Configurable I/O
AC1	GP_PDM_1B	GPIO_27	P3	DO B-PD:nppukp	General-purpose PDM output 1B Configurable I/O
P26	GP_PDM_2A	GPIO_22	P4	DO BH-PD:nppukp	General-purpose PDM output 2A Configurable I/O
AB2	GP_PDM_2B	GPIO_28	P3	DO B-PD:nppukp	General-purpose PDM output 2B Configurable I/O
P29	GP_CLK_1A	GPIO_49	P6	DO BH-PD:nppukp	General-purpose clock output 1A Configurable I/O
L29	GP_CLK_1B	GPIO_14	P3	DO B-PD:nppukp	General-purpose clock output 1B Configurable I/O
R29	GP_CLK_2A	GPIO_50	P6	DO BH-PD:nppukp	General-purpose clock output 2A Configurable I/O
K28	GP_CLK_2B	GPIO_12	P3	DO B-PD:nppukp	General-purpose clock output 2B Configurable I/O
R28	GP_CLK_3A	GPIO_51	P6	DO BH-PD:nppukp	General-purpose clock output 3A Configurable I/O
L28	GP_CLK_3B	GPIO_13	P3	DO B-PD:nppukp	General-purpose clock output 3B Configurable I/O

Table 2-6 Pin descriptions – internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [2]		Functional description
			Voltage	Type	
Resets and mode controls					
AD26	MODE_0		P3	DIS-PD	Mode control bit 0
AD27	MODE_1		P3	DIS-PD	Mode control bit 1
AD2	RESOUT_N		P3	DO	Reset output
D2	FORCED_USB_BOOT	GPIO_37	P3	DI B-PD:nppukp	Force USB boot control Configurable I/O
Y28	BOOT_CONFIG_14	GPIO_60	P3	DI B-PD:nppukp	Boot configuration control bit 14 Configurable I/O
AB28	BOOT_CONFIG_13	GPIO_64	P3	DI B-PD:nppukp	Boot configuration control bit 13 Configurable I/O
AA28	BOOT_CONFIG_12	GPIO_63	P3	DI B-PD:nppukp	Boot configuration control bit 12 Configurable I/O
AA29	BOOT_CONFIG_11	GPIO_62	P3	DI B-PD:nppukp	Boot configuration control bit 11 Configurable I/O
AF25	BOOT_CONFIG_10	GPIO_88	P3	DI B-PD:nppukp	Boot configuration control bit 10 Configurable I/O
AD23	BOOT_CONFIG_9	GPIO_86	P3	DI B-PD:nppukp	Boot configuration control bit 9 Configurable I/O
AG27	BOOT_CONFIG_8	GPIO_68	P3	DI B-PD:nppukp	Boot configuration control bit 8 Configurable I/O
AG29	BOOT_CONFIG_7	GPIO_66	P3	DI B-PD:nppukp	Boot configuration control bit 7 Configurable I/O
AG24	BOOT_CONFIG_6	GPIO_84	P3	DI B-PD:nppukp	Boot configuration control bit 6 Configurable I/O
AG25	BOOT_CONFIG_5	GPIO_82	P3	DI B-PD:nppukp	Boot configuration control bit 5 Configurable I/O
AE8	BOOT_CONFIG_4	GPIO_80	P3	DI B-PD:nppukp	Boot configuration control bit 4 Configurable I/O
AD22	BOOT_CONFIG_3	GPIO_79	P3	DI B-PD:nppukp	Boot configuration control bit 3 Configurable I/O
AE23	BOOT_CONFIG_2	GPIO_78	P3	DI B-PD:nppukp	Boot configuration control bit 2 Configurable I/O
AE7	BOOT_CONFIG_1	GPIO_77	P3	DI B-PD:nppukp	Boot configuration control bit 1 Configurable I/O
AD8	BOOT_CONFIG_0	GPIO_76	P3	DI B-PD:nppukp	Boot configuration control bit 0 Configurable I/O

1. GPIO ‘A/B’ multiplexing is explained in Figure 2-3.
2. See to Table 2-1 for parameter and acronym definitions.

Table 2-7 MSM8x0x wakeup pins for modem power management (MPM)

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
AF2	GPIO_5	P3	B-PD:nppukp	UART Rx wakeup
F29	GPIO_11	P3	B-PD:nppukp	General purpose wakeup
K28	GPIO_12	P3	B-PD:nppukp	General purpose wakeup
L28	GPIO_13	P3	B-PD:nppukp	General-purpose wakeup
N25	GPIO_20	P4	BH-PD:nppukp	General-purpose wakeup
P25	GPIO_21	P3	B-PD:nppukp	UART Rx wakeup
H1	GPIO_25	P3	B-PD:nppukp	General-purpose wakeup
AB2	GPIO_28	P3	B-PD:nppukp	General-purpose wakeup
Y4	GPIO_31	P3	B-PD:nppukp	General-purpose wakeup
AA2	GPIO_34	P3	B-PD:nppukp	General-purpose wakeup
AA1	GPIO_35	P3	B-PD:nppukp	General-purpose wakeup
E4	GPIO_36	P3	B-PD:nppukp	General-purpose wakeup
D2	GPIO_37	P3	B-PD:nppukp	General-purpose wakeup
J4	GPIO_38	P3	B-PD:nppukp	General-purpose wakeup
AG5	GPIO_39	P3	B-PD:nppukp	General-purpose wakeup
AF5	GPIO_40	P3	B-PD:nppukp	General-purpose wakeup
AD6	GPIO_41	P3	B-PD:nppukp	General-purpose wakeup
AF4	GPIO_42	P3	B-PD:nppukp	General-purpose wakeup
AE5	GPIO_43	P3	B-PD:nppukp	General-purpose wakeup
AD5	GPIO_44	P3	B-PD:nppukp	General-purpose wakeup
AF3	GPIO_45	P3	B-PD:nppukp	General-purpose wakeup
AG2	GPIO_46	P3	B-PD:nppukp	General-purpose wakeup
AE4	GPIO_47	P3	B-PD:nppukp	General-purpose wakeup
AG3	GPIO_48	P3	B-PD:nppukp	General-purpose wakeup
P29	GPIO_49	P6	BH-PD:nppukp	General-purpose wakeup
R29	GPIO_50	P6	BH-PD:nppukp	General-purpose wakeup
G26	GPIO_58	P3	B-PD:nppukp	General-purpose wakeup
AB28	GPIO_64	P3	B-PD:nppukp	General-purpose wakeup
G27	GPIO_65	P3	B-PD:nppukp	General-purpose wakeup
AE3	GPIO_90	P3	B-PD:nppukp	General-purpose wakeup
AD4	GPIO_91	P3	B-PD:nppukp	General-purpose wakeup
AC4	GPIO_92	P3	B-PD:nppukp	General-purpose wakeup
J27	GPIO_94	P3	B-PD:nppukp	General-purpose wakeup
J29	GPIO_95	P3	B-PD:nppukp	General-purpose wakeup
J26	GPIO_96	P3	B-PD:nppukp	General-purpose wakeup
J25	GPIO_97	P3	B-PD:nppukp	General-purpose wakeup
AD28	GPIO_98	P3	B-PD:nppukp	General-purpose wakeup
B29	GPIO_105	P7	B-PD:nppukp	SDIO wakeup

Table 2-7 MSM8x0x wakeup pins for modem power management (MPM) (cont.)

Pad #	Pad name	Pad characteristics [1]		Wakeup functional description
		Voltage	Type	
E29	GPIO_107	P7	B-PD:nppukp	SDC card detect wakeup
J28	GPIO_110	P3	B-PD:nppukp	General-purpose wakeup
T25	GPIO_111	P3	B-PD:nppukp	General-purpose wakeup
R25	GPIO_112	P3	B-PD:nppukp	General-purpose wakeup
C1	SDC2_DATA_1	P2	BH-PD:nppukp	SDIO wakeup
C2	SDC2_DATA_3	P2	BH-PD:nppukp	SDC card detect wakeup
H4	SRST_N	P3	DI-PU	JTAG

1. See to Table 2-1 for parameter and acronym definitions.

Table 2-8 Pin descriptions – chipset interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
WTR– Rx baseband interfaces					
AF18	BBRX_CH0_I		–	AI	Baseband receiver input, channel 0, in-phase
AG18	BBRX_CH0_Q		–	AI	Baseband receiver input, channel 0, quadrature
AG16	BBRX_CH1_I		–	AI	Baseband receiver input, channel 1, in-phase
AF16	BBRX_CH1_Q		–	AI	Baseband receiver input, channel 1, quadrature
AF15	BBRX_CH2_I		–	AI	Baseband receiver input, channel 2, in-phase
AG15	BBRX_CH2_Q		–	AI	Baseband receiver input, channel 2, quadrature
AG13	BBRX_CH3_I		–	AI	Baseband receiver input, channel 3, in-phase
AF13	BBRX_CH3_Q		–	AI	Baseband receiver input, channel 3, quadrature
WTR – GNSS Rx baseband interface					
AG10	GNSS_BBI		–	AI	GNSS receiver baseband input, in-phase
AF11	GNSS_BBQ		–	AI	GNSS receiver baseband input, quadrature
WTR – Tx baseband interface					
AF20	TX_DAC0_IM		–	AO	Transmitter DAC 0 output, in-phase minus
AE20	TX_DAC0_IP		–	AO	Transmitter DAC 0 output, in-phase plus
AF21	TX_DAC0_QM		–	AO	Transmitter DAC 0 output, quadrature minus
AG21	TX_DAC0_QP		–	AO	Transmitter DAC 0 output, quadrature plus
AE19	TX_DAC0_VREF		–	AI	Transmitter DAC 0 voltage reference
WTR – GSM transmit phase adjust signals					
AF24	GSM0_TX_PHASE	GPIO_85	P3	DO-Z B-PD:nppukp	GSM0 transmit phase adjust data Configurable I/O
WTR status and control buses					
MIPI_RFFE buses are used to communicate with the WTR device(s); see Table 2-9					

Table 2-8 Pin descriptions – chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
QFE status and control buses					
MIPI_RFFE buses are used to communicate with the QFE devices; see Table 2-9					
PMIC interfaces					
AC29	PMIC_SPMI_CLK		P3	DO	Slave and PBUS interface for PMICs – data
AD29	PMIC_SPMI_DATA		P3	B	Slave and PBUS interface for PMICs – clock
AA27	PS_HOLD		P3	DO	Power-supply hold signal to PMIC
F26	RESIN_N		P3	DI	Reset input
AA26	SLEEP_CLK		P3	DI	Sleep clock
Y25	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz
AA25	CXO_EN		P3	DO	Core crystal oscillator enable
WCN – WLAN signals					
AC11	WLAN_BB_IM		–	AI, AO	WLAN baseband Rx/Tx switched, in-phase minus
AD11	WLAN_BB_IP		–	AI, AO	WLAN baseband Rx/Tx switched, in-phase plus
AE10	WLAN_BB_QM		–	AI, AO	WLAN baseband Rx/Tx switched, quadrature minus
AD10	WLAN_BB_QP		–	AI, AO	WLAN baseband Rx/Tx switched, quadrature plus
AG9	WLAN_REXT		–	AI	WLAN external resistor
AA6	WLAN_XO		–	DI	WLAN reference clock
AF5	WLAN_DATA2	GPIO_40	P3	B B-PD:nppukp	WLAN data bit 2 Configurable I/O
AD6	WLAN_DATA1	GPIO_41	P3	B B-PD:nppukp	WLAN data bit 1 Configurable I/O
AF4	WLAN_DATA0	GPIO_42	P3	B B-PD:nppukp	WLAN data bit 0 Configurable I/O
AE5	WLAN_SET	GPIO_43	P3	DO-Z B-PD:nppukp	WLAN set Configurable I/O
AD5	WLAN_CLK	GPIO_44	P3	DO-Z B-PD:nppukp	WLAN clock Configurable I/O
WCN – Bluetooth signals					
AG3	BT_DATA_STB	GPIO_48	P3	B B-PD:nppukp	Bluetooth dual-function: data and strobe Configurable I/O
AE4	BT_CTL	GPIO_47	P3	DO B-PD:nppukp	Bluetooth control Configurable I/O
AG5	BT_SSBI	GPIO_39	P3	B B-PD:nppukp	Bluetooth single-wire serial bus interface Configurable I/O
WCN – FM signals					
AG2	FM_DATA	GPIO_46	P3	B B-PD:nppukp	FM radio serial data interface Configurable I/O
AF3	FM_SSBI	GPIO_45	P3	B B-PD:nppukp	FM radio single-wire serial bus interface Configurable I/O

1. See to Table 2-1 for parameter and acronym definitions.

Table 2-9 Pin descriptions – RF front-end functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
MIPI_RFFE interfaces					
AG29	RFFE1_CLK	GPIO_66	P3	DO B-PD:nppukp	MIPI_RFFE 1 clock Configurable I/O
AG28	RFFE1_DATA	GPIO_67	P3	B B-PD:nppukp	MIPI_RFFE 1 data Configurable I/O
AG27	RFFE2_CLK	GPIO_68	P3	DO B-PD:nppukp	MIPI_RFFE 2 clock Configurable I/O
AF27	RFFE2_DATA	GPIO_69	P3	B B-PD:nppukp	MIPI_RFFE 2 data Configurable I/O
AE26	RFFE3_CLK	GPIO_70	P3	DO B-PD:nppukp	MIPI_RFFE 3 clock Configurable I/O
AD25	RFFE3_DATA	GPIO_72	P3	B B-PD:nppukp	MIPI_RFFE 3 data Configurable I/O
AF25	RFFE4_CLK	GPIO_88	P3	DO B-PD:nppukp	MIPI_RFFE 4 clock Configurable I/O
AF26	RFFE4_DATA	GPIO_89	P3	B B-PD:nppukp	MIPI_RFFE 4 data Configurable I/O
AD23	RFFE5_CLK	GPIO_86	P3	DO B-PD:nppukp	MIPI_RFFE 5 clock Configurable I/O
AD24	RFFE5_DATA	GPIO_87	P3	B B-PD:nppukp	MIPI_RFFE 5 data Configurable I/O
GPS control signal					
AG24	EXT_GPS_LNA_EN	GPIO_84	P3	DO B-PD:nppukp	External GPS LNA enable Configurable I/O
Power amplifier control signals					
AE26	PA_ON0	GPIO_70	P3	DO B-PD:nppukp	Power amplifier enable 0; only high for Tx Configurable I/O
AE25	PA_ON1	GPIO_71	P3	DO B-PD:nppukp	Power amplifier enable 1; only high for Tx Configurable I/O
AD25	PA_ON2	GPIO_72	P3	DO B-PD:nppukp	Power amplifier enable 2; only high for Tx Configurable I/O
AG6	PA_ON3	GPIO_73	P3	DO B-PD:nppukp	Power amplifier enable 3; only high for Tx Configurable I/O
AF7	PA_ON4	GPIO_74	P3	DO B-PD:nppukp	Power amplifier enable 4; only high for Tx Configurable I/O
AD7	PA_ON5	GPIO_75	P3	DO B-PD:nppukp	Power amplifier enable 5; only high for Tx Configurable I/O
AD22	PA0_RANGE1	GPIO_79	P3	DO B-PD:nppukp	PA set 0 range control bit 1 Configurable I/O
AE23	PA0_RANGE0	GPIO_78	P3	DO B-PD:nppukp	PA set 0 range control bit 0 Configurable I/O

Table 2-9 Pin descriptions – RF front-end functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
General RF control (GRFC) signals					
AG24	GRFC_28	GPIO_84	P3	DO B-PD:nppukp	Generic RF controller bit 28 Configurable I/O
AF24	GRFC_27	GPIO_85	P3	DO B-PD:nppukp	Generic RF controller bit 27 Configurable I/O
AF23	GRFC_13	GPIO_83	P3	DO B-PD:nppukp	Generic RF controller bit 13 Configurable I/O
AG25	GRFC_12	GPIO_82	P3	DO B-PD:nppukp	Generic RF controller bit 12 Configurable I/O
AF8	GRFC_11	GPIO_81	P3	DO B-PD:nppukp	Generic RF controller bit 11 Configurable I/O
AE8	GRFC_10	GPIO_80	P3	DO B-PD:nppukp	Generic RF controller bit 10 Configurable I/O
AD22	GRFC_9	GPIO_79	P3	DO B-PD:nppukp	Generic RF controller bit 9 Configurable I/O
AE23	GRFC_8	GPIO_78	P3	DO B-PD:nppukp	Generic RF controller bit 8 Configurable I/O
AE7	GRFC_7	GPIO_77	P3	DO B-PD:nppukp	Generic RF controller bit 7 Configurable I/O
AD8	GRFC_6	GPIO_76	P3	DO B-PD:nppukp	Generic RF controller bit 6 Configurable I/O
AD7	GRFC_5	GPIO_75	P3	DO B-PD:nppukp	Generic RF controller bit 5 Configurable I/O
AF7	GRFC_4	GPIO_74	P3	DO B-PD:nppukp	Generic RF controller bit 4 Configurable I/O
AG6	GRFC_3	GPIO_73	P3	DO B-PD:nppukp	Generic RF controller bit 3 Configurable I/O
AD25	GRFC_2	GPIO_72	P3	DO B-PD:nppukp	Generic RF controller bit 2 Configurable I/O
AE25	GRFC_1	GPIO_71	P3	DO B-PD:nppukp	Generic RF controller bit 1 Configurable I/O
AE26	GRFC_0	GPIO_70	P3	DO B-PD:nppukp	Generic RF controller bit 0 Configurable I/O

1. See to Table 2-1 for parameter and acronym definitions.

Table 2-10 Pin descriptions – general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AF29	GPIO_0	 BLSP3_3 MI2S_2_WS	P3	B-PD:nppukp B DO	Configurable I/O BLSP #3, bit 3; SPI only MI2S #2 word select (L/R)
AE28	GPIO_1	 BLSP3_2 MI2S_2_SCK	P3	B-PD:nppukp B B	Configurable I/O BLSP #3, bit 2; SPI only MI2S #2 bit clock
AE27	GPIO_2	 BLSP3_1 MI2S_2_D0	P3	B-PD:nppukp B B	Configurable I/O BLSP #3, bit 1; SPI only MI2S #2 serial data channel 0
AF28	GPIO_3	 BLSP3_0 MI2S_2_D1	P3	B-PD:nppukp B B	Configurable I/O BLSP #3, bit 0; SPI only MI2S #2 serial data channel 1
AE2	GPIO_4	 BLSP1_3 BLSP3_SPI_CS3_N DMIC0_CLK	P3	B-PD:nppukp B DO-Z DO	Configurable I/O BLSP #1, bit 3; SPI, UART Chip select 3 for SPI on BLSP3 Digital MIC0 clock
AF2	GPIO_5	 BLSP1_2 BLSP2_SPI_CS3_N DMIC0_DATA	P3	B-PD:nppukp B DO-Z DI	Configurable I/O BLSP #1, bit 2; SPI, UART Chip select 3 for SPI on BLSP2 Digital MIC0 data
AF1	GPIO_6	 BLSP1_1	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 1; SPI, UART, or I2C
AG1	GPIO_7	 BLSP1_0	P3	B-PD:nppukp B	Configurable I/O BLSP #1, bit 0; SPI, UART, or I2C
F28	GPIO_8	 BLSP6_3 EBI2_A_D[2]	P3	B-PD:nppukp B B	Configurable I/O BLSP #6, bit 3; SPI only EBI2 address data bit 2
G28	GPIO_9	 BLSP6_2 EBI2_A_D[1]	P3	B-PD:nppukp B B	Configurable I/O BLSP #6, bit 2; SPI only EBI2 address data bit 1
H28	GPIO_10	 BLSP6_1 EBI2_A_D[0]	P3	B-PD:nppukp B B	Configurable I/O BLSP #6, bit 1; SPI or I2C EBI2 address data bit 0
F29	GPIO_11	 BLSP6_0 EBI2_NAND_CS_N	P3	B-PD:nppukp B DO	Configurable I/O BLSP #6, bit 0; SPI or I2C EBI2 chip select for NAND
K28	GPIO_12	 BLSP4_3 GP_CLK_2B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #4, bit 3; SPI only General-purpose clock output 2B
L28	GPIO_13	 BLSP4_2 GP_CLK_3B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #4, bit 2; SPI only General-purpose clock output 3B
L29	GPIO_14	 BLSP4_1 GP_CLK_1B	P3	B-PD:nppukp B DO	Configurable I/O BLSP #4, bit 1; SPI or I2C General-purpose clock output 1B

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
M29	GPIO_15	BLSP4_0	P3	B-PD:nppukp B	Configurable I/O BLSP #4, bit 0; SPI or I2C
F4	GPIO_16	BLSP5_3	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 3; SPI only
F2	GPIO_17	BLSP5_2 BLSP2_SPI_CS2_N	P3	B-PD:nppukp B DO-Z	Configurable I/O BLSP #5, bit 2; SPI only Chip select 2 for SPI on BLSP2
E1	GPIO_18	BLSP5_1	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 1; SPI or I2C
E2	GPIO_19	BLSP5_0	P3	B-PD:nppukp B	Configurable I/O BLSP #5, bit 0; SPI or I2C
N25	GPIO_20	UIM3_DATA BLSP2_3 GP_PDM_0A	P4	BH-PD:nppukp B B DO	Configurable I/O UIM3 data BLSP #2, bit 3; SPI, UART General-purpose PDM output 0A
P25	GPIO_21	UIM3_PRESENT BLSP2_2 GP_PDM_1A	P3	B-PD:nppukp DI B DO	Configurable I/O UIM3 presence detection BLSP #2, bit 2; SPI, UART General-purpose PDM output 1A
P26	GPIO_22	UIM3_RESET GP_PDM_2A	P4	BH-PD:nppukp DO DO	Configurable I/O UIM3 reset General-purpose PDM output 2A
P27	GPIO_23	UIM3_CLK	P4	BH-PD:nppukp DO	Configurable I/O UIM3 clock
H2	GPIO_24	MDP_VSYNC_P	P3	B-PD:nppukp DI	Configurable I/O MDP vertical sync – primary
H1	GPIO_25	DSI_RST MDP_VSYNC_S	P3	B-PD:nppukp DO DI	Configurable I/O Display reset MDP vertical sync – secondary
AC2	GPIO_26	CAM_MCLK0 GP_PDM_0B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 0 General-purpose PDM output 0B
AC1	GPIO_27	CAM_MCLK1 GP_PDM_1B	P3	B-PD:nppukp DO DO	Configurable I/O Camera master clock 1 General-purpose PDM output 1B
AB2	GPIO_28	WEBCAM_RST_N GP_PDM_2B	P3	B-PD:nppukp DO DO	Configurable I/O Webcam reset General-purpose PDM output 2B
AB3	GPIO_29	BLSP3_3	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 3; I2C only
AB4	GPIO_30	BLSP3_2	P3	B-PD:nppukp B	Configurable I/O BLSP #3, bit 2; I2C only
Y4	GPIO_31	CCI_TIMER0 GP_CLK0	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 0 General-purpose clock 0

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AA4	GPIO_32	 CCI_TIMER1 GP_CLK1	P3	B-PD:nppukp DO DO	Configurable I/O Camera control interface timer 1 General-purpose clock 1
Y3	GPIO_33	 CCI_ASYNC0	P3	B-PD:nppukp DI	Configurable I/O Camera control interface async 0
AA2	GPIO_34	 CAM1_STANDBY_N	P3	B-PD:nppukp DO	Configurable I/O Camera 1 standby
AA1	GPIO_35	 CAM1_RST_N	P3	B-PD:nppukp DO	Configurable I/O Camera 1 reset
E4	GPIO_36		P3	B-PD:nppukp	Configurable I/O
D2	GPIO_37	 BACKLIGHT_EN BLSP1_SPI_CS2_N FORCED_USB_BOOT	P3	B-PD:nppukp DO DO-Z DI	Configurable I/O Backlight enable Chip select 2 for SPI on BLSP1 Force USB boot control
J4	GPIO_38	 SD_CARD_DET_N CCI_TIMER2	P3	B-PD:nppukp DI DO	Configurable I/O Secure digital card detection Camera control interface timer 2
AG5	GPIO_39	 BT_SSBI	P3	B-PD:nppukp B	Configurable I/O Bluetooth single-wire serial bus interface
AF5	GPIO_40	 WLAN_DATA2	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 2
AD6	GPIO_41	 WLAN_DATA1	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 1
AF4	GPIO_42	 WLAN_DATA0	P3	B-PD:nppukp B	Configurable I/O WLAN data bit 0
AE5	GPIO_43	 WLAN_SET	P3	B-PD:nppukp DO-Z	Configurable I/O WLAN set
AD5	GPIO_44	 WLAN_CLK	P3	B-PD:nppukp DO-Z	Configurable I/O WLAN clock
AF3	GPIO_45	 FM_SSBI	P3	B-PD:nppukp B	Configurable I/O FM radio single-wire serial bus interface
AG2	GPIO_46	 FM_DATA	P3	B-PD:nppukp B	Configurable I/O FM radio serial data interface
AE4	GPIO_47	 BT_CTL	P3	B-PD:nppukp DO	Configurable I/O Bluetooth control
AG3	GPIO_48	 BT_DATA_STB	P3	B-PD:nppukp B	Configurable I/O Bluetooth dual function: data and strobe
P29	GPIO_49	 UIM2_DATA GP_CLK_1A	P6	BH-PD:nppukp B DO	Configurable I/O UIM2 data General-purpose clock output 1A
R29	GPIO_50	 UIM2_CLK GP_CLK_2A	P6	BH-PD:nppukp DO DO	Configurable I/O UIM2 clock General-purpose clock output 2A

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
R28	GPIO_51	 UIM2_RESET GP_CLK_3A	P6	BH-PD:nppukp DO DO	Configurable I/O UIM2 reset General-purpose clock output 3A
T28	GPIO_52	 UIM2_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM2 presence detection
N28	GPIO_53	 UIM1_DATA	P5	BH-PD:nppukp B	Configurable I/O UIM1 data
P28	GPIO_54	 UIM1_CLK	P5	BH-PD:nppukp DO	Configurable I/O UIM1 clock
M28	GPIO_55	 UIM1_RESET	P5	BH-PD:nppukp DO	Configurable I/O UIM1 reset
U28	GPIO_56	 UIM1_PRESENT	P3	B-PD:nppukp DI	Configurable I/O UIM1 presence detection
W27	GPIO_57	 UIM_BATT_ALARM	P3	B-PD:nppukp DI	Configurable I/O UIM battery alarm
G26	GPIO_58	 SMB_INT	P3	B-PD:nppukp DO	Configurable I/O SMB charger interrupt
W28	GPIO_59	 CDC_PDM0_CLK SPKR_MI^{2}S_1_MCLK_A	P3	B-PD:nppukp DO B	Configurable I/O Audio codec PDM 0 clock Speaker MI^{2}S #1 master clock A
Y28	GPIO_60	 CDC_PDM0_SYNC SPKR_MI^{2}S_1_SCK_A BOOT_CONFIG_14	P3	B-PD:nppukp DO B DI	Configurable I/O Audio codec PDM 0 sync Speaker MI^{2}S #1 bit clock A Boot configuration control bit 14
Y29	GPIO_61	 CDC_PDM0_TX0 SPKR_MI^{2}S_1_WS_A	P3	B-PD:nppukp DI B	Configurable I/O Audio codec PDM 0 transmit 0 Speaker MI^{2}S #1 word select (L/R) A
AA29	GPIO_62	 CDC_PDM0_RX0 SPKR_MI^{2}S_1_D0_A BOOT_CONFIG_11	P3	B-PD:nppukp DO DO DI	Configurable I/O Audio codec PDM 0 receive 0 Speaker MI^{2}S #1 serial data channel 0 A Boot configuration control bit 11
AA28	GPIO_63	 CDC_PDM0_RX1 SPKR_MI^{2}S_1_D1_A BOOT_CONFIG_12	P3	B-PD:nppukp DO DO DI	Configurable I/O Audio codec PDM 0 receive 1 Speaker MI^{2}S #1 serial data channel 1 A Boot configuration control bit 12
AB28	GPIO_64	 CDC_PDM0_RX2 BOOT_CONFIG_13	P3	B-PD:nppukp DO DI	Configurable I/O Audio codec PDM 0 receive 2 Boot configuration control bit 13
G27	GPIO_65	 MAG_INT BLSP3_SPI_CS2_N BLSP1_SPI_CS3_N	P3	B-PD:nppukp DI DO-Z DO-Z	Configurable I/O Magnometer interrupt Chip select 2 for SPI on BLSP3 Chip select 3 for SPI on BLSP1
AG29	GPIO_66	 RFFE1_CLK BOOT_CONFIG_7	P3	B-PD:nppukp DO DI	Configurable I/O MIPI_RFFE 1 clock Boot configuration control bit 7

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AG28	GPIO_67		P3	B-PD:nppukp	Configurable I/O
		RFFE1_DATA		B	MIPI_RFFE 1 data
AG27	GPIO_68		P3	B-PD:nppukp	Configurable I/O
		RFFE2_CLK		DO	MIPI_RFFE 2 clock
		BOOT_CONFIG_8		DI	Boot configuration control bit 8
AF27	GPIO_69		P3	B-PD:nppukp	Configurable I/O
		RFFE2_DATA		B	MIPI_RFFE 2 data
AE26	GPIO_70		P3	B-PD:nppukp	Configurable I/O
		GRFC_0		DO	Generic RF controller bit 0
		PA_ON0		DO	Power amplifier enable 0; only high for Tx
		RFFE3_CLK		DO	MIPI_RFFE 3 clock
AE25	GPIO_71		P3	B-PD:nppukp	Configurable I/O
		GRFC_1		DO	Generic RF controller bit 1
		PA_ON1		DO	Power amplifier enable 1; only high for Tx
AD25	GPIO_72		P3	B-PD:nppukp	Configurable I/O
		GRFC_2		DO	Generic RF controller bit 2
		PA_ON2		DO	Power amplifier enable 2; only high for Tx
		RFFE3_DATA		B	MIPI_RFFE 3 data
AG6	GPIO_73		P3	B-PD:nppukp	Configurable I/O
		GRFC_3		DO	Generic RF controller bit 3
		PA_ON3		DO	Power amplifier enable 3; only high for Tx
AF7	GPIO_74		P3	B-PD:nppukp	Configurable I/O
		GRFC_4		DO	Generic RF controller bit 4
		PA_ON4		DO	Power amplifier enable 4; only high for Tx
AD7	GPIO_75		P3	B-PD:nppukp	Configurable I/O
		GRFC_5		DO	Generic RF controller bit 5
		PA_ON5		DO	Power amplifier enable 5; only high for Tx
AD8	GPIO_76		P3	B-PD:nppukp	Configurable I/O
		GRFC_6		DO	Generic RF controller bit 6
		BOOT_CONFIG_0		DI	Boot configuration control bit 0
AE7	GPIO_77		P3	B-PD:nppukp	Configurable I/O
		GRFC_7		DO	Generic RF controller bit 7
		BOOT_CONFIG_1		DI	Boot configuration control bit 1
AE23	GPIO_78		P3	B-PD:nppukp	Configurable I/O
		GRFC_8		DO	Generic RF controller bit 8
		PA0_RANGE0		DO	PA set 0 range control bit 0
		BOOT_CONFIG_2		DI	Boot configuration control bit 2
AD22	GPIO_79		P3	B-PD:nppukp	Configurable I/O
		GRFC_9		DO	Generic RF controller bit 9
		PA0_RANGE1		DO	PA set 0 range control bit 1
		BOOT_CONFIG_3		DI	Boot configuration control bit 3
AE8	GPIO_80		P3	B-PD:nppukp	Configurable I/O
		GRFC_10		DO	Generic RF controller bit 10
		BOOT_CONFIG_4		DI	Boot configuration control bit 4
AF8	GPIO_81		P3	B-PD:nppukp	Configurable I/O
		GRFC_11		DO	Generic RF controller bit 11

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AG25	GPIO_82		P3	B-PD:nppukp	Configurable I/O
		GRFC_12		DO	Generic RF controller bit 12
		BOOT_CONFIG_5		DI	Boot configuration control bit 5
AF23	GPIO_83		P3	B-PD:nppukp	Configurable I/O
		GRFC_13		DO	Generic RF controller bit 13
AG24	GPIO_84		P3	B-PD:nppukp	Configurable I/O
		EXT_GPS_LNA_EN		DO	GPS external LNA enable
		GRFC_28		DO	Generic RF controller bit 28
		BOOT_CONFIG_6		DI	Boot configuration control bit 6
AF24	GPIO_85		P3	B-PD:nppukp	Configurable I/O
		GSM0_TX_PHASE		DO-Z	GSM0 transmit phase adjust data
		GRFC_27		DO	Generic RF controller bit 27
AD23	GPIO_86		P3	B-PD:nppukp	Configurable I/O
		RFFE5_CLK		DO	MIPI_RFFE 5 clock
		BOOT_CONFIG_9		DI	Boot configuration control bit 9
AD24	GPIO_87		P3	B-PD:nppukp	Configurable I/O
		RFFE5_DATA		B	MIPI_RFFE 5 data
AF25	GPIO_88		P3	B-PD:nppukp	Configurable I/O
		RFFE4_CLK		DO	MIPI_RFFE 4clock
		BOOT_CONFIG_10		DI	Boot configuration control bit 10
AF26	GPIO_89		P3	B-PD:nppukp	Configurable I/O
		RFFE4_DATA		B	MIPI_RFFE 4 data
AE3	GPIO_90		P3	B-PD:nppukp	Configurable I/O
		KYPD_SNS0		DI	Keypad sense bit 0
AD4	GPIO_91		P3	B-PD:nppukp	Configurable I/O
		KYPD_SNS1		DI	Keypad sense bit 1
AC4	GPIO_92		P3	B-PD:nppukp	Configurable I/O
		KYPD_SNS2		DI	Keypad sense bit 2
AC3	GPIO_93		P3	B-PU:nppdkp	Configurable I/O
J27	GPIO_94		P3	B-PD:nppukp	Configurable I/O
		ALSP_INT		DI	Ambient light sensor interrupt
		SPKR_MI^{2}S_1_SCK_B		B	Speaker MI^{2}S #1 bit clock B
J29	GPIO_95		P3	B-PD:nppukp	Configurable I/O
		BLSP3_SPI_CS1_N		DO-Z	Chip select 1 for SPI on BLSP3
		SPKR_MI^{2}S_1_D0_B		DO	Speaker MI^{2}S #1 serial data channel 0 B
J26	GPIO_96		P3	B-PD:nppukp	Configurable I/O
		GYRO_ACCEL_INT_N		DI	Gyro/accelerator interrupt
		SPKR_MI^{2}S_1_D1_B		DO	Speaker MI^{2}S #1 serial data channel 1 B
		GP_MN		DO	General-purpose M/N:D counter output
J25	GPIO_97		P3	B-PD:nppukp	Configurable I/O
		HDSET_DET		DI	Headset detection
		BLSP1_SPI_CS1_N		DO-Z	Chip select 1 for SPI on BLSP1

Table 2-10 Pin descriptions – general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AD28	GPIO_98	MI2S_2_MCLK SPKR_MI2S_1_MCLK_B BLSP2_SPI_CS1_N	P3	B-PD:nppukp B DO DO-Z	Configurable I/O MI2S #2 master clock Speaker MI2S #1 master clock B Chip select 1 for SPI on BLSP2
H29	GPIO_99	SD_WRITE_PROTECT	P3	B-PD:nppukp DI	Configurable I/O Secure digital card write protection
C28	GPIO_100	SDC1_CLK EBI2_OE_N	P7	B-NP:pdpukp B DO	Configurable I/O Secure digital controller 1 clock EBI2 output enable
E26	GPIO_101	SDC1_DATA_7 EBI2_ALE_N	P7	B-PD:nppukp B DO	Configurable I/O Secure digital controller 1 data bit 7 EBI2 address latch enable
D28	GPIO_102	SDC1_DATA_6 EBI2_CLE_N	P7	B-PD:nppukp B DO	Configurable I/O Secure digital controller 1 data bit 6 EBI2 command latch enable
D27	GPIO_103	SDC1_DATA_5 EBI2_A_D[4]	P7	B-PD:nppukp B B	Configurable I/O Secure digital controller 1 data bit 5 EBI2 address data bit 4
A29	GPIO_104	SDC1_DATA_4 EBI2_A_D[5]	P7	B-PD:nppukp B B	Configurable I/O Secure digital controller 1 data bit 4 EBI2 address data bit 5
B29	GPIO_105	SDC1_DATA_3 EBI2_A_D[7]	P7	B-PD:nppukp B B	Configurable I/O Secure digital controller 1 data bit 3 EBI2 address data bit 7
C29	GPIO_106	SDC1_DATA_2 EBI2_A_D[6]	P7	B-PD:nppukp B B	Configurable I/O Secure digital controller 1 data bit 2 EBI2 address data bit 6
E29	GPIO_107	SDC1_DATA_1 EBI2_A_D[3]	P7	B-PD:nppukp B B	Configurable I/O Secure digital controller 1 data bit 1 EBI2 address data bit 3
E28	GPIO_108	SDC1_DATA_0 EBI2_WE_N	P7	B-PD:nppukp B DO	Configurable I/O Secure digital controller 1 data bit 0 EBI2 write enable
E27	GPIO_109	SDC1_CMD EBI2_BUSY_N	P7	B-PD:nppukp B DI	Configurable I/O Secure digital controller 1 command EBI2 busy signal for NAND
J28	GPIO_110	SPKR_MI2S_1_WS_B	P3	B-PD:nppukp DO	Configurable I/O Speaker MI2S #1 word select (L/R) B
T25	GPIO_111	BLSP2_1	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 1; SPI, UART, or I2C
R25	GPIO_112	BLSP2_0	P3	B-PD:nppukp B	Configurable I/O BLSP #2, bit 0; SPI, UART, or I2C

1. See to Table 2-1 for parameter and acronym definitions.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take necessary steps to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pullup or pulldown
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, QTI provides an Excel spreadsheet that lists all GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the link below to download the *MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) GPIO Configuration Spreadsheet* (80-NP408-1B) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-NP408-1B

If you have permission to view the document, a prompt will be presented for initiating the download.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

Table 2-11 Pin descriptions – No connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
A1, A28, B28, M22, P21, W25, W26, Y5, AA5, AB20, AB22, AB26, AC5, AC26, AG8	DNC	Do not connect; connected internally, do not connect externally

Table 2-12 Pin descriptions – power supply pins

Pad #	Pad name	Functional description
AB13, AC15	VDD_A1	Power for analog circuits – low voltage
AB14, AB15, AB18	VDD_A2	Power for analog circuits – high voltage
J16, J17, J20, J21, K16, K17, K20, L18, L19, M16, M17, M20, M21, N17, N20, N21	VDD_APC	Power for applications microprocessors
H16, H22, K8, K14, M10, M12, M14, T12, T14, T20, T22, Y8, Y12, Y16	VDD_CORE	Power for digital core circuits
G13, G15, G19, H9, H11, H12, H14, H17, H19, J15, K21, K22, L15, T10, T16, V10, V20, Y14, Y19	VDD_MEM	Power for on-chip memory
R5, V5, V6	VDD_MIPI	Power for MIPI circuits (CSI and DSI)
M5	VDD_MIPI_DSI_PLL	Power for MIPI _DSI PHY PLL
E7, E8, E9, E23, E24, F9, F10, F14, F18, F19, F22	VDD_P1	Power for pad group 1 – EBI pads
E3	VDD_P2	Power for pad group 2 – SDC2 pads
H24, K6, K7, AB8, AB24, AC8, AC23	VDD_P3	Power for pad group 3 – most I/O pads
L25	VDD_P4	Power for pad group 4 – UIM3 pads
L27	VDD_P5	Power for pad group 5 – UIM1 pads
L26	VDD_P6	Power for pad group 6 – UIM2 pads
G24	VDD_P7	Power for pad group 7 – SDC1 pads
T18	VDD_PLL1	Power for PLL circuits – low voltage
P16, Y10, Y18	VDD_PLL2	Power for PLL circuits – high voltage
P8	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise GND
G23, J8	VDD_SDC_CDC	Power for secure digital calibration delay circuits
U25	VDD_USB_1P8	Power for USB PHY interface – low voltage
T26	VDD_USB_3P3	Power for USB PHY interface – high voltage
V25	VDD_USB_CORE	Power for USB core
AB11	VDD_WLAN	Power for WLAN ADC circuits

Table 2-13 Pin descriptions – ground pins

Pad #	Pad name	Functional description
A14, B9, B24, C3, C4, C17, C26, C27, D3, D4, D5, D6, D8, D11, D12, D16, D17, D20, D23, D26, E5, E6, E25, F6, F11, F13, F15, F17, F21, F23, F24, F25, G9, G11, G25, H5, H8, H10, H25, H26, J5, J6, J18, J19, J24, K4, K5, K10, K12, K18, K19, K23, L4, L5, L16, L17, L20, L21, L24, M4, M8, M18, M19, M25, M26, M27, N5, N16, N18, N19, N26, N27, P1, P4, P10, P12, P14, P17, P18, P19, P20, P22, R4, R7, T4, T8, U24, V4, V8, V12, V14, V16, V18, V22, V24, W5, W6, W11, W12, W14, W17, W18, Y1, Y20, Y22, AB9, AB25, AB27, AC9, AC12, AC13, AC14, AC16, AC17, AC18, AC24, AC25, AC27, AC28, AD1, AD9, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD20, AD21, AE6, AE9, AE11, AE12, AE13, AE14, AE15, AE16, AE17, AE21, AE22, AF6, AF9, AF10, AF12, AF14, AF17, AF22, AG12, AG22	GND	Ground

3 Electrical specifications

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-1) reflect conditions that the MSM8x0x device may be exposed to beyond the operating limits, without experiencing immediate functional failure. They are limiting values, to be considered individually when all other parameters are within their specified operating ranges. Functionality and long-term reliability can only be expected within the operating conditions, as described in Section 3.2.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power-supply voltages				
VDD_A1	Analog circuits	-0.30	1.56	V
VDD_A2	Analog circuits	-0.30	2.16	V
VDD_APC	Application microprocessors	-0.30	1.62	V
VDD_CORE	Digital core circuits	-0.30	1.62	V
VDD_MEM	On-chip memory	-0.30	1.62	V
VDD_MIPI_DSI_PLL	Power for MIPI _DSI PHY PLL	-0.30	2.16	V
VDD_P1	Digital pad circuits	-0.30	1.44	V
VDD_P2	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P3	Digital pad circuits	-0.30	2.16	V
VDD_P4	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P5	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P6	Digital pad circuits – 2.95 V Digital pad circuits – 1.80 V	-0.30 -0.30	3.25 2.16	V
VDD_P7	Digital pad circuits	-0.30	2.45	V
VDD_PLL1	PLL circuits	-0.30	1.62	V
VDD_PLL2	PLL circuits	-0.30	2.16	V
VDD_QFPROM_ PRG	QFPROM programming voltage	-0.30	2.16	V
VDD_USBPHY_1P8	USB PHY low-voltage circuit	-0.30	2.16	V
VDD_USBPHY_3P3	USB PHY high-voltage circuit	-0.30	3.63	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_USB_CORE	Core circuits for USB	-0.30	1.44	V
VDD_WLAN	WLAN ADC circuits	-0.30	1.56	V
Signal pins				
V_IN	Voltage on any nonpower input pin	-0.3	V_{xx} + 20% [1]	V
VIN_P7	Voltage on any eMMC input pin	-0.30	2.45	V
I_IN	Latch-up current	-100	100	mA
ESD protection – see Section 5.3.2				
Thermal conditions – see Section 4.5				

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters that are under the control of the design team: power-supply voltage, power-distribution impedances, and thermal conditions (Table 3-3). The MSM8x0x meets all performance specifications listed in Section 3.3 through Section 3.12, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions for APC and CORE rails

Parameter		Min	Typ	Max	Unit
PM8916-1					
VDD_APC	Quad Cortex A7 [operating at a maximum frequency of 1.094 GHz] or 1.267 GHz (-AA variants)]				
	Turbo mode	1.06	–	1.41	V
	Nominal mode	1.00	–	1.29	V
	SVS* mode	1.00	1.05	1.11	V
VDD_CORE	Turbo mode	1.065	–	1.41	V
	Nominal mode	1.00	–	1.29	V
	SVS mode	0.84	–	1.11	V
PM8909					
VDD_CORE + VDD_APC	Turbo mode	1.065	–	1.41	V
	Nominal mode	1.00	–	1.29	V
	SVS* mode	1.00	1.05	1.11	V
	SVS mode (APC power collapse)	0.84	–	1.11	V
NOTE: Parts with voltages outside the specified ranges are not guaranteed to operate properly. * AVS Type I is not enabled on APC rail in SVS mode.					

Table 3-3 Operating conditions

Parameter		Min	Typ [2]	Max	Unit
Power-supply voltages					
VDD_A1 VDD_WLAN	Power for analog circuits – low voltage for PA DAC and Tx DAC circuits Power for WLAN ADC circuits	1.25	1.35	1.39	V
VDD_MEM	Power supply for internal memory cores				V
VDD_PLL1	Power for PLL circuits – low voltage				
	Turbo mode	1.14		1.39	
	Nominal mode	1.02		1.27	
	SVS mode	1.00		1.09	
VDD_PLL2	Power for PLL circuits – high voltage	1.75	1.80	1.93	V
VDD_A2	Power for analog circuits – high voltage for analog baseband receiver and S-Video circuits				
VDD_USBPHY_1P8	Power for USB PHY interface – low voltage				
VDD_P1	Power for pad group 1 – EBI pads	1.15	1.20	1.25	V
VDD_MIPI	Power for MIPI circuits (CSI and DSI)				
VDD_USB_HS	Power for core circuits of USB				
VDD_P2	Power for pad group 2				
	SDC2 pads low voltage	1.67	1.8	1.93	V
	SDC2 pads high voltage	2.75	2.95	3.04	V
VDD_P3	Power for pad group 3 – most I/O pads	1.67	1.8	1.93	V
VDD_P4	Power for pad group 4				
	UIM3 pads low voltage	1.67	1.8	1.93	V
	UIM3 pads high voltage	2.75	2.95	3.04	V
VDD_P5	Power for pad group 5				
	UIM1 pads low voltage	1.67	1.8	1.93	V
	UIM1 pads high voltage	2.75	2.95	3.04	V
VDD_P6	Power for pad group 6				
	UIM2 pads low voltage	1.67	1.8	1.93	V
	UIM2 pads high voltage	2.75	2.95	3.04	V
VDD_P7	Power for pad group 7 – SDC1 pads	1.67	1.8	1.93	V
VDD_MIPI_DSI_PLL	Power for MIPI _DSI PHY PLL	1.72	1.8	1.95	V
VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise ground	1.67	1.8	1.93	V
VDD_USBPHY_3P3	Power for USB PHY interface – high voltage	2.97	3.08	3.50	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
T_A [1]	3GPP2-mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP-mode operating temperature (ambient)	-20	+25	+60	°C

1. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.
2. Typical voltages represent the recommended output settings of the companion PMIC device.

3.2.1 Core voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE retention mode. This technique reduces the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization. As in any normal distribution, retention voltages vary across devices. Three fuses are blown to set the core voltage in retention mode. These fuses are used by software.

The fuse locations in Table 3-4 refer to register 0x0005C00C QFPROM_CORR_PTE2.

Table 3-4 Core voltage in retention mode

VDD_CORE [1]	Bit 7 (MSB)	Bit 6	Bit 5 (LSB)
0.65 V	0	0	0
0.5 V	0	0	1

1. The specified VDD_CORE voltages are PMIC settings.

3.3 Power delivery network specification

The following subsections contain the maximum impedance specifications for the power delivery network (PDN).

Design guidelines for the PDN are listed in *Training: Power Delivery Network Design* (80-VT310-13). If PCB designers have difficulty meeting these impedances, contact QTI for assistance.

3.3.1 MSM8x0x PDN specification (PCB only) except MSM8905

The impedances of the distribution networks that deliver power to the MSM are critical to its supply voltages, not just at DC but over a wide range of frequencies. An inadequate PDN could cause the voltage min/max values of MSM power pads to be violated. Table 3-5 and Table 3-6 lists the PDN maximum impedance specifications (for all MSM8x0x variants (including -AA variants) except MSM8905).

Table 3-5 Power distribution network impedance vs. frequency

Power domain	Max impedance (mΩ)				Pin number of positive ports	Pin number of negative ports
	DC	10 Hz	13 MHz	25 MHz		
VDD_MEM	20	79	79	79	All VDD_MEM pins (G13, G15, G19, H9, H11, H12, H14, H17, H19, J15, K21, K22, L15, T10, T16, V10, V20, Y14, Y19)	All GND pins

Table 3-5 Power distribution network impedance vs. frequency

Power domain	Max impedance (mΩ)				Pin number of positive ports	Pin number of negative ports
	DC	10 Hz	13 MHz	25 MHz		
VDD_CORE	6	29	29	59	All VDD_CORE pins (H16, H22, K8, K14, M10, M12, M14, T12, T14, T20, T22, Y8, Y12, Y16)	All GND pins
VDD_APC	9	26	26	52	All VDD_APC pins (J16, J17, J20, J21, K16, K17, K20, L18, L19, M16, M17, M20, M21, N17, N20, N21)	All GND pins

NOTE: PDN AC impedance spec curve is obtained by connecting the max impedance point at 10 Hz, 13 MHz and 25 MHz sequentially.

NOTE: Table 3-5 applies to power grid with separate VDD_CORE/VDD_APC and with combined VDD_CORE/VDD_APC.

NOTE: See *MSM8909/MSM8609/MSM8209/MSM8208/MSM8905 (SDM205) Digital Baseband Design Guidelines/training Slides* (80-NP408-5B) PDN section for distributed PDN guidelines on VDD_CORE.

Table 3-6 Power distribution network impedance vs. frequency

Power domain	Max impedance mΩ	Max effective impedance mΩ			Port number	Pin number of positive ports	Pin number of negative ports
	DC	10 Hz	19 MHz	25 MHz			
VDD_P1	39	110	110	146	1	F9, F10, E7, E8, E9	D6, D8, E6, F6, F11, G9, G11
		110	110	146	2	F14	D12, D16, F13, F15
		110	110	146	3	F18, F19	D17, D20, F17, F21
		110	110	146	4	F22, E23, E24	D23, E25, F23, F24, F25

NOTE: PDN AC effective impedance specification curve is obtained by connecting the max effective impedance point at 10 Hz, 19 MHz and 25 MHz sequentially.

NOTE: Max effective impedance is the sum of self-impedance and coupling impedance with other three ports.

NOTE: See *MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) Digital Baseband Design Guidelines/training Slides* (80-NP408-5B) PDN section for detailed instructions on how to calculate effective impedance.

3.3.2 MSM8905 PDN Specification (PCB only)

The impedances of the distribution networks that deliver power to the MSM are critical to its supply voltages, not just at DC but over a wide range of frequencies. An inadequate PDN could cause the voltage min/max values of MSM power pads to be violated. Table 3-7 and Table 3-8 lists the PDN maximum impedance specifications (for MSM8905 variants (including -AA variants).

Table 3-7 Power distribution network impedance vs. frequency

Power domain	Max impedance (mΩ)			Port number	Pin number of positive ports	Pin number of negative ports
	DC to 10 Hz	1 MHz to 13 MHz	25 MHz			
VDD_APC	9	30	60	1	J16, J17, J20, J21, K16, K17, K20, L18, L19, M16, M17, M20, M21, N17, N20, N21	All GND pins
VDD_CORE	6	29	59	1	H16, H22, K8, K14, M10, M12, M14, T12, T14, T20, T22, Y8, Y12, Y16	All GND pins
VDD_MEM	20	79	79	1	G13, G15, G19, H9, H11, H12, H14, H17, H19, J15, K21, K22, L15, T10, T16, V10, V20, Y14, Y19	All GND pins
VDD_CORE (Distributed)	10	38	38	1	M14, M12, M10, K14, K8	G9, G11, H8, H10, J6, K10, K12, M8,P10, P12, P14
	20	100	100	2	Y16, T22, T20	V16, V18, Y20, Y22, V22
	20	100	100	3	T14, T12, Y12, Y8	AB9, AC9, V8, V12, V14

NOTE: PDN AC impedance spec curve is obtained by connecting the max impedance point at 10 Hz, 13 MHz and 25 MHz sequentially.

NOTE: Table 3-7 applies to power grid with separate VDD_CORE/VDD_APC and with combined VDD_CORE/VDD_APC.

NOTE: See *MSM8909/MSM8609/MSM8209/MSM8208/MSM8905 (SDM205) Digital Baseband Design Guidelines/training Slides* (80-NP408-5B) PDN section for distributed PDN guidelines on VDD_CORE.

Table 3-8 Power distribution network impedance vs. frequency

Power domain	Max impedance mΩ	Max effective impedance mΩ			Port number	Pin number of positive ports	Pin number of negative ports
	DC to 10 Hz	1 MHz	19 MHz	25 MHz			
VDD_P1	39	144	144	188	1	F9, F10, E7, E8, E9	D6, D8, D11, E6, F6, F11, G9, G11
		144	144	188	2	F14	D12, D16, F13, F15
		144	144	188	3	F18, F19	D17, D20, F17, F21
		144	144	188	4	F22, E23, E24	D23, E25, F23, F24, F25

NOTE: PDN AC effective impedance specification curve is obtained by connecting the max effective impedance point at 10 Hz, 19 MHz and 25 MHz sequentially.

NOTE: Max effective impedance is the sum of self-impedance and coupling impedance with other three ports.

NOTE: Refer to *MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) Digital Baseband Design Guidelines/training Slides* (80-NP408-5B) PDN section for detailed instructions on how to calculate effective impedance.

3.4 DC power characteristics

3.4.1 Average operating current

Detailed current-consumption information and details about the operating modes tested are available in the *MSM8x09 Linux Android Current Consumption Data* (80-NP408-7).

3.4.2 Dhrystone and rock bottom maximum power

Table 3-9 lists values for Dhrystone and rock bottom power specifications.

Table 3-9 Dhrystone and rock bottom power specifications

MSM version	Dhrystone (W) at 85°C (T_j) [1] [2]	Rock bottom (mW) at 25°C (T_j) [3]
MSM8909 (1.094 GHz)	2.1	8
MSM8909 (1.267 GHz)	2.3	8

1. Dhrystone should be measured using the QTI custom Dhrystone script that will be provided upon request.
2. The Dhrystone specification applies only to MSM8x0x CS devices. Dhrystone should be run and measured on all four APC together.
3. Rock bottom (VDD_CORE and VDD_MEM) should be measured at VDD_CORE and VDD_MEM rails when
VDD_CORE and VDD_MEM are at retention voltage. Refer to AIR1, Table 3-1 in *MSM8x09 Linux Android Current Consumption Data* (80-NP408-7) for the test setup.

3.5 Power sequencing

The PM8909/PM8208/PM8916-1 includes power-on circuits that provide the proper power sequencing for the entire MSM8x0x chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins. Refer to *PM8909 Power Management IC Device Specification* (80-NP409-1) and *PM8916/PM8916-1 Power Management IC Device Specification* (80-NK808-1) for details.

A high-level summary of the required power-on sequence is as follows:

- VDD_MEM (on-chip memory), VDD_PLL1
- VDD_CORE (digital core circuits), VDD_APC (Cortex A7)
- VREF_SDC (SDC reference voltage)
- VDD_P3 (I/Os), VDD_P7 (SDC1), VDD_DDR_1P8
- VDD_USBPHY_1P8, VDD_PLL2
- VDD_QFPROM_PRG
- VDD_P1 (EBI and DDR I/Os), VDD_DDR_1P2
- EBI0_VREF_XX (LPDDR2/3 reference voltage)
- VDD_USB_3P3
- VDD_P2 (SDC2)

Comments regarding this sequence:

- The core voltage (VDD_CORE) needs to power up before the pad circuits (VDD_Px), so that internal circuits can take control of the I/Os and pads.
- If pad voltages power-up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until VDD_CORE powers on.
- The general-purpose pad voltage (VDD_P3) needs to precede the analog voltages (VDD_Ax), since the SSBIs are initialized to their default states before VDD_Ax powers up (analog circuits are controlled by SSBI).

- Other noncritical supplies are included within the power-on sequence. Any other desired supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when VDD_MEM reaches 90% of its value, then the VDD_CORE supply can start ramping up.

3.6 Digital-logic characteristics

A digital I/O's performance specification depends upon its pad type, its usage, and/or its supply voltage:

- Some are dedicated for interconnections between the MSM8x0x chipset and other ICs within the QTI chipset, and therefore do not require specification.
- Some are defined by existing standards (such as I^2C, SPI). QTI devices comply with those standards and additional specifications are not required.
- All other digital I/Os require performance specifications, and are organized within this section as described in Table 3-10.

Table 3-10 Digital I/Os specified in this section

Pad voltage	Usage	Table
1.2 V	EBI0 (P1)	Table 3-11
1.8 V	GPIO (P3), SDC1 (P7)	Table 3-12
Dual- V (1.8 V/2.95 V)	SDC2 (P2), GPIO (P5, P6, P4), UIM1 (P5), UIM2 (P6), UIM3 (P4)	Table 3-13

Table 3-11 1.2 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
EBI0 pads only (as identified in Table 3-10)					
V_{REF}	Reference voltage		0.49 * V_{DD_Px}	0.51 * V_{DD_Px}	V
V_{IH}	High-level input voltage	CMOS/Schmitt	V_{REF} + 0.13	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	V_{REF} - 0.13	V
I_{IH}	Input high leakage current	No pull-down	–	2	µA
I_{IL}	Input low leakage current	No pull-up	-2	–	µA
I_{IHPD}	Input high leakage current with pull-down		40	200	µA
I_{ILPU}	Input low leakage current with pull-up		-200	-40	µA
I_{OZHKP}	High-level, tri-state leakage current with keeper		-120	-10	µA
I_{OZLKP}	Low-level, tri-state leakage current with keeper		10	120	µA

Table 3-11 1.2 V digital I/O characteristics (cont.)

Parameter		Comments	Min	Max	Unit
V_{OH}	High-level output voltage	CMOS, at rated drive strength[1]	0.9 * V_{DD_Px}	–	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[1]	–	0.1 * V_{DD_Px}	V
$C_{I/O}$	I/O capacitance[2]		1.25	2.50	pF

1. See to Table 2-1 for each output pin's drive strength (IOH and IOL); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.
2. Input capacitance and I/O capacitance values are guaranteed by design, but not 100% tested.

Table 3-12 1.8 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
GPIO (P3) (as identified in Table 3-10)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_Px}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength[1]	V_{DD_Px} - 0.45		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[3]	–	0.45	V
R_P	Pull resistance[2]	Pull-up and pull down	55	390	kΩ
R_K	Keeper resistance[5]		30	150	kΩ
I_{IH}	Input high leakage current[3]	No pull-down	–	1	µA
I_{IL}	Input low leakage current[4]	No pull-up	-1	–	µA
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
$C_{I/O}$	I/O capacitance		–	5	pF
SDC (P7)(as identified in Table 3-10)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_Px}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	V_{DD_Px} - 0.45	–	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.45	V
I_{IH}	Input high leakage current	No pull-down	–	2	µA
I_{IL}	Input low leakage current	No pull-up	-2	–	µA
R_P	Pull resistance[5]	Pull-up and pull-down	10	100	kΩ
R_K	Keeper resistance[1]		10	100	kΩ
C_{IN}	Input capacitance		–	5	pF
RFFE and SPMI pins					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	–	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	–	0.35 * V_{DD_Px}	V

Table 3-12 1.8 V digital I/O characteristics (cont.)

Parameter		Comments	Min	Max	Unit
V_{OH}	High-level output voltage	CMOS, at rated drive strength	0.8 * V_{DD_PX}		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	–	0.2 * V_{DD_Px}	V
R_P	Pull resistance	Pull-up and pull-down	10	50	kΩ
R_K	Keeper resistance		10	50	kΩ
I_{IH}	Input high leakage current	No pull-down	–	1	µA
I_{IL}	Input low leakage current	No pull-up	-1	–	µA
V_{SHYS}	Schmitt hysteresis voltage		165	–	mV

1. See to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.
2. See to Table 2-1 for pull-up, pull-down, and keeper options for each pad (where appropriate).
3. Pad voltage = V_{DD_Px} max.
4. Over all valid pad voltages.
5. See to Table 2-1 for pull-up, pull-down, and keeper options for each pad (where appropriate).

Table 3-13 Dual-voltage 1.8 V/2.95 V digital I/O characteristics

Parameter		Comments	Min	Max	Unit
Common to dual-voltage pads 1.8 V/2.95 V (as identified in Table 3-10)					
R_P	Pull resistance[1]	Pull-up and pull-down	10	100	kΩ
R_K	Keeper resistance[1]		10	100	kΩ
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
$C_{I/O}$	I/O capacitance		–	5	pF
Common to SDC2 pad and UIM pad at 2.95 V only (as identified in Table 3-10)					
I_{IH}	Input high leakage current	No pull-down	–	10	µA
I_{IL}	Input low leakage current	No pull-up	-10	–	µA
Common to UIM pads, either voltage (as identified in Table 3-10)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.7 * V_{DD_Px}	V_{DD_Px} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.2 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength[2]	0.8 * V_{DD_Px}	V_{DD_Px}	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[5]	0	0.4	V
SDC2 pads at 2.95 V only (as identified in Table 3-10)					
V_{IH}	High-level input voltage	CMOS/Schmitt	0.625 * V_{DD_Px}	V_{DD_Px} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.25 * V_{DD_Px}	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength [5]	0.75 * V_{DD_Px}	V_{DD_Px}	V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength[5]	0	0.125 * V_{DD_Px}	V

Table 3-13 Dual-voltage 1.8 V/2.95 V digital I/O characteristics (cont.)

Parameter		Comments	Min	Max	Unit
Common to SDC2 pad and UIM pad at 1.8 V only (as identified in Table 3-10)					
I_{IH}	Input high leakage current	No pull-down	–	2	µA
I_{IL}	Input low leakage current	No pull-up	-2	–	µA
SDC2 pads at 1.8 V only (as identified in Table 3-10)					
V_{IH}	High-level input voltage	CMOS/Schmitt	1.27	2	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.58	V
V_{OH}	High-level output voltage	CMOS, at rated drive strength	1.4		V
V_{OL}	Low-level output voltage	CMOS, at rated drive strength	0	0.45	V

1. See to Table 2-1 for pull-up, pull down, and keeper options for each pad (where appropriate).
2. See to Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 3-1) with respect to the drive current (drive currents are given in Table 2-1). They can be calculated using these relationships:

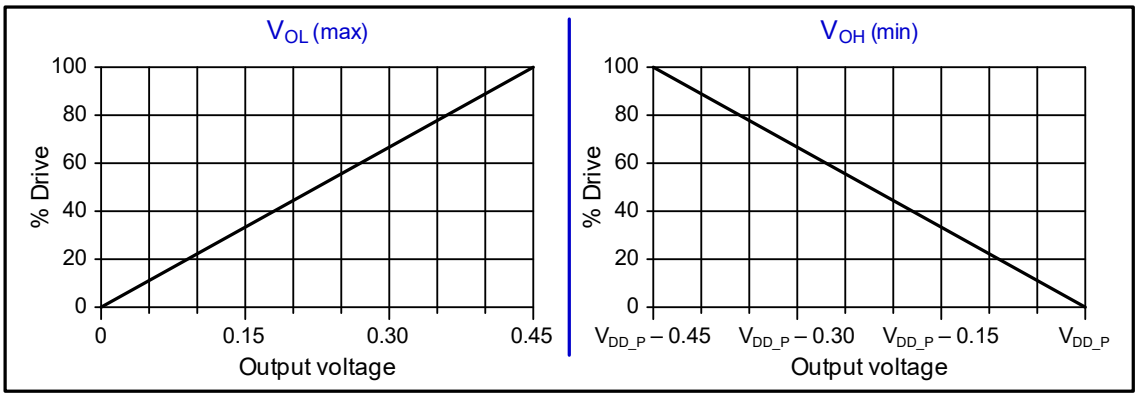


Figure 3-1 IV curve for V_{OL} and V_{OH} (valid for all V_{DD_Px})

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad-design methodologies are included here.

NOTE: All MSM8x0x devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is described further in Section 3.7.2.

3.7.1 Timing-diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-2.

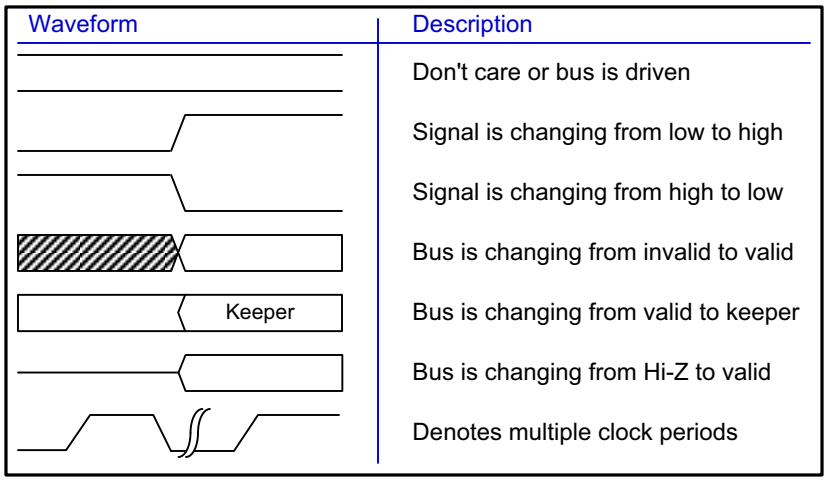


Figure 3-2 Timing-diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus-type signal (multiple bits) – the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal – indicates *don't care*.

3.7.2 Rise and fall time specifications

The testers that characterize MSM8x0x devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-3.

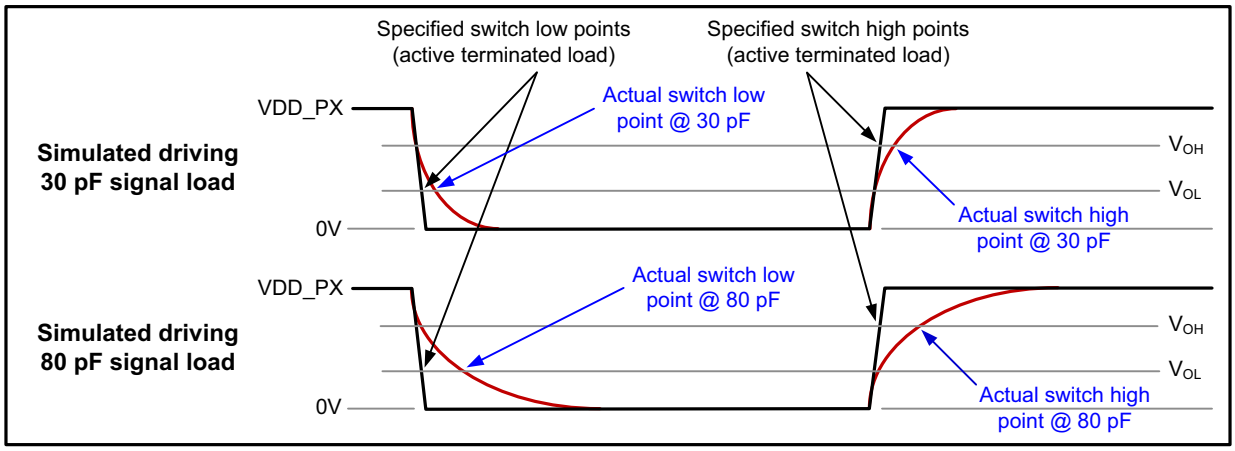


Figure 3-3 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the MSM device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The MSM8x0x device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric with respect to the associated V_{DD_Px} supply (Figure 3-4). The input switch point for pure input-only pads is designed to be $V_{DD\_Px}/2$ (or 50% of V_{DD_Px}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DD_Px} for V_{IL} and 65% of V_{DD_Px} for V_{IH}.

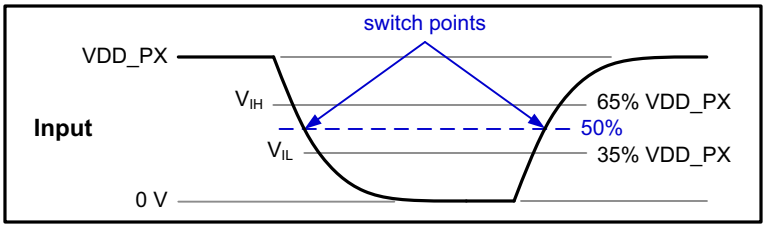


Figure 3-4 Digital input signal switch points

Outputs (address, chip selects, clocks, and so on) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over worst-case process/voltage/temperature. Since the pad output structures (Figure 3-5) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected *zero DC load* outputs are *estimated* to be:

- V_{OH} ~ V_{DD_Px} - 50 mV or more
- V_{OL} ~ 50 mV or less

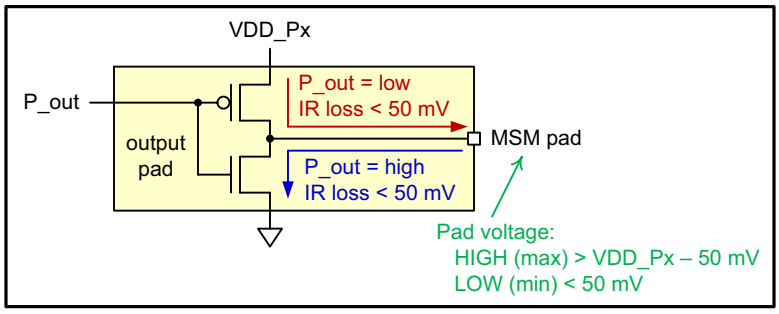


Figure 3-5 Output-pad equivalent circuit

The DC output drive strength can be *approximated* by linear interpolations between V_{OH} (min) and V_{DD_Px} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) will provide approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) will provide approximately 1.25 mA or more at ½ × [V_{DD_Px} - 50 mV + V_{OH} (min)].

The output pads are essentially CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that tend to desensitize the companion radio.

Output drivers' rise time (**t**(r)) and fall time (**t**(f)) values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described above.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers will get worse and hold-time numbers may get better.

3.8.1 EBI0 memory support

The EBI0 port is dedicated to the LPDDR2/3 SDRAM memory that is attached to the top of the MSM8x0x device.

3.8.1.1 EBI0 pad drive strength

Pads for EBI0 are tailored for its 1.2 V interface and are source-terminated. Before the source termination, the pad drive strength is 15 mA to 60 mA. But at the pads, after the source termination, the drive strength at $I_{OL,}$ I_{OH} is equivalent to 0.90 mA to 3.35 mA in nonlinear steps when the JEDEC standard range (90% – 10%) is followed.

3.8.1.2 LPDDR2/3 SDRAM clock

For any timing analysis, the measurement point for all signals is at 50% of VDD_Px. All output timing parameters represent the point of the output signal transition; additional accounting for signal rise and fall times for specific bus loading is required.

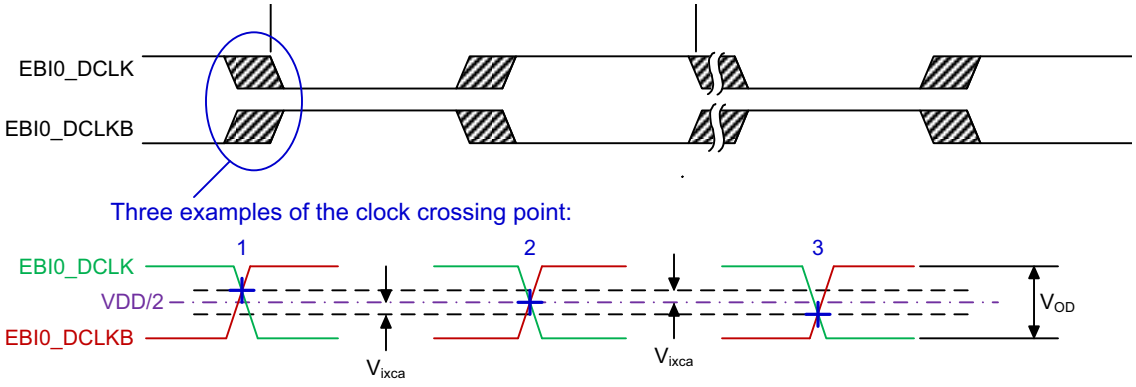


Figure 3-6 DDR SDRAM DCLK and DCLKB

Table 3-14 DDR SDRAM clock-timing parameters

Parameter		Comments	Min	Typ	Max	Unit
$1/t_{CK}$	DDR clock frequency		10	–	533 (LPDDR2) 533 (LPDDR3)	MHz
	Duty cycle		45	–	55	%
V_{ixca} [1]	Clock crossover-point	± offset from VDD/2	–	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

1. Crosstalk due to high CA activity might cause parameters to exceed the VIXCA limit

3.8.1.3 LPDDR2/3 SDRAM strobe

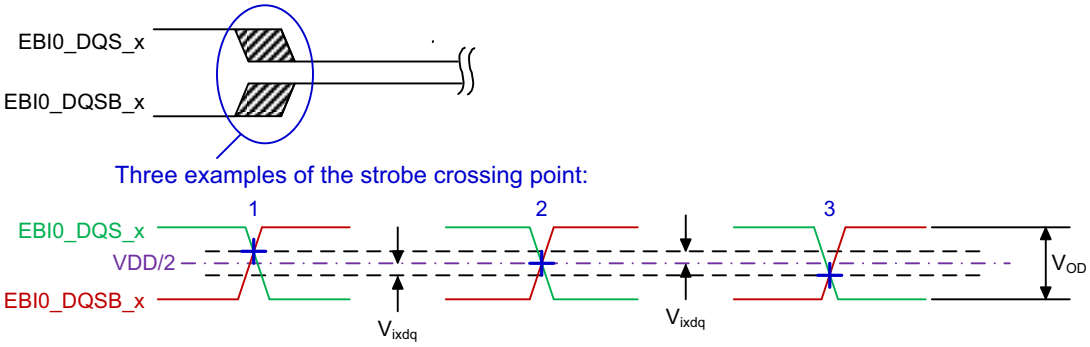


Figure 3-7 DDR SDRAM DQS_x and DQSB_x

Table 3-15 DDR SDRAM strobe timing parameters

Parameter		Comments	Min	Typ	Max	Unit
V_{IXDQ}	Clock cross-over point	± offset from VDDQ/2	–	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

3.8.1.4 LPDDR2 SDRAM read and write timing

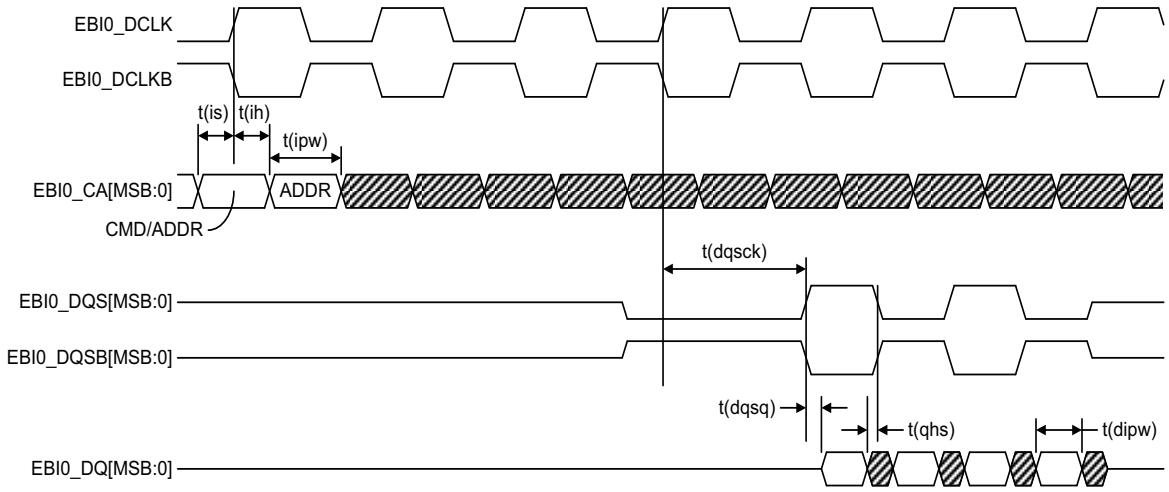


Figure 3-8 DDR SDRAM read timing

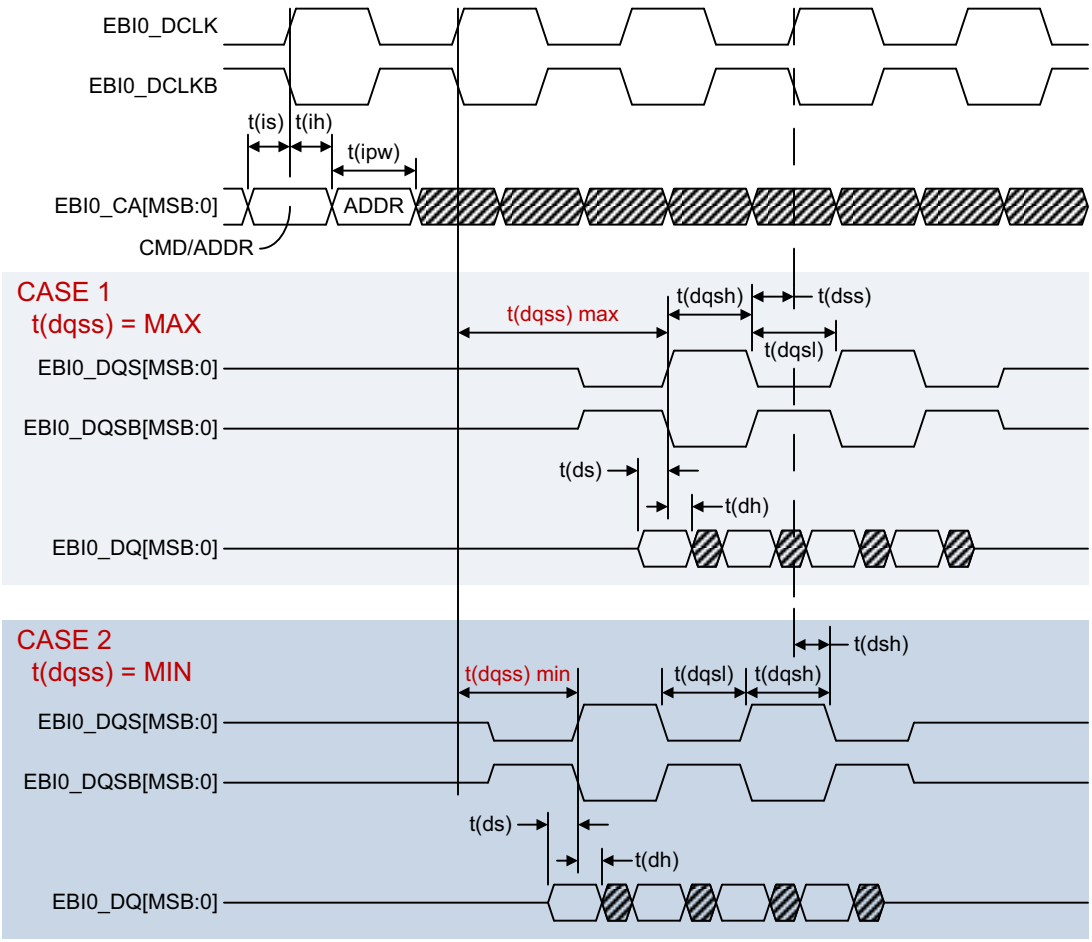


Figure 3-9 DDR SDRAM write timing

Table 3-16 DDR SDRAM read and write timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR2 (533 MHz) – common to read and write						
t(is)	Address and control in setup time before CK		0.22	–	–	ns
t(ih)	Address and control input hold time after CK		0.22	–	–	ns
t(dipw)	DQ and DM pulse width		0.35	–	–	tCK
t(ipw)	Address and control input pulse width		0.40	–	–	tCK
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns
LPDDR2 (533 MHz) – read cycle						
t(dqsck)	DQS access time from clock		2.50	–	5.50	ns

Table 3-16 DDR SDRAM read and write timing specifications (cont.)

Parameter		Comments	Min	Typ	Max	Unit
t(dqsq)	DQS to DQ skew limit		–	–	0.2	ns
t(rpre)	Read preamble		0.90	–	–	t(ck)
t(qhs)	Data hold skew factor		–	–	0.23	ns
LPDDR2 (533 MHz) – write cycle						
t(ds)	DQ and DM input setup time before DQS		0.21	–	–	ns
t(dh)	DQ and DM input hold time after DQS		0.21	–	–	ns
t(dqsh)	DQS input high-level width		0.40	–	–	t(ck)
t(dqsl)	DQS input low-level width		0.40	–	–	t(ck)
t(dqss)	First DQS latching transition		0.75	–	1.25	t(ck)
t(dss)	DQS falling edge to CK setup time		0.20	–	–	t(ck)
t(dsh)	DQS falling edge hold time after CK		0.20	–	–	t(ck)

3.8.1.5 LPDDR3 SDRAM read and write timing

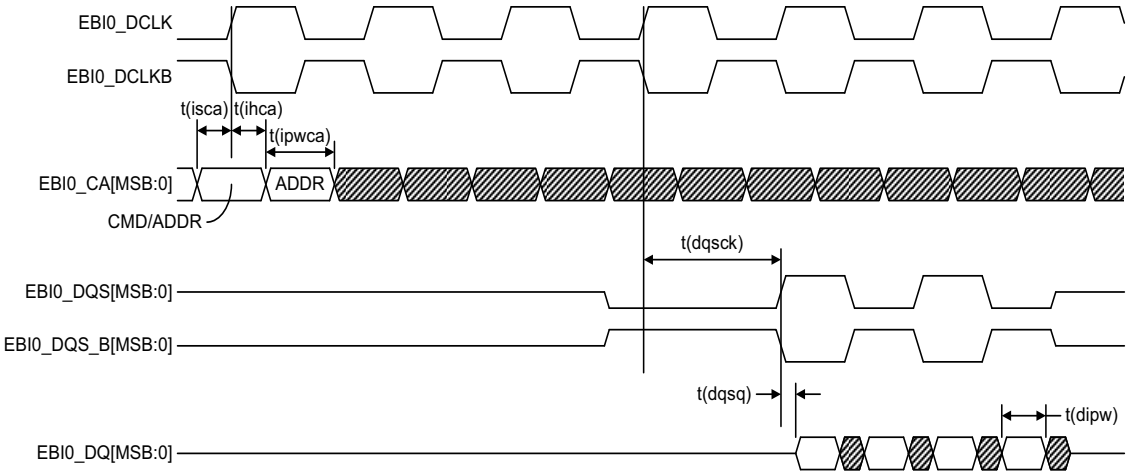


Figure 3-10 DDR SDRAM read timing

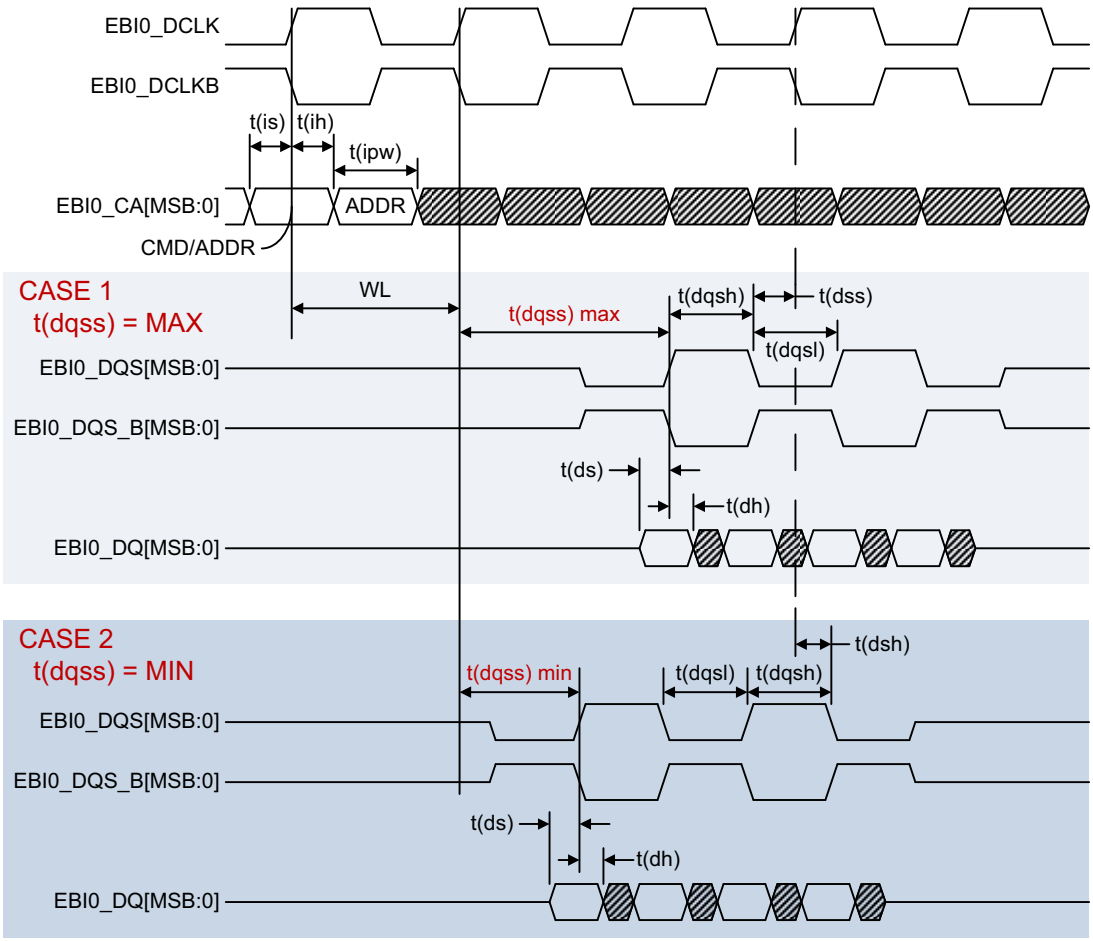


Figure 3-11 DDR SDRAM write timing

Table 3-17 DDR SDRAM read and write timing specifications

Parameter		Comments	Min	Typ	Max	Unit
LPDDR3 (533 MHz) – common to read and write						
t(isca)	Address and control in setup time before CK		0.175	–	–	ns
t(ihca)	Address and control input hold time after CK		0.175	–	–	ns
t(dipw)	DQ and DM pulse width		0.35	–	–	tCK
t(iscs)	CS_n input setup time		0.29	–	–	ns
t(ihcs)	CS_n input hold time		0.29	–	–	ns
t(ipwcs)	CS_n input pulse width		0.7	–	–	t(ck)
t(ipw)	Address and control input pulse width		0.35	–	–	tCK
t(tdiff)	Input transition slew rate from VIL to VIH	Differential clock	2.0	–	–	V/ns
t(t)	Input transition time from VIL to VIH	Other than diff clock	1.0	–	–	V/ns

Table 3-17 DDR SDRAM read and write timing specifications (cont.)

Parameter		Comments	Min	Typ	Max	Unit
LPDDR3 (533 MHz) – read cycle						
t(dqsck)	DQS access time from clock		2.50	–	5.50	ns
t(dqsq)	DQS to DQ skew limit		–	–	0.165	ns
t(qh)	Data hold time from DQS		–	–	0.713	ns
t(rpre)	Read preamble		0.9	–	–	t(ck)
LPDDR3 (533 MHz) – write cycle						
t(ds)	DQ and DM input setup time before DQS		0.175	–	–	ns
t(dh)	DQ and DM input hold time after DQS		0.175	–	–	ns
t(dqsh)	DQS input high-level width		0.40	–	–	t(ck)
t(dqsl)	DQS input low-level width		0.40	–	–	t(ck)
t(dqss)	First DQS latching transition		0.75	–	1.25	t(ck)
t(dss)	DQS falling edge to CK setup time		0.2	–	–	t(ck)
t(dsh)	DQS falling edge hold time after CK		0.2	–	–	t(ck)

3.8.2 eMMC on SDC1

See Section 3.10.1 for secure digital interface details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The MSM8x0x supports two MIPI_CSIs.

- CSI0 is a single 4-lane CSI
- CSI1 is a 2-lane CSI

Table 3-18 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for D-PHY, v0.65 and v0.9/v1.0, October 8, 2007 http://www.mipi.org/specifications/physical-layer (Complete specifications are available to MIPI members only.)	Supports only unidirectional data receiving.	None

3.9.2 Audio support

The MSM8x0x device provides the system's audio functions with the analog audio codec integrated into PMIC device. A proprietary audio PDM interface through GPIO[59:64] is used for transmission of audio data with PM8909/PM8208/PM8916-1 integrated analog codec. Refer to *PM8909/PM8208 Power Management IC Device Specification* (80-NP409-1) and *PM8916/PM8916-1 Device Specification* (80-NK808-1) for its performance characteristics.

MSM audio-related audio interface that supports other audio devices included:

- I^2S – Section 3.10.4
- I^2C – Section 3.10.5

3.9.3 Display support

The MSM8x0x supports a 4-lane MIPI_DSI.

Table 3-19 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification v1.01 for Display Serial Interface http://www.mipi.org/specifications/display-interface (Specifications are available to MIPI members only.)	None	None
MIPI D-PHY Specification v0.65, v0.81, v0.90 http://www.mipi.org/specifications/physical-layer (Complete specifications are available to MIPI members only.)	None	None

3.10 Connectivity

The connectivity functions supported by the MSM8x0x device that requires electrical specifications include:

- Secure digital (SD), including SD cards and multimedia cards (MMC)
- High-speed universal serial bus/on-the-go (host mode only) with built-in physical layer (PHY)
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections
- Through proper configuration of the six BLSP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - User identity module (UIM) ports, including dual-voltage options
  - Interintegrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are included in the following subsections:

NOTE: In addition to reviewing the following hardware specifications, also be sure to review the latest software release notes for software-based performance features or limitations.

3.10.1 Secure digital interfaces

Table 3-20 Supported SD standards and exceptions

Applicable standard	Feature exceptions	Device variations
Multi-Media Card Host Specification, version 4.4.1 http://www.jedec.org/ (Available for free download.)	None	Timing specifications – see Figure 3-12 and Table 3-21
Secure Digital: Physical Layer Specification, version 3.0 https://www.sdcard.org/downloads/pls/ (Simplified version of the Physical Layer Specification is available for free download.)	None	
SDIO Card Specification, version 2.0 https://www.sdcard.org/downloads/pls/simplified_specs/archive/partE1_200.pdf (Simplified specification version 3.00 is available for free download.)	None	

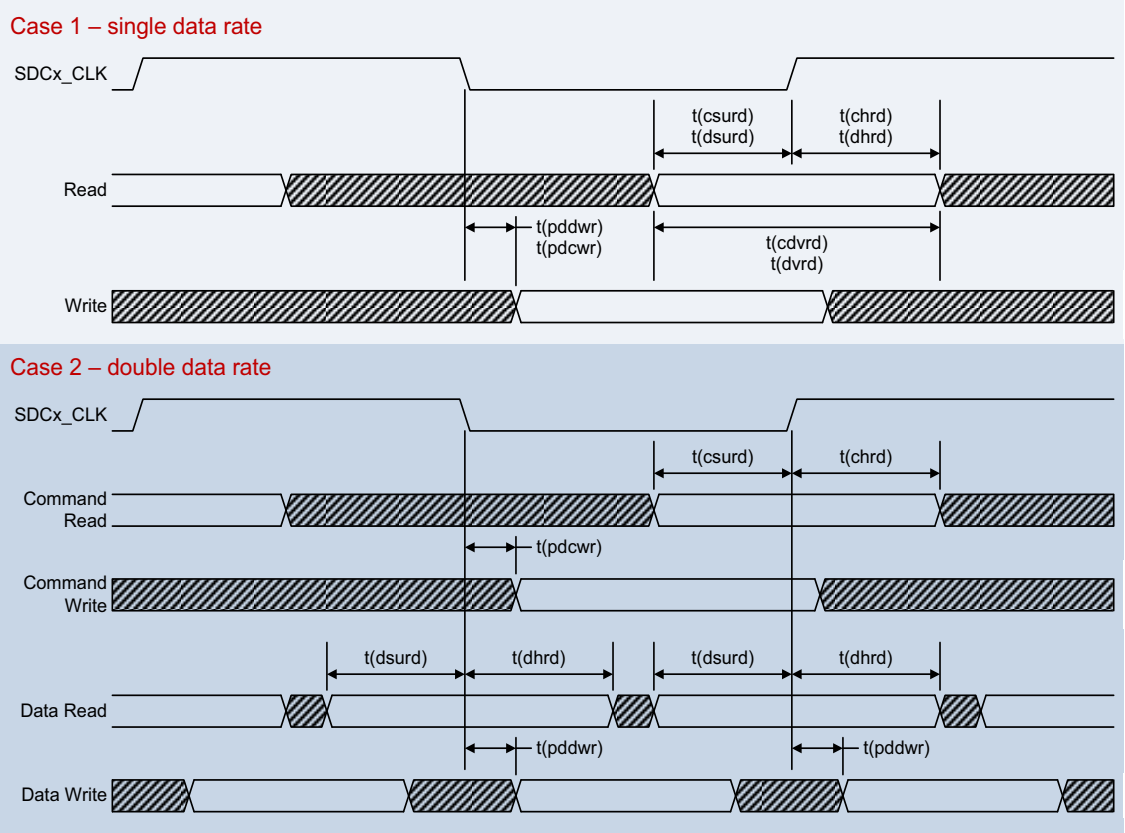


Figure 3-12 Secure digital interface timing

Table 3-21 Secure digital interface timing

Parameter		Min	Typ	Max	Unit
Single data rate (SDR) mode – SDC1 up to 200 MHz					
t(cvdrd)	Command valid	2.4	–	–	ns
t(dvdrd)	Data valid	2.4	–	–	ns
t(pddwr)	Propagation delay on data write	-1.45	–	0.85	ns
t(pdcwr)	Propagation delay on command write	-1.45	–	0.85	ns
Double data rate (DDR) mode – SDC1 up to 52 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	5.53	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	1.65	–	–	ns
t(pddwr)	Propagation delay on data write	2.5	–	6.15	ns
t(pdcwr)	Propagation delay on command write	-7.85	–	2.65	ns

Table 3-21 Secure digital interface timing (cont.)

Parameter		Min	Typ	Max	Unit
SDR mode – SDC2 up to 208 MHz					
t(cvdrd)	Command valid	2.4	–	–	ns
t(dvdrd)	Data valid	2.4	–	–	ns
t(pddwr)	Propagation delay on data write	-1.36	–	0.76	ns
t(pdcwr)	Propagation delay on command write	-1.36	–	0.76	ns
DDR mode – SDC2 up to 50 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	6.3	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	2	–	–	ns
t(pddwr)	Propagation delay on data write	0.8	–	6	ns
t(pdcwr)	Propagation delay on command write	-8.2	–	3	ns
SDR mode – SDC2 up to 100 MHz					
t(chrd)	Command hold	1.5	–	–	ns
t(csurd)	Command setup	2.5	–	–	ns
t(dhrd)	Data hold	1.5	–	–	ns
t(dsurd)	Data setup	2.5	–	–	ns
t(pddwr)	Propagation delay on data write	-3.7	–	1.5	ns
t(pdcwr)	Propagation delay on command write	-3.7	–	1.5	ns

3.10.2 UIM interface

Table 3-22 Supported UIM standards and exceptions

Applicable standard	Feature exceptions	MSM variations
ISO/IEC 7816-3 http://webstore.ansi.org/ (Available to ANSI site licensees or for a fee).	None	None

3.10.3 USB interfaces

Table 3-23 Supported USB standards and exceptions

Applicable standard	Feature exceptions	Device variations
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later) http://www.usb.org/developers/docs/ (Available for free download.)	None	Operating voltages, system clock, and VBUS – see Table 3-24
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0 A or later) http://www.usb.org/developers/docs/ (Available for free download as part of the USB 2.0	Supports host mode aspect of OTG only	None

Table 3-24 Device-specific USBPHY specifications

Parameter	Comments	Min	Typ	Max	Unit
Supply voltages					
Dual-supply (see Table 3-3 for specifications)					
VDD_USB_1P8		–	1.80	–	V
VDD_USB_3P3		–	3.075	–	V
USB_SYSCLK					
Frequency	19.2 MHz clock is required.	–	19.2	–	MHz
Clock deviation		-400	–	400	ppm
Jitter (peak-to-peak)	0.5 MHz to 1.75 MHz	0	–	60	ps
Duty cycle		40	–	60	%
Low-level input voltage (V_{IL})		–	–	0.85	V
High-level input voltage (V_{IH})		1.27	–	–	V
USB_VBUS					
Valid USB_HS_VBUS detection voltage		2.00	–	5.25	V

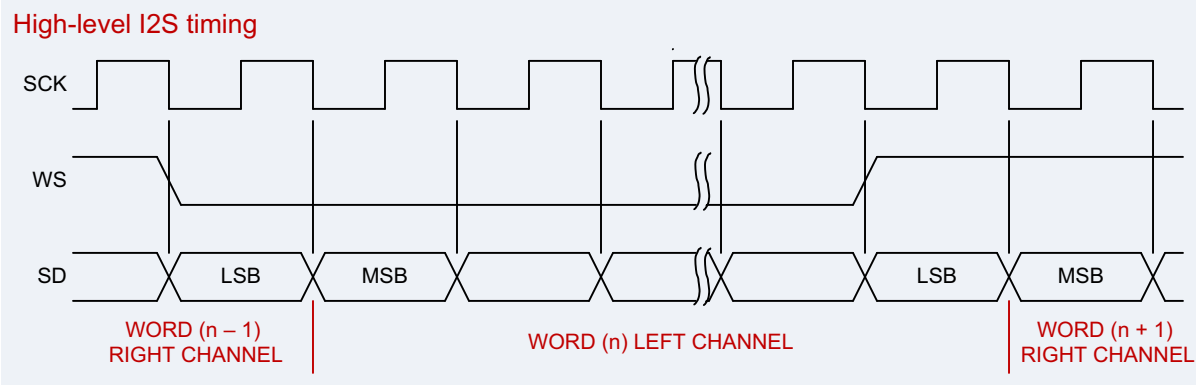
3.10.4 I²S interface

The MI²S (multiple I²S) interface for microphone and speaker functions is supported by the MSM8x0x.

The following information applies to MI²S.

Table 3-25 Supported I²S standards and exceptions

Applicable standards	Feature exceptions	MSM variations
Phillips I2S Bus Specifications revised June 5, 1996 http://www.classic.nxp.com/acrobat_download2/various/I2SBUS.pdf (Available for free download.)	None	When an external SCK clock is used, a duty cycle between 45% to 55% is required.



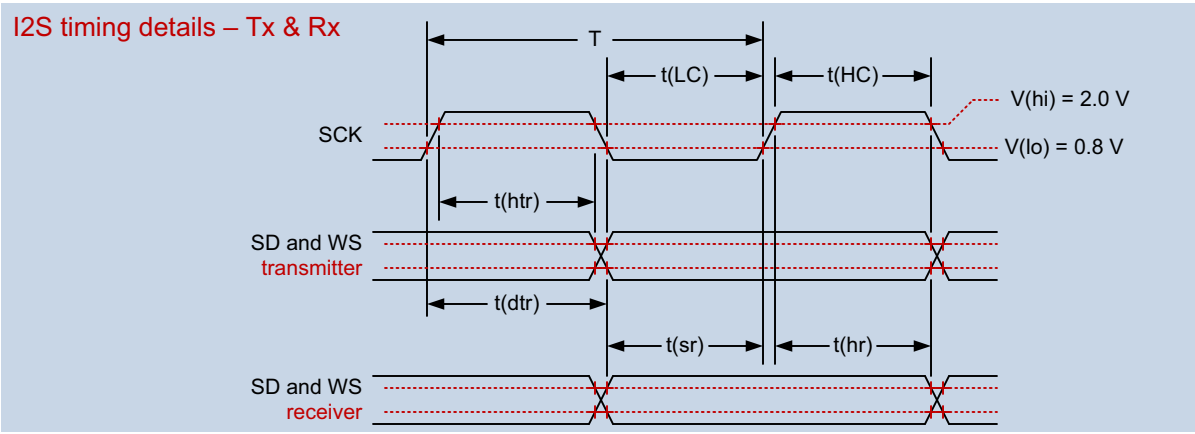


Figure 3-13 I²S timing diagram

Table 3-26 I²S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit
Using internal SCK						
	Frequency		–	–	12.288	MHz
T	Clock period		81.380	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns
t(sr)	SD and WS input setup time		16.276	–	–	ns
t(hr)	SD and WS input hold time		0	–	–	ns
t(dtr)	SD and WS output delay		–	–	65.100	ns
t(htr)	SD and WS output hold time		0	–	–	ns
Using external SCK						
	Frequency		–	–	12.288	MHz
T	Clock period		81.380	–	–	ns
t(HC)	Clock high		0.45 · T	–	0.55 · T	ns
t(LC)	Clock low		0.45 · T	–	0.55 · T	ns

Table 3-26 I²S interface timing (cont.)

Parameter		Comments [1]	Min	Typ	Max	Unit
t(sr)	SD and WS input setup time		16.276	–	–	ns
t(hr)	SD and WS input hold time		0	–	–	ns
t(dtr)	SD and WS output delay		–	–	65.100	ns
t(htr)	SD and WS output hold time		0	–	–	ns

1. Load capacitance is between 10 pF and 40 pF.

3.10.5 I²C interface

Table 3-27 Supported I²C standards and exceptions

Applicable standard	Feature exceptions	MSM variations
I2C Specification, version 5.0, October 2012	None	Multimaster is not supported

3.10.6 Serial peripheral interface

The MSM8x0x supports SPI as a master only. Any one of the six BLSP ports can be configured as an SPI master:

- BLSP at 52 MHz (see Table 3-28)
- BLSP at 26 MHz (see Table 3-29)

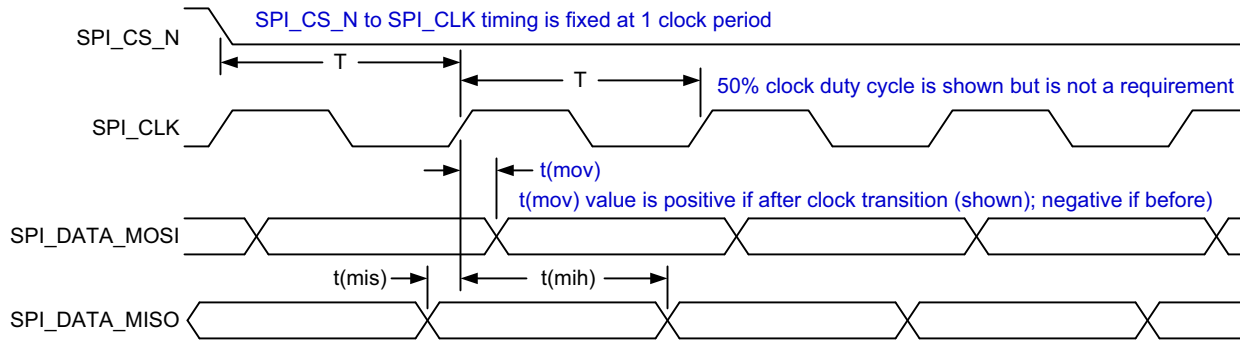


Figure 3-14 SPI master timing diagram

Table 3-28 SPI master timing characteristics at 48 MHz

Parameter	Comments	Min	Typ	Max	Unit
T [1]	SPI clock period: 48 MHz max	20.0	–	–	ns
t(ch)	Clock high	9.0	–	–	ns
t(cl)	Clock low	9.0	–	–	ns
t(mov)	Master output valid	-5.0	–	5.0	ns
t(mis)	Master input setup	5.0	–	–	ns
t(mih)	Master input hold	1.0	–	–	ns

1. The minimum clock period includes 1% jitter of the maximum frequency.

Table 3-29 SPI master timing characteristics at 26 MHz

Parameter	Comments	Min	Typ	Max	Unit
T	SPI clock period: 26 MHz max	38	–	–	ns
t(ch)	Clock high	17	–	–	ns
t(cl)	Clock low	17	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	3	–	–	ns
t(mih)	Master input hold	1	–	–	ns

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions – as specified in the following subsections.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz XO input

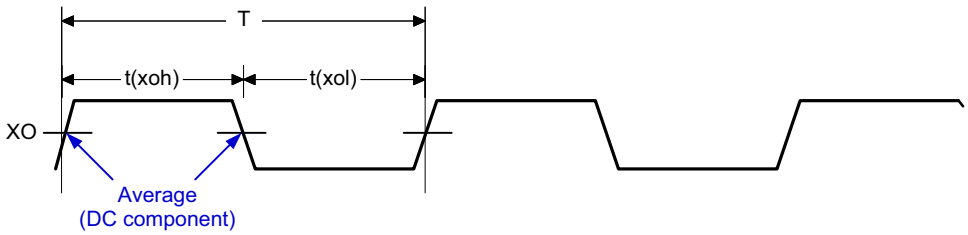


Figure 3-15 XO timing parameters

Table 3-30 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. Refer to the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal, and TH + Xtal Mini-Specification* (80-V9690-24) for more details.

3.11.1.2 Sleep clock

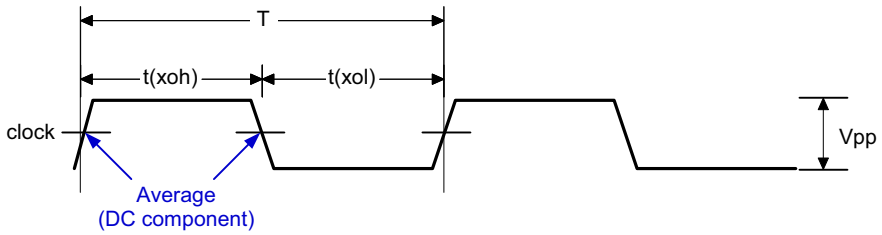


Figure 3-16 Sleep-clock timing parameters

Table 3-31 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T	Sleep-clock period		–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage		–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

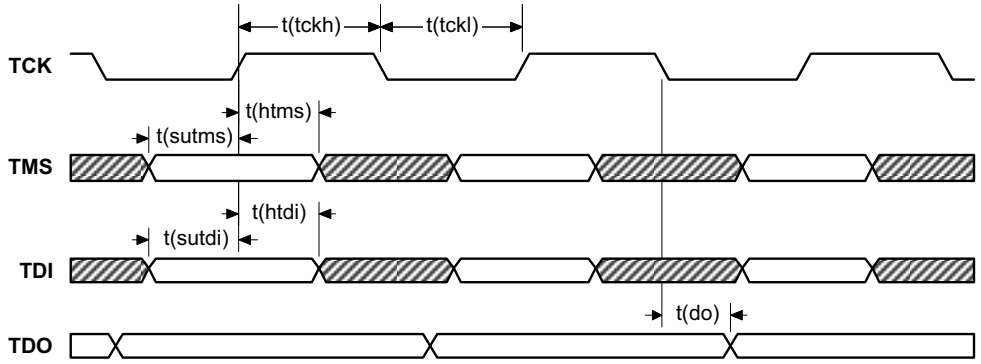


Figure 3-17 JTAG-interface timing diagram

Table 3-32 JTAG-interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		50	–	–	ns
t(tckh)	TCK pulse width high		20	–	–	ns
t(tckl)	TCK pulse width low		20	–	–	ns
t(sutms)	TMS input setup time		5	–	–	ns
t(htms)	TMS input hold time		20	–	–	ns
t(sutdi)	TDI input setup time		5	–	–	ns
t(htdi)	TDI input hold time		20	–	–	ns
t(do)	TDO data-output delay		–	–	15	ns

3.12 RF and power management interfaces

The supported chipset and RF front-end (RFFE) interfaces are listed in Table 3-33 and Table 3-34, respectively. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary, and therefore are not specified.

3.12.1 RF front-end (RFFE)

Table 3-33 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None	None

The maximum operation frequency of SCLK is 26 MHz, although lower rates may be utilized. A slave might not be able to support a 26 MHz clock frequency during a read operation. In this

case, known as Half Speed operation, a 13 MHz clock frequency may be implemented for only the read back.

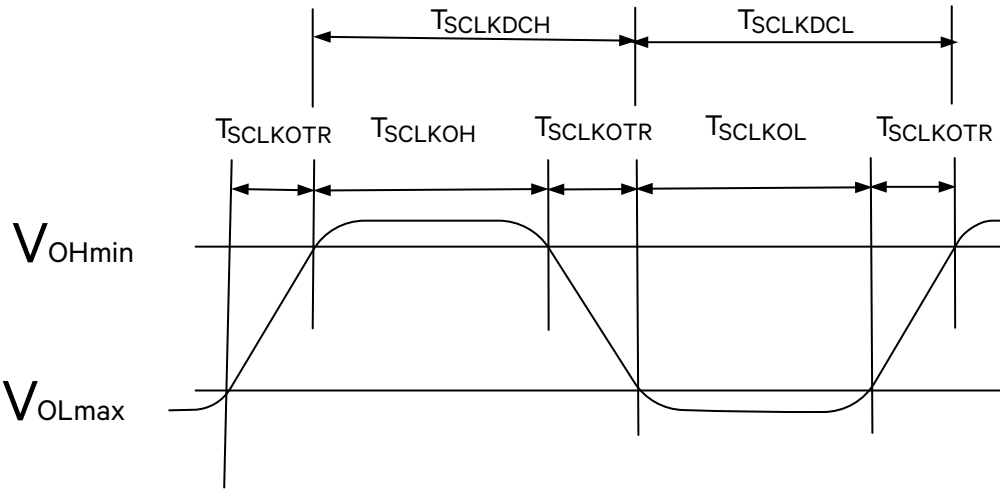


Figure 3-18 Clock driver output waveform

Table 3-34 RFFE data

Symbol	Description	Half-speed device		Full-speed device		Units
		Min	Max	Min	Max	
T_{sclkoh}	Clock output high time	24	–	11.25	–	ns
T_{sclkol}	Clock output low time	24	–	11.25	–	ns
$T_{sclkotr}$	Clock output transition (rise/fall) time[1]	3.5	10	3.5	6.5	ns
$T_{sclkdch}$	Clock output duty cycle high time[2,3]	45	55	45	55	ns
$T^{sclkdcl}$	Clock output duty cycle low time [2,3]	45	55	45	55	ns

1. The minimum limit for $T_{SCLKOTR}$ applies for all valid SCLK frequencies.
2. $T_{SCLKDCH}$ is defined to consist of T_{SCLKOH} + $T_{SCLKOTR}$(Fall); thus, it consists of the time that SCLK is a valid high level, plus the time until SCLK achieves a valid low level by exceeding V_{OLmax}. Similarly, $T_{SCLKDCL}$ is defined to consist of T_{SCLKOL} + $T_{SCLKOTR}$(Rise); it is thus the time that SCLK is a valid low level, combined with the time until SCLK exceeds VOHmin.
3. $T_{SCLKDCH}$ and $T_{SCLKDCL}$ are expressed as a percentage of the SCLK period. The limits expressed apply for any valid SCLK frequency.

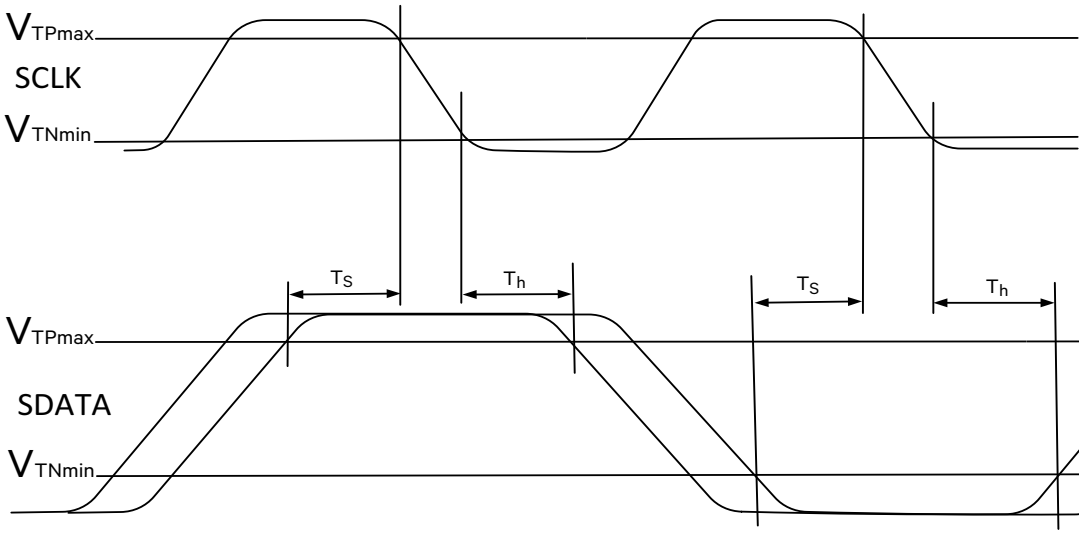


Figure 3-19 Set up and hold timing waveform

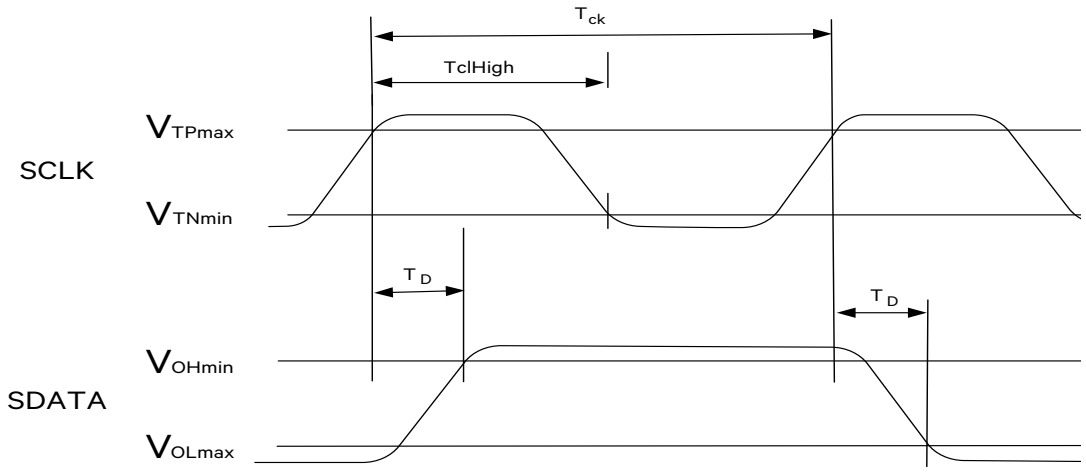


Figure 3-20 Tx data output delay with respect to rising edge of clock

Table 3-35 Rx/Tx data

Parameter	Description	LSL	USL	units
Ts	Rx Data setup time w.r.t falling edge of clock	15.75	N/A	ns
Th	Rx Data hold time w.r.t falling edge of clock	0	N/A	ns
T_D	Tx data output delay w.r.t rising edge of clock	NA	10.25	ns
TclHigh	Tx clock duty cycle - high time	0.45*Tck	0.55*Tck	ns

3.12.2 System power management interface (SPMI)

Table 3-36 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

Table 3-37 Supported SPMI standards and exceptions

Interface	Parameter	Description	Target frequency	Spec min	Spec max	Units
SPMI	tsu	Input data set up time	19.2 MHz	1	–	ns
	thd	Input data hold time		5	–	ns
	tdataZ	data release time		–	10	ns
	tpd	Output data delay		–	11	ns

4 Mechanical information

4.1 Device physical dimensions

The MSM8x0x is available in the 504-pin nanoscale package (NSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 504 NSP has an 11.1 mm × 12.0 mm body with a maximum height of 0.96 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 504 NSP outline drawing is shown in Figure 4-1.

NOTE: Click the following links to download *Package Outline Drawing, 504 NSP, 11.1 × 12.0 × 0.96 mm, S266, M450* (NT90-NP526-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-NP526-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

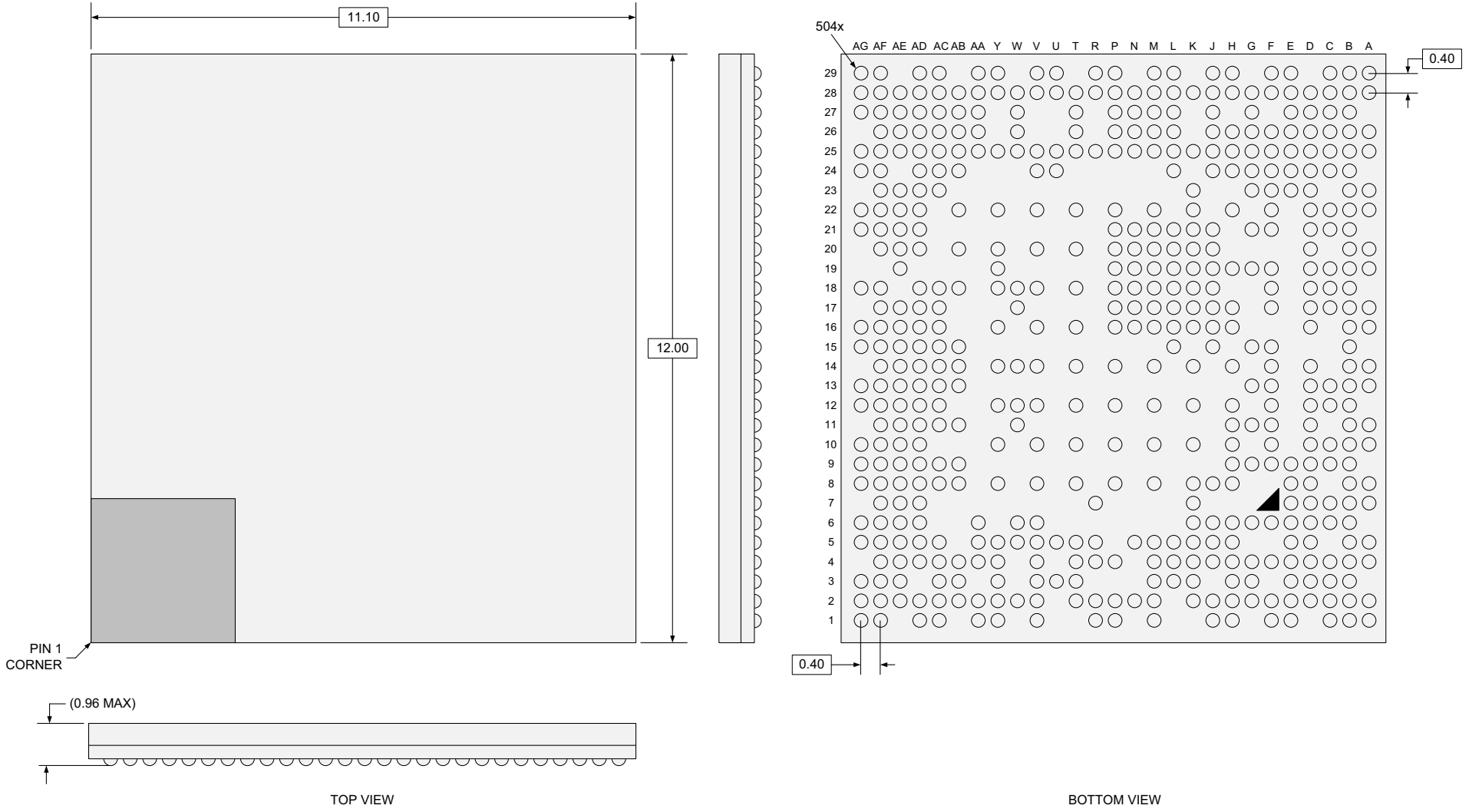


Figure 4-1 504 NSP (11.1 × 12.0 × 0.96 mm) outline drawing

NOTE: This is a simplified outline drawing. Click the link below to download the complete, up-to-date package outline drawing:

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-NP526-1

4.2 Part marking

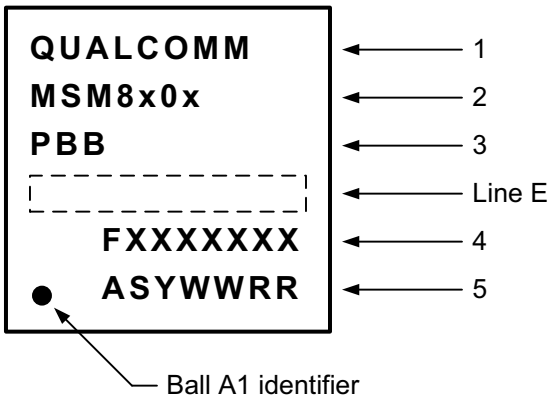


Figure 4-2 MSM8x0x device marking (top view, not to scale)

4.2.1 Specification-compliant devices

Table 4-1 MSM8x0x device marking line definitions

Line	Marking	Description
1	Qualcomm®	Qualcomm name or logo
2	MSM8x0x	QTI product name 8x0x = 8909, 8209, 8208, 8905 (see Table 4-3 for differences)
3	PBB	P = product configuration code (see Table 4-3) BB = feature code
E	Blank or random	Additional content as necessary
4	FXXXXXXX	F = supply source code ■ F = F (for TSMC) ■ F = H (for GLOBALFOUNDRIES) ■ F = P (for SMIC) XXXXXXX = traceability number
5	ASYWWRR	A = assembly site code ■ A = U (Amkor, Shanghai) ■ A = K (SPIL, Taiwan) ■ A = H (STATS ChipPAC, South Korea) ■ A = E (ASE, Taiwan) S = assembly sequence number Y = single-digit year code WW = work week (based on calendar year) RR = product revision

NOTE: For complete marking definitions of all MSM8x0x variants and revisions, refer to the *MSM8909/MSM8209/MSM8208/MSM8905 (SDM205) Device Revision Guide* (80-NP408-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 QFPROM_CORR_JTAG_ID_LSB register

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number

4.3 Device ordering information

4.3.1 Specification-complaint devices

This device can be ordered using the identification code shown in Figure 4-3, and explained below.

Device ID code ►	AAA-AAAA	— P	— CCC	DDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product version	Source code	Feature code
Example ►	MSM-8909	— 0	— 504	NSP	— TR	— 01	— 0	— VV
Example ►	MSM-8909	— 2	— 504	NSP	— TR	— 01	— 0	— AA

Figure 4-3 Device identification code

Device identification details for all samples available to date are summarized in Table 4-3.

Table 4-3 Device identification code details

Device	Product config. code (P)	Product revision (RR)	HW revision number	Feature ID[1]	BB value[2]	Sample type	Comments	Description				
								RF airlink interface	Display	Video decode	Camera	A7 μP core/GPU
MSM8909	0	00	0x009600E1	02	VV	ES1	–	LTE Cat 4, CDMA 1xEV-DO, DC-HSPA+, TD-SCDMA, GSM	qHD	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109600E1			ES2/CS	YWW ≥ 509 is CS sample					
	1	00	0x009600E1	03	VV	ES1	–	LTE Cat 4 w/2x10 CA, CDMA 1xEV-DO, DC-HSPA+, TD-SCDMA, GSM	qHD	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109600E1			ES2/CS	YWW ≥ 509 is CS sample					
	2	00	0x009600E1	04	VV	ES1	–	LTE Cat 4, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109600E1			ES2/CS	YWW ≥ 509 is CS sample					
		01	0x109600E1	0D	AA	ES/CS	YWW ≥ 522 is CS sample	LTE Cat 4, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.267 GHz quad/ 456 MHz
	3	00	0x009600E1	05	VV	ES1	–	LTE Cat 4 w/2x10 CA, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109600E1			ES2/CS	YWW ≥ 509 is CS sample					
		01	0x109600E1	0E	AA	ES/CS	YWW ≥ 522 is CS sample	LTE Cat 4 w/2x10 CA, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.267 GHz quad/ 456 MHz
	4	00	0x009600E1	06	VV	ES1	–	LTE Cat 4, DC-HSPA+, TD-SCDMA, GSM	qHD	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109600E1			ES2/CS	YWW ≥ 509 is CS sample					

Table 4-3 Device identification code details (cont.)

Device	Product config. code (P)	Product revision (RR)	HW revision number	Feature ID[1]	BB value[2]	Sample type	Comments	Description				
								RF airlink interface	Display	Video decode	Camera	A7 μP core/GPU
MSM8909	5	00	0x009600E1	07	VV	ES1	–	LTE Cat 4, CDMA 1xEV-DO, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109600E1			ES2/CS	YWW ≥ 509 is CS sample					
		01	0x109600E1	0F	AA	ES/CS	YWW ≥ 522 is CS sample	LTE Cat 4, CDMA 1xEV-DO, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.267 GHz quad/ 456 MHz
	6	00	0x009600E1	0 A	VV	ES1	–	LTE Cat 4 with 2 x 10 CA, CDMA, 1xEV-DO, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109600E1			ES2/CS	YWW ≥ 509 is CS sample					
		01	0x109600E1	0C	AA	ES/CS	YWW ≥ 522 is CS sample	LTE Cat 4 with 2 x 10 CA, CDMA, 1xEV-DO, DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.267 GHz quad/ 456 MHz
MSM8209	0	00	0x009610E1	01	VV	ES1	–	DC-HSPA+, TD-SCDMA, GSM	HD (720p)	1080p	8 MP	1.094 GHz quad/ 409.6 MHz
		01	0x109610E1			ES2/CS	YWW ≥ 509 is CS sample					
MSM8208	0	00	0x009620E1	01	VV	ES1	–	DC-HSPA+, TD-SCDMA, GSM	qHD	720p	5 MP	1.094 GHz dual/ 307.2 MHz
		01	0x109620E1			ES2/CS	YWW ≥ 509 is CS sample					
MSM8905 (SDM205)	0	01	0x000940E1	00	VV	CS	YWW ≥ 652	LTE Cat 4, DC-HSPA+, GSM	VGA (with 512 MB) QVGA (with 256 MB)	720p	3 MP (with 512 MB) 2 MP (with 256 MB)	1.094 GHz dual/ 307.2 MHz
MSM8905 (SDM205)	0	01	0x000940E1	00	AA	CS	YWW ≥ 652	LTE Cat 4, DC-HSPA+, GSM	VGA (with 512 MB) QVGA (with 256 MB)	720p	3 MP (with 512 MB) 2 MP (with 256 MB)	1.267 GHz dual/ 307.2 MHz

1. See to Table 4-2. FEATURE_ID combined with hardware revision number defines unique product variants. This information is shown identification information (such as device marking information) is not easily accessible.
2. Device with BB value = VV are 1.094 GHz devices and with BB value = AA are 1.267 GHz devices.

See to Section 5.4 for details on identifying MSM parts with service key provisioning support.

Table 4-4 Source configuration codes – MSM8909/MSM8209/MSM8208/MSM8905

S value	Die	F value = H	F value = F	F value = P
0	Digital	GLOBALFOUNDRIES	TSMC	–
1	Digital	GLOBALFOUNDRIES	TSMC	SMIC
Other columns and rows will be added in future revisions of this document, if needed.				

Table 4-5 Source configuration codes–MSM8905 (SDM205)

S value	Die	F value = H	F value = F	F value = P
0	Digital	GLOBALFOUNDRIES	TSMC	SMIC
Other columns and rows will be added in future revisions of this document, if needed.				

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture-sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C / 85% RH
2	1 year	≤ 30°C / 60% RH
2a	4 weeks	≤ 30°C / 60% RH
3	168 hours	≤ 30°C / 60% RH
4	72 hours	≤ 30°C / 60% RH
5	48 hours	≤ 30°C / 60% RH
5a	24 hours	≤ 30°C / 60% RH
6	Mandatory bake before use. After bake, must be re-flowed within the time limit specified on the label.	≤ 30°C / 60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The MSM8909 device samples are currently classified as MSL3 at 255 (+5, -0)°C.*** This qualification temperature (255 (+5, -0)°C) should not be confused with the peak temperature within the recommended solder reflow profile (see Section 6.2.3 for more details).

4.5 Thermal characteristics

Rather than provide thermal resistance values Θ_{JC} and Θ_{JA}, validated thermal-package models are provided through the CDMATech Support website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can obtain thermal resistance values by conducting their own thermal simulations.

NOTE: Click the following links to download the MSM8x0x thermal package models– *MSM8909 504 NSP Thermal Package Model Icepak* (HS11-NP408-5HW) and *MSM8909 504 NSP Thermal Package Model* FloTHERM (HS11-NP408-6HW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-NP408-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-NP408-6HW

After successfully logging in, the documents are downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

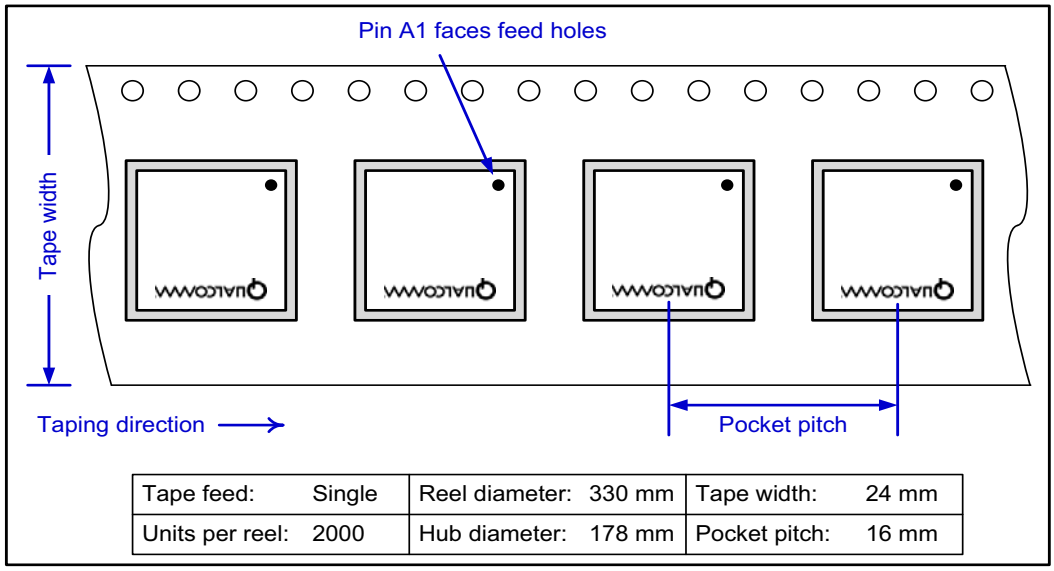
5 Carrier, storage, & handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI carrier tape systems conform to EIA-481-D standards.

A simplified sketch of the MSM8x0x tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	178 mm	Pocket pitch:	16 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

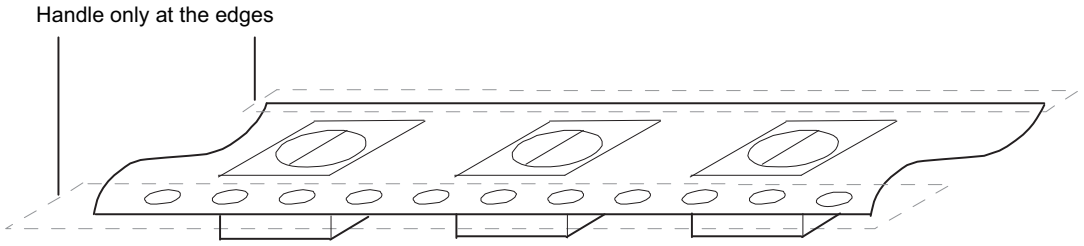


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

MSM8x0x devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. If the storage environment maintains an ambient temperature lower than 40°C and relative humidity less than 90%, the expected shelf life is at least 24 months.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB. It is defined by the device MSL rating, as described in Section 4.4.

5.3 Handling

Tape handling was discussed in Section 5.1.1. Other (IC-specific) handling guidelines are presented below.

5.3.1 Baking

It is **not necessary** to bake the MSM8x0x if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the MSM8x0x if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; see *ASIC Packing Methods and Materials Specification* (80-VK055-1) for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, it may result in destructive damage.

ESD counter measures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the MSM8x0x device ESD ratings.

5.4 Bar code label and packing for shipment

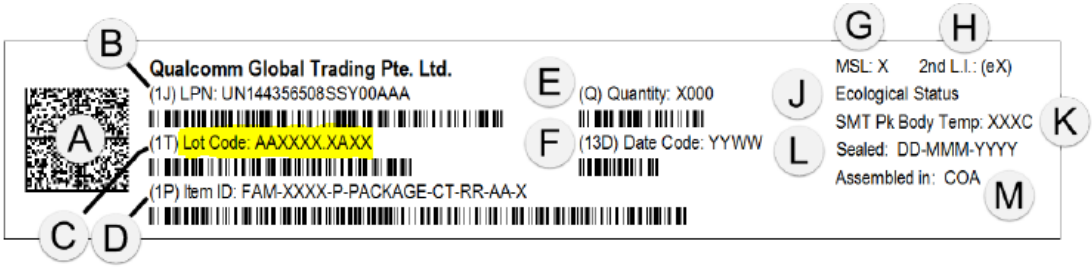


Figure 5-3 Bar code label

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) for all packing-related information, including barcode-label details.

5.4.1 Service key provisioning support for Windows

- All MSM8909 parts with date code YWW ≥ 543 support service key provisioning.
- All MSM8909 SMIC parts (F code = P) supports service key provisioning.

Refer to Section 4.2 for date code and F code details.

Also, the Lot Code present on the barcode label (format shown in Figure 5-3) can be used to segregate the MSM8909 parts supporting service key provisioning. Lot Code will have prefix “5” for service key provisioning support.

- Prefix “5”: Service key provisioning is supported (good for retail Windows image)

  For example, Lot Code: 50FTCN008.U2U02

- Prefix other than “5”: Service key provisioning is not supported (not good for retail Windows image)

  For example, Lot Code: 00FTCN008.U2U02

6 PCB mounting guidelines

6.1 RoHS compliance

The device is lead-free and RoHS-compliant. Its SnAgCu solder balls use SAC305 composition on the top and SAC125/Ni on the bottom. QTI defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. QTI package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all QTI ASIC products are described in the *IC Package Environmental Roadmap* (80-VA832-1).

6.2 SMT parameters

This section describes QTI board-level characterization process parameters. It is included to assist customers with their SMT process development; it is not intended to be a specification for their SMT processes.

6.2.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based on QTI internal characterizations for lead-free solder pastes on an eight-layer PCB, built primarily to the specifications described in JEDEC JESD22-B111.

QTI recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile prior to PCB production. Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

General land pattern guidelines:

- Non-solder-mask-defined (NSMD) pads provide the best reliability.
- Keep the solderable area consistent for each pad, especially when mixing via-in-pad and non-via-in-pad in the same array.
- Avoid large solder mask openings over ground planes.
- Traces for external routing are recommended to be less than or equal to half the pad diameter, to ensure consistent solder-joint shapes.

One key parameter that should be evaluated is the ratio of aperture area to sidewall area, known as the area ratio (AR). QTI recommends square apertures for optimal solder-paste release. In this case, a simple equation can be used relating the side length of the aperture to the stencil thickness (as shown and explained in Figure 6-1). Larger area ratios enable better transfer of solder paste to the PCB, minimize defects, and ensure a more stable printing process. Inter-aperture spacing should be at least as thick as the stencil; otherwise, paste deposits may bridge.

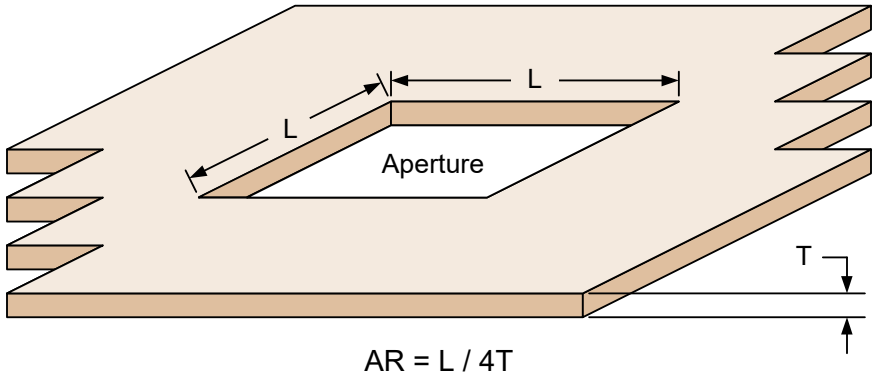


Figure 6-1 Area ratio (AR)

QTI provides an example PCB land pattern and stencil design for the 504 NSP.

NOTE: Click the link below to download the 504 NSP land/stencil drawing (LS90-NG134-1) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/LS90-NG134-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the Qualcomm CreatePoint User Guide (80-NC193-2).

6.2.2 Reflow profile

Reflow profile conditions typically used by QTI for lead-free systems are listed in Table 6-1, and are shown in Figure 6-2.

Table 6-1 QTI typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Temp range	Condition
Preheat	Initial ramp	< 150°C	3°C/sec max
Soak	Flux activation	150 to 190°C	60 to 75 sec
Ramp	Transition to liquidus (solder-paste melting point)	190 to 220°C	< 30 sec

Table 6-1 QTI typical SMT reflow profile conditions (for reference only) (cont.)

Profile stage	Description	Temp range	Condition
Reflow	Time above liquidus	220 to 245°C [1]	50 to 70 sec
Cool down	Cool rate – ramp to ambient	< 220°C	6°C/sec max

1. During the reflow process, the recommended peak temperature is 245°C (minimum). This temperature should not be confused with the peak temperature reached during MSL testing, as described in Section 6.2.3.

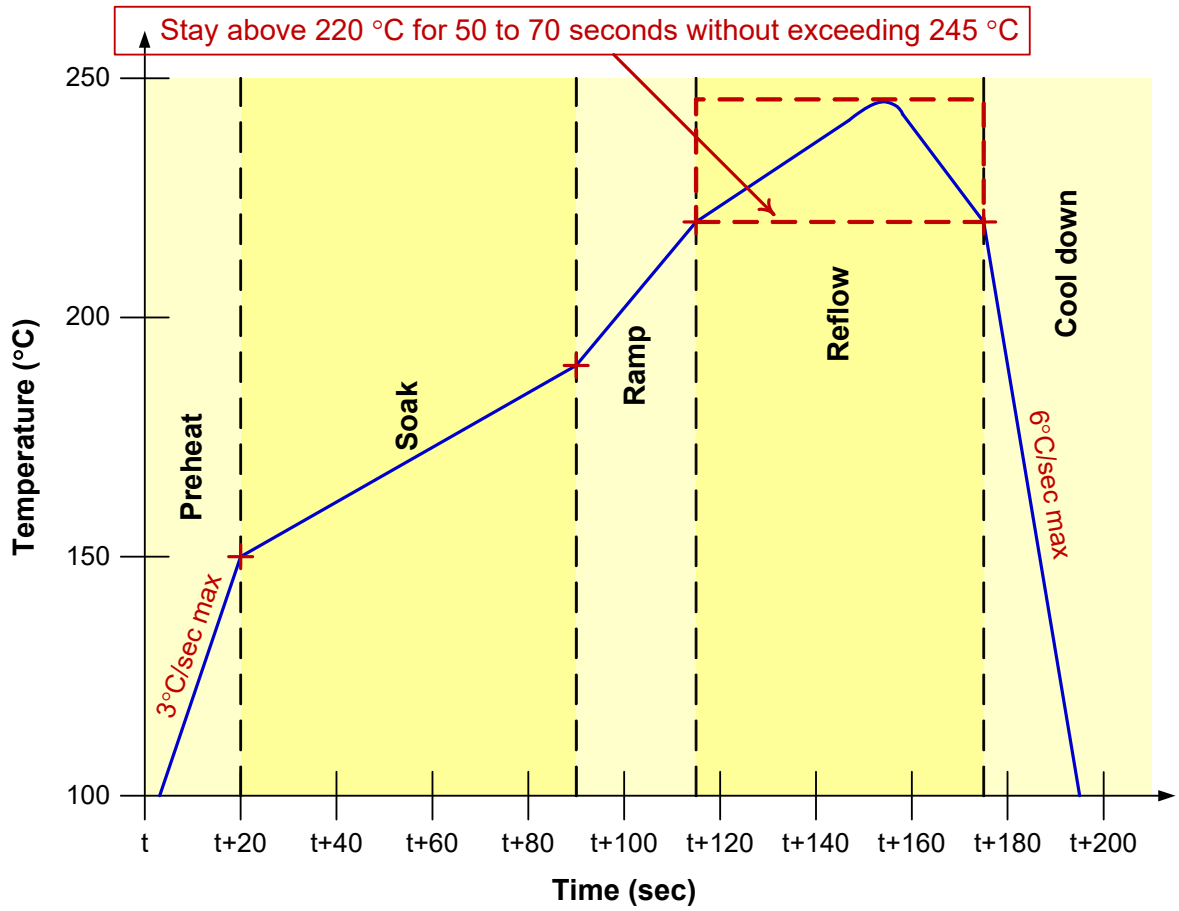


Figure 6-2 QTI typical SMT reflow profile

6.2.3 SMT peak package-body temperature

This document states a peak package-body temperature in three other places within this document; without explanation, they may appear to conflict. The three places are listed below, along with an explanation of the stated value and its meaning within that section's context.

- Section 4.4 – *Device moisture-sensitivity level*

  MSM8x0x devices are classified as MSL3@255°C. The temperature (255°C) included in this designation is the lower limit of the range stated for moisture resistance testing during the device qualification process, as explained immediately below.

- Section 7.1 – *Reliability qualifications summary*

  One of the tests conducted for device qualification is the moisture resistance test. QTI follows J-STD-020-C, and hits a peak reflow temperature that falls within the range of 260°C +0/-5°C (255°C to 260°C).

- Section 6.2.2 – *Reflow profile*

  During a production board's reflow process, the temperature experienced by the package must be controlled. Obviously, the temperature must be high enough to melt the solder and provide reliable connections, but it must not go so high that the device can be damaged. The recommended peak temperature during production assembly is 245°C. This is comfortably above the solder melting point (220°C), yet well below the proven temperature reached during qualification (255°C or more).

6.2.4 SMT process verification

QTI recommends verification of the SMT process prior to high-volume board assembly, including:

- In-line solder-paste deposition monitoring
- Reflow profile measurement and verification
- Visual and x-ray inspection after soldering to confirm adequate alignment, solder voids, solder-ball shape, and solder bridging
- Cross-section inspection of solder joints for wetting, solder-ball shape, and voiding

6.3 Daisy-chain components

Daisy-chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. In fact, all SMT process recommendations described above can be performed using daisy-chain components.

Ordering information is given in Section 4.3.

Daisy-chain PCB routing recommendations are available for download.

NOTE: Click the link below to download the 504 NSP daisy-chain interconnect drawing (DS90-NP526-1) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-NP526-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.4 Board-level reliability

QTI conducts characterization tests to assess the device's board-level reliability, including the following physical tests on evaluation boards:

- Drop shock (JESD22-B111)
- Temperature cycling (JESD22-A104)
- Cyclic bend testing – optional (JESD22-B113)

Board-level reliability data is available for download.

NOTE: Click the link below to download the *Board Level Reliability, 504 NSP* (BR80-NP526-1) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/BR80-NP526-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the Qualcomm CreatePoint User Guide (80-NC193-2).

6.5 High-temperature warpage

QTI measures high-temperature warpage using a shadow moire system; the measured data is available for download.

NOTE: Click the link below to download the 504 NSP high-temperature warpage data (WR80-NP526-1) from the Qualcomm CreatePoint website.

This link will be included in future revisions of this document

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

7 Part reliability

7.1 Reliability evaluation summary

7.1.1 MSM8x0x reliability evaluation report for device from TSMC

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and AFR in FIT (λ) failure in billion device-hours: ■ HTOL: JESD22-A108-A ■ Use conditions: □ Temperature: 70°C; □ Voltage: 1.15 V ■ Total samples from three different wafer lots	240	Passed DPPM < 1000 DPPM[1]
MTTF t = 1/λ in million hours: ■ Total samples from three different wafer lots	240	Passed MTTF > 40
ESD – human body model (HBM) rating: ■ JESD22-A114-F ■ Total samples from one wafer lot	3	2000 V
ESD – charged device model (CDM) rating: ■ JESD22-C101-D ■ Target: 500 V ■ Total samples from one wafer lot	3	500 V
Latch-up (I-test): ■ EIA/JESD78A ■ Trigger current: ±100 mA ■ Temperature: 85°C ■ Total samples from one wafer lot	6	Passed
Latch-up (V supply overvoltage): ■ EIA/JESD78A ■ Trigger voltage: stress each VDD pin at 1.5 × VDD maximum per the device specification ■ Temperature: 85°C ■ Total samples from one wafer lot	6	Passed

1. The cumulative DPPM/FITs from multiple products were under the TSMC 28 nm LP process.

Table 7-2 TSMC package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
Moisture resistance test (MRT): ■ J-STD-020 ■ Reflow at 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	600	600	600	600	Pass
Temperature cycle: ■ JESD22-A104-D ■ Temperature: -55°C to 125°C ■ Number of cycles: 1000 ■ Soak time at minimum/maximum temperature: 8–10 minutes ■ Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** ■ JESD22-A113 ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass
uHAST: ■ JESD22-A118 ■ Temperature: 130°C/85% RH ■ Duration: 96 hrs **Preconditioning:** ■ JESD22-A113-F ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass

Table 7-2 TSMC package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
Biased HAST: ■ JESD22-A110 ■ Temperature: 130°C/85% RH ■ Duration: 96 hrs **Preconditioning:** ■ JESD22-A113-F ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	96	96	96	96	Pass
High-temperature storage life: ■ JESD22-A103-C ■ Temperature: 150°C ■ Duration: 500, 1000 hrs ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass
Flammability: UL-STD-94 The flammability test is not required. QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most QTI PWBs are rated V-0 (better than V-1).	NA	NA	NA	NA	–
Physical dimensions: ■ JESD22-B100-A ■ Case outline drawing: QTI internal document ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	78	78	78	78	Pass
Solder bump shear: ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	15	15	15	15	Pass

Table 7-2 TSMC package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
■ Solder ball shear: JESD22-B117 ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	15	15	15	15	Pass
Internal/external visual: ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	78	78	78	78	Pass

7.1.2 MSM8x0x reliability evaluation report for device from GLOBALFOUNDARIES

Table 7-3 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and AFR in FIT (λ) failure in billion device-hours: ■ HTOL: JESD22-A108-A ■ Use conditions: □ Temperature: 70°C; □ Voltage: 1.15 V ■ Total samples from three different wafer lots	240	Passed DPPM < 1000 DPPM[1]
MTTF t = 1/λ in million hours: ■ Total samples from three different wafer lots	240	Passed MTTF > 40
ESD – HBM rating: ■ JESD22-A114-F ■ Total samples from one wafer lot	3	2000 V
ESD – CDM rating: ■ JESD22-C101-D ■ Target: 500 V ■ Total samples from one wafer lot	3	500 V

Table 7-3 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
Latch-up (I-test): ■ EIA/JESD78A ■ Trigger current: ±100 mA ■ Temperature: 85°C ■ Total samples from one wafer lot	6	Passed
Latch-up (V supply overvoltage): ■ EIA/JESD78A ■ Trigger voltage: stress each VDD pin at 1.5 × VDD maximum per the device specification ■ Temperature: 85°C ■ Total samples from one wafer lot	6	Passed

1. The cumulative DPPM/FITs from multiple products were under the GLOBALFOUNDRIES 28 nm LP process.

Table 7-4 GLOBALFOUNDRIES package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
Moisture resistance test (MRT): ■ J-STD-020 ■ Reflow at 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	600	600	600	600	Pass
Temperature cycle: ■ JESD22-A104-D ■ Temperature: -55°C to 125°C ■ Number of cycles: 1000 ■ Soak time at minimum/maximum temperature: 8–10 minutes ■ Cycle rate: 2 cph **Preconditioning:** ■ JESD22-A113 ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass

Table 7-4 GLOBALFOUNDRIES package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
uHAST: ■ JESD22-A118 ■ Temperature: 130°C/85% RH ■ Duration: 96 hrs **Preconditioning:** ■ JESD22-A113-F ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass
Biased HAST: ■ JESD22-A110 ■ Temperature: 130°C/85% RH ■ Duration: 96 hrs **Preconditioning:** ■ JESD22-A113-F ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	96	96	96	96	Pass
High-temperature storage life: ■ JESD22-A103-C ■ Temperature: 150°C ■ Duration: 500, 1000 hrs ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass
Flammability: UL-STD-94 The flammability test is not required. QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most QTI PWBs are rated V-0 (better than V-1).	NA	NA	NA	NA	–

Table 7-4 GLOBALFOUNDRIES package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
Physical dimensions: ■ JESD22-B100-A ■ Case outline drawing: QTI internal document ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	78	78	78	78	Pass
Solder bump shear: ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	15	15	15	15	Pass
■ Solder ball shear: JESD22-B117 ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	15	15	15	15	Pass
Internal/external visual: ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	78	78	78	78	Pass

7.1.3 MSM8x0x reliability evaluation report for device from SMIC

Table 7-5 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
DPPM rate (ELFR) and AFR in FIT (λ) failure in billion device-hours: ■ HTOL: JESD22-A108-A ■ Use conditions: □ Temperature: 70°C; □ Voltage: 1.15 V ■ Total samples from three different wafer lots	480	Passed DPPM < 1000 DPPM[1]
MTTF t = 1/λ in million hours: ■ Total samples from three different wafer lots	480	Passed MTTF > 40
ESD – HBM rating: ■ JESD22-A114-F ■ Total samples from one wafer lot	3	2000 V
ESD – CDM rating: ■ JESD22-C101-D ■ Target: 500 V ■ Total samples from one wafer lot	3	500 V
Latch-up (I-test): ■ EIA/JESD78A ■ Trigger current: ±100 mA ■ Temperature: 85°C ■ Total samples from one wafer lot	6	Passed
Latch-up (V supply overvoltage): ■ EIA/JESD78A ■ Trigger voltage: stress each VDD pin at 1.5 × VDD maximum per the device specification ■ Temperature: 85°C ■ Total samples from one wafer lot	6	Passed

1. The cumulative DPPM/FITs from multiple products were under the SMIC 28 nm LP process.

Table 7-6 SMIC package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
Moisture resistance test (MRT): ■ J-STD-020 ■ Reflow at 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	600	600	600	600	Pass
Temperature cycle: ■ JESD22-A104-D ■ Temperature: -55°C to 125°C ■ Number of cycles: 1000 ■ Soak time at minimum/maximum temperature: 8–10 minutes ■ Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** ■ JESD22-A113 ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass
uHAST: ■ JESD22-A118 ■ Temperature: 130°C/85% RH ■ Duration: 96 hrs **Preconditioning:** ■ JESD22-A113-F ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass

Table 7-6 SMIC package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
Biased HAST: ■ JESD22-A110 ■ Temperature: 130°C/85% RH ■ Duration: 96 hrs **Preconditioning:** ■ JESD22-A113-F ■ MSL 3 ■ Reflow temperature: 260°C +0/-5°C ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	90	90	90	90	Pass
High-temperature storage life: ■ JESD22-A103-C ■ Temperature: 150°C ■ Duration: 500, 1000 hrs ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	240	240	240	240	Pass
Flammability: UL-STD-94 The flammability test is not required. QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most QTI PWBs are rated V-0 (better than V-1).	NA	NA	NA	NA	–
Physical dimensions: ■ JESD22-B100-A ■ Case outline drawing: QTI internal document ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	78	78	78	78	Pass
Solder bump shear: ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	15	15	15	15	Pass

Table 7-6 SMIC package reliability results

Tests, standards, and conditions	ATC assembly source sample size	SPIL assembly source sample size	ASE assembly source sample size	SCK assembly source sample size	Result
■ Solder ball shear: JESD22-B117 ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	15	15	15	15	Pass
Internal/external visual: ■ ATC, SPIL, ASE, and SCC total samples are from three different assembly lots at each SAT	78	78	78	78	Pass

7.2 Qualification sample description

Device characteristics

Device name: MSM8x0x

Package type: 504 NSP

Package body size: 11.1 mm × 12.0 mm × 0.96 mm

Fab process: 28 nm CMOS

Fab sites: TSMC
GLOBALFOUNDRIES
SMIC

Assembly sites: Amkor, Shangai
SPIL, Taiwan
STATS ChipPAC, South Korea
ASE, Taiwan

Solder ball pitch: 0.4 mm