Qualcomm Technologies, Inc.

Device description

The MSM™ device uses the advanced 14 nm FinFET process for lower active power dissipation and faster peak CPU performance. It includes a customized 64-bit ARM Cortex A-53 octa-core applications processor non-package-on-package (non-PoP) LPDDR3 SDRAM memory.

The latest air interface standards are supported, including:

- LTE up to Cat 7 (FDD and TDD), including 2 × 20 CA
- WCDMA up to Rel-10 HSPA+, including 4C-HSDPA+ and HSDPA 2 + 1 CA
- TD-SCDMA up to DC-HSPA+ 64 QAM
- GSM, GPRS, EDGE
- CDMA up to 1X Advanced and 1xEV-DOrB

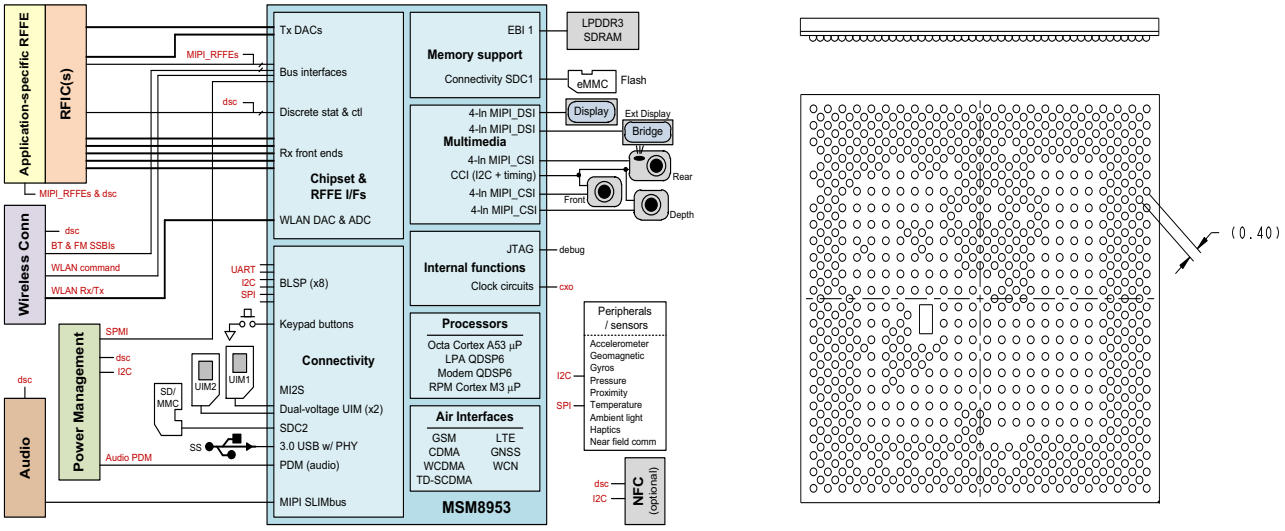
Key processor and memory characteristics include:

- Customized octa-core applications processor
  - Eight high performance cores (2.0 GHz and 2.2 GHz SKUs)
- Qualcomm® Adreno™ GPU 506 graphics processing unit (GPU) with 64-bit addressing; designed for 650 MHz

Key features (see Section 1.2 for details)

- Advanced RF techniques with WTR2965 device
  - Downlink carrier aggregation (DLCA)
  - Uplink carrier aggregation (ULCA)
- Two 4-lane DSI D-PHY 1.1, FHD
- Video 4k at 30 fps, 1080p at 60 fps, 2560 buffer width (10 layers blending), VESA DSC 1.1 Adreno GPU with Qualcomm® Universal Bandwidth Compression
- Three 4-lane CSI (4 + 4 + 4) D-PHY 1.2 at 2.1 Gbps per lane
- Dual 14-bit image signal processing (ISP): 13 MP and 13 MP; 24 MP at 30 fps ZSL with dual-ISP; 13 MP 30 fps ZSL with single-ISP
- Support for USB 3.0, eMMC 5.1, and SD 3.0
- Low-power Snapdragon sensor core with Qualcomm® Hexagon™ DSP to support always-on use cases
- WLAN 802.11 b/g/n/ac, DBS, Bluetooth 4.2, and FM with WCN3615, WCN3660B, and WCN3680B
- Non-PoP high-speed memory, LPDDR3 SDRAM designed for 933 MHz clock

MSM8953 high-level block diagram and 857 NSP package drawing



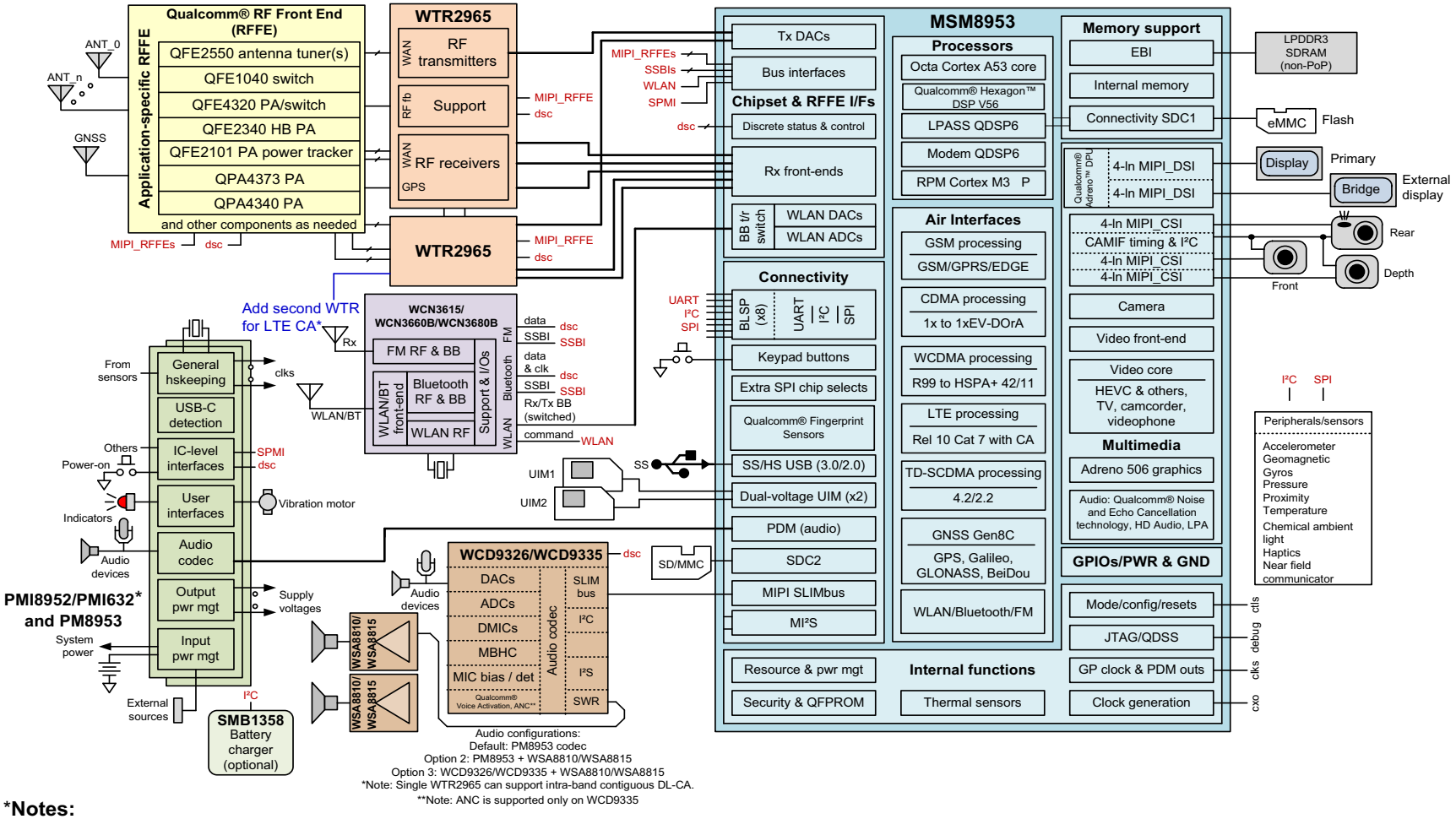
Contents

1 Introduction

Document updates

See the Revision history for details on the changes included in this revision.

1.1 Functional block diagram



***Notes:**

Qualcomm continues the support on MSM8953 + PM8953 + PMI8952 platform with Android P (OTA upgrades only)

Qualcomm will support MSM8953 + PM8953 + PMI632 for new launches with O MR1 and P

Figure 1-1 MSM8953 functional block diagram and example application

1.2 MSM8953 features

NOTE: Software enables some of the hardware features integrated within the MSM8953. To identify the enabled MSM8953 features, refer to the latest revision of the applicable software release notes.

Table 1-1 MSM8953 features

Feature	MSM8953 capability
Processors	
Applications	ARM Cortex-A53 microprocessor cores at 2.0 GHz or 2.2 GHz ■ 64-bit processor ■ Octa core: one quad with 1 MB L2 cache + one quad with 512 KB L2 cache ■ Primary boot processor
Modem system	aDSP: Hexagon DSP V56 850 MHz 768 KB L2 caches ■ MSM8953: DSDS
RPM system	Cortex M3: Modem power manager (MPM) MPM coordinates shutdown/wakeup, clock rates, and VDDs
Memory support	
System memory via EBI	Non-PoP LPDDR3 SDRAM; 32-bit wide; up to 933 MHz
Graphics internal memory	136 KB unified SRAM pool on-chip memory (GMEM)
External memory via SDC	eMMC v5.1/SD3.0 flash devices
RF support	
RF operating bands	Defined by WTR device
Air interfaces GSM CDMA WCDMA TD-SCDMA LTE WLAN/BT/FM/NFC	 Yes Yes Yes Yes Yes Yes; all (with WCN3680B/WCN3660B); Yes
GNSS: Qualcomm® Location Suite	Gen 8C supports GPS, BeiDou, GLONASS, and Galileo
Multimedia	
Display interfaces MIPI_DSI General display features	FHD; 16, 18, and 24 bpp RGB **NOTE:** Contact QTI for assistance on the display type and on the supported aspect ratio. Dual MIPI DSI four-lane Wi-Fi display: 1080p 30 fps (Snapdragon UBWC) FHD + 1080p 30 fps external wireless display

Table 1-1 MSM8953 features (cont.)

Feature	MSM8953 capability
Camera interfaces	Camera
Number of CSIs	Three; 2.1 Gbps per lane
Primary (CSI0)	Four-lane; supports CMOS and CCD sensors up to 24 MP sensors
Secondary (CSI1)	Four-lane; supports CMOS and CCD sensors up to 24 MP sensors
Tertiary (CSI2)	Four-lane; supports CMOS and CCD sensors up to 24 MP sensors
Configurations supported	Pixel manipulations, camera modes, image effects, and postprocessing techniques, including defective pixel correction
General camera features	I^2C controls
Mobile display processor	Snapdragon Display Engine 515 for display processing
Video applications performance	
Encode	4k at 30 fps, 1080p60, H.264, H.265, and VP8
Decode	4k at 30 fps, 1080p60, H.264, H.265, VP8, and VP9
Wireless display support (decode + encode)	1080p60D + 1080p30E
Graphics	Adreno 506; up to 650 MHz 3D graphics accelerator
Audio	
Low-power audio	Low-power audio for mp3 and AAC 5.1 playback; surround sound
Voice codec support	Versatile: many audio playback and voice modes; encoders for audio and FM recording; many concurrency modes
Audio codec support	G711; QCELP; EVRC, EVRC-B, EVRC-WB; AMR-NB, AMR-WB; GSM-EFR, GSM-FR, GSM-HR
Enhanced audio	MP3; aacPlus, eAAC; AMR-NB, AMR-WB, G.711, Windows Media Audio (WMA) 9/10 Pro
Synthesizer	Dolby Digital Plus and DTS-HD surround sound
	Fluence V6.1 and Qualcomm® Fluence™ Pro noise cancellation technology
	Enhanced 3D audio solution/Stereo audio expansion feature/Intelligent mixing algorithm
	128-voice polyphony wavetable
Web technologies	V8 JavaScript Engine optimizations
	WebKit browser JPEG hardware decode acceleration
	Networking stack IP and HTTP tuning
	Flash 10.x and video processor decode optimization
Messaging	Text messages; text encoding for SMS
	Multimedia messaging services: combined video (MPEG-4), still image (JPEG), voice tag (AMR), and text sent as message
Connectivity	
BLSP ports	Eight, 4 bits each; multiplexed serial interface functions
UART	Yes: up to 4 Mbps (only four ports)
I^2C	Yes: cameras, sensors, near field communicator (NFC), SMB, and so on.
SPI (master only)	Yes: cameras, sensors, and so on.
User-integrated module (UIM)	Two ports: dual voltage (1.8 V/2.85 V)
USB	One USB 3.0/2.0

Table 1-1 MSM8953 features (cont.)

Feature	MSM8953 capability
Secure digital interfaces	Up to two ports One 8-bit and one 4-bit SD 3.0; SD/multimedia card (MMC); eMMC v5.1
Wireless connectivity WLAN Bluetooth FM radio	With WCN3680B/WCN3660B/WCN3615 802.11 b/g/n/ac Bluetooth 4.2 LE and earlier Rx
Touchscreen support	Capacitive panels via ext IC (I^2C, SPI, and interrupts)
Audio interfaces MI^{2}S Serial low-power interchip media bus (SLIMbus) CDC PDM port	 Two ports (primary and secondary ports) One port SLIMbus interface to WCD9326/WCD9335 Interface between PM8953 and MSM8953 for audio application
Configurable GPIOs	
Number of GPIO ports	142 GPIOs: GPIO_0 to GPIO_141
Input configurations	Pull-up, pull-down, keeper, or no pull
Output configurations	Programmable drive current
Top-level mode multiplexer	Provides a convenient way to program groups of GPIOs
Internal functions	
Security Crypto engine QFPROM Security controller	Secure boot, SFS, ARM TrustZone, Qualcomm® Trusted Execution Environment, secure debug, and Microsoft Windows Media DRM10 Increased throughput via, increased frequencies, and a new internal AXI-based data master; support for multiple execution environments per Crypto; algorithm to accelerate file system encryption (AES-XTS), IPSec, and SSL (HMAC-SHA, CCM, CMAC) Large fuse array, replaces previous-generation Qfuse chains; nonvolatile memory with faster and simpler programming Chip-wide configuration for security, feature enable, and debug; persistent storage of ID numbers and sensitive key data; secure HDCP key provisioning and secure debug facility; primary and secondary hardware key blocking for SFS
PLLs and clocks	Multiple clock regimes; watchdog and sleep timers 19.2 MHz CXO master clock input General-purpose outputs: M/N:D counter and PDM
Resource and power manager	Fundamental to power management Key blocks: RPM core, Cortex M3, security controller, and MPM Improved efficiency via clock control, split-rail power collapse, and voltage scaling; several low-power sleep modes
Debug	JTAG and QDSS
Others	Thermal sensors; modes and resets; and peripheral subsystem

Table 1-1 MSM8953 features (cont.)

Feature	MSM8953 capability
Chipset and RF front-end (RFFE) interface features	
WTR RFICs; WLAN baseband data GNSS baseband data Status and control	WTR2965; One Rx and one Tx analog interface Rx analog interface SSBIs and discrete signals, as needed, via GPIOs
Power management	PM8953 + PMI8952/PMI632 Two 2-line SPMI; dedicated clock and reset lines; plus other GPIOs as needed
Package dimensions	857 NSP; 14 × 14 × 0.84 mm

2 Pin definitions

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high impedance) output
Pad pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters, and is a prefix to other programmable options: NP: pdpukp = default no-pull, with programmable options following the colon (:) PD: nppukp = default pull-down, with programmable options following the colon (:) PU: nppdkp = default pull-up, with programmable options following the colon (:) KP: nppdpu = default keeper, with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad-voltage groupings for baseband circuits	
P1	Pad group 1 (EBI); tied to VDDPX_1 pins (1.2 V only)
P2	Pad group 2 (SDC2); tied to VDDPX_2 pins (1.8 V or 2.95 V)
P3	Pad group 3 (most peripherals); tied to VDDPX_3 pins (1.8 V only)
P5	Pad group 5 (UIM1); tied to VDDPX_5 pins (1.8 V or 2.95 V)
P6	Pad group 6 (UIM2); tied to VDDPX_6 pins (1.8 V or 2.95 V)
P7	Pad group 7 (eMMC I/O); tied to VDDPX_7 pins (1.8 V)
MIPI	Supply voltage for MIPI_CSI and MIPI_DSI circuits and I/Os

Table 2-1 I/O description (pad type) parameters (cont.)

Symbol	Description
Output-current drive strength	
EBI pads	Pads for EBI are tailored for 1.2 V interfaces and are source terminated.
3.0 V (H) pads	Programmable drive strength, 2–8 mA, in 2 mA steps
Others [1]	Programmable drive strength, 2–16 mA, in 2 mA steps

1. Digital pads other than EBI0 pads or high-voltage tolerant pads.

2.2 Pin assignments

2.2.1 Pin map

The MSM8953 is available in the 857 NSP. The bottom surface is equivalent to an 857 NSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details.

A high-level view of the pin assignments is shown in Figure 2-2. Each pin is colored to indicate the function type that it supports; these colors are defined in Figure 2-1.

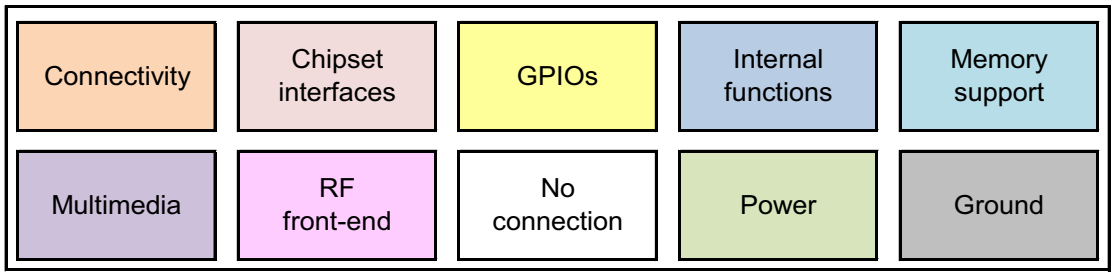


Figure 2-1 MSM8953 pin assignment legend

The text within Figure 2-2 is difficult to read when viewing an 8½" × 11" hard copy. Other viewing options are available:

- Print that one page on an 11" × 17" sheet.
- View the graphic's PDF soft copy and zoom in — the resolution is sufficient for comfortable reading.
- Download the *MSM8953 Pin Assignment Spreadsheet* (80-P2472-1A). This Microsoft Excel spreadsheet lists all MSM8953 pad numbers (in alphanumeric order), pad names, pad voltages, pad types, and functional descriptions.

NOTE: Click the following link to download the pin assignment spreadsheet (80-P2472-1A) from the Qualcomm® CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-P2472-1A

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

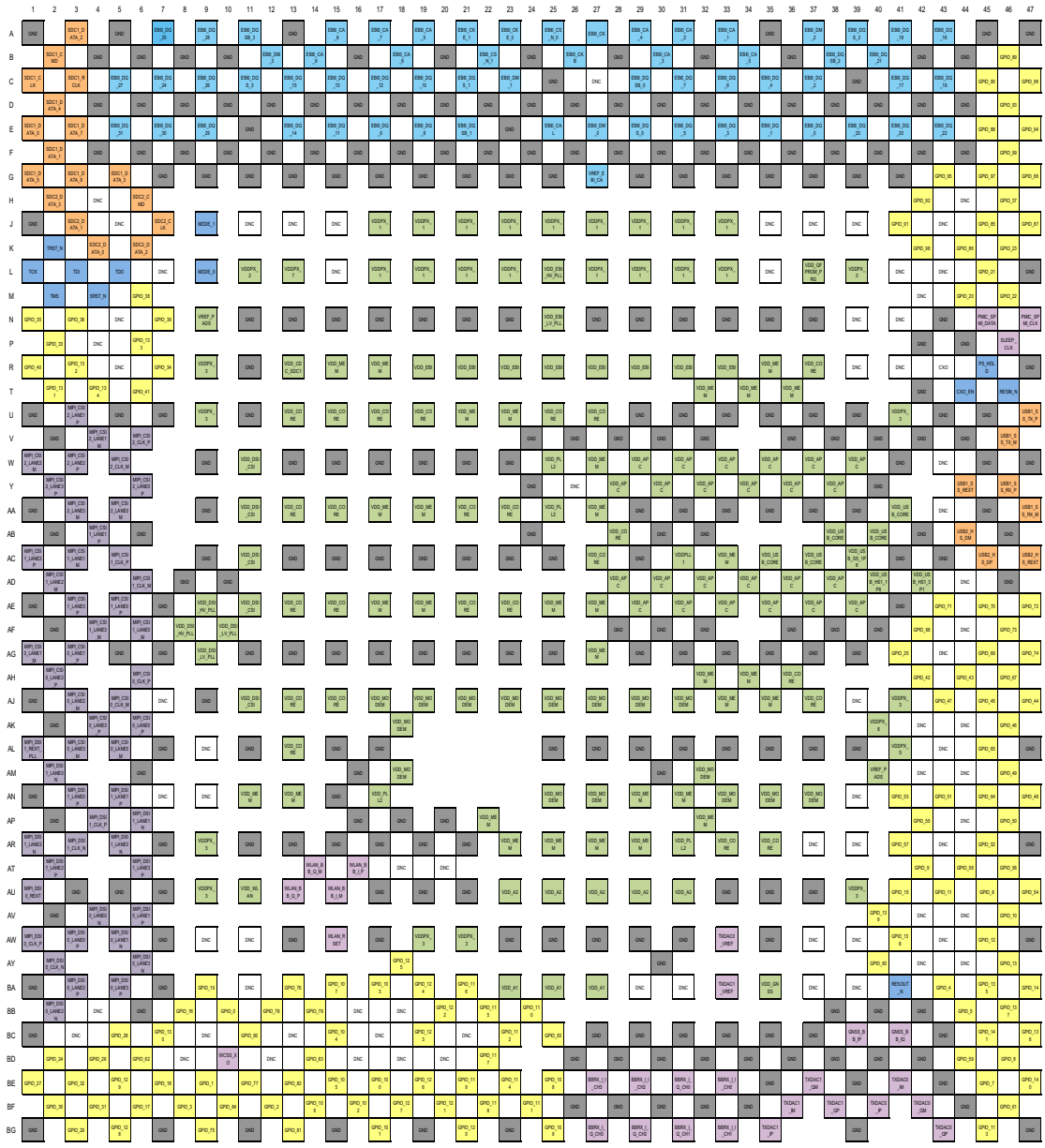


Figure 2-2 MSM8953 pin assignments

2.2.2 Pin descriptions

Descriptions of bottom pins are presented in the following tables, organized by functional group:

Table 2-2: Boot configuration GPIOs

Table 2-3: Memory support functions

Table 2-4: Multimedia functions

Table 2-5: Connectivity functions

Table 2-2 Boot configuration GPIOs

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Pad	Voltage	
BF14	BOOT_CONFIG[0]	GPIO_106	P3	DI B-PD:nppukp	fast_boot_select bit 0 Configurable I/O
BG45	BOOT_CONFIG[1]	GPIO_113	P3	DI B-PD:nppukp	fast_boot_select bit 1 Configurable I/O
BA15	BOOT_CONFIG[2]	GPIO_107	P3	DI B-PD:nppukp	fast_boot_select bit 2 Configurable I/O
BG25	BOOT_CONFIG[3]	GPIO_109	P3	DI B-PD:nppukp	fast_boot_select bit 3 Configurable I/O
BE15	BOOT_CONFIG[4]	GPIO_105	P3	DI B-PD:nppukp	fast_boot_select bit 4 Configurable I/O
BE25	BOOT_CONFIG[5]	GPIO_108	P3	DI B-PD:nppukp	fast_boot_select bit 5 Configurable I/O
BE23	BOOT_CONFIG[6]	GPIO_114	P3	DI B-PD:nppukp	fast_boot_select bit 6 Configurable I/O
BC15	BOOT_CONFIG[7]	GPIO_104	P3	DI B-PD:nppukp	fast_boot_select bit 7 Configurable I/O
BB24	BOOT_CONFIG[8]	GPIO_110	P3	DI B-PD:nppukp	fast_boot_select bit 8 Configurable I/O
T6	BOOT_CONFIG[9]	GPIO_41	P3	DI B-PD:nppukp	fast_boot_select bit 9 Configurable I/O
BC23	BOOT_CONFIG[10]	GPIO_112	P3	DI B-PD:nppukp	fast_boot_select bit 10 Configurable I/O
BF24	BOOT_CONFIG[11]	GPIO_111	P3	DI B-PD:nppukp	fast_boot_select bit 11 Configurable I/O
N1	BOOT_CONFIG[12]	GPIO_35	P3	DI B-PD:nppukp	fast_boot_select bit 12 Configurable I/O
R3	BOOT_CONFIG[13]	GPIO_132	P3	DI B-PD:nppukp	fast_boot_select bit 13 Configurable I/O

Table 2-2 Boot configuration GPIOs

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Pad	Voltage	
BC7	BOOT_CONFIG[14]	GPIO_130	P3	DI B-PD:nppukp	fast_boot_select bit 14 Configurable I/O
H46	FORCED_USB_BOOT	GPIO_37	P3	DI B-PD:nppukp	Forced USB boot Configurable I/O

1. See Table 2-1 for parameter and acronym definitions.

Table 2-3 Pin descriptions: memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
LPDDR3 interface					
B34	EBI0_CA_0		P1	DO	LPDDR3 command/address bit 0
A33	EBI0_CA_1		P1	DO	LPDDR3 command/address bit 1
A31	EBI0_CA_2		P1	DO	LPDDR3 command/address bit 2
B30	EBI0_CA_3		P1	DO	LPDDR3 command/address bit 3
A29	EBI0_CA_4		P1	DO	LPDDR3 command/address bit 4
A19	EBI0_CA_5		P1	DO	LPDDR3 command/address bit 5
B18	EBI0_CA_6		P1	DO	LPDDR3 command/address bit 6
A17	EBI0_CA_7		P1	DO	LPDDR3 command/address bit 7
A15	EBI0_CA_8		P1	DO	LPDDR3 command/address bit 8
B14	EBI0_CA_9		P1	DO	LPDDR3 command/address bit 9
E25	EBI0_CAL		P1	AI	LPDDR3 calibration resistor
A27	EBI0_CK		P1	DO	LPDDR3 differential clock (+)
B26	EBI0_CKB		P1	DO	LPDDR3 differential clock (-)
A23	EBI0_CKE_0		P1	DO	LPDDR3 clock enable 0
A21	EBI0_CKE_1		P1	DO	LPDDR3 clock enable 1
A25	EBI0_CS_N_0		P1	DO	LPDDR3 chip select 0
B22	EBI0_CS_N_1		P1	DO	LPDDR3 chip select 1
E27	EBI0_DM_0		P1	DO	LPDDR3 data mask for byte 0
C23	EBI0_DM_1		P1	DO	LPDDR3 data mask for byte 1
A37	EBI0_DM_2		P1	DO	LPDDR3 data mask for byte 2
B12	EBI0_DM_3		P1	DO	LPDDR3 data mask for byte 3
E37	EBI0_DQ_0		P1	B	LPDDR3 data bit 0
E35	EBI0_DQ_1		P1	B	LPDDR3 data bit 1
C19	EBI0_DQ_10		P1	B	LPDDR3 data bit 10
E15	EBI0_DQ_11		P1	B	LPDDR3 data bit 11
C17	EBI0_DQ_12		P1	B	LPDDR3 data bit 12
C15	EBI0_DQ_13		P1	B	LPDDR3 data bit 13
E13	EBI0_DQ_14		P1	B	LPDDR3 data bit 14
C13	EBI0_DQ_15		P1	B	LPDDR3 data bit 15

Table 2-3 Pin descriptions: memory support functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
A43	EBI0_DQ_16		P1	B	LPDDR3 data bit 16
C41	EBI0_DQ_17		P1	B	LPDDR3 data bit 17
A41	EBI0_DQ_18		P1	B	LPDDR3 data bit 18
C43	EBI0_DQ_19		P1	B	LPDDR3 data bit 19
C37	EBI0_DQ_2		P1	B	LPDDR3 data bit 2
E41	EBI0_DQ_20		P1	B	LPDDR3 data bit 20
B40	EBI0_DQ_21		P1	B	LPDDR3 data bit 21
E43	EBI0_DQ_22		P1	B	LPDDR3 data bit 22
E39	EBI0_DQ_23		P1	B	LPDDR3 data bit 23
C7	EBI0_DQ_24		P1	B	LPDDR3 data bit 24
A7	EBI0_DQ_25		P1	B	LPDDR3 data bit 25
C9	EBI0_DQ_26		P1	B	LPDDR3 data bit 26
C5	EBI0_DQ_27		P1	B	LPDDR3 data bit 27
A9	EBI0_DQ_28		P1	B	LPDDR3 data bit 28
E9	EBI0_DQ_29		P1	B	LPDDR3 data bit 29
E33	EBI0_DQ_3		P1	B	LPDDR3 data bit 3
E7	EBI0_DQ_30		P1	B	LPDDR3 data bit 30
E5	EBI0_DQ_31		P1	B	LPDDR3 data bit 31
C35	EBI0_DQ_4		P1	B	LPDDR3 data bit 4
E31	EBI0_DQ_5		P1	B	LPDDR3 data bit 5
C33	EBI0_DQ_6		P1	B	LPDDR3 data bit 6
C31	EBI0_DQ_7		P1	B	LPDDR3 data bit 7
E19	EBI0_DQ_8		P1	B	LPDDR3 data bit 8
E17	EBI0_DQ_9		P1	B	LPDDR3 data bit 9
E29	EBI0_DQS_0		P1	B	LPDDR3 differential data strobe for byte 0 (+)
C21	EBI0_DQS_1		P1	B	LPDDR3 differential data strobe for byte 1 (+)
A39	EBI0_DQS_2		P1	B	LPDDR3 differential data strobe for byte 2 (+)
C11	EBI0_DQS_3		P1	B	LPDDR3 differential data strobe for byte 3 (+)
C29	EBI0_DQSB_0		P1	B	LPDDR3 differential data strobe for byte 0 (-)
E21	EBI0_DQSB_1		P1	B	LPDDR3 differential data strobe for byte 1 (-)
B38	EBI0_DQSB_2		P1	B	LPDDR3 differential data strobe for byte 2 (-)
A11	EBI0_DQSB_3		P1	B	LPDDR3 differential data strobe for byte 3 (-)

1. See Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions: multimedia functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Primary camera serial interface: four-lane MIPI-CSI (CSI0)					
AH6	MIPI_CSI0_CLK_P		CSI	AI	MIPI camera serial interface 0 clock – positive
AJ5	MIPI_CSI0_CLK_M		CSI	AI	MIPI camera serial interface 0 clock – negative
AK6	MIPI_CSI0_LANE0_P		CSI	AI	MIPI camera serial interface 0 lane 0 – positive
AL5	MIPI_CSI0_LANE0_M		CSI	AI	MIPI camera serial interface 0 lane 0 – negative
AG3	MIPI_CSI0_LANE1_P		CSI	AI	MIPI camera serial interface 0 lane 1 – positive
AG1	MIPI_CSI0_LANE1_M		CSI	AI	MIPI camera serial interface 0 lane 1 – negative
AH2	MIPI_CSI0_LANE2_P		CSI	AI	MIPI camera serial interface 0 lane 2 – positive
AJ3	MIPI_CSI0_LANE2_M		CSI	AI	MIPI camera serial interface 0 lane 2 – negative
AK4	MIPI_CSI0_LANE3_P		CSI	AI	MIPI camera serial interface 0 lane 3 – positive
AL3	MIPI_CSI0_LANE3_M		CSI	AI	MIPI camera serial interface 0 lane 3 – negative
Four-lane MIPI-CSI (CSI1)					
AC5	MIPI_CSI1_CLK_P		CSI	AI	MIPI camera serial interface 1 clock – positive
AD6	MIPI_CSI1_CLK_M		CSI	AI	MIPI camera serial interface 1 clock – negative
AE5	MIPI_CSI1_LANE0_P		CSI	AI	MIPI camera serial interface 1 lane 0 – positive
AF6	MIPI_CSI1_LANE0_M		CSI	AI	MIPI camera serial interface 1 lane 0 – negative
AB4	MIPI_CSI1_LANE1_P		CSI	AI	MIPI camera serial interface 1 lane 1 – positive
AC3	MIPI_CSI1_LANE1_M		CSI	AI	MIPI camera serial interface 1 lane 1 – negative
AC1	MIPI_CSI1_LANE2_P		CSI	AI	MIPI camera serial interface 1 lane 2 – positive
AD2	MIPI_CSI1_LANE2_M		CSI	AI	MIPI camera serial interface 1 lane 2 – negative
AE3	MIPI_CSI1_LANE3_P		CSI	AI	MIPI camera serial interface 1 lane 3 – positive
AF4	MIPI_CSI1_LANE3_M		CSI	AI	MIPI camera serial interface 1 lane 3 – negative
Four-lane MIPI CSI (CSI2)					
V6	MIPI_CSI2_CLK_P		CSI	AI	MIPI camera serial interface 2 clock – positive
W5	MIPI_CSI2_CLK_M		CSI	AI	MIPI camera serial interface 2 clock – negative
Y6	MIPI_CSI2_LANE0_P		CSI	AI	MIPI camera serial interface 2 lane 0 – positive
AA5	MIPI_CSI2_LANE0_M		CSI	AI	MIPI camera serial interface 2 lane 0 – negative
U3	MIPI_CSI2_LANE1_P		CSI	AI	MIPI camera serial interface 2 lane 1 – positive
V4	MIPI_CSI2_LANE1_M		CSI	AI	MIPI camera serial interface 2 lane 1 – negative
W3	MIPI_CSI2_LANE2_P		CSI	AI	MIPI camera serial interface 2 lane 2 – positive
W1	MIPI_CSI2_LANE2_M		CSI	AI	MIPI camera serial interface 2 lane 2 – negative
Y2	MIPI_CSI2_LANE3_P		CSI	AI	MIPI camera serial interface 2 lane 3 – positive
AA3	MIPI_CSI2_LANE3_M		CSI	AI	MIPI camera serial interface 2 lane 3 – negative
Camera-timing and CCI signals					
BD4	CAM_MCLK0	GPIO_26	P3	DO B-PD:nppukp	Camera master clock 0 – rear camera Configurable I/Os
BE1	CAM_MCLK1	GPIO_27	P3	DO B-PD:nppukp	Camera master clock 1 – front camera Configurable I/Os

Table 2-4 Pin descriptions: multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BC5	CAM_MCLK2	GPIO_28	P3	DO B-PD:nppukp	Camera master clock 2 – depth camera Configurable I/Os
BG5	CAM_MCLK3	GPIO_128	P3	DO B-PD:nppukp	Camera master clock 3 – depth camera Configurable I/Os
BG3	CCI_I2C_SDA0	GPIO_29	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 0 serial data Configurable I/Os
BF2	CCI_I2C_SCL0	GPIO_30	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 0 clock Configurable I/Os
BF4	CCI_I2C_SDA1	GPIO_31	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 1 serial data Configurable I/Os
BE3	CCI_I2C_SCL1	GPIO_32	P3	B B-PD:nppukp	Dedicated camera control interface I^2C 1 clock Configurable I/Os
P2	CCI_TIMER0	GPIO_33	P3	DO B-PD:nppukp	Camera control interface timer 0 Configurable I/Os
R7	CCI_TIMER1	GPIO_34	P3	DO B-PD:nppukp	Camera control interface timer 1 Configurable I/Os
N1	CCI_TIMER2	GPIO_35	P3	DO B-PD:nppukp	Camera control interface timer 2 Configurable I/Os
N3	CCI_TIMER3	GPIO_36	P3	DO B-PD:nppukp	Camera control interface timer 3 Configurable I/Os
T6	CCI_TIMER4	GPIO_41	P3	DO B-PD:nppukp	Camera control interface timer 4 Configurable I/Os
M6	CCI_ASYNC_IN0	GPIO_38	P3	DI B-PD:nppukp	Camera control interface async 0 Configurable I/Os
N7	CAM1_STANDBY_N	GPIO_39	P3	DO B-PD:nppukp	Rear camera standby Configurable I/Os
R1	CAM1_RST_N	GPIO_40	P3	DO B-PD:nppukp	Rear camera reset Configurable I/Os
BC7	CAM2_STANDBY_N	GPIO_130	P3	DO B-PD:nppukp	Depth camera standby Configurable I/Os
BE5	CAM2_RST_N	GPIO_129	P3	DO B-PD:nppukp	Depth camera reset Configurable I/Os
R3	CAM3_STANDBY_N	GPIO_132	P3	DO B-PD:nppukp	Front camera standby Configurable I/Os
T2	CAM3_RST_N	GPIO_131	P3	DO B-PD:nppukp	Front camera reset Configurable I/Os
Snapdragon Display Engine vertical sync					
BD2	GPIO_24		P3	DI	Snapdragon Display Engine vertical sync – primary
AG41	GPIO_25		P3	DI	Snapdragon Display Engine vertical sync – secondary
Display serial interface: Four-lane DSI0					

Table 2-4 Pin descriptions: multimedia functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AY2	MIPI_DSI0_CLK_N		DSI	AO	MIPI display serial interface 0 clock – negative
AW1	MIPI_DSI0_CLK_P		DSI	AO	MIPI display serial interface 0 clock – positive
AV4	MIPI_DSI0_LANE0_N		DSI	AI, AO	MIPI display serial interface 0 lane 0 – negative
AW3	MIPI_DSI0_LANE0_P		DSI	AI, AO	MIPI display serial interface 0 lane 0 – positive
AW5	MIPI_DSI0_LANE1_N		DSI	AI, AO	MIPI display serial interface 0 lane 1 – negative
AV6	MIPI_DSI0_LANE1_P		DSI	AI, AO	MIPI display serial interface 0 lane 1 – positive
BB2	MIPI_DSI0_LANE2_N		DSI	AI, AO	MIPI display serial interface 0 lane 2 – negative
BA3	MIPI_DSI0_LANE2_P		DSI	AI, AO	MIPI display serial interface 0 lane 2 – positive
AY6	MIPI_DSI0_LANE3_N		DSI	AI, AO	MIPI display serial interface 0 lane 3 – negative
BA5	MIPI_DSI0_LANE3_P		DSI	AI, AO	MIPI display serial interface 0 lane 3 – positive
AU1	MIPI_DSI0_REXT		DSI	AI, AO	MIPI display serial interface 0 external calibration resistor
Display serial interface: Four-lane DSI1					
AR3	MIPI_DSI1_CLK_N		DSI	AO	MIPI display serial interface 1 clock – negative
AP4	MIPI_DSI1_CLK_P		DSI	AO	MIPI display serial interface 1 clock – positive
AM2	MIPI_DSI1_LANE0_N		DSI	AI, AO	MIPI display serial interface 1 lane 0 – negative
AN3	MIPI_DSI1_LANE0_P		DSI	AI, AO	MIPI display serial interface 1 lane 0 – positive
AP6	MIPI_DSI1_LANE1_N		DSI	AI, AO	MIPI display serial interface 1 lane 1 – negative
AN5	MIPI_DSI1_LANE1_P		DSI	AI, AO	MIPI display serial interface 1 lane 1 – positive
AR1	MIPI_DSI1_LANE2_N		DSI	AI, AO	MIPI display serial interface 1 lane 2 – negative
AT2	MIPI_DSI1_LANE2_P		DSI	AI, AO	MIPI display serial interface 1 lane 2 – positive
AR5	MIPI_DSI1_LANE3_N		DSI	AI, AO	MIPI display serial interface 1 lane 3 – negative
AT6	MIPI_DSI1_LANE3_P		DSI	AI, AO	MIPI display serial interface 1 lane 3 – positive
AL1	MIPI_DSI1_REXT		DSI	AI, AO	MIPI display serial interface 1 external calibration resistor

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

Table 2-5 Pin descriptions: connectivity functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
Super-speed USB 3.0					
Y44	USB1_SS_REXT		P3	AI, AO	USB1 super-speed – external resistor
AA47	USB1_SS_RX_M		P3	AI	USB1 super-speed receive – minus
Y46	USB1_SS_RX_P		P3	AI	USB1 super-speed receive – plus
V46	USB1_SS_TX_M		P3	AO	USB1 super-speed transmit – minus
U47	USB1_SS_TX_P		P3	AO	USB1 super-speed transmit – plus
AB44	USB2_HS_DM		P3	AI, AO	USB2 high-speed data – minus
AC45	USB2_HS_DP		P3	AI, AO	USB2 high-speed data – plus
AC47	USB2_HS_REXT		P3	AI	USB2 high-speed data – external resistor
AV40	USB_SS_SWITCH_SEL	GPIO_139	P3	DO B-PD:nppukp	USB Type-C switch control input Configurable I/O
Secure digital controller 1 (SDC 1) interface–supports dual voltage eMMC/NAND and interface					
C1	SDC1_CLK		P7	B-NP:pdpukp	Secure digital controller 1 clock
C3	SDC1_RCLK		P7	DI-PD:nppukp	Secure digital controller 1 return clock
B2	SDC1_CMD		P7	B-PD:nppukp	Secure digital controller 1 command
E1	SDC1_DATA_0		P7	B-PD:nppukp	Secure digital controller 1 data bit 0
F2	SDC1_DATA_1		P7	B-PD:nppukp	Secure digital controller 1 data bit 1
A3	SDC1_DATA_2		P7	B-PD:nppukp	Secure digital controller 1 data bit 2
G5	SDC1_DATA_3		P7	B-PD:nppukp	Secure digital controller 1 data bit 3
D2	SDC1_DATA_4		P7	B-PD:nppukp	Secure digital controller 1 data bit 4
G1	SDC1_DATA_5		P7	B-PD:nppukp	Secure digital controller 1 data bit 5
G3	SDC1_DATA_6		P7	B-PD:nppukp	Secure digital controller 1 data bit 6
E3	SDC1_DATA_7		P7	B-PD:nppukp	Secure digital controller 1 data bit 7
Secure digital controller 2 (SDC 2) interface–supports dual voltage SD 3.0 card interface					
J7	SDC2_CLK		P2	BH-NP:pdpukp	Secure digital controller 2 clock
H6	SDC2_CMD		P2	BH-PD:nppukp	Secure digital controller 2 command
K4	SDC2_DATA_0		P2	BH-PD:nppukp	Secure digital controller 2 data bit 0
J3	SDC2_DATA_1		P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
K6	SDC2_DATA_2		P2	BH-PD:nppukp	Secure digital controller 2 data bit 2
H2	SDC2_DATA_3		P2	BH-PD:nppukp	Secure digital controller 2 data bit 3
P6	SD_CARD_DET_N	GPIO_133	P3	DI B-PD:nppukp	Secure digital card detection Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AP46	SD_WRITE_PROTECT	GPIO_50	P3	DI B-PD:nppukp	Secure digital card write protection Configurable I/O
UIM interface –UIM 1					
AN43	UIM1_DATA	GPIO_51	P5	B B-PD:nppukp	Dual voltage UIM1 data Configurable I/O
AR45	UIM1_CLK	GPIO_52	P5	DO B-PD:nppukp	Dual voltage UIM1 clock Configurable I/O
AN41	UIM1_RESET	GPIO_53	P5	DO B-PD:nppukp	Dual voltage UIM1 reset Configurable I/O
AU47	UIM1_DETECT	GPIO_54	P3	DI B-PD:nppukp	UIM1 detect (non-dual voltage) Configurable I/O
UIM interface –UIM 2					
AP42	UIM2_DATA	GPIO_55	P6	B B-PD:nppukp	Dual voltage UIM2 data Configurable I/O
AT46	UIM2_CLK	GPIO_56	P6	DO B-PD:nppukp	Dual voltage UIM2 clock Configurable I/O
AR41	UIM2_RESET	GPIO_57	P6	DO B-PD:nppukp	Dual voltage UIM2 reset Configurable I/O
AT44	UIM2_DETECT	GPIO_58	P3	DI B-PD:nppukp	UIM2 detect (non-dual voltage) Configurable I/O
Additional UIM control					
AM46	UIM_BATT_ALARM	GPIO_49	P3	DI B-PD:nppukp	UIM battery alarm Configurable I/O
Sensor and keypad					
AH42	ACCEL_INT	GPIO_42	P3	DI B-PD:nppukp	Accelerometer sensor interrupt Configurable I/O
AH44	ALSP_INT_N	GPIO_43	P3	DI B-PD:nppukp	Ambient light sensor interrupt Configurable I/O
AJ47	MAG_INT	GPIO_44	P3	DI B-PD:nppukp	Magnetic sensor interrupt Configurable I/O
AJ45	GYRO_INT	GPIO_45	P3	DI B-PD:nppukp	Gyro sensor interrupt Configurable I/O
AK46	PRESSURE_INT	GPIO_46	P3	DI B-PD:nppukp	Pressure sensor interrupt Configurable I/O
J45	KEY_VOLP_N	GPIO_85	P3	DI B-PD:nppukp	Volume key interrupt Configurable I/O
K44	KEY_SNAPSHOT	GPIO_86	P3	DI B-PD:nppukp	Snapshot interrupt Configurable I/O
J47	KEY_FOCUS	GPIO_87	P3	DI B-PD:nppukp	Focus interrupt Configurable I/O
E45	KEY_HOME	GPIO_88	P3	DI B-PD:nppukp	Home key interrupt Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BE9	SMB_INT	GPIO_1	P3	DO B-PD:nppukp	SMB charger interrupt Configurable I/O
Audio MI^{2}S master clocks					
AG41	PRI_MI2S_MCLK_A	GPIO_25	P3	DO B-PD:nppukp	Primary MI^{2}S master clock A Configurable I/O
AG41	SEC_MI2S_MCLK_A	GPIO_25	P3	DO B-PD:nppukp	Secondary MI^{2}S master clock A Configurable I/O
AG45	PRI_MI2S_MCLK_B	GPIO_69	P3	DO B-PD:nppukp	Primary MI^{2}S master clock B Configurable I/O
G47	PRI_MI2S_MCLK_C	GPIO_66	P3	DO B-PD:nppukp	Primary MI^{2}S master clock C Configurable I/O
G47	SEC_MI2S_MCLK_B	GPIO_66	P3	DO B-PD:nppukp	Secondary MI^{2}S master clock B Configurable I/O
Audio MI2S interface #1 –primary					
J41	MI2S_1_SCK	GPIO_91	P3	B B-PD:nppukp	MI^{2}S #1-bit clock Configurable I/O
H42	MI2S_1_WS	GPIO_92	P3	B B-PD:nppukp	MI^{2}S #1 word select (L/R) Configurable I/O
D46	MI2S_1_D0	GPIO_93	P3	B B-PD:nppukp	MI^{2}S #1 serial data channel 0 Configurable I/O
E45	MI2S_1_D1	GPIO_88	P3	B B-PD:nppukp	MI^{2}S #1 serial data channel 1 Configurable I/O
E47	MI2S_1_D2	GPIO_94	P3	B B-PD:nppukp	MI^{2}S #1 serial data channel 2 Configurable I/O
G43	MI2S_1_D3	GPIO_95	P3	B B-PD:nppukp	MI^{2}S #1 serial data channel 3 Configurable I/O
Audio MI2S interface #2 –secondary					
BA45	MI2S_2_SCK	GPIO_135	P3	B B-PD:nppukp	MI^{2}S #2-bit clock Configurable I/O
BC47	MI2S_2_WS	GPIO_136	P3	B B-PD:nppukp	MI^{2}S #2 word select (L/R) Configurable I/O
BB46	MI2S_2_D0	GPIO_137	P3	B B-PD:nppukp	MI^{2}S #2 serial data channel 0 Configurable I/O
AW41	MI2S_2_D1	GPIO_138	P3	B B-PD:nppukp	MI^{2}S #2 serial data channel 1 Configurable I/O
Audio codec interface					
AG47	CDC_PDM_RX2	GPIO_74	P3	DO B-PD:nppukp	PDM receive data channel 2 Configurable I/O
AF46	CDC_PDM_RX1	GPIO_73	P3	DO B-PD:nppukp	PDM receive data channel 1 Configurable I/O
AE47	CDC_PDM_RX0	GPIO_72	P3	DO B-PD:nppukp	PDM receive data channel 0 Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AE43	CDC_PDM_TX0	GPIO_71	P3	DI B-PD:nppukp	PDM transmit data channel 0 Configurable I/O
AE45	CDC_PDM_SYNC	GPIO_70	P3	DO B-PD:nppukp	PDM synchronization signal Configurable I/O
AG45	CDC_PDM_CLK	GPIO_69	P3	DO B-PD:nppukp	Audio codec PDM clock signal and codec master clock Configurable I/O
AF42	CDC_PDM_RX1_DRE	GPIO_68	P3	DO B-PD:nppukp	PDM Rx1 DRE data channel Configurable I/O
AH46	CDC_PDM_RX0_DRE	GPIO_67	P3	DO B-PD:nppukp	PDM Rx0 DRE data channel Configurable I/O
Audio SLIMbus –low-power audio subsystem					
AE45	SLIMBUS_CLK	GPIO_70	P3	DO B-PD:nppukp	Low-power audio SLIMbus clock Configurable I/O
AE43	SLIMBUS_DATA0	GPIO_71	P3	DO B-PD:nppukp	Low-power audio SLIMbus data 0 Configurable I/O
AE47	SLIMBUS_DATA1	GPIO_72	P3	DO B-PD:nppukp	Low-power audio SLIMbus data 1 Configurable I/O
Digital MIC interface					
B46	DMIC0_CLK	GPIO_89	P3	DO B-PD:nppukp	Digital MIC0 clock Configurable I/O
C45	DMIC0_DATA	GPIO_90	P3	DI B-PD:nppukp	Digital MIC0 data Configurable I/O
E47	WSA_IO_DATA	GPIO_94	P3	DI B-PD:nppukp	WSA8810 current/voltage sense data for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326) Configurable I/O
G43	WSA_IO_CLK	GPIO_95	P3	DO B-PD:nppukp	WSA8810 current/voltage sense clock for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326) Configurable I/O
BAM-based low-speed peripheral interface 1–BLSP 1					
BB10	BLSP1_3	GPIO_0	P3	B B-PD:nppukp	BLSP 1 bit 3; SPI Configurable I/O
BE9	BLSP1_2	GPIO_1	P3	B B-PD:nppukp	BLSP 1 bit 2; SPI Configurable I/O
BF12	BLSP1_1	GPIO_2	P3	B B-PD:nppukp	BLSP 1 bit 1; SPI/I^2C Configurable I/O
BF8	BLSP1_0	GPIO_3	P3	B B-PD:nppukp	BLSP 1 bit 0; SPI/I^2C Configurable I/O
BAM-based low speed peripheral interface 2 –BLSP 2					
BA43	BLSP2_3	GPIO_4	P3	B B-PD:nppukp	BLSP 2 bit 3; SPI/UART Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BB44	BLSP2_2	GPIO_5	P3	B B-PD:nppukp	BLSP 2 bit 2; SPI/UART Configurable I/O
BD46	BLSP2_1	GPIO_6	P3	B B-PD:nppukp	BLSP 2 bit 1; SPI/I^{2}C/UART Configurable I/O
BE45	BLSP2_0	GPIO_7	P3	B B-PD:nppukp	BLSP 2 bit 0; SPI/I^{2}C/UART Configurable I/O
BAM-based low speed peripheral interface 3–BLSP 3					
AU45	BLSP3_3	GPIO_8	P3	B B-PD:nppukp	BLSP 3 bit 3; SPI Configurable I/O
AT42	BLSP3_2	GPIO_9	P3	B B-PD:nppukp	BLSP 3 bit 2; SPI Configurable I/O
AV46	BLSP3_1	GPIO_10	P3	B B-PD:nppukp	BLSP 3 bit 1; SPI/I^{2}C Configurable I/O
AU43	BLSP3_0	GPIO_11	P3	B B-PD:nppukp	BLSP 3 bit 0; SPI/I^{2}C Configurable I/O
BAM-based low speed peripheral interface 4 –BLSP 4					
AW45	BLSP4_3	GPIO_12	P3	B B-PD:nppukp	BLSP 4 bit 3; SPI/UART Configurable I/O
AY46	BLSP4_2	GPIO_13	P3	B B-PD:nppukp	BLSP 4 bit 2; SPI/UART Configurable I/O
BA47	BLSP4_1	GPIO_14	P3	B B-PD:nppukp	BLSP 4 bit 1; SPI/I^{2}C/UART Configurable I/O
AU41	BLSP4_0	GPIO_15	P3	B B-PD:nppukp	BLSP 4 bit 0; SPI/I^{2}C/UART Configurable I/O
BAM-based low speed peripheral interface 5–BLSP 5					
BB8	BLSP5_3	GPIO_16	P3	B B-PD:nppukp	BLSP 5 bit 3; SPI/UART Configurable I/O
BF6	BLSP5_2	GPIO_17	P3	B B-PD:nppukp	BLSP 5 bit 2; SPI/UART Configurable I/O
BE7	BLSP5_1	GPIO_18	P3	B B-PD:nppukp	BLSP 5 bit 1; SPI/I^{2}C/UART Configurable I/O
BA9	BLSP5_0	GPIO_19	P3	B B-PD:nppukp	BLSP 5 bit 0; SPI/I^{2}C/UART Configurable I/O
BAM-based low speed peripheral interface 6–BLSP 6					
M44	BLSP6_3	GPIO_20	P3	B B-PD:nppukp	BLSP 6 bit 3; SPI/UART Configurable I/O
L45	BLSP6_2	GPIO_21	P3	B B-PD:nppukp	BLSP 6 bit 2; SPI/UART Configurable I/O
M46	BLSP6_1	GPIO_22	P3	B B-PD:nppukp	BLSP 6 bit 1; SPI/I^{2}C/UART Configurable I/O
K46	BLSP6_0	GPIO_23	P3	B B-PD:nppukp	BLSP 6 bit 0; SPI/I^{2}C/UART Configurable I/O

Table 2-5 Pin descriptions: connectivity functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BAM-based low speed peripheral interface 7–BLSP 7					
BB46	BLSP7_3	GPIO_137	P3	B B-PD:nppukp	BLSP 7 bit 3; SPI Configurable I/O
AW41	BLSP7_2	GPIO_138	P3	B B-PD:nppukp	BLSP 7 bit 2; SPI Configurable I/O
BC47	BLSP7_1	GPIO_136	P3	B B-PD:nppukp	BLSP 7 bit 1; SPI/I^2C Configurable I/O
BA45	BLSP7_0	GPIO_135	P3	B B-PD:nppukp	BLSP 7 bit 0; SPI/I^2C Configurable I/O
BAM-based low speed peripheral interface 8–BLSP 8					
C47	BLSP8_3	GPIO_96	P3	B B-PD:nppukp	BLSP 8 bit 3; SPI Configurable I/O
G45	BLSP8_2	GPIO_97	P3	B B-PD:nppukp	BLSP 8 bit 2; SPI Configurable I/O
K42	BLSP8_1	GPIO_98	P3	B B-PD:nppukp	BLSP 8 bit 1; SPI/I^2C Configurable I/O
F46	BLSP8_0	GPIO_99	P3	B B-PD:nppukp	BLSP 8 bit 0; SPI/I^2C Configurable I/O
Serial peripheral interface (SPI) extra chip selects (supplements BLSP ports configured for the SPI protocol)					
N1	SPI1_CS1	GPIO_35	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP1
N3	SPI1_CS2	GPIO_36	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP1
T6	SPI3_CS1	GPIO_41	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP3 Configurable I/O
AP46	SPI3_CS2	GPIO_50	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP3 Configurable I/O
AN47	SPI6_CS1	GPIO_48	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP6 Configurable I/O
AJ43	SPI6_CS2	GPIO_47	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP6 Configurable I/O
B46	SPI7_CS1	GPIO_89	P3	DO-Z B-PD:nppukp	Chip select 1 for SPI on BLSP7 Configurable I/O
C45	SPI7_CS2	GPIO_90	P3	DO-Z B-PD:nppukp	Chip select 2 for SPI on BLSP7 Configurable I/O

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

BLSP interfaces

The BAM integrates three serial bus cores: UARTDM, SPI, and I^{2}C. The SPI and I^{2}C cores are, in turn, integrated into a single core called the Qualcomm Unified Peripheral (QUP) where both the subcores share the same FIFO. The UARTDM is integrated separately with its own FIFO. All the cores share the same bus interface.

The external I/O ports of these cores are shared and only one of the cores can be used at any given time. However, in the mode where UARTDM is used as a two-pin UART interface, the I^{2}C, which is also a two-pin two-pin interface, can be used simultaneously with UART functionality.The BLSP supports the following serial protocols:

- UART_DM
- I^{2}C (master only), driven by QUP
- SPI, driven by QUP

Table 2-6 BLSP alternate function configurations

Pad name	Alternate functions		
GPIO[0]	SPI1_MOSI		
GPIO[1]	SPI1_MISO		
GPIO[2]	SPI1_CS		I2C1_SDA
GPIO[3]	SPI1_CLK		I2C1_SCL
GPIO[4]	SPI2_MOSI	UART2_Tx	
GPIO[5]	SPI2_MISO	UART2_Rx	
GPIO[6]	SPI2_CS	UART2_CTS	I2C2_SDA
GPIO[7]	SPI2_CLK	UART2_RTS	I2C2_SCL
GPIO[8]	SPI3_MOSI		
GPIO[9]	SPI3_MISO		
GPIO[10]	SPI3_CS		I2C3_SDA
GPIO[11]	SPI3_CLK		I2C3_SCL
GPIO[12]	SPI4_MOSI	UART4_Tx	
GPIO[13]	SPI4_MISO	UART4_Rx	
GPIO[14]	SPI4_CS	UART4_CTS	I2C4_SDA
GPIO[15]	SPI4_CLK	UART4_RTS	I2C4_SCL
GPIO[16]	SPI5_MOSI	UART5_Tx	
GPIO[17]	SPI5_MISO	UART5_Rx	
GPIO[18]	SPI5_CS	UART5_CTS	I2C5_SDA
GPIO[19]	SPI5_CLK	UART5_RTS	I2C5_SCL
GPIO[20]	SPI6_MOSI	UART6_Tx	
GPIO[21]	SPI6_MISO	UART6_Rx	
GPIO[22]	SPI6_CS	UART6_CTS	I2C6_SDA
GPIO[23]	SPI6_CLK	UART6_RTS	I2C6_SCL
GPIO[137]	SPI7_MOSI		

Table 2-6 BLSP alternate function configurations (cont.)

Pad name	Alternate functions		
GPIO[138]	SPI7_MISO		
GPIO[136]	SPI7_CS		I2C7_SDA
GPIO[135]	SPI7_CLK		I2C7_SCL
GPIO[96]	SPI8_MOSI		
GPIO[97]	SPI8_MISO		
GPIO[98]	SPI8_CS		I2C8_SDA
GPIO[99]	SPI8_CLK		I2C8_SCL

Table 2-7 BLSP internal pin mapping

Options	Configuration	BLSP bit 3	BLSP bit 2	BLSP bit 1	BLSP bit 0
GPIO pins BLSP 1		GPIO[0]	GPIO[1]	GPIO[2]	GPIO[3]
GPIO pins BLSP 2		GPIO[4]	GPIO[5]	GPIO[6]	GPIO[7]
GPIO pins BLSP 3		GPIO[8]	GPIO[9]	GPIO[10]	GPIO[11]
GPIO pins BLSP 4		GPIO[12]	GPIO[13]	GPIO[14]	GPIO[15]
GPIO pins BLSP 5		GPIO[16]	GPIO[17]	GPIO[18]	GPIO[19]
GPIO pins BLSP 6		GPIO[20]	GPIO[21]	GPIO[22]	GPIO[23]
GPIO pins BLSP 7		GPIO_137	GPIO_138	GPIO_136	GPIO_135
GPIO pins BLSP 8		GPIO_96	GPIO_97	GPIO_98	GPIO_99
1	4-Pin UART	UART_Tx DO 4-pin UART Transmit data	UART_Rx DI 4-pin UART Receive data	UART_CTS DI 4-pin UART Clear-to-send	UART_RTS DO 4-pin UART Ready-for-receive
2	2-Pin UART+I2C	UART_Tx DO 2-pin UART Transmit data	UART_Rx DI 2-pin UART Receive data	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
3	4-Pin SPI	SPI_MOSI B SPI master out Slave in	SPI_MISO B SPI master in Slave out	SPI_CS B SPI chip select	SPI_CLK B SPI clock
4	2-Pin UART+GPIO	UART_Tx DO 2-pin UART Transmit data	UART_Rx DI 2-pin UART Receive data	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O
5	I2C+GPIO	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O	I2C_SDA B I2C serial data	I2C_SCL B I2C serial clock
6	GPIO	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O	GPIO_xx B Configurable I/O

As noted throughout the pin definition tables, GPIO assignments must be done carefully to avoid conflicts, and to ensure that the desired functionality is achieved. For GPIOs that can be used as BLSPs, additional factors should be considered when making functional assignments:

1. Extra chip selects are available when certain BLSPs are used for SPI:
   - BLSP 1, BLSP 3, BLSP 6, and BLSP 7 have an extra CS for SPI.
2. SPI is only supported via BLSP, and each BLSPs supports a different SPI.
3. I^2C is supported by each BLSP. All BLSPs use bits [1:0] for I^2C.
4. Additional I^2C ports (besides the BLSP versions) are available:
   - Camera
   - Audio codec (connected internally)

Table 2-8 Pin descriptions: internal functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
JTAG					
M4	SRST_N		P3	DI	JTAG reset for debug
L1	TCK		P3	DI	JTAG clock input
L3	TDI		P3	DI	JTAG data input
L5	TDO		P3	DO-Z	JTAG data output
M2	TMS		P3	B	JTAG mode-select input
K2	TRST_N		P3	DI	JTAG reset
General-purpose clocks, PDM, and related signals					
P2	GP_CLK0_A	GPIO_33	P3	DO B-PD:nppukp	General-purpose clock output 0 A Configurable I/O
N3	GP_CLK0_B	GPIO_36	P3	DO B-PD:nppukp	General-purpose clock output 0 B Configurable I/O
R7	GP_CLK1_A	GPIO_34	P3	DO B-PD:nppukp	General-purpose clock output 1 A Configurable I/O
T6	GP_CLK1_B	GPIO_41	P3	DO B-PD:nppukp	General-purpose clock output 1 B Configurable I/O
N7	GP_MN	GPIO_39	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
G47	GP_PDM_0A	GPIO_66	P3	DO B-PD:nppukp	General-purpose PDM output 0 A Configurable I/O
AN47	GP_PDM_0B	GPIO_48	P3	DO B-PD:nppukp	General-purpose PDM output 0 B Configurable I/O
AJ45	GP_PDM_1A	GPIO_45	P3	DO B-PD:nppukp	General-purpose PDM output 1 A Configurable I/O
B46	GP_PDM_1B	GPIO_89	P3	DO B-PD:nppukp	General-purpose PDM output 1 B Configurable I/O
AY40	GP_PDM_2A	GPIO_60	P3	DO B-PD:nppukp	General-purpose PDM output 2 A Configurable I/O

Table 2-8 Pin descriptions: internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
M6	GP_PDM_2B	GPIO_38	P3	DO B-PD:nppukp	General-purpose PDM output 2 B Configurable I/O
Reset and mode control					
L9	MODE_0		P3	DIS-PD	Mode control bit 0
J9	MODE_1		P3	DIS-PD	Mode control bit 1
BA41	RESOUT_N		P3	DO	Reset output
Wake-up pins for MSM power management					
BE9	GPIO_1		P3	B-PD:nppukp	General-purpose wake interrupt
AW45	GPIO_12		P3	B-PD:nppukp	General-purpose wake interrupt
BE5	GPIO_129		P3	B-PD:nppukp	General-purpose wake interrupt
AY46	GPIO_13		P3	B-PD:nppukp	General-purpose wake interrupt
BC7	GPIO_130		P3	B-PD:nppukp	General-purpose wake interrupt
T2	GPIO_131		P3	B-PD:nppukp	General-purpose wake interrupt
R3	GPIO_132		P3	B-PD:nppukp	General-purpose wake interrupt
P6	GPIO_133		P3	B-PD:nppukp	General-purpose wake interrupt
BB46	GPIO_137		P3	B-PD:nppukp	General-purpose wake interrupt
AW41	GPIO_138		P3	B-PD:nppukp	General-purpose wake interrupt
AV40	GPIO_139		P3	B-PD:nppukp	General-purpose wake interrupt
BE47	GPIO_140		P3	B-PD:nppukp	General-purpose wake interrupt
BC45	GPIO_141		P3	B-PD:nppukp	General-purpose wake interrupt
BF6	GPIO_17		P3	B-PD:nppukp	General-purpose wake interrupt
L45	GPIO_21		P3	B-PD:nppukp	General-purpose wake interrupt
AG41	GPIO_25		P3	B-PD:nppukp	General-purpose wake interrupt
BC5	GPIO_28		P3	B-PD:nppukp	General-purpose wake interrupt
BF4	GPIO_31		P3	B-PD:nppukp	General-purpose wake interrupt
R7	GPIO_34		P3	B-PD:nppukp	General-purpose wake interrupt
N1	GPIO_35		P3	B-PD:nppukp	General-purpose wake interrupt
N3	GPIO_36		P3	B-PD:nppukp	General-purpose wake interrupt
H46	GPIO_37		P3	B-PD:nppukp	General-purpose wake interrupt
M6	GPIO_38		P3	B-PD:nppukp	General-purpose wake interrupt
AH42	GPIO_42		P3	B-PD:nppukp	General-purpose wake interrupt
AH44	GPIO_43		P3	B-PD:nppukp	General-purpose wake interrupt
AJ47	GPIO_44		P3	B-PD:nppukp	General-purpose wake interrupt
AJ45	GPIO_45		P3	B-PD:nppukp	General-purpose wake interrupt
AK46	GPIO_46		P3	B-PD:nppukp	General-purpose wake interrupt
AN47	GPIO_48		P3	B-PD:nppukp	General-purpose wake interrupt
BB44	GPIO_5		P3	B-PD:nppukp	General-purpose wake interrupt
AU47	GPIO_54		P3	B-PD:nppukp	UIM1 presence detection

Table 2-8 Pin descriptions: internal functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
AT44	GPIO_58		P3	B-PD:nppukp	UIM2 presence detection
BD44	GPIO_59		P3	B-PD:nppukp	General-purpose wake interrupt
AY40	GPIO_60		P3	B-PD:nppukp	General-purpose wake interrupt
BF46	GPIO_61		P3	B-PD:nppukp	General-purpose wake interrupt
BD6	GPIO_62		P3	B-PD:nppukp	General-purpose wake interrupt
BC25	GPIO_63		P3	B-PD:nppukp	General-purpose wake interrupt
AL45	GPIO_65		P3	B-PD:nppukp	General-purpose wake interrupt
AH46	GPIO_67		P3	B-PD:nppukp	General-purpose wake interrupt
AE45	GPIO_70		P3	B-PD:nppukp	General-purpose wake interrupt
AE43	GPIO_71		P3	B-PD:nppukp	General-purpose wake interrupt
AE47	GPIO_72		P3	B-PD:nppukp	General-purpose wake interrupt
AF46	GPIO_73		P3	B-PD:nppukp	General-purpose wake interrupt
AG47	GPIO_74		P3	B-PD:nppukp	General-purpose wake interrupt
BG13	GPIO_81		P3	B-PD:nppukp	General-purpose wake interrupt
J45	GPIO_85		P3	B-PD:nppukp	General-purpose wake interrupt
K44	GPIO_86		P3	B-PD:nppukp	General-purpose wake interrupt
J47	GPIO_87		P3	B-PD:nppukp	General-purpose wake interrupt
AT42	GPIO_9		P3	B-PD:nppukp	General-purpose wake interrupt
C45	GPIO_90		P3	B-PD:nppukp	General-purpose wake interrupt
J41	GPIO_91		P3	B-PD:nppukp	General-purpose wake interrupt
D46	GPIO_93		P3	B-PD:nppukp	General-purpose wake interrupt
G45	GPIO_97		P3	B-PD:nppukp	General-purpose wake interrupt
F2	SDC1_DATA_1		P7	BH-PD:nppukp	Secure digital controller 1 data bit 1
G5	SDC1_DATA_3		P7	BH-PD:nppukp	Secure digital controller 1 data bit 3
J3	SDC2_DATA_1		P2	BH-PD:nppukp	Secure digital controller 2 data bit 1
H2	SDC2_DATA_3		P2	BH-PD:nppukp	SD card detect wake-up interrupt
M4	SRST_N		P3	DI	JTAG reset for debug

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

Table 2-9 Pin descriptions: chipset interface functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
WTR-Rx baseband interface					
BE33	BBRX_I_I_CH0			AI	Baseband receiver input, channel 0, in-phase
BG33	BBRX_I_I_CH1			AI	Baseband receiver input, channel 1, in-phase
BE29	BBRX_I_I_CH2			AI	Baseband receiver input, channel 2, in-phase
BE27	BBRX_I_I_CH3			AI	Baseband receiver input, channel 3, in-phase
BE31	BBRX_I_Q_CH0			AI	Baseband receiver input, channel 0, quadrature
BG31	BBRX_I_Q_CH1			AI	Baseband receiver input, channel 1, quadrature
BG29	BBRX_I_Q_CH2			AI	Baseband receiver input, channel 2, quadrature
BG27	BBRX_I_Q_CH3			AI	Baseband receiver input, channel 3, quadrature
WTR-Tx baseband interface					
BE41	TXDAC0_IM			AO	Transmitter DAC 0 output, in-phase minus
BF40	TXDAC0_IP			AO	Transmitter DAC 0 output, in-phase plus
BF42	TXDAC0_QM			AO	Transmitter DAC 0 output, quadrature minus
BG43	TXDAC0_QP			AO	Transmitter DAC 0 output, quadrature plus
AW33	TXDAC0_VREF			AI	Transmitter DAC 0 voltage reference
BF36	TXDAC1_IM			AO	Transmitter DAC 1 output, in-phase minus
BG35	TXDAC1_IP			AO	Transmitter DAC 1 output, in-phase plus
BE37	TXDAC1_QM			AO	Transmitter DAC 1 output, quadrature minus
BF38	TXDAC1_QP			AO	Transmitter DAC 1 output, quadrature plus
BA33	TXDAC1_VREF			AI	Transmitter DAC 1 voltage reference
GNSS					
BC39	GNSS_BB_IP			AI	GNSS receiver baseband input, in-phase plus
BC41	GNSS_BB_QP			AI	GNSS receiver baseband input, quadrature plus
GSM					
BB22	GSM_TX_PHASE_TXDAC1	GPIO_115	P3	DO B-PD:nppukp	GSM transmit phase adjust data bit associated with TXDAC1 Configurable I/O
BD22	GSM_TX_PHASE_TXDAC0	GPIO_117	P3	DO B-PD:nppukp	GSM transmit phase adjust data bit associated with TXDAC0 Configurable I/O
PMIC					
N47	PMIC_SPMI_CLK		P3	DO	Slave and PBUS interface for PMICs – Clock
N45	PMIC_SPMI_DATA		P3	B	Slave and PBUS interface for PMICs – Data
R45	PS_HOLD		P3	DO	Power supply hold signal to PMIC
T46	RESIN_N		P3	DI	Reset input
P46	SLEEP_CLK		P3	DI	Sleep clock
R43	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz)
T44	CXO_EN		P3	DO	Core crystal oscillator enable

Table 2-9 Pin descriptions: chipset interface functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
WLAN signals					
AU15	WLAN_BB_I_M			AI, AO	WLAN baseband Rx/Tx switched, in-phase minus
AT16	WLAN_BB_I_P			AI, AO	WLAN baseband Rx/Tx switched, in-phase plus
AT14	WLAN_BB_Q_M			AI, AO	WLAN baseband Rx/Tx switched, quadrature minus
AU13	WLAN_BB_Q_P			AI, AO	WLAN baseband Rx/Tx switched, quadrature plus
AW15	WLAN_RSET			AI	WLAN external resistor
BD10	WCSS_XO			DI	WLAN reference clock
BA13	WLAN_DATA[2]	GPIO_76	P3	B-PD:nppukp	WLAN data bit 2 Configurable I/Os
BE11	WLAN_DATA[1]	GPIO_77	P3	B-PD:nppukp	WLAN data bit 1 Configurable I/Os
BB12	WLAN_DATA[0]	GPIO_78	P3	B-PD:nppukp	WLAN data bit 0 Configurable I/Os
BB14	WLAN_SET	GPIO_79	P3	B-PD:nppukp	WLAN set Configurable I/Os
BC11	WLAN_CLK	GPIO_80	P3	B-PD:nppukp	WLAN clock Configurable I/Os
Bluetooth signals					
BD14	BT_CTRL	GPIO_83	P3	B-PD:nppukp	Bluetooth control Configurable I/Os
BF10	BT_DAT_STB	GPIO_84	P3	B-PD:nppukp	Bluetooth dual-function: data and strobe Configurable I/Os
BG9	BT_SSBI	GPIO_75	P3	B-PD:nppukp	Bluetooth single-wire serial bus interface Configurable I/Os
FM signals					
BG13	FM_SSBI	GPIO_81	P3	B-PD:nppukp	FM radio serial data interface Configurable I/O **Note**: If FM is not used, leave GPIO_81 as no connect (floating).
BE13	FM_SDI	GPIO_82	P3	B-PD:nppukp	FM radio single-wire serial bus interface Configurable I/O **Note**: If FM is not used, leave GPIO_82 as no connect (floating).

1. See Table 2-1 for parameter and acronym definitions.

Table 2-10 Pin descriptions: RF front-end functions

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
General RF control signal					
BE17	GRFC(0)	GPIO_100	P3	DO B-PD:nppukp	Generic RF controller bit 0 Configurable I/Os
BG17	GRFC(1)	GPIO_101	P3	DO B-PD:nppukp	Generic RF controller bit 1 Configurable I/O

Table 2-10 Pin descriptions: RF front-end functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BF16	GRFC(2)	GPIO_102	P3	DO B-PD:nppukp	Generic RF controller bit 2 Configurable I/O
BA17	GRFC(3)	GPIO_103	P3	DO B-PD:nppukp	Generic RF controller bit 3 Configurable I/O
BC15	GRFC(4)	GPIO_104	P3	DO B-PD:nppukp	Generic RF controller bit 4 Configurable I/O
BE15	GRFC(5)	GPIO_105	P3	DO B-PD:nppukp	Generic RF controller bit 5 Configurable I/O
BF14	GRFC(6)	GPIO_106	P3	DO B-PD:nppukp	Generic RF controller bit 6 Configurable I/O
BA15	GRFC(7)	GPIO_107	P3	DO B-PD:nppukp	Generic RF controller bit 7 Configurable I/O
BE25	GRFC(8)	GPIO_108	P3	DO B-PD:nppukp	Generic RF controller bit 8 Configurable I/O
BG25	GRFC(9)	GPIO_109	P3	DO B-PD:nppukp	Generic RF controller bit 9 Configurable I/O
BB24	GRFC(10)	GPIO_110	P3	DO B-PD:nppukp	Generic RF controller bit 10 Configurable I/O
BF24	GRFC(11)	GPIO_111	P3	DO B-PD:nppukp	Generic RF controller bit 11 Configurable I/O
BC23	GRFC(12)	GPIO_112	P3	DO B-PD:nppukp	Generic RF controller bit 12 Configurable I/O
BG45	GRFC(13)	GPIO_113	P3	DO B-PD:nppukp	Generic RF controller bit 13 Configurable I/O
BE23	GRFC(14)	GPIO_114	P3	DO B-PD:nppukp	Generic RF controller bit 14 Configurable I/O
BB22	GRFC(15) / gsm1_tx_ phase_d	GPIO_115	P3	DO B-PD:nppukp	Generic RF controller bit 15 Configurable I/O
BA21	GRFC(28) / ext_gps_lna_ en0	GPIO_116	P3	DO B-PD:nppukp	Generic RF controller bit 28 Configurable I/O
BD22	GRFC(27) / gsm0_tx_ phase_d	GPIO_117	P3	DO B-PD:nppukp	Generic RF controller bit 27 Configurable I/O
Qualcomm RF360 Interface					
BF22	RFFE1_CLK	GPIO_118	P3	DO B-PD:nppukp	MIPI_RFFE 1 clock Configurable I/O
BE21	RFFE1_DATA	GPIO_119	P3	B B-PD:nppukp	MIPI_RFFE 1 data Configurable I/O
BG21	RFFE2_CLK	GPIO_120	P3	DO B-PD:nppukp	MIPI_RFFE 2 clock Configurable I/Os
BF20	RFFE2_DATA	GPIO_121	P3	B B-PD:nppukp	MIPI_RFFE 2 data Configurable I/O
BE19	RFFE3_CLK	GPIO_126	P3	DO B-PD:nppukp	MIPI_RFFE 3 clock Configurable I/O

Table 2-10 Pin descriptions: RF front-end functions (cont.)

Pad #	Pad name and/or function	Pad name or alt function	Pad characteristics [1]		Functional description
			Voltage	Type	
BF18	RFFE3_DATA	GPIO_127	P3	B B-PD:nppukp	MIPI_RFFE 3 data Configurable I/O
BB20	RFFE4_CLK	GPIO_122	P3	DO B-PD:nppukp	MIPI_RFFE 4 clock Configurable I/O
BC19	RFFE4_DATA	GPIO_123	P3	B B-PD:nppukp	MIPI_RFFE 4 data Configurable I/O
BA19	RFFE5_CLK	GPIO_124	P3	DO B-PD:nppukp	MIPI_RFFE 5 clock Configurable I/O
AY18	RFFE5_DATA	GPIO_125	P3	B B-PD:nppukp	MIPI_RFFE 5 data Configurable I/O

1. See Table 2-1 for parameter and acronym definitions.

NOTE: GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the preceding table), designers must identify all their application's requirements and map each GPIO to its function—carefully avoiding conflicts in GPIO assignments. See Table 2-11 for a list of all supported functions for each GPIO.

NOTE: Handset designers must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

To help designers define their products' GPIO assignments, Qualcomm Technologies, Inc. (QTI) provides an Excel spreadsheet that lists all MSM8953 GPIOs (in numeric order), pad numbers, pad voltages, pull states, and available configurations.

NOTE: Click the following link to download the *MSM8953 GPIO Configuration Spreadsheet* (80-P2472-1B80-P5462-1B) from the Qualcomm CreatePoint website.

NOTE: https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/80-P5462-1B

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For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

Table 2-11 Pin descriptions: general-purpose input/output ports

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BB10	GPIO_0		P3	B-PD:nppukp	Configurable I/O
		SPI1_MOSI		B	BLSP 1 bit 3; SPI
BE9	GPIO_1		P3	B-PD:nppukp	Configurable I/O
		SPI1_MISO		B	BLSP 1 bit 2; SPI
		SMB_INT		DO	SMB charger interrupt
BF12	GPIO_2		P3	B-PD:nppukp	Configurable I/O
		SPI1_CS		B	BLSP 1 bit 1; SPI
		I2C1_SDA		B	BLSP 1 bit 1; I^2C
BF8	GPIO_3		P3	B-PD:nppukp	Configurable I/O
		SPI1_CLK		B	BLSP 1 bit 0; SPI
		I2C1_SCL		B	BLSP 1 bit 0; I^2C
BA43	GPIO_4		P3	B-PD:nppukp	Configurable I/O
		SPI2_MOSI		B	BLSP 2 bit 3; SPI
		UART2_TX		B	BLSP 2 bit 3; UART
BB44	GPIO_5		P3	B-PD:nppukp	Configurable I/O
		SPI2_MISO		B	BLSP 2 bit 2; SPI
		UART2_RX		B	BLSP 2 bit 2; UART
		LDO_EN		DO	External LDO Enable
BD46	GPIO_6		P3	B-PD:nppukp	Configurable I/O
		SPI2_CS		B	BLSP 2 bit 1; SPI
		UART2_CTS		B	BLSP 2 bit 1; UART
		I2C2_SDA		B	BLSP 2 bit 1; I^2C
BE45	GPIO_7		P3	B-PD:nppukp	Configurable I/O
		SPI2_CLK		B	BLSP 2 bit 0; SPI
		UART2_RTS		B	BLSP 2 bit 0; UART
		I2C2_SCL		B	BLSP 2 bit 0; I^2C
AU45	GPIO_8		P3	B-PD:nppukp	Configurable I/O
		SPI3_MOSI		B	BLSP 3 bit 3; SPI
AT42	GPIO_9		P3	B-PD:nppukp	Configurable I/O
		SPI3_MISO		B	BLSP 3 bit 2; SPI
AV46	GPIO_10		P3	B-PD:nppukp	Configurable I/O
		SPI3_CS		B	BLSP 3 bit 1; SPI
		I2C3_SDA		B	BLSP 3 bit 1; I^2C
AU43	GPIO_11		P3	B-PD:nppukp	Configurable I/O
		SPI3_CLK		B	BLSP 3 bit 0; SPI
		I2C3_SCL		B	BLSP 3 bit 0; I^2C

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AW45	GPIO_12		P3	B-PD:nppukp	Configurable I/O
		SPI4_MOSI		B	BLSP 4 bit 3; SPI
		UART4_TX		B	BLSP 4 bit 3; UART
AY46	GPIO_13		P3	B-PD:nppukp	Configurable I/O
		SPI4_MISO		B	BLSP 4 bit 2; SPI
		UART4_RX		B	BLSP 4 bit 2; UART
BA47	GPIO_14		P3	B-PD:nppukp	Configurable I/O
		UART4_CTS		B	BLSP 4 bit 1; UART
		I2C4_SDA		B	BLSP 4 bit 1; I^2C
		SPI4_CS		B	BLSP 4 bit 1 SPI
AU41	GPIO_15		P3	B-PD:nppukp	Configurable I/O
		UART4_RTS		B	BLSP 4 bit 0; UART
		I2C4_SCL		B	BLSP 4 bit 0; I^2C
		SPI4_CLK		B	BLSP 4 bit 0; SPI
BB8	GPIO_16		P3	B-PD:nppukp	Configurable I/O
		UART5_TX		B	BLSP 5 bit 3; UART
		SPI5_MOSI		B	BLSP 5 bit 3; SPI
BF6	GPIO_17		P3	B-PD:nppukp	Configurable I/O
		UART5_RX		B	BLSP 5 bit 2; UART
		SPI5_MISO		B	BLSP 5 bit 2; SPI
BE7	GPIO_18		P3	B-PD:nppukp	Configurable I/O
		UART5_CTS		B	BLSP 5 bit 1; UART
		I2C5_SDA		B	BLSP 5 bit 1; I^2C
		SPI5_CS		B	BLSP 5 bit 1; SPI
BA9	GPIO_19		P3	B-PD:nppukp	Configurable I/O
		UART5_RTS		B	BLSP 5 bit 0; UART
		I2C5_SCL		B	BLSP 5 bit 0; I^2C
		SPI5_CLK		B	BLSP 5 bit 0; SPI
M44	GPIO_20		P3	B-PD:nppukp	Configurable I/O
		UART6_TX		B	BLSP 6 bit 3; UART
		SPI6_MOSI		B	BLSP 6 bit 3; SPI
L45	GPIO_21		P3	B-PD:nppukp	Configurable I/O
		UART6_RX		B	BLSP 6 bit 2; UART
		SPI6_MISO		B	BLSP 6 bit 2; SPI
M46	GPIO_22		P3	B-PD:nppukp	Configurable I/O
		UART6_CTS		B	BLSP 6 bit 1; UART
		I2C6_SDA		B	BLSP 6 bit 1; I^2C
		SPI6_CS		B	BLSP 6 bit 1; SPI

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
K46	GPIO_23		P3	B-PD:nppukp	Configurable I/O
		UART6_RTS		B	BLSP 6 bit 0; UART
		I2C6_SCL		B	BLSP 6 bit 0; I2C
		SPI6_CLK		B	BLSP 6 bit 0; SPI
BD2	GPIO_24		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_P		DI	SDE vertical sync–primary
AG41	GPIO_25		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_S		DI	SDE vertical sync–secondary
		PRI_MI2S_MCLK_A		DO	Primary MI2S master clock A
		SEC_MI2S_MCLK_A		DO	Secondary MI2S master clock A
BD4	GPIO_26		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK0		DO	Camera master clock 0–rear camera
BE1	GPIO_27		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK1		DO	Camera master clock 1–front camera
BC5	GPIO_28		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK2		DO	Camera master clock 2–depth
BG3	GPIO_29		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SDA0		B	Dedicated camera control interface I2C 0 Serial data
BF2	GPIO_30		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SCL0		B	Dedicated camera control interface I2C 0 clock
BF4	GPIO_31		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SDA1		B	Dedicated camera control interface I2C 1 serial data
BE3	GPIO_32		P3	B-PD:nppukp	Configurable I/O
		CCI_I2C_SCL1		B	Dedicated camera control interface I2C 1 clock
P2	GPIO_33		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER0		DO	Camera control interface timer 0
		GP_CLK0_A		DO	General-purpose clock output 0 A
R7	GPIO_34		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER1		DO	Camera control interface timer 1
		GP_CLK1_A		DO	General-purpose clock output 1 A
N1	GPIO_35		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER2		DO	Camera control interface timer 2
		BOOT_CONFIG[12]		DI	fast_boot_select bit 12 (configure external boot device)
		SPI1_CS1		DO-Z	Chip select 1 for SPI on BLSP1

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
N3	GPIO_36		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER3		DO	Camera control interface timer 3
		SPI1_CS2		DO-Z	Chip select 2 for SPI on BLSP1
		GP_CLK0_B		DO	General-purpose clock output 0 B
H46	GPIO_37		P3	B-PD:nppukp	Configurable I/O
		FORCED_USB_BOOT		DI	Forced USB boot
M6	GPIO_38		P3	B-PD:nppukp	Configurable I/O
		CCI_ASYNC_IN0		DI	Camera control interface async 0
		GP_PDM_2B		DO	General-purpose PDM output 2 B
N7	GPIO_39		P3	B-PD:nppukp	Configurable I/O
		CAM1_STANDBY_N		DO	Rear camera standby
		GP_MN		DO	General-purpose M/N:D counter output
R1	GPIO_40		P3	B-PD:nppukp	Configurable I/O
		CAM1_RST_N		DO	Rear camera reset
T6	GPIO_41		P3	B-PD:nppukp	Configurable I/O
		CCI_TIMER4		DO	Camera control interface timer 4
		SPI3_CS1		DO-Z	Chip select 1 for SPI on BLSP3
		GP_CLK1_B		DO	General-purpose clock output 1 B
		BOOT_CONFIG[9]		DI	fast_boot_select bit 9 (configure external boot device)
AH42	GPIO_42		P3	B-PD:nppukp	Configurable I/O
		ACCEL_INT		DI	Accelerometer sensor interrupt
AH44	GPIO_43		P3	B-PD:nppukp	Configurable I/O
		ALSP_INT_N		DI	Ambient light sensor interrupt
AJ47	GPIO_44		P3	B-PD:nppukp	Configurable I/O
		MAG_INT		DI	Magnetic sensor interrupt
AJ45	GPIO_45		P3	B-PD:nppukp	Configurable I/O
		GYRO_INT		DI	Gyro sensor interrupt
		GP_PDM_1A		DO	General-purpose PDM output 1 A
AK46	GPIO_46		P3	B-PD:nppukp	Configurable I/O
		PRESSURE_INT		DI	Pressure sensor interrupt
AJ43	GPIO_47		P3	B-PD:nppukp	Configurable I/O
		SPI6_CS2		DO-Z	Chip select 2 for SPI on BLSP6
AN47	GPIO_48		P3	B-PD:nppukp	Configurable I/O
		SPI6_CS1		DO-Z	Chip select 1 for SPI on BLSP6
		GP_PDM_0B		DO	General-purpose PDM output 0 B
AM46	GPIO_49		P3	B-PD:nppukp	Configurable I/O
		UIM_BATT_ALARM		DI	UIM battery alarm

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
AP46	GPIO_50		P3	B-PD:nppukp	Configurable I/O
		SPI3_CS2		DO-Z	Chip select 2 for SPI on BLSP3
		SD_WRITE_PROTECT		DI	Secure digital card write protection
AN43	GPIO_51		P5	B-PD:nppukp	Configurable I/O
		UIM1_DATA		B	Dual voltage UIM1 data
AR45	GPIO_52		P5	B-PD:nppukp	Configurable I/O
		UIM1_CLK		DO	Dual voltage UIM1 clock
AN41	GPIO_53		P5	B-PD:nppukp	Configurable I/O
		UIM1_RESET		DO	Dual voltage UIM1 reset
AU47	GPIO_54		P3	B-PD:nppukp	Configurable I/O
		UIM1_PRESENT		DI	UIM1 detect (nondual voltage)
AP42	GPIO_55		P6	B-PD:nppukp	Configurable I/O
		UIM2_DATA		B	Dual voltage UIM2 data
AT46	GPIO_56		P6	B-PD:nppukp	Configurable I/O
		UIM2_CLK		DO	Dual voltage UIM2 clock
AR41	GPIO_57		P6	B-PD:nppukp	Configurable I/O
		UIM2_RESET		DO	Dual voltage UIM2 reset
AT44	GPIO_58		P3	B-PD:nppukp	Configurable I/O
		UIM2_PRESENT		DI	UIM2 detect (nondual voltage)
BD44	GPIO_59		P3	B-PD:nppukp	Configurable I/O
AY40	GPIO_60		P3	B-PD:nppukp	Configurable I/O
		GP_PDM_2A		DO	General-purpose PDM output 2 A
BF46	GPIO_61		P3	B-PD:nppukp	Configurable I/O
BD6	GPIO_62		P3	B-PD:nppukp	Configurable I/O
BC25	GPIO_63		P3	B-PD:nppukp	Configurable I/O
AN45	GPIO_64		P3	B-PD:nppukp	Configurable I/O
AL45	GPIO_65		P3	B-PD:nppukp	Configurable I/O
G47	GPIO_66		P3	B-PD:nppukp	Configurable I/O
		PRI_MI2S_MCLK_C		DO	Primary MI^{2}S master clock C
		SEC_MI2S_MCLK_B		DO	Secondary MI^{2}S master clock B
		GP_PDM_0A		DO	General-purpose PDM output 0 A
AH46	GPIO_67		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX0_DRE		DO	PDM Rx0 DRE data channel
AF42	GPIO_68		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX1_DRE		DO	PDM Rx1 DRE data channel
AG45	GPIO_69		P3	B-PD:nppukp	Configurable I/O
		PRI_MI2S_MCLK_B		DO	Primary MI^{2}S master clock B

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
		CDC_PDM_CLK		DO	Audio codec PDM clock signal and codec master clock
AE45	GPIO_70		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_SYNC		DO	PDM synchronization signal
		SLIMBUS_CLK		DO	Low-power audio SLIMbus clock
AE43	GPIO_71		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_TX0		DI	PDM transmit data channel 0
		SLIMBUS_DATA0		DO	Low-power audio SLIMbus data 0
AE47	GPIO_72		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX0		DO	PDM receive data channel 0
		SLIMBUS_DATA1		DO	Low-power audio SLIMbus data 1
AF46	GPIO_73		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX1		DO	PDM receive data channel 1
AG47	GPIO_74		P3	B-PD:nppukp	Configurable I/O
		CDC_PDM_RX2		DO	PDM receive data channel 2
BG9	GPIO_75		P3	B-PD:nppukp	Configurable I/O
		BT_SSBI		B	Bluetooth single-wire serial bus interface
BA13	GPIO_76		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA[2]		B	WLAN data bit 2
BE11	GPIO_77		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA[1]		B	WLAN data bit 1
BB12	GPIO_78		P3	B-PD:nppukp	Configurable I/O
		WLAN_DATA[0]		B	WLAN data bit 0
BB14	GPIO_79		P3	B-PD:nppukp	Configurable I/O
		WLAN_SET		B	WLAN set
BC11	GPIO_80		P3	B-PD:nppukp	Configurable I/O
		WLAN_CLK		B	WLAN clock
BG13	GPIO_81		P3	B-PD:nppukp	Configurable I/O
		FM_SSBI		B	FM radio serial data interface **Note**: If FM is not used, leave GPIO_81 as no connect (floating).
BE13	GPIO_82		P3	B-PD:nppukp	Configurable I/O
		FM_SDI		B	FM radio single-wire serial bus interface **Note**: If FM is not used, leave GPIO_82 as no connect (floating).
BD14	GPIO_83		P3	B-PD:nppukp	Configurable I/O
		BT_CTRL		B	Bluetooth control
BF10	GPIO_84		P3	B-PD:nppukp	Configurable I/O
		BT_DATA_STB		B	Bluetooth dual-function: data and strobe

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
J45	GPIO_85		P3	B-PD:nppukp	Configurable I/O
		KEY_VOLP_N		DI	Volume key interrupt
K44	GPIO_86		P3	B-PD:nppukp	Configurable I/O
		KEY_SNAPSHOT		DI	Snapshot interrupt
J47	GPIO_87		P3	B-PD:nppukp	Configurable I/O
		KEY_FOCUS		DI	Focus interrupt
E45	GPIO_88		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_D1		B	MI^{2}S #1 serial data channel 1
		KEY_HOME		DI	Home key interrupt
B46	GPIO_89		P3	B-PD:nppukp	Configurable I/O
		DMIC0_CLK		DO	Digital MIC0 clock
		SPI7_CS1		DO-Z	Chip select 1 for SPI on BLSP7
		GP_PDM_1B		DO	General-purpose PDM output 1 B
C45	GPIO_90		P3	B-PD:nppukp	Configurable I/O
		DMIC0_DATA		DI	Digital MIC0 data
		SPI7_CS2		DO-Z	Chip select 2 for SPI on BLSP7
J41	GPIO_91		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_SCK		B	MI^{2}S #1-bit clock
H42	GPIO_92		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_WS		B	MI^{2}S #1 word select (L/R)
D46	GPIO_93		P3	B-PD:nppukp	Configurable I/O
		MI2S_1_D0		B	MI^{2}S #1 serial data channel 0
E47	GPIO_94		P3	B-PD:nppukp	Configurable I/O
		WSA_IO_DATA		DI	WSA8810 current/voltage sense data for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326)
		MI2S_1_D2		B	MI^{2}S #1 serial data channel 2
G43	GPIO_95		P3	B-PD:nppukp	Configurable I/O
		WSA_IO_CLK		DO	WSA8810 current/voltage sense clock for speaker protection in WSA8810 analog mode (PM8953 integrated codec); not required in PDM mode (WCD9326)
		MI2S_1_D3		B	MI^{2}S #1 serial data channel 3
C47	GPIO_96		P3	B-PD:nppukp	Configurable I/O
		WSA_EN		DO	WSA8810 enable
		SPI8_MOSI		B	BLSP 8 bit 0; SPI
G45	GPIO_97		P3	B-PD:nppukp	Configurable I/O
		WSA_INTR		DO	WSA8810 interrupt
		SPI8_MISO		B	BLSP 8 bit 1; SPI

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
K42	GPIO_98		P3	B-PD:nppukp	Configurable I/O
		I2C8_SDA		B	BLSP 8 bit 2; I^2C
		SPI8_CS		B	BLSP 8 bit 2; SPI
F46	GPIO_99		P3	B-PD:nppukp	Configurable I/O
		I2C8_SCL		B	BLSP 8 bit 3; I^2C
		SPI8_CLK		B	BLSP 8 bit 3; SPI
BE17	GPIO_100		P3	B-PD:nppukp	Configurable I/O
		GRFC[0]		DO	Generic RF controller bit 0
BG17	GPIO_101		P3	B-PD:nppukp	Configurable I/O
		GRFC[1]		DO	Generic RF controller bit 1
BF16	GPIO_102		P3	B-PD:nppukp	Configurable I/O
		GRFC[2]		DO	Generic RF controller bit 2
BA17	GPIO_103		P3	B-PD:nppukp	Configurable I/O
		GRFC[3]		DO	Generic RF controller bit 3
BC15	GPIO_104		P3	B-PD:nppukp	Configurable I/O
		GRFC[4]		DO	Generic RF controller bit 4
		BOOT_CONFIG[7]		DI	fast_boot_select bit 7 (configure external boot device)
BE15	GPIO_105		P3	B-PD:nppukp	Configurable I/O
		GRFC[5]		DO	Generic RF controller bit 5
		BOOT_CONFIG[4]		DI	fast_boot_select bit 4 (configure external boot device)
BF14	GPIO_106		P3	B-PD:nppukp	Configurable I/O
		GRFC[6]		DO	Generic RF controller bit 6
		BOOT_CONFIG[0]		DI	fast_boot_select bit 0 (configure external boot device)
BA15	GPIO_107		P3	B-PD:nppukp	Configurable I/O
		GRFC[7]		DO	Generic RF controller bit 7
		BOOT_CONFIG[2]		DI	fast_boot_select bit 2 (configure external boot device)
BE25	GPIO_108		P3	B-PD:nppukp	Configurable I/O
		GRFC[8]		DO	Generic RF controller bit 8
		BOOT_CONFIG[5]		DI	fast_boot_select bit 5 (configure external boot device)
BG25	GPIO_109		P3	B-PD:nppukp	Configurable I/O
		GRFC[9]		DO	Generic RF controller bit 9
		BOOT_CONFIG[3]		DI	fast_boot_select bit 3 (configure external boot device)

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BB24	GPIO_110		P3	B-PD:nppukp	Configurable I/O
		GRFC[10]		DO	Generic RF controller bit 10
		BOOT_CONFIG[8]		DI	fast_boot_select bit 8 (configure external boot device)
BF24	GPIO_111		P3	B-PD:nppukp	Configurable I/O
		GRFC[11]		DO	Generic RF controller bit 11
		BOOT_CONFIG[11]		DI	fast_boot_select bit 11 (configure external boot device)
BC23	GPIO_112		P3	B-PD:nppukp	Configurable I/O
		GRFC[12]		DO	Generic RF controller bit 12
		BOOT_CONFIG[10]		DI	fast_boot_select bit 10 (configure external boot device)
BG45	GPIO_113		P3	B-PD:nppukp	Configurable I/O
		GRFC[13]		DO	Generic RF controller bit 13
		BOOT_CONFIG[1]		DI	fast_boot_select bit 1 (configure external boot device)
BE23	GPIO_114		P3	B-PD:nppukp	Configurable I/O
		GRFC[14]		DO	Generic RF controller bit 14
		BOOT_CONFIG[6]		DI	fast_boot_select bit 6 (configure external boot device)
BB22	GPIO_115		P3	B-PD:nppukp	Configurable I/O
		GRFC[15]		DO	Generic RF controller bit 15
		GSM_TX_PHASE_TXDAC1		DO	GSM transmit phase adjust data bit associated with TXDAC1
BA21	GPIO_116		P3	B-PD:nppukp	Configurable I/O
		EXT_GPS_LNA_EN0		DO	External LNA GPS Enable
		GRFC[28]		DO	Generic RF controller bit 28
BD22	GPIO_117		P3	B-PD:nppukp	Configurable I/O
		GSM_TX_PHASE_TXDAC0		DO	GSM transmit phase adjust data bit associated with TXDAC0
		GRFC[27]		DO	Generic RF controller bit 27
BF22	GPIO_118		P3	B-PD:nppukp	Configurable I/O
		RFFE1_CLK		DO	MIPI_RFFE 1 clock
BE21	GPIO_119		P3	B-PD:nppukp	Configurable I/O
		RFFE1_DATA		B	MIPI_RFFE 1 data
BG21	GPIO_120		P3	B-PD:nppukp	Configurable I/O
		RFFE2_CLK		DO	MIPI_RFFE 2 clock
BF20	GPIO_121		P3	B-PD:nppukp	Configurable I/O
		RFFE2_DATA		B	MIPI_RFFE 2 data
BB20	GPIO_122		P3	B-PD:nppukp	Configurable I/O
		RFFE4_CLK		DO	MIPI_RFFE 4 clock

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BC19	GPIO_123		P3	B-PD:nppukp	Configurable I/O
		RFFE4_DATA		B	MIPI_RFFE 4 data
BA19	GPIO_124		P3	B-PD:nppukp	Configurable I/O
		RFFE5_CLK		DO	MIPI_RFFE 5 clock
AY18	GPIO_125		P3	B-PD:nppukp	Configurable I/O
		RFFE5_DATA		B	MIPI_RFFE 5 data
BE19	GPIO_126		P3	B-PD:nppukp	Configurable I/O
		RFFE3_CLK		DO	MIPI_RFFE 3 clock
BF18	GPIO_127		P3	B-PD:nppukp	Configurable I/O
		RFFE3_DATA		B	MIPI_RFFE 3 data
BG5	GPIO_128		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK3		DO	Camera master clock 3 – depth camera
BE5	GPIO_129		P3	B-PD:nppukp	Configurable I/O
		CAM2_RST_N		DO	Depth camera reset
BC7	GPIO_130		P3	B-PD:nppukp	Configurable I/O
		CAM2_STANDBY_N		DO	Depth camera standby
		BOOT_CONFIG[14]		DI	fast_boot_select bit 14 (configure external boot device)
T2	GPIO_131		P3	B-PD:nppukp	Configurable I/O
		CAM3_RST_N		DO	Front camera reset
R3	GPIO_132		P3	B-PD:nppukp	Configurable I/O
		CAM3_STANDBY_N		DO	Front camera standby
		BOOT_CONFIG[13]		DI	fast_boot_select bit 13 (configure external boot device)
P6	GPIO_133		P3	B-PD:nppukp	Configurable I/O
		SD_CARD_DET_N		DI	Secure digital card detection
T4	GPIO_134		P3	B-PD:nppukp	Configurable I/O
BA45	GPIO_135		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_SCK		B	MI^{2}S #2-bit clock
		I2C7_SCL		B	BLSP 7 bit 2; I^{2}C
		SPI7_CLK		B	BLSP 7 bit 2; SPI
BC47	GPIO_136		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_WS		B	MI^{2}S #2 word select (L/R)
		I2C7_SDA		B	BLSP 7 bit 3; I^{2}C
		SPI7_CS		B	BLSP 7 bit 3; SPI

Table 2-11 Pin descriptions: general-purpose input/output ports (cont.)

Pad #	Pad name	Configurable function	Pad characteristics [1]		Functional description
			Voltage	Type	
BB46	GPIO_137		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_D0		B	MI^{2}S #2 serial data
		SPI7_MOSI		B	BLSP 7 bit 0; SPI
AW41	GPIO_138		P3	B-PD:nppukp	Configurable I/O
		MI2S_2_D1		B	MI^{2}S #2 serial data channel 1
		SPI7_MISO		B	BLSP 7 bit 1; SPI
AV40	GPIO_139		P3	B-PD:nppukp	Configurable I/O
		USB_SS_SWITCH_SEL		DO	USB Type-C switch control
BE47	GPIO_140		P3	B-PD:nppukp	Configurable I/O
BC45	GPIO_141		P3	B-PD:nppukp	Configurable I/O

1. See Table 2-1 for the parameter and acronym definitions.

Table 2-12 Pin descriptions: no connection, do not connect, and reserved pins

Pad #	Pad name	Functional description
L43, M42, AA43, AD44, AF44, AG43, AJ7, AJ39, AK42, AK44, AL9, AL43, AM42, AM44, AN7, AN9, AN39, AP44, AR37, AR39, AR43, AT18, AT20, AV42, AV44, AW9, AW11, AW37, AW39, AW43, AY42, AY44, BA11, BA29, BA31, BA37, BA39, BB4, BB16, BB18, BC3, BC9, BC13, BC17, BC21, BD8, BD12, BD16, BD18, BD20, C27, H4, H44, J5, J11, J13, J15, J35, J37, J39, J43, L7, L15, L35, L41, N5, N39, P4, R5, R39, Y26, R41, N41, W43	DNC	Do not connect; connected internally, do not connect externally

Table 2-13 Pin descriptions: power-supply pins

Pad #	Pad name	Functional description
AD28, AD30, AD32, AD34, AD36, AD38, AE29, AE31, AE33, AE35, AE37, AE39, W29, W31, W33, W35, W37, W39, Y28, Y30, Y32, Y34, Y36, Y38	VDD_APC	Power for applications microprocessors
AA13, AA15, AA21, AA23, AB28, AC27, AE13, AE15, AE21, AE23, AH36, AJ13, AJ15, AJ37, AL13, AR33, AR35, R37, U13, U15, U17, U19, U25, U27	VDDCX_1	Power for digital core circuits
AA17, AA19, AA27, AC33, AE17, AE19, AE25, AE27, AG27, AH32, AH34, AJ33, AJ35, AN11, AN13, AN29, AN31, AP22, AP32, AR23, AR25, R15, R17, R35, T32, T34, T36, U21, U23, W27, AR27, AR29	VDD_MEM (MX)	Power for on-chip memory
AC11, AA11, W11, AJ11, AE11	VDD_DSI_CSI	Power for MIPI CSI DSI circuits
AF8, AE9	VDD_DSI_HV_PLL	Power pad for MIPI_DSI 1.2 V circuits
AG9, AF10	VDD_DSI_LV_PLL	Power pad for MIPI_DSI 0.9 V circuits
R23, R27, R29, R25, R31, R33, R19, R21	VDD_EBI	Power for EBI
L25	VDD_EBI_HV_PLL	Power pad for EBI 1.2 V circuits
N25	VDD_EBI_LV_PLL	Power pad for EBI 0.9 V circuits
AU31, AU29, AU23, AU25, AU27	VDD_A2	Power for analog circuits – high voltage
BA23, BA25, BA27	VDD_A1	Power for analog circuits – low voltage

Table 2-13 Pin descriptions: power-supply pins (cont.)

Pad #	Pad name	Functional description
N9	VREF_PADS	Power for Vbias pads – UIM and SDC1 Vbias pads
AM40	VREF_PADS	Power for Vbias pads – UIM and SDC1 Vbias pads
G27	VREF_EBI_CA	LPDDR3 CA reference voltage
AJ17, AJ19, AJ21, AJ23, AJ25, AJ27, AJ29, AJ31, AK18, AM18, AM32, AN25, AN27, AN33, AN35, AN37	VDD_MODEM	Power for modem circuits
BA35	VDD_GNSS	Power for GNSS circuits
J17, J19, J21, J23, J27, J29, J31, J33, L17, L19, L21, L23, L27, L29, L31, L33, J25	VDDPX_1	Power for pad group 1 – EBI pads
L11	VDDPX_2	Power for pad group 2 – SDC2 pads
AJ41, AR9, AU9, AU39, AW19, AW21, L39, R9, U9, U41	VDDPX_3	Power for pad group 2 – most I/O pads
AL41	VDDPX_5	Power for pad group 5 – UIM1 pads
AK40	VDDPX_6	Power for pad group 6 – UIM2 pads
L13	VDDPX_7	Power for pad group 7 – eMMC I/O pads
AC31	VDD_PLL1	Power for PLL circuits – low voltage
AN17, W25, AA25, AR31	VDD_PLL2	Power for PLL circuits – high voltage
L37	VDD_QFPROM_PRG	Power for programming the QFPROM; otherwise GND
R13	VDD_CDC_SDC1	Power for secure digital calibration delay circuits
AC39	VDD_USB_SS_1P8	Power for USB PHY interface – low voltage
AD40	VDD_USB_HS1_1P8	Power for USB PHY interface – low voltage
AD42	VDD_USB_HS1_3P1	Power for USB PHY interface – high voltage
AC35, AC37, AA41, AB38, AB40	VDD_USB_CORE	Power for USB core 0.925 V
AU11	VDD_WLAN	Power for WLAN ADC circuits

Table 2-14 Pin descriptions: ground pins

Pad #	Pad name	Functional description
AW35, BB38, V24, AC25, AP16, AM16, AB32, AB30, AL29, AW23, AW27, BB40, BC27, BC29, BC31, BD26, BD28, BD30, BD32, BF26, BF28, BF30, BF32, AW25, V26, AB24, AM30, AW31, BD40, BD42, BE39, BE43, BF44, AW29, BC33, BC35, BC37, BD34, BD36, BD38, BE35, BF34, AY30, BG39, AR13, AW13, AR15, A1, A5, A13, A35, A45, A47, AA1, AA9, AA29, AA31, AA33, AA35, AA37, AA39, AA45, AB2, AB6, AB42, AB46, AC9, AC13, AC15, AC17, AC19, AC21, AC23, AC29, AC41, AC43, AD8, AD10, AD46, AE1, AE7, AE41, AF2, AF28, AF30, AF32, AF36, AF38, AF40, AG5, AG7, AG11, AG13, AG15, AG17, AG19, AG21, AG23, AG25, AG29, AG31, AG33, AG35, AG37, AG39, AJ1, AJ9, AK2, AL7, AL11, AL15, AL17, AL25, AL27, AL31, AL33, AL35, AL37, AL39, AL47, AM6, AN1, AN15, AP2, AP18, AP20, AR7, AR11, AR17, AR19, AR21, AR47, AU3, AU5, AU7, AU17, AU19, AU21, AU33, AU35, AU37, AV2, AW7, AW17, AW47, B4, B6, B8, B10, B16, B20, B24, B28, B32, B36, B42, B44, BA1, BA7, BB6, BB42, BC1, BC43, BG1, BG7, BG11, BG15, BG19, BG23, BG47, C25, C39, D4, D6, D8, D10, D12, D14, D16, D18, D20, D22, D24, D26, D28, D30, D32, D34, D36, D38, D40, D42, D44, E11, E23, F4, F6, F8, F10, F12, F14, F16, F18, F20, F22, F24, F26, F28, F30, F32, F34, F36, F38, F40, F42, F44, G7, G9, G11, G13, G15, G17, G19, G21, G23, G25, G29, G31, G33, G35, G37, G39, G41, J1, L47, N11, N13, N15, N17, N19, N21, N23, N27, N29, N31, N33, N35, N37, N43, P42, P44, R11, R47, T42, U1, U5, U7, U11, U29, U31, U33, U35, U37, U39, U43, U45, V2, V28, V30, V32, V36, V38, V40, V42, V44, W9, W13, W15, W17, W19, W21, W23, W41, W45, W47, Y24, Y40	GND	Ground

3 Electrical specifications

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-2) reflect conditions that the MSM8953 device may be exposed to beyond the operating limits, without experiencing immediate functional failure. They are limiting values, to be considered individually when all other parameters are within their specified operating ranges. Functionality and long-term reliability can only be expected within the operating conditions, as described in Section 3.2 and Section 3.3.

Table 3-1 Absolute maximum ratings

Parameter		Min	Max	Unit
Power-supply voltages				
VDD_A1 VDD_DSI_CSI VDD_DSI_HV_PLL VDD_EBI_HV_PLL VDD_GNSS VDDPX_1	Power for analog circuits – low voltage for PA DAC and Tx DAC circuits Power for MIPI DSI pads Power for DSI high-voltage PLL pads Power for EBI high-voltage PLL pads Power for GNSS circuits Power for pad group 1 – EBI pads	-0.3	1.441	V
VDD_A2	Power for analog circuits - high voltage for analog baseband receiver circuits	-0.3	2.09	V
VDDPX_2	Power for pad group 2 SDC2 pads low voltage SDC2 pads high voltage	 -0.3 -0.3	 2.09 3.344	 V V
VDD_PLL2	Power for PLL circuits – high voltage	-0.3	2.09	V
VDD_USB_HS1_1P8/ VDD_USB_SS_1P8	Power for USB PHY interface – low voltage	-0.3	2.057	V
VDD_USB_CORE VDD_EBI_LV_PLL	Power for USB core circuits Power for EBI low voltage PLL pads	-0.3	1.0505	V
VDDPX_3	Power for pad group 3 – most I/O pads	-0.3	2.09	V
VDDPX_5	Power for pad group 5 UIM1 pads low voltage UIM1 pads high voltage	 -0.3 -0.3	 2.09 3.344	 V V
VDDPX_6	Power for pad group 6 UIM2 pads low voltage UIM2 pads high voltage	 -0.3 -0.3	 2.09 3.344	 V V
VDDPX_7	Power for pad group 7 – SDC1 pads	-0.3	2.09	V

Table 3-1 Absolute maximum ratings (cont.)

Parameter		Min	Max	Unit
VDD_WLAN	Power for WLAN ADC circuits	-0.3	1.463	V
VDD_DSI_LV_PLL	Power for DSI low voltage PLL pads	-0.3	1.0505	V
VDD_QFPROM_PRG	Power for programming the QFPROM	-0.3	2.079	V
VDD_USB_HS1_3P1	Power for USB PHY interface – high voltage	-0.3	3.52	V
VDD_APC	Power for VDD_APC pads	-0.3	1.267	V
VDD_CORE	Power for VDD_CORE pads	-0.3	1.1781	V
VDD_MODEM	Power for VDD_MODEM pads	-0.3	1.1781	V
VDD_MEM	Power for VDD_MEM pads	-0.3	1.1781	V
Signal pins				
V_IN	Voltage on any nonpower input pin	-0.3	V_{xx} + 20% [1]	V
VIN_P7	Voltage on any eMMC input pin	-0.30	2.45	V
I_IN	Latch-up current	-100	100	mA
ESD protection – see Section 7.1.				

1. V_{XX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include design team-controlled parameters such as power supply voltage, power distribution impedances, and thermal conditions (Table 3-2). The MSM8953 meets all performance specifications listed in Section 3.3 through Section 3.12, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter		Min	Typ[2]	Max	Unit
Power-supply voltages					
VDD_A1	Power for analog circuits – low voltage for PA DAC and Tx DAC circuits				
VDD_DSI_CSI	Power for MIPI DSI pads				
VDD_DSI_HV_PLL	Power for DSI high-voltage PLL pads	1.18	1.225	1.31	V
VDD_EBI_HV_PLL	Power for EBI high-voltage PLL pads				
VDD_GNSS	Power for GNSS circuits				
VDDPX_1	Power for pad group 1 – EBI pads				
VDD_A2	Power for analog circuits–high voltage for analog baseband receiver circuits	1.70	1.8	1.90	V
VDDPX_2	Power for pad group 2				
	SDC2 pads low voltage	1.70	1.8	1.90	V
	SDC2 pads high voltage	2.70	2.95	3.04	V
VDD_PLL2	Power for PLL circuits – high voltage	1.70	1.8	1.90	V

Table 3-2 Operating conditions (cont.)

Parameter		Min	Typ[2]	Max	Unit
VDD_USB_HS1_1P8/ VDD_USB_SS_1P8	Power for USB PHY interface – low voltage	1.72	1.8	1.87	V
VDD_USB_CORE VDD_EBI_LV_PLL	Power for USB core circuits Power for EBI low voltage PLL pads	0.910	0.925	0.955	V
VDDPX_3	Power for pad group 3 – most I/O pads	1.70	1.8	1.90	V
VDDPX_5	Power for pad group 5 UIM1 pads low voltage UIM1 pads high voltage	 1.70 2.70	 1.8 2.95	 1.90 3.04	 V V
VDDPX_6	Power for pad group 6 UIM2 pads low voltage UIM2 pads high voltage	 1.70 2.70	 1.8 2.95	 1.90 3.04	 V V
VDDPX_7	Power for pad group 7 – SDC1 pads	1.70	1.8	1.90	V
VDD_WLAN	Power for WLAN ADC circuits	1.19	1.3	1.377	V
VDD_DSI_LV_PLL	Power for DSI low voltage PLL pads	0.910	0.925	0.955	V
VDD_QFPROM_PRG	Power for programming the QFPROM	1.71	1.8	1.89	V
VDD_USB_HS1_3P1	Power for USB PHY interface – high voltage	2.94	3.075	3.20	V
Thermal conditions					
T_C	Device operating temperature (case)	-30	+25	+85	°C
	Fuse programming temperature (case)	+10	+25	+85	°C
T_A[1]	3GPP2 mode operating temperature (ambient)	-30	+25	+60	°C
	3GPP mode operating temperature (ambient)	-20	+25	+60	°C

1. These temperature ranges are defined by the 3GPP and 3GPP2 system specifications.
2. Typical voltages represent the recommended output settings of the companion PMIC device

Table 3-3 Operating conditions for voltage rails with AVS

Parameter [1]		Min	Typ	Max	Unit
VDD_APC	Quad Cortex A53 (operating at maximum frequency of 2.0/2.2 GHz)				
	Turbo_L1	0.810	–	1.152	V
	Nominal mode	0.680	–	0.932	V
	SVS [2] mode	0.575	–	0.805	V
	Low SVS	0.510	–	0.693	V

Table 3-3 Operating conditions for voltage rails with AVS (cont.)

Parameter [1]		Min	Typ	Max	Unit
VDD_CORE	Turbo mode	0.760	–	1.071	V
	Nominal mode	0.660	–	0.930	V
	SVS mode	0.560	–	0.772	V
	Low SVS	0.510	–	0.693	V
VDD_MODEM	Turbo mode	0.760	–	1.071	V
	Nominal mode	0.660	–	0.930	V
	SVS mode	0.560	–	0.772	V
	Low SVS	0.510	–	0.693	V
VDD_MEM	Turbo mode	0.790	–	1.071	V
	Nominal mode	0.790	–	0.983	V

1. Parts with voltages outside of the specified ranges are not guaranteed to operate properly.
2. AVS Type I is not enabled on the APC rail in SVS mode.

3.2.1 Core voltage minimization (retention mode)

The MPM supports VDD minimization, also known as VDD_CORE retention mode. This technique decreases the leakage of the digital logic by reducing VDD to the minimum required to maintain the register and memory state.

The V(MIN) for state retention is found through characterization. As in any normal distribution, retention voltages vary across devices. Three fuses are blown to set the core voltage in retention mode. These fuses are used by the software.

The fuse locations in Table 3-4 refer to Bits[5:3] of address 0xA4124 for VDD_CORE. The fuse locations in Table 3-5 refer to Bits [2:0] of address 0xA4124 for VDD_MEM. For more information, refer to the *MSM8953 Hardware Register Description* (80-P2472-2X).

Table 3-4 Core voltage in retention mode

VDD_CORE [1]	Bit 31 (MSB)	Bit 30	Bit 29 (LSB)
0.4	1	0	0
0.448	0	1	1
0.504	0	1	0
0.552	0	0	1
0.6	0	0	0

1. The specified VDD_CORE voltages are PMIC settings.

Table 3-5 Core voltage in retention mode

VDD_MEM [1]	Bit 31 (MSB)	Bit 30	Bit 29 (LSB)
0.488	1	0	0
0.552	0	1	1
0.584	0	1	0
0.648	0	0	1
0.696	0	0	0

1. The specified VDD_MEM voltages are PMIC settings.

3.3 Power delivery network (PDN) specification

The following subsections contain the maximum impedance specifications for the PDN.

NOTE: Design guidelines for the PDN are listed in *Training: Power Delivery Network Design* (80-VT310-13). If PCB designers have difficulty meeting these impedances, contact QTI for assistance. The *MSM8953 Digital Baseband Design Guidelines/training Slides* (80-P2472-5B) also provides guidance.

NOTE: The PDN specifications are applicable to both the 2.0 GHz and the 2.2 GHz parts.

Table 3-6 Power distribution network impedance vs. frequency

Power domain	Maximum impedance (mΩ)[1]			Port number	Pin number of positive ports	Pin number of negative ports
	DCR	1 MHz to 25 MHz	100 MHz			
VDD_APC	5	25	100	1	Y28, AD28, Y38, Y36, Y34, Y32, Y30, W39, W37, W35, W33, W31, W29, AE39, AE37, AE35, AE33, AE31, AE29, AD38, AD36, AD34, AD32, AD30	AC29, AF40, V28, Y40, V40, V38, V36, V32, V30, U39, U37, U35, U33, U31, U29, AG39, AG37, AG35, AG33, AG31, AG29, AF38, AF36, AF32, AF30, AF28, AA39, AA37, AA35, AA33, AA31, AA29
VDD_MODEM	5	25	100	1	AN37, AN35, AN33, AN27, AN25, AM32, AM18, AK18, AJ31, AJ29, AJ27, AJ25, AJ23, AJ21, AJ19, AJ17	AR17, AR21, AR19, AP20, AP18, AL39, AL37, AL35, AL33, AL29, AL27, AL25, AL17, AL15, AG31, AG29, AG25, AG23, AG21, AG19, AG17
VDD_CORE	15	46	184	1	AA15, AA13, U19, U17, U15, U13	R11, U11, N19, N13, W15, W17, N17, N15, W19, W13
	30	236	942	2	AJ37, AH36	AF36, AG37, AG35
	30	236	942	3	AR35, AR33	AP20, AR21, AL33, AL31, AL27, AL25, AU37, AU35
	30	236	942	4	R37	N35, N37
	15	40	160	5	AB28, AC27, U27, U25, AL13, AJ15, AJ13, AE23, AE21, AE15, AE13, AA23, AA21	AL15, Y24, W23, W21, V28, U29, AP16, AL17, AL11, AA29, AG25, AG23, AG21, AC15, AG19, AG17, AG15, AG13, AG11, AC29, AC23, AC21, AC19, AC17, AC13
VDD_MEM	20	94	376	1	AN13, AN11	AL15, AP16, AL11, AR11
	20	55	220	2	AR25, AR23, AP22	AR17, AP18, AP20, AR19, AR21
	15	42	168	3	AC33, AA27, W27, T32, T34, R35, T36	V36, V32, V30, V28, U37, U35, U33, U31, U29, AC29, AA37, AA35, AA33, AA31, AA29
	15	42	168	4	AE25, AE27, AG27, AH32, AJ33, AH34, AJ35	AG25, AF28, AF30, AF32, AF36, AF38, AG37, AG35, AG33, AG31, AG29
	20	94	376	5	AE19, AE17, AA19, AA17, U23, U21, R17, R15	Y24, AG21, AG15, AG19, AG17, N19, N13, N17, N15, W23, W21, W19, W17, W15, W13, AC23, AC21, AC19, AC17, AC13, AC15
	20	94	376	6	AN29, AN31, AP32	AL31, AL33, AL27

1. The PDN AC impedance specification (mask) is obtained by connecting the maximum impedance points sequentially starting at 1 MHz, and proceeding to each higher frequency point defined.

Table 3-7 VDDPX_1 and VDD_EBI PDN specification

Power domain	Maximum impedance (mΩ)	Maximum effective impedance (mΩ) [1, 2]				Port number	Pin number of positive port	Pin number of negative port
	DCR	1 MHz	3 MHz	10 MHz	200 MHz			
VDDPX_1	45	75	200	200	1500	1	J25	F26, F24, G25
		75	200	200	1250	2	J17, J19, L17, L19	G17, G19, N17, N19
		75	200	200	1250	3	J31, J33, L31, L33	G31, G33, N31, N33
		75	200	200	1250	4	J21, L21	G21, N21
		75	200	200	1250	5	J29, L29	N29, G29
		75	200	200	1250	6	J27, L27, J23, L23	N27, G23, N23
VDD_EBI	45	100	230	330	3250	1	R19, R21	N19, N21
		100	230	330	3250	2	R31, R33	N31, N33
		100	230	330	3250	3	R27, R29	N29
		100	230	330	3400	4	R23	N23
		100	230	330	3400	5	R25	N27

1. The PDN AC impedance specification (mask) is obtained by connecting the maximum impedance points sequentially starting at 1 MHz, and proceeding to each higher frequency point defined.
2. The PDN specification at 1 MHz is defined when the PMIC output pin is shorted to GND in simulation.

3.4 DC power characteristics

3.4.1 Average operating current

Detailed current consumption information and details about the operating modes tested are available in the *MSM8953 Linux Android Current Consumption Data* (80-P2472-7).

3.4.2 Dhrystone and rock bottom maximum power

Table 3-8 Dhrystone and rock bottom maximum power for MSM8953 devices

MSM version	Octa Core Dhrystone (Watt) [1, 2, 3] at 85 °C (Tj)	Rock bottom (mW) [4] at 30 °C (Tj)
MSM8953 2.0 GHz	5	7.5
MSM8953 2.2 GHz	5.8	7.5

1. This octa core Dhrystone specification applies to the MSM CS device.
2. Dhrystone power should be measured on the VDD_APC rail, at the point right before PDN capacitors (with a small serial sampling resistor inserted if necessary).
3. Measurement sampling rate should be > 1.25 Msps (or < 0.8 µs), and average window should be > 1 ms (or > 1250 samples)
4. Rock bottom (VDD_CORE and VDD_MEM) should be measured at the VDD_CORE and VDD_MEM rails when VDD_CORE and VDD_MEM are at the retention voltage. Refer to *AIR1* in Table 3-1 (Test definitions) of the *MSM8953 Linux Android Current Consumption Data* (80-P2472-7) document for the test setup.

3.5 Power sequencing

The PMIC includes power-on circuits that provide the proper power sequencing for the entire MSM8953 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of certain PMIC pins. Dedicated circuits continuously monitor several events that might trigger a power-on sequence. If any of these events occur, the PMIC circuits are powered on, the handset's available power sources are determined, the correct source is enabled, and the modem IC is taken out of reset. The PM8953 device complements the PMI8952/PMI632 device to meet the system's power management needs. For details, refer to the *PM8953 Power Management IC Device Specification* (80-P2536-1).

The power-on sequence is shown in Figure 3-1.

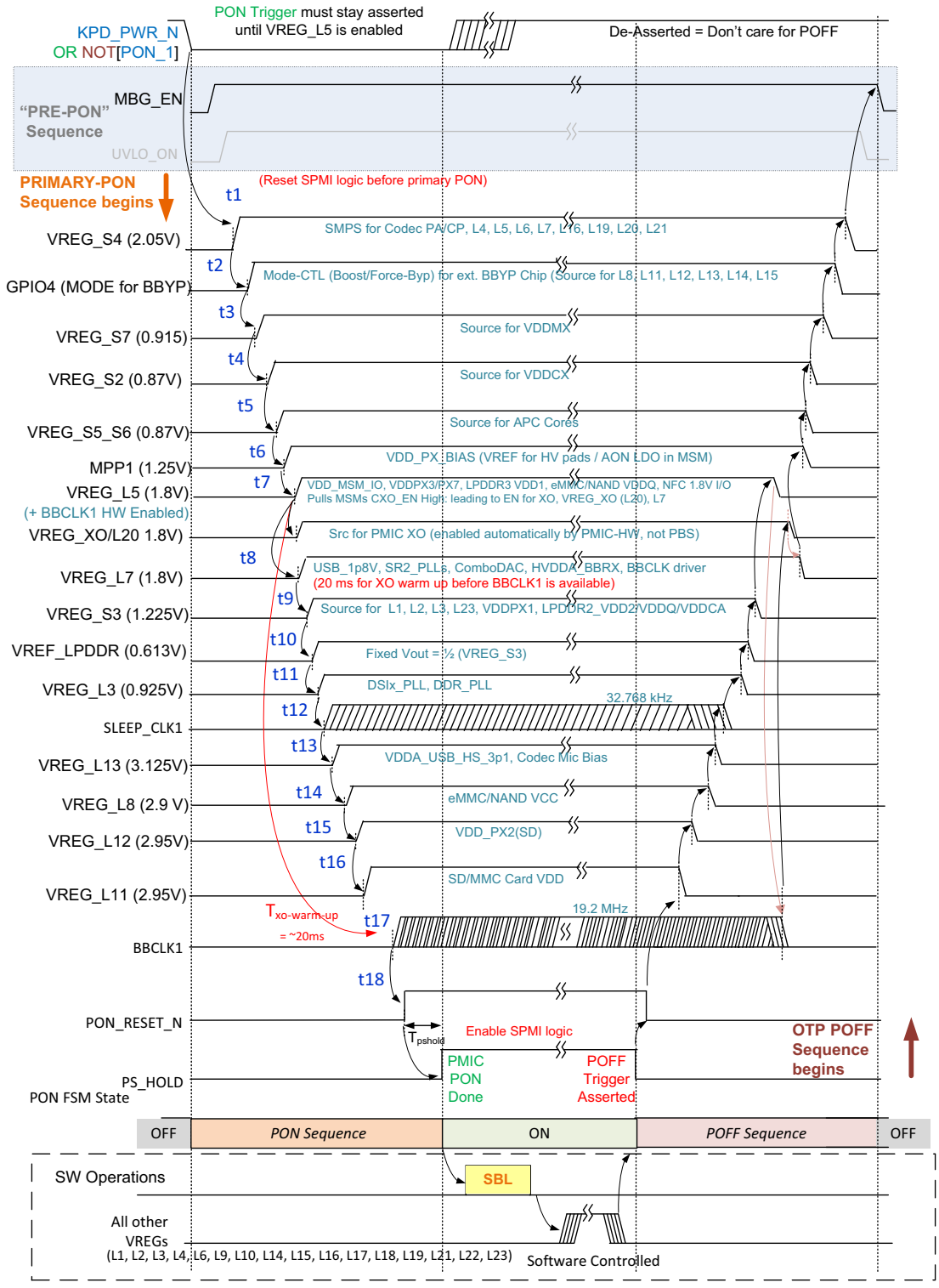


Figure 3-1 power-on sequence

3.6 Digital-logic characteristics

A digital I/O's performance specification depends on its pad type, its usage, and/or its supply voltage:

- Some digital I/Os are dedicated for interconnections between the MSM8953 and other ICs within the QTI chipset; therefore, specifications are not required.
- Some digital I/Os are defined by existing standards, such as I^2C and SPI. QTI devices comply with those standards; therefore, additional specifications are not required.
- All other digital I/Os require performance specifications

Table 3-9 Digital I/O characteristics for VDDPX_1 (1.2 V)

Parameter	Comments	Min	Max	Unit
V_{REF}	Reference voltage	0.49 × VDDPX_1	0.51 × VDDPX_1	V
V_{IH}	High-level input voltage, CMOS/Schmitt-LPRx	0.65 × VDDPX_1	–	V
V_{IL}	Low-level input voltage CMOS/Schmitt-LPRx	–	0.35 × VDDPX_1	V
V_{IH}	High-level input voltage, CMOS/Schmitt-MPRx	VDDPX_1/2 + 0.1	–	V
V_{IL}	Low-level input voltage CMOS/Schmitt-MPRx	–	VDDPX_1/2 - 0.1	V
I_{IH}	Input high leakage current, no pull-down	–	5	µA
I_{IL}	Input low leakage current, no pull up	-5	–	µA
I_{IHPD}	Input high leakage current, with pull down	40	3000	µA
I_{ILPU}	Input low leakage current, with pull up	-3000	-40	µA
V_{OH}	High-level output voltage, CMOS, at rated drive strength-config G[1]	0.355	–	V
V_{OL}	Low-level output voltage, CMOS, at rated drive strength- config G[2]	–	0.35	V
I_{OZHKP}	High-level, tri-state leakage, with keeper	-1200	-10	µA
I_{OZLKP}	Low-level, tri-state leakage, with keeper	10	1200	µA
CI/O	I/O capacitance	1.25	2.5	pF

1. See Table 2-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable, and depend on the associated supply voltage.
2. Input capacitance and I/O capacitance values are guaranteed by design, but not 100% tested.

Table 3-10 DC specification of VDDPX_3 = 1.8 V GPIOs

Parameter	Description	Min	Max	Units
V_{IH}	High-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	0.65 × VDDPX_3	VDDPX_3 + 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt, (hihys_en = LOW)	-0.3 V	0.35 × VDDPX_3	V
V_{IH}	High-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	0.7 × VDDPX_3	VDDPX_3+ 0.3 V	V
V_{IL}	Low-level input voltage, CMOS/Schmitt, (hihys_en = HIGH)	-0.3 V	0.3 × VDDPX_3	V
V_{SHYS}	Schmitt hysteresis voltage, (hihys_en = LOW)	100	–	mV
V_{SHYS}	Schmitt hysteresis voltage, (hihys_en = HIGH)	300	–	mV
I_{IH}	Input high leakage current with no pulldow [1]	–	1	µA
I_{IL}	Input low leakage current with no pull-up[1]	-1	–	µA
I_{IHPD}	Input high leakage current with pull-down	27.5 (60 K)	97.5 (20 K)	µA Ω
I_{ILPU}	Input low leakage current with pull-up	-97.5 (20 K)	-27.5 (60 K)	µA Ω
I_{OZH}	High-level, tri-state leakage current with no pulldown[1]	–	1	µA
I_{OZL}	Low-level, tri-state leakage current with no pullup[1]	-1	–	µA
I_{OZHPD}	High-level, tri-state leakage current with pull-down	27.5 (60 K)	97.5 (20 K)	µA Ω
I_{OZLPU}	Low-level, tri-state leakage current with pull-up	97.5 (20 K)	27.5 (60 K)	µA Ω
I_{OZHKP}	High-level, tri-state leakage current with keeper [2]	-22.5 (20 K)	-7.5 (60 K)	µA Ω
I_{OZLKP}	Low-level, tri-state leakage current with keeper [2]	7.5 (60 K)	22.5 (20 K)	µA Ω
V_{OH}	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V
V_{OL}	Low-level output voltage, CMOS	0.0	0.45	V
$R_{PULL-UP}$	Pull-up resistance	20 K	60 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	20 K	60 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	20 K	60 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	20 K	60 K	Ω
RFFE pins				
$R_{PULL-UP}$	Pull-up resistance	–	41.25 K	Ω

Table 3-10 DC specification of VDDPX_3 = 1.8 V GPIOs (cont.)

Parameter	Description	Min	Max	Units
$R_{PULL-DOWN}$	Pull-down resistance	–	41.25 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	–	41.25 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	–	41.25 K	Ω

1. Pin voltage = VDDPX_3 maximum. For keeper pins, pin voltage = VDDPX_3 maximum - 0.45 V.
2. Pin voltage = GND and supply = VDDPX_3 maximum. For keeper pins, pin voltage = 0.45 V and supply = VDDPX_3 maximum.

Table 3-11 Digital I/O characteristics for VDDPX_7 = 1.8 V nominal (SDC1)

Parameter	Description	Min	Typ	Max	Units
V_{OH}	High-level output voltage	VDDPX_7 - 0.45 V	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45 V	V
V_{IH}	High-level input voltage	0.65 × VDDPX_7	–	VDDPX_7 + 0.3 V	V
V_{IL}	Low-level input voltage	-0.3 V	–	0.35 × VDDPX_7	V
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω

Table 3-12 Digital I/O characteristics for VDDPX_2 = 2.95 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	0.625 × VDDPX_2	–	VDDPX_2 + 0.3	V
V_{IL}	Low-level input voltage	-0.3	–	0.25 × VDDPX_2	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current with no pull down	–	–	10	µA
I_{IL}	Input low leakage current with no pull up	-10	–	–	µA
I_{OZH}	High-level, tri-state leakage current with no pull down	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current with no pull up	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω

Table 3-12 Digital I/O characteristics for VDDPX_2 = 2.95 V nominal (SDC2) (cont.)

Parameter	Description	Min	Typ	Max	Units
$R_{KEEPER-UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω
V_{OH}	High-level output voltage	0.75 × VDDPX_2	–	VDDPX_2	V
V_{OL}	Low-level output voltage	0.0	–	0.125 × VDDPX_2	V

Table 3-13 Digital I/O characteristics for VDDPX_2 = 1.8 V nominal (SDC2)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage	1.27	–	2	V
V_{IL}	Low-level input voltage	-0.3	–	0.58	V
V_{HYS}	Schmitt hysteresis voltage	100	–	–	mV
I_{IH}	Input high leakage current with no pull down	–	–	5	µA
I_{IL}	Input low leakage current with no pull up	-5	–	–	µA
I_{OZH}	High-level, tri-state leakage current with no pull-down	-	–	5	µA
I_{OZL}	Low-level, tri-state leakage current with no pull up	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω
V_{OH}	High-level output voltage	1.4	–	–	V
V_{OL}	Low-level output voltage	–	–	0.45	V

Table 3-14 Digital I/O characteristics for VDDPX_X = 2.95 V nominal (UIM1 and UIM2 – Class B)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_X	–	VDDPX_X + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_X	V
V_{HYS}	Schmitt hysteresis voltage [1]	100	–	–	mV
I_{IH}	Input high leakage current with no pull down	-20	–	20	µA
I_{IL}	Input low leakage current with no pull up	–	–	1000	µA

Table 3-14 Digital I/O characteristics for VDDPX_X = 2.95 V nominal (UIM1 and UIM2 – Class B) (cont.)

Parameter	Description	Min	Typ	Max	Units
I_{OZH}	High-level, tri-state leakage current with no pull-down	–	–	10	µA
I_{OZL}	Low-level, tri-state leakage current with no pull-up	-10	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω
V_{OH}	High-level output voltage [2]	0.8 × VDDPX_X	–	VDDPX_X	V
V_{OL}	Low-level output voltage [2]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.
2. UIM specifies V_{OL} = 0.2 × VDDPX_X (RST, CLK) and 0.4 V (I/O) and V_{OH} = 0.8 × VDDPX_X (RST) and 0.7 × VDDPX_X (CLK, I/O). The worst-case V_{OL} and V_{OH} values are used in the table.

Table 3-15 Digital I/O characteristics for VDDPX_X = 1.8 V nominal (UIM1 and UIM2 – Class B)

Parameter	Description	Min	Typ	Max	Units
V_{IH}	High-level input voltage [1]	0.7 × VDDPX_X	–	VDDPX_X + 0.3	V
V_{IL}	Low-level input voltage [1]	-0.3	–	0.2 × VDDPX_X	V
V_{HYS}	Schmitt hysteresis voltage [1]	100	–	–	mV
I_{IH}	Input high leakage current with no pull-down	-20	–	20	µA
I_{IL}	Input low leakage current with no pull-up	–	–	1000	µA
I_{OZH}	High-level, tri-state leakage current with no pull-down	–	–	5	µA
I_{OZL}	Low-level, tri-state leakage current with no pull up	-5	–	–	µA
$R_{PULL-UP}$	Pull-up resistance	10 K	–	100 K	Ω
$R_{PULL-DOWN}$	Pull-down resistance	10 K	–	100 K	Ω
$R_{KEEPER-UP}$	Keeper-up resistance	10 K	–	100 K	Ω
$R_{KEEPER-DOWN}$	Keeper-down resistance	10 K	–	100 K	Ω
V_{OH}	High-level output voltage [2]	0.8 × VDDPX_X	–	VDDPX_X	V
V_{OL}	Low-level output voltage [2]	0.0	–	0.4	V

1. V_{IH} and V_{IL} are only applicable for the I/O signal.

2. UIM specifies V_{OL} = 0.2 × VDDPX_X (RST, CLK) and 0.4 V (I/O) and VOH = 0.8 × VDDPX_X (RST) and 0.7 × VDDPX_X (CLK, I/O). The worst-case V_{OL} and V_{OH} are used in the table.

In all digital I/O cases, V_{OL}, and V_{OH} are linear functions (Figure 3-2) regarding the drive current (drive currents are given in Table 2-1). They can be calculated using the following relationships:

$$Vol[\max] = \frac{\%drive \times 450}{100} mV$$

$$Voh[\min] = V_{DDPX\_X} - \left(\frac{\%drive \times 450}{100} \right) mV$$

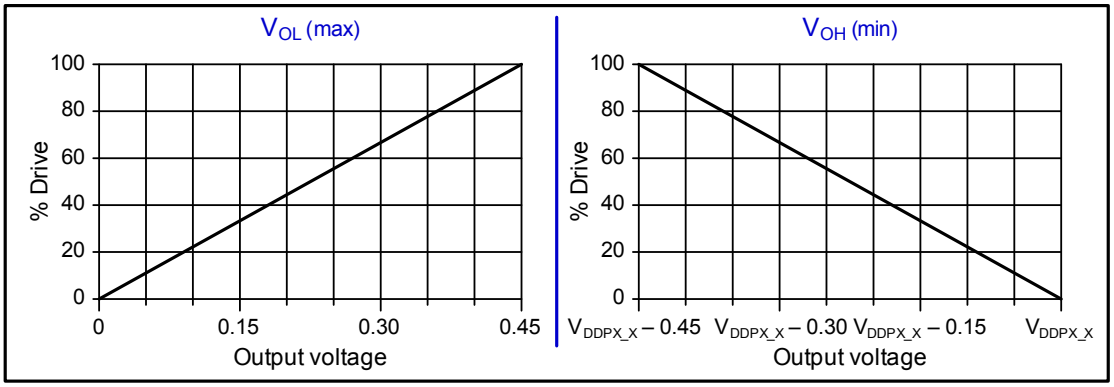


Figure 3-2 IV curve for V_{OL} and V_{OH} (valid for all V_{DDPX_X})

3.7 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics and pertinent pad design methodologies are included in this section.

NOTE: All MSM8953 devices are characterized with actively terminated loads; therefore, all baseband timing parameters in this document assume no bus loading. This is described in more detail in Section 3.7.2.

3.7.1 Timing diagram conventions

The conventions used within timing diagrams throughout this document are shown in Figure 3-3.

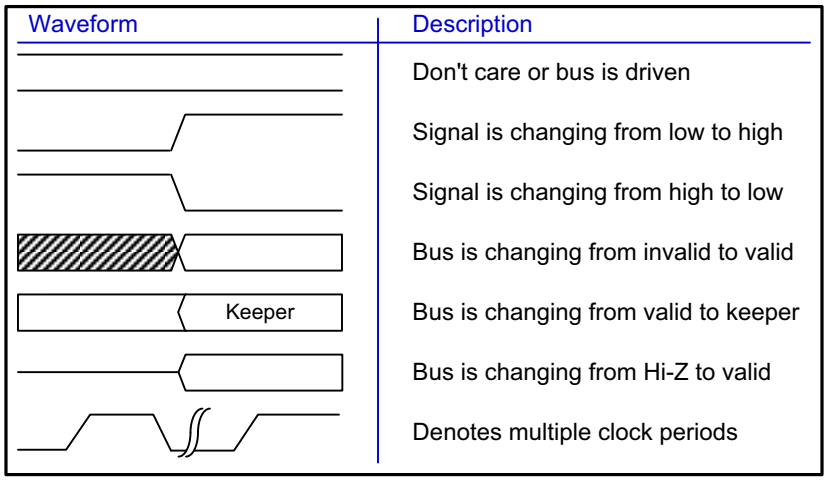


Figure 3-3 Timing diagram conventions

For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown over the same time interval, the meaning depends on the signal type:
  - For a bus type signal (multiple bits), the processor or external interface is driving a value, but that value may or may not be valid.
  - For a single signal, this indicates *don't care*.

3.7.2 Rise and fall time specifications

The testers that characterize MSM8953 devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 3-4.

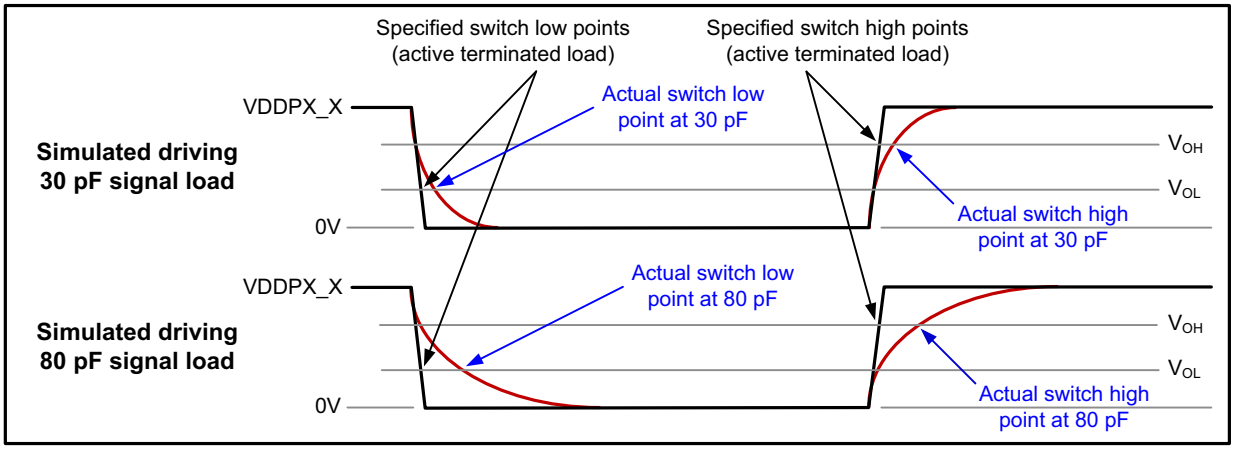


Figure 3-4 Rise and fall times under different load conditions

To account for external load conditions, rise or fall times must be added to parameters that start timing at the MSM8953 and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors.

3.7.3 Pad design methodology

The MSM8953 device uses a generic CMOS pad driver design. The intent of the pad design is to create pin response and behavior that is symmetric regarding the associated V_{DDPX_X} supply (Figure 3-5). The input switch point for pure input-only pads is designed to be $V_{DDPX\_X}/2$ (or 50% of V_{DDPX_X}). The documented switch points (guaranteed over worst-case combinations of process, voltage, and temperature by both design and characterization) are 35% of V_{DDPX_X} for V_{IL} and 65% of V_{DDPX_X} for V_{IH}.

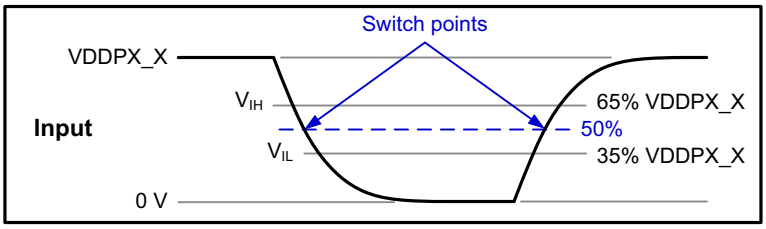


Figure 3-5 Digital input-signal switch points

Outputs (address, chip selects, clocks, and so on.) are designed and characterized to source or sink a large DC output current (several mA) at the documented V_{OH} (min) and V_{OL}(max) levels over the worst-case process/voltage/temperature. Since the pad output structures (Figure 3-6) are essentially CMOS drivers that possibly have a small amount of IR loss (estimated at less than 50 mV under worst-case conditions), the expected zero DC load outputs are estimated to be:

- $V_{OH} \sim V_{DDPX\_X}$ - 50 mV or more
- $V_{OL} \sim$ 50 mV or less

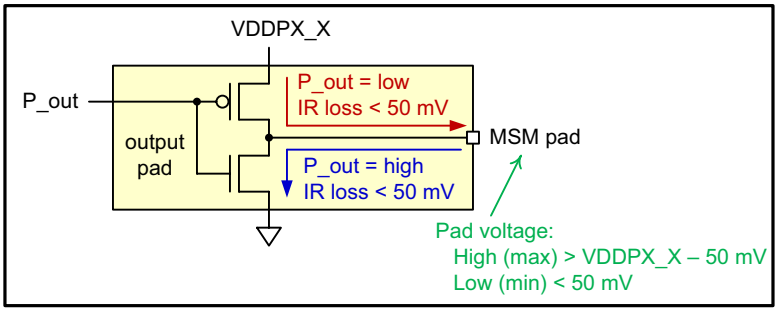


Figure 3-6 Output pad equivalent circuit

The DC output drive strength can be approximated by linear interpolations between V_{OH} (min) and V_{DDPX_X} - 50 mV, and between V_{OL} (max) and 50 mV. For example, an output pad driving low that guarantees 4.5 mA at V_{OL} (max) provides approximately 3.0 mA or more at 2/3 × [V_{OL} (max) - 50 mV], and 1.5 mA or more at 1/3 × [V_{OL} (max) - 50 mV]. Likewise, an output pad driving high that guarantees 2.5 mA at V_{OH} (min) provides approximately 1.25 mA or more at ½ × [V_{DDPX_X} - 50 mV + V_{OH} (min)].

The output pads are CMOS outputs with a corresponding FET-type output voltage/current transfer function. When an output pad is shorted to the opposite power rail, the pad is capable of sourcing or sinking I_{SC} (SC = short-circuit) of current, where the magnitude of I_{SC} is larger than the current capability at the intended output logic levels.

Since the target application includes a radio, output pads are designed to *minimize* output slew rates. Decreased slew rates limit high-frequency spectral components that desensitize the companion radio.

The output drivers' rise time [**t**(r)] and fall time [**t**(f)] values are functions of board loading. Bidirectional pins include both input and output pad structures, and behave accordingly when used as inputs or outputs within the system. Both input and output behaviors were described previously.

3.8 Memory support

All timing parameters in this document assume no bus loading. Rise/fall time numbers must be factored into the numbers in this document. For example, setup-time numbers may get worse, and hold time numbers may get better.

3.8.1 EBI0 memory support

The EBI0 port is dedicated to the non-PoP LPDDR3 SDRAM memory that is attached to the MSM8953 chipset.

3.8.1.1 LPDDR3 SDRAM strobe

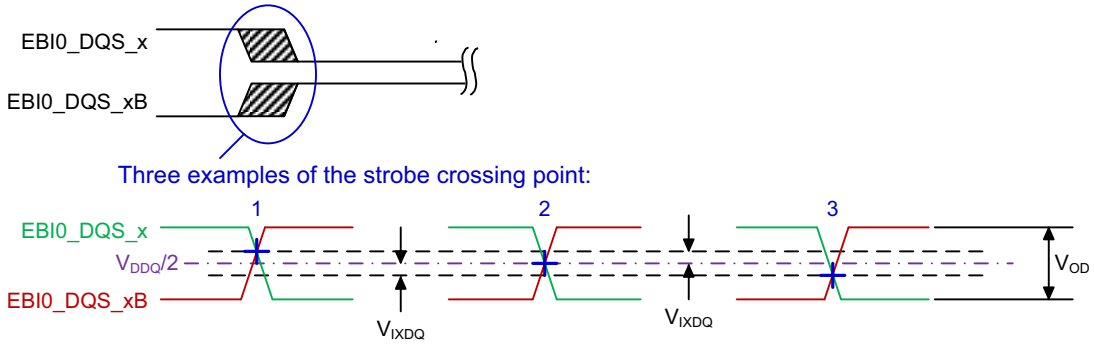


Figure 3-7 DDR SDRAM EBI0_DQS_x and EBI0_DQS_xB

Table 3-16 DDR SDRAM DQS timing parameters

Parameter		Comments	Min	Typ	Max	Unit
V_{IXDQ}	Clock crossover point	± offset from VDDQ/2	-120	–	120	mV
V_{OD}	Differential output voltage		0.44	–	–	V

3.8.1.2 LPDDR3 SDRAM read and write timing

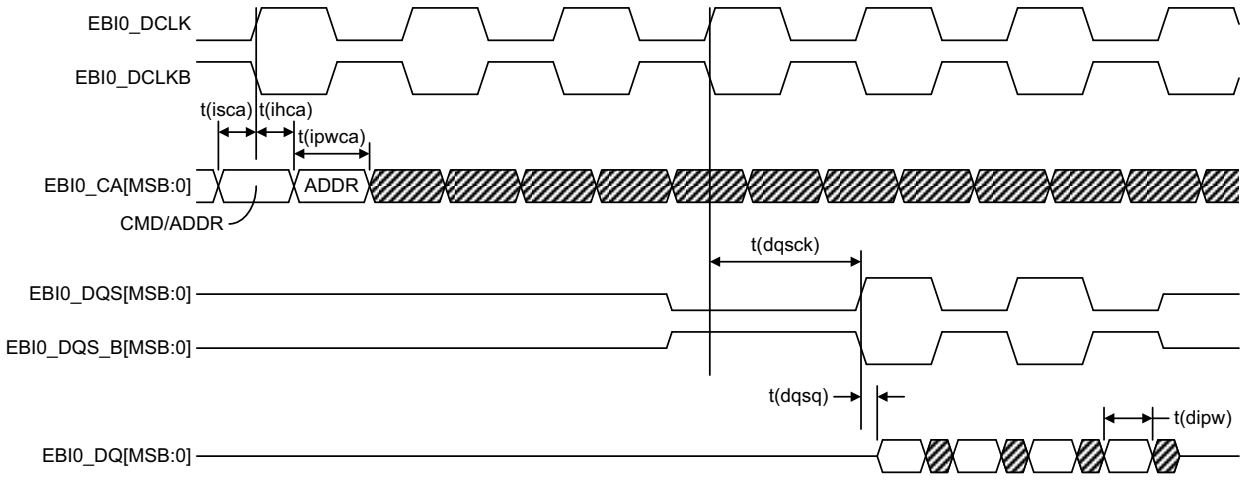


Figure 3-8 DDR SDRAM read timing

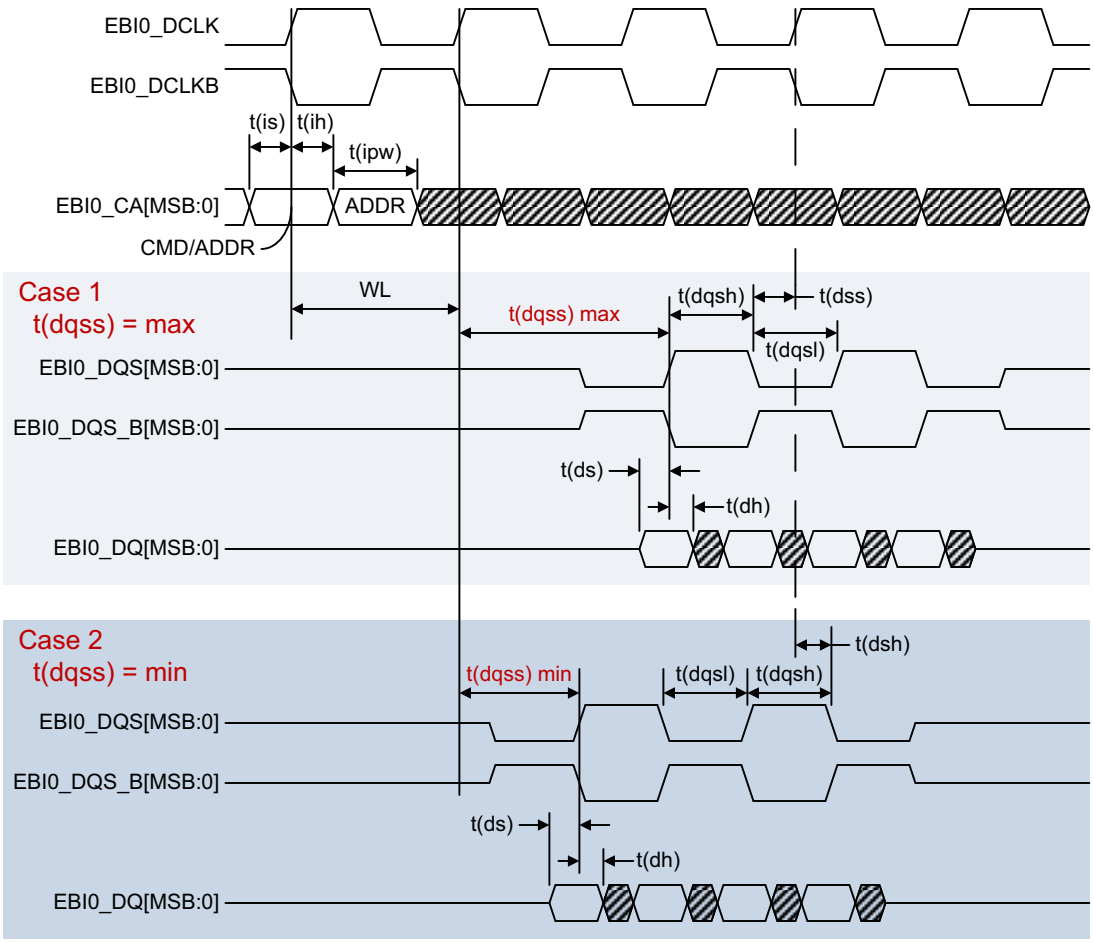


Figure 3-9 DDR SDRAM write timing

3.8.2 eMMC on SDC1

eMMC NAND flash can be supported via the SDC1 port. See Section 3.10.1 for secure digital interface details.

3.8.3 NOR memory on SPI

SPI can be used to support NOR memory devices with appropriate user-modified software. See Section 3.10.8 for serial peripheral interface details.

3.9 Multimedia

Multimedia parameters requiring performance specification are addressed in this section.

3.9.1 Camera interfaces

The MSM8953 device supports up to three four-lane camera interfaces or up to four (two four-lane and two one-lane) camera interfaces.

Table 3-17 Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported	None
MIPI Alliance Specification for DPHY v1.2	None	None
MIPI Alliance Specification for CPHY v1.0	None	None

3.9.2 Audio support

The MSM8953 supports the WCD9326 and WCD9335 audio codec ICs to provide the system's audio functions. MSM audio-related interface options with the WCD include:

- SLIMbus: Section 3.10.4
- I2S: Section 3.10.5
- I^2C: Section 3.10.7

Refer to the *WCD9326 Audio Codec Device Specification* (80-NT793-1) and the *WCD9335 Audio Codec Device Specification* (80-NT781-1) for the performance characteristics.

3.9.3 Display support

MSM8953 supports two 4-lane MIPI_DSI.

Table 3-18 Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for Display Serial Interface	None	None
MIPI Alliance Specification for D-PHY V1.2	None	None

3.10 Connectivity

The connectivity functions supported by the MSM8953 that require electrical specifications include:

- SD, including SD cards and MMC
- USB host/slave support with built-in physical layer (PHY)
- UIM ports, including dual-voltage options
- SLIMbus interface
- Inter-IC sound (I^2S) interfaces
- Touchscreen connections
- Through proper configuration of the eight BLSP ports:
  - Universal asynchronous receiver/transmitter (UART) ports
  - Inter-integrated circuit (I^2C) interfaces
  - Serial peripheral interface (SPI) ports

Pertinent specifications for these functions are detailed in the following subsections.

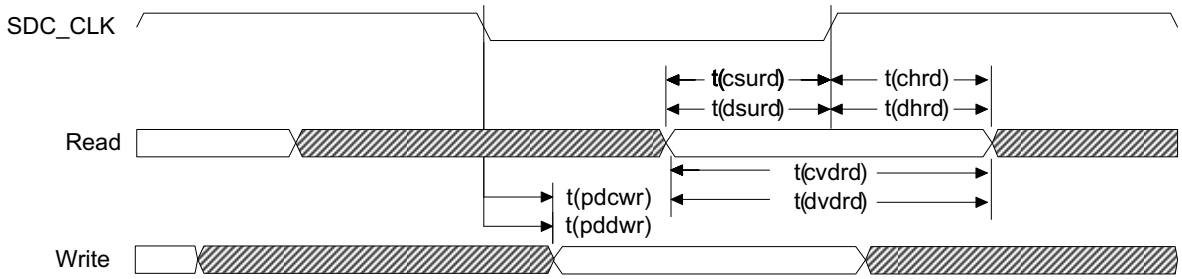
NOTE: In addition to the following hardware specifications, refer to the latest software release notes for software-based performance features or limitations.

3.10.1 SD interfaces

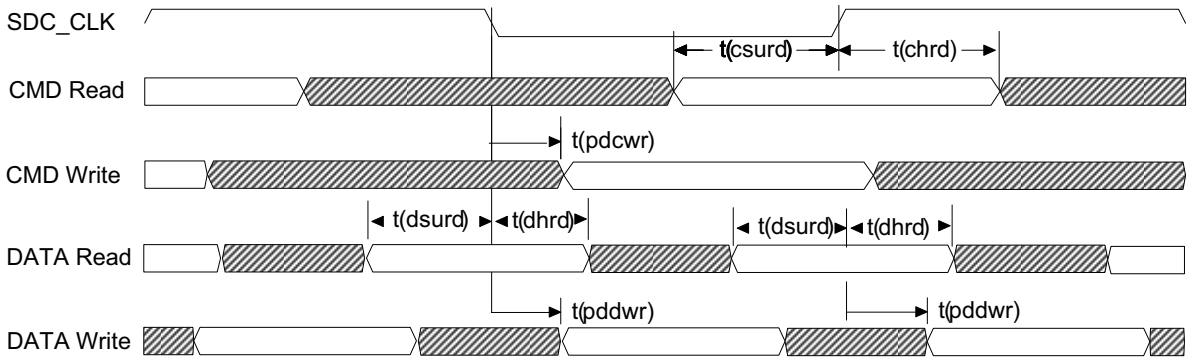
Table 3-19 Supported SD standards and exceptions

Applicable standard	Feature exceptions	MSM variations
Embedded Multimedia Card (e.MMC) Specification version 5.1	None	Timing specifications: see Figure 3-10
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 3.0	None	

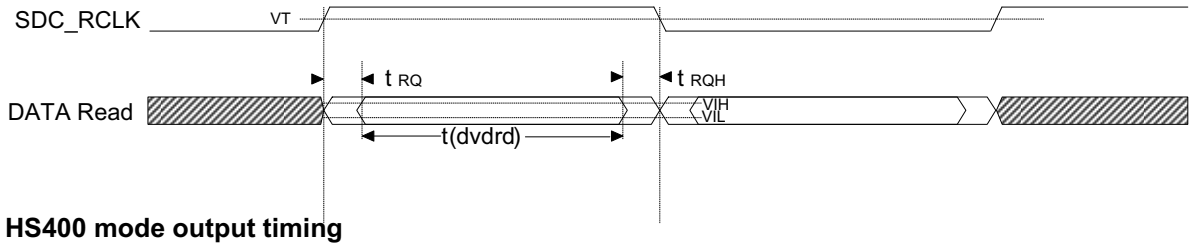
Single data rate – SDR mode



Double data rate – DDR mode



HS400 mode input timing



HS400 mode output timing

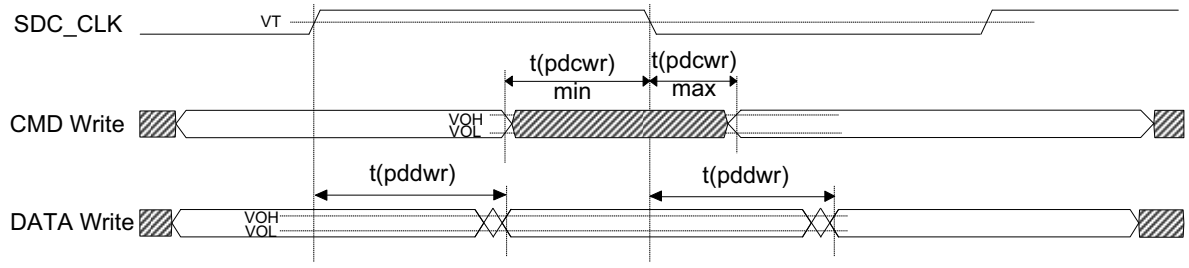


Figure 3-10 SD interface timing

3.10.2 USB interfaces

Table 3-20 Supported USB standards and exceptions

Applicable standard	Feature exceptions	MSM variations
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2	Operating voltages, system clock, and VBUS
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None	None

3.10.3 UIM interface

Table 3-21 Supported UIM standards and exceptions

Applicable standard	Feature exceptions	MSM variations
ISO/IEC 7816-3	None	None

3.10.4 SLIMbus interface

Table 3-22 Supported SLIMbus standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None	None

3.10.5 I2S interfaces

Legacy I2S interfaces for primary and secondary microphones and speakers.

Table 3-23 Supported I2S standards and exceptions

Applicable standards	Feature exceptions	MSM variations
Philips I2S Bus Specifications revised June 5, 1996 (Available for free download.)	None	Timing - see Figure 3-11 When an external SCK clock is used, a duty cycle between 45% to 55% is required.

Figure 3-11 I2S timing diagram

Table 3-24 I2S interface timing

Parameter		Comments [1]	Min	Typ	Max	Unit	Note x% of T
Using internal SCK							
Frequency		–	–	–	12.288	MHz	–
T	Clock period	–	81.380	–	–	ns	–
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns	–
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns	–

Table 3-24 I²S interface timing (cont.)

Parameter		Comments [1]	Min	Typ	Max	Unit	Note x% of T
t(sr)	SD and WS input setup time	–	16.276	–	–	ns	20
t(hr)	SD and WS input hold time	–	0	–	–	ns	–
t(dtr)	SD and WS output delay	–	–	–	24.414	ns	30
t(htr)	SD and WS output hold time	–	0	–	–	ns	–
Using external SCK							
Frequency		–	–	–	12.288	MHz	–
T	Clock period	–	81.380	–	–	ns	–
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns	–
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns	–
t(sr)	SD and WS input setup time	–	16.276	–	–	ns	20
t(hr)	SD and WS input hold time	–	0	–	–	ns	–
t(dtr)	SD and WS output delay	–	–	–	24.414	ns	15
t(htr)	SD and WS output hold time	–	0	–	–	ns	–

1. Load capacitance between 10 pF to 40 pF.

3.10.6 Touchscreen connections

Touchscreen panels are supported using I²C buses (Section 3.10.7) and GPIOs configured as discrete digital inputs (Section 3.6). Additional specifications are not required.

3.10.7 I²C interface

Table 3-25 Supported I²C standards and exceptions

Applicable standard	Feature exceptions	MSM variations
I²C Specification, version 3.0	None	Multi-master, slave mode, and 10-bit addressing are not supported.

3.10.8 Serial peripheral interface

The MSM8953 supports SPI as a master only. Any one of the eight BLSP ports can be configured as an SPI master.

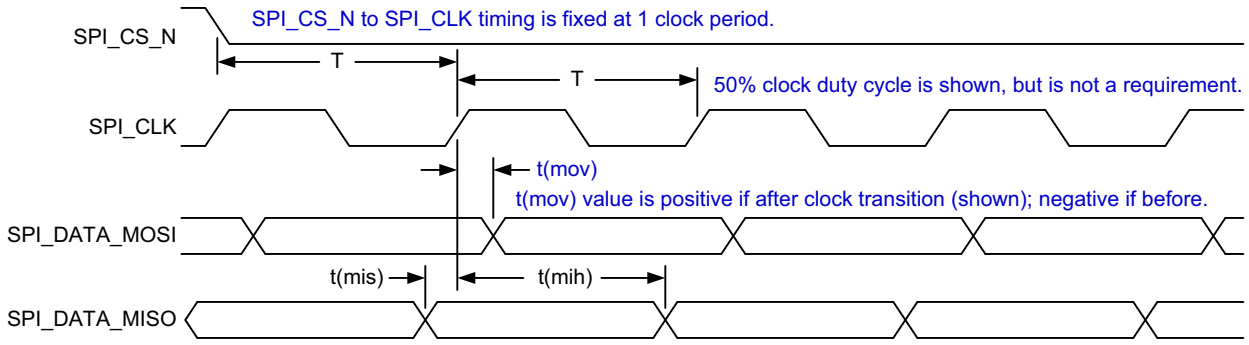


Figure 3-12 SPI master timing diagram

Table 3-26 SPI master timing characteristics

Parameter	Comments	Min	Typ	Max	Unit
T (SPI clock period) [1]	50 MHz maximum	20	–	–	ns
t(ch)	Clock HIGH	8	–	–	ns
t(cl)	Clock LOW	8	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

1. The minimum clock period includes 1% jitter of maximum frequency.

3.11 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions.

3.11.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

3.11.1.1 19.2 MHz XO input

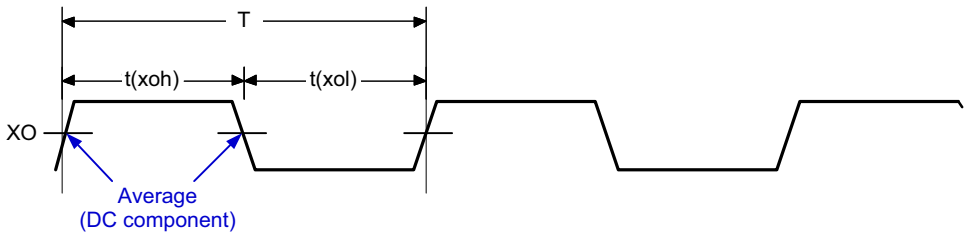


Figure 3-13 XO timing parameters

Table 3-27 XO timing parameters

Parameter		Comments [1]	Min	Typ	Max	Unit
t(xoh)	XO logic high		22.6	–	29.5	ns
t(xol)	XO logic low		22.6	–	29.5	ns
T	XO clock period		–	52.083	–	ns
1/T	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

1. Refer the *GPS Quality, 19.2 MHz 2520 Package Size, Crystal, and TH+Xtal Mini-Specification* (80-V9690-24) for more information.

3.11.1.2 Sleep clock

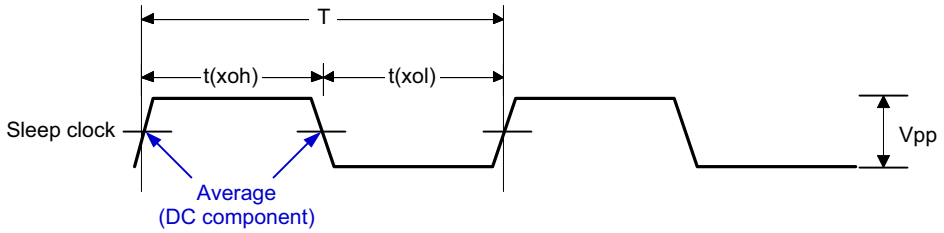


Figure 3-14 Sleep-clock timing parameters

Table 3-28 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T	Sleep-clock period		–	30.518	–	µs
F	Sleep-clock frequency	F = 1/T	–	32.768	–	kHz
Vpp	Peak-to-peak voltage		–	1.8	–	V

3.11.2 Modes and resets

Mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 3.6.

3.11.3 JTAG

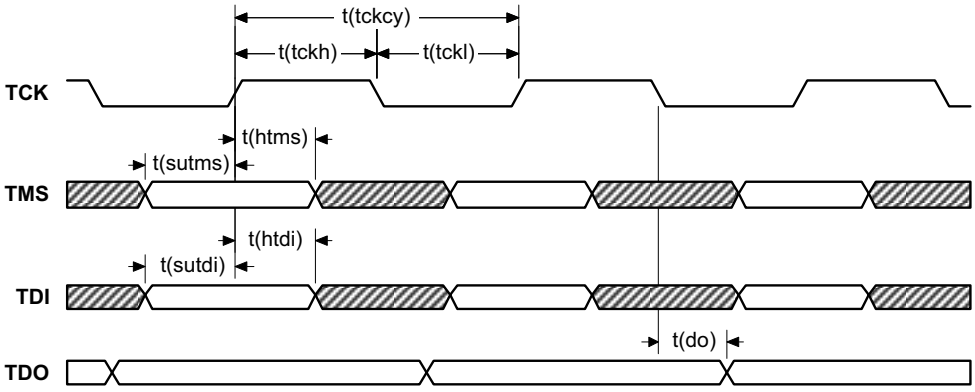


Figure 3-15 JTAG interface timing diagram

Table 3-29 JTAG interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		50	–	–	ns
t(tckh)	TCK pulse width high		20	–	–	ns
t(tckl)	TCK pulse width low		20	–	–	ns
t(sutms)	TMS input setup time		5	–	–	ns
t(htms)	TMS input hold time		20	–	–	ns
t(sutdi)	TDI input setup time		5	–	–	ns
t(htdi)	TDI input hold time		20	–	–	ns
t(do)	TDO data output delay		–	–	15	ns

3.11.4 SWD

Figure 3-16 SWD write and read AC timing diagram

Table 3-30 AC timing parameters

Parameter		Min	Max	Unit
T_{os}	SWDIO output skew to falling edge of SWDCLK	0	17.5	ns
T_{su}	Input setup time between SWDIO and rising edge of SWDCLK	4	–	ns
T_{hd}	Input hold time between SWDIO and rising edge of SWDCLK	1	–	ns

3.12 RF and power management interfaces

The supported chipset and RFFE interfaces are listed in Table 2-9 and Table 2-11. The digital I/Os must meet the logic-level requirements specified in Section 3.6. The Rx and Tx baseband interfaces are proprietary and therefore are not specified.

3.12.1 RFFE

Table 3-31 Supported RFFE standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for RF Front-End Control Interface version 1.0	None	None

3.12.2 SPMI

Table 3-32 Supported SPMI standards and exceptions

Applicable standard	Feature exceptions	MSM variations
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None	None

4 Mechanical information

4.1 Device physical dimensions

The MSM8953 is available in the 857 NSP that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 857 NSP has a 14 mm by 14 mm body, with a maximum height of 0.84 mm. Pin A1 is located by an indicator mark on the top of the package, and by the ball pattern when viewed from below. A simplified version of the 857 NSP outline drawing is shown in Figure 4-1.

NOTE: Click the following links to download *Package Outline Drawing, 857 NSP, 14.0 14.0 x 0.84 mm, S145, M450* (NT90-P2391-2) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/NT90-P2391-2

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

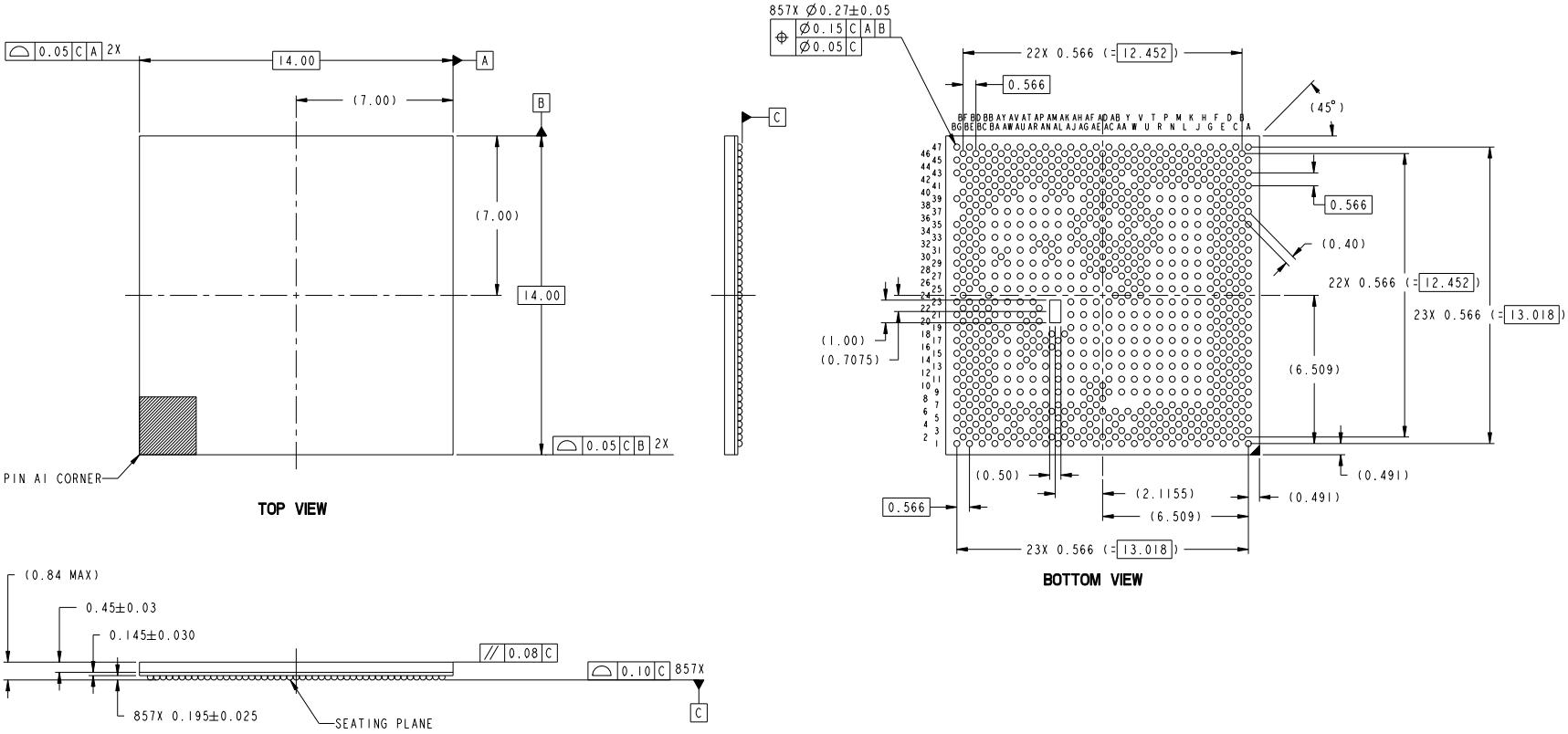


Figure 4-1 857 NSP (14 × 14 × 0.84 mm) outline drawing

4.2 Part marking

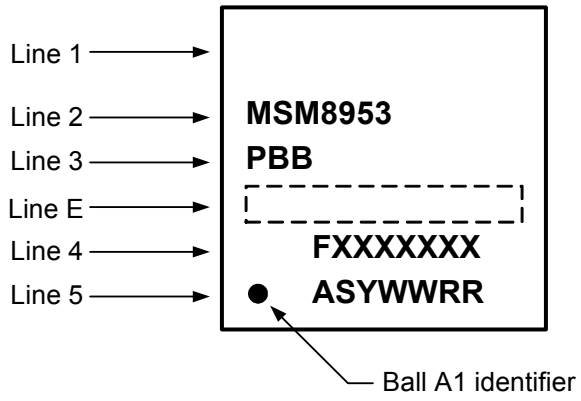


Figure 4-2 MSM8953 device marking (top view, not to scale)

Table 4-1 MSM8953 marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	MSM8953	Qualcomm Technologies Inc. (QTI) product name
3	PBB	P = product configuration code ■ See Table 4-3 for assigned values. BB = feature code ■ See Table 4-3 for assigned values.
E	Blank or variable	Additional content as necessary
4	FXXXXXXX	F = supply source code ■ F = J (Samsung) ■ F = H (GLOBALFOUNDRIES) ■ XXXXXXX = traceability number
5	ASYWWRR	A = assembly site code ■ A = E (ASE, Taiwan) ■ A = U (Amkor, China) ■ A = K (SPIL, Taiwan) ■ A = H (JCET STATS ChipPAC, Korea) S = Assembly sequence number Y = single-digit year WW = work week (based on calendar year) RR = product revision ■ See Table 4-3 for assigned values.

NOTE: For complete marking definitions of all MSM8953 variants and revisions, refer to the *MSM8953 Device Revision Guide* (80-P2472-4).

The 28-bit QFPROM JTAG register is summarized in Table 4-2.

Table 4-2 QFPROM_CORR_JTAG_ID_LSB register

Bit location	Name	Description
bits [27:20]	FEATURE_ID	These bits are used for defining various feature variants.
bits [19:0]	JTAG_ID	These bits map to bits [31:12] of the hardware revision number.

4.3 Device ordering information

4.3.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table 4-3.

Device ID code ►	AAA-AAAA	— P	— CCC	DDDD	— EE	— RR	— S	— BB
Symbol definition ►	Product name	Config code	Number of pins	Package type	Shipping package	Product revision	Source code	Feature code
Example ►	MSM-8953	— 0	— 857	NSP	— TR or MT	— 00	— 0	— AB

'CCC' is not a fixed length; it depends on the # of pins in the package

Package type varies in the # of characters

Feature code (BB) may not be included when identifying older devices.

Figure 4-3 Device identification code

Device identification details for all samples available to date are summarized in Table 4-3.

Table 4-3 Device identification details

Device	Product configuration code (*P*)	Product revision (*RR*)	Hardware revision number	Sample type [1]	S value [2]	BB value [3]	Comments
MSM8953	0	00	0x0 0046 0E1	ES1	0	AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 4, TDS, UMTS, GSM, CDMA
	1	00	0x0 0046 0E1	ES1		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 7, TDS, UMTS, GSM, CDMA
	2	00	0x0 0046 0E1	ES1		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 4, TDS, UMTS, GSM
	3	00	0x0 0046 0E1	ES1		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 7, TDS, UMTS, GSM
MSM8953	0	01	0x1 0046 0E1	ES2/CS	0	AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 4, TDS, UMTS, GSM, CDMA
	1	01	0x1 0046 0E1	ES2/CS		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 7, TDS, UMTS, GSM, CDMA
	2	01	0x1 0046 0E1	ES2/CS		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 4, TDS, UMTS, GSM
	3	01	0x1 0046 0E1	ES2/CS		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE Cat 7, TDS, UMTS, GSM

Table 4-3 Device identification details

Device	Product configuration code (*P*)	Product revision (*RR*)	Hardware revision number	Sample type [1]	S value [2]	BB value [3]	Comments
MSM8953	0	01	0x1 0046 0E1	CS	1	AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT4, TDS, UMTS, GSM, CDMA
	1	01	0x1 0046 0E1	CS		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT7, TDS, UMTS, GSM, CDMA
	2	01	0x1 0046 0E1	CS		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT4, TDS, UMTS, GSM
	3	01	0x1 0046 0E1	CS		AB	2.0 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT7, TDS, UMTS, GSM
MSM8953	1	01	0x1 0046 0E1	ES/CS	0	AC	2.2 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT7, TDS, UMTS, GSM, CDMA
	3	01	0x1 0046 0E1	ES/CS		AC	2.2 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT7, TDS, UMTS, GSM
MSM8953	1	01	0x1 0046 0E1	CS	1	AC	2.2 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT7, TDS, UMTS, GSM, CDMA
	3	01	0x1 0046 0E1	CS		AC	2.2 GHz octa-core CPU, 933 MHz DDR, 650 MHz GPU, 24 MP camera, 4k video, FHD display, LTE CAT7, TDS, UMTS, GSM

1. Table 4-4 lists the date code information for MSM8953 devices.
2. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available at the time a particular sample type was shipped. S values are defined in Table 4-5.
3. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants.

Table 4-4 Date code information for MSM8953 devices

Device	BB value	Sample type	Assembly site	Date code (YWW)
MSM8953	AB	CS	E for ASE, Taiwan K for SPIL, Taiwan H for JCET STATS ChipPAC, Korea	≥ 616
			U for Amkor, China[1]	≥ 615
	AC	CS	E for ASE, Taiwan K for SPIL, Taiwan H for JCET STATS ChipPAC, Korea U for Amkor, China	≥ 628

1. Supply with lot ID JSZ5TC from Amkor is not CS quality.

Table 4-5 Source configuration code

S value	Die	F value = J	F value =H
0	Digital	Samsung	–
1	Digital	Samsung	GLOBALFOUNDRIES
Other columns and rows will be added in future revisions of this document, if needed.			

4.3.2 Daisy chain devices

The MSM8953 daisy chain ordering part number is TP-857NSP-1.

4.4 Device moisture sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. A package's moisture sensitivity level (MSL) indicates its ability to withstand exposure after it is removed from its shipment bag, while it is on the factory floor awaiting PCB installation. A low MSL rating is better than a high rating; a low MSL device can be exposed on the factory floor longer than a high MSL device. All pertinent MSL ratings are summarized in Table 4-6.

Table 4-6 MSL ratings summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤ 30°C/85% RH
2	1 year	≤ 30°C/60% RH
2a	4 weeks	≤ 30°C/60% RH
3	168 hours	≤ 30°C/60% RH; **MSM8953 rating**
4	72 hours	≤ 30°C/60% RH
5	48 hours	≤ 30°C/60% RH

Table 4-6 MSL ratings summary (cont.)

MSL	Out-of-bag floor life	Comments
5a	24 hours	≤ 30°C/60% RH
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.	≤ 30°C/60% RH

QTI follows the latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification. ***The MSM8953 devices are classified as MSL3; the qualification temperature was 255ºC.*** This qualification temperature (255°C) should not be confused with the peak temperature within the recommended solder reflow profile.

4.5 Thermal characteristics

Rather than provide thermal resistance values θ_{JC} and θ_{JA}, validated thermal package models are provided through the CreatePoint website. A thermal model for each device is provided within the *Power_Thermal* subfolder for each chipset family. Designers can extract thermal resistance values by conducting their own thermal simulations.

NOTE: Click the following links to download the MSM8953 thermal package models– *MSM8953 876 NSP Thermal Package Model Icepak* (HS11-P2472-5HW) and *MSM8953 876 NSP Thermal Package Model FloTHERM* (HS11-P2472-6HW) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-P2472-5HW

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/HS11-P2472-6HW

After successfully logging in, the documents are downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

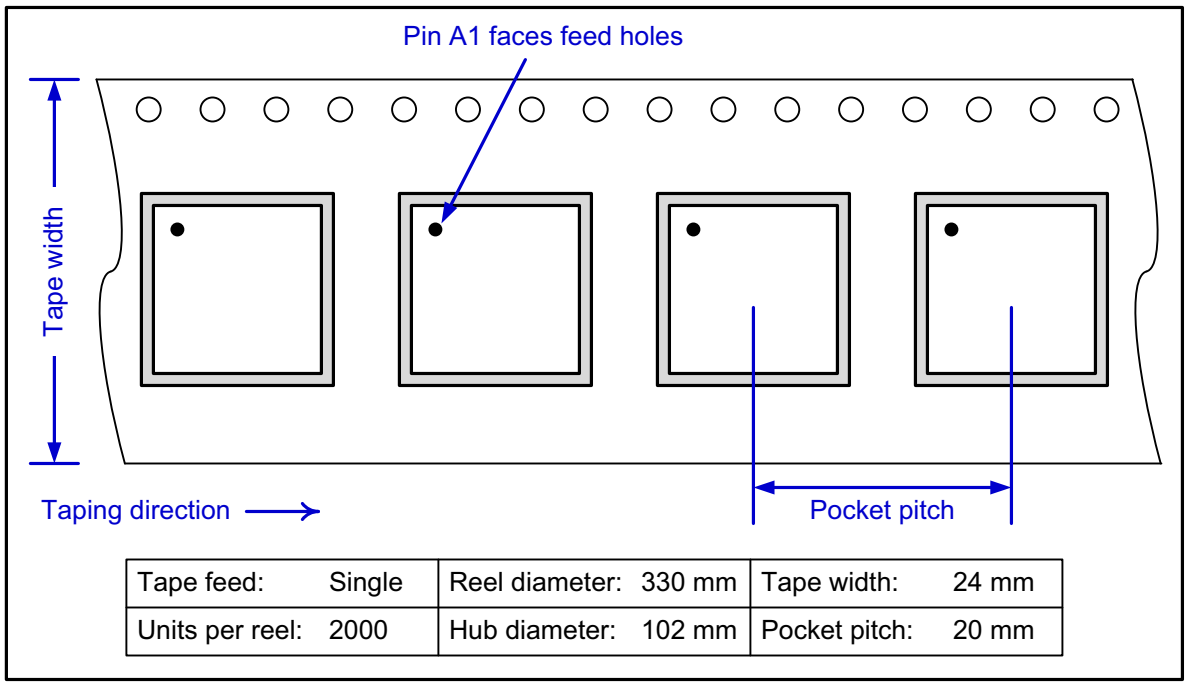
5 Carrier, storage, and handling information

5.1 Carrier

5.1.1 Tape and reel information

All QTI tape carrier systems conform to EIA-481 standards.

A simplified sketch of the MSM8953 tape carrier is shown in Figure 5-1, including the proper part orientation, maximum number of devices per reel, and key dimensions.



Tape feed:	Single	Reel diameter:	330 mm	Tape width:	24 mm
Units per reel:	2000	Hub diameter:	102 mm	Pocket pitch:	20 mm

Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in Figure 5-2.

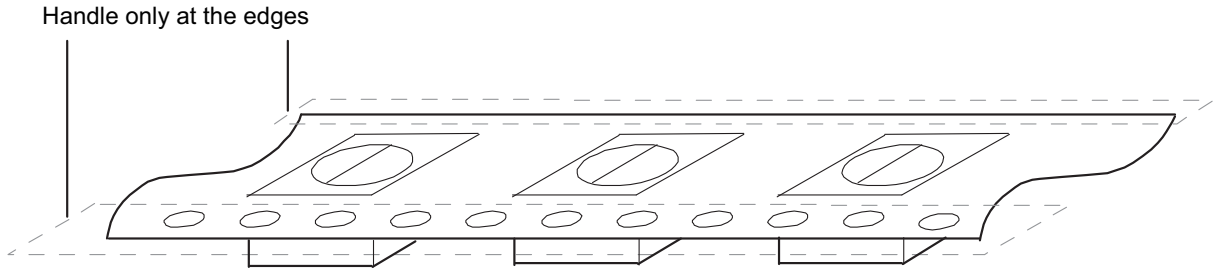


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

MSM8953 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *IC Products Packing Method* (80-VK055-1) for the expected shelf life.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB.

5.3 Handling

Tape handling was described in Section 5.1.1. Other (IC-specific) handling guidelines are presented in the following subsections.

5.3.1 Baking

It is **not necessary** to bake the MSM8953 if the conditions specified in Section 5.2.1 and Section 5.2.2 have **not been exceeded**.

It is **necessary** to bake the MSM8953 if any condition specified in Section 5.2.1 or Section 5.2.2 has **been exceeded**. The baking conditions are specified on the moisture-sensitive caution label attached to each bag; refer to the *IC Products Packing Method* (80-VK055-1) document for details.

CAUTION: If baking is required, the devices must be transferred into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QTI products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

5.4 Bar code label and packing for shipment

Refer to the *IC Products Packing Method* (80-VK055-1) document for all packing-related information, including bar code label details.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU RoHS directive. Its Sn/Ag/Cu solder balls use SAC125/Ni composition. A product material declaration (PMD) that provides RoHS and other product environmental governance information is published when the data is available.

6.2 SMT assembly guidelines

For recommendations on SMT process development, refer to the *SMT Assembly Guidelines* (SM80-P0982-1).

NOTE: Click the following link to download the *SMT Assembly Guidelines* (SM80-P0982-1) from the Qualcomm CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/SM80-P0982-1

After successfully logging in, the document is downloaded.

NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

6.3 Daisy chain components

Daisy chain packages use the same processes and materials as actual products; they are recommended for SMT characterization and board-level reliability testing. All SMT process recommendations described in Section 6.2 can be performed using daisy chain components.

Ordering information is given in Section 4.3.

Daisy chain PCB routing recommendations are available for download.

NOTE: Click the following link to download *Daisy Chain Interconnect, 857 NSP, 14.0 ×14.0 mm* (DS90-P2391-1) from the CreatePoint website.

https://createpoint.qti.qualcomm.com/search/contentdocument/stream/dcn/DS90-P2391-1

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NOTE: Make this document a favorite to be notified of any changes.

For more details on using CreatePoint, refer to the *Qualcomm CreatePoint User Guide* (80-NC193-2).

7 Part reliability

7.1 Reliability qualifications summary

Table 7-1 lists the MSM8953 reliability evaluation report for 857 NSP from Samsung.

Table 7-1 Silicon reliability results – Samsung

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	240	Passed DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	240	Passed FIT < 50 [1]
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	240	Passed MTTF > 20 [1]
ESD – human body model (HBM) rating JESD22-A114-F Target 1000 V[1] (Total samples from one wafer lot)	3	Passed 1000 V
ESD – charged device model (CDM) rating JESD22-C101-D Target 250 V (Total samples from one wafer lot)	3	Passed 250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA Temperature: 85°C (Total samples from one wafer lot)	6	Passed
Latch-up (V-supply over voltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{DD} maximum per the device specification Temperature: 85°C (Total samples from one wafer lot)	6	Passed

1. The cumulative DPPM, FIT, and MTTF is based on multiple products under the Samsung 14 nm LPP process.

Table 7-2 Package reliability results – Samsung

Tests, standards, and conditions	AST sample size	ATC sample size	SCK sample size	SPIL sample size	Results
Moisture resistance test (MRT): J-STD-020C Reflow at 260 +0/-5°C Total samples from three different assembly lots	693	693	693	693	Passed [1]
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	96	96	96	96	Passed [1]
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	231	231	Passed [1]
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	–	–	N/A (see note)
Physical dimensions: JESD22-B100-A (Total samples from three different assembly lots at each SAT)	30	30	30	30	Passed [1]
Die shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	15	15	15	15	Passed [1]

1. Data is leveraged from other previously qualified NSP packages that are similar to this configuration.

7.2 Reliability qualifications summary

Table 7-3 lists the MSM8953 reliability evaluation report for 857 NSP from GLOBALFOUNDRIES.

Table 7-3 Silicon reliability results – GLOBALFOUNDRIES

Tests, standards, and conditions	Sample size	Results
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	357	Passed DPPM < 1000 [1]
HTOL in FIT (λ) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	357	Passed FIT < 50 [1]
Mean time to failure (MTTF) t = 1/λ in million hours (Total samples from three different wafer lots)	357	Passed MTTF > 20 [1]
ESD – HBM rating JESD22-A114-F Target 1000 V (Total samples from one wafer lot)	3	Passed 1000 V
ESD – CDM rating JESD22-C101-D Target 250 V (Total samples from one wafer lot)[1]	3	Passed 250 V
Latch-up (I-test): EIA/JESD78A Trigger current: ±100 mA Temperature: 85°C[1] (Total samples from one wafer lot)	6	Passed
Latch-up (V-supply over voltage): EIA/JESD78A Trigger voltage: each VDD pin, stress at 1.5 × V_{DD} maximum per the device specification Temperature: 85°C (Total samples from one wafer lot)	6	Passed

1. The cumulative DPPM, FIT, and MTTF is based on multiple products under the GLOBALFOUNDRIES 14 nm LPP process.

Table 7-4 Package reliability results – GLOBALFOUNDRIES

Tests, standards, and conditions	AST sample size	ATC sample size	SCK sample size	SPIL sample size	Results
Moisture resistance test (MRT): J-STD-020C Reflow at 260 +0/-5°C Total samples from three different assembly lots	693	693	693	693	Passed [1]
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8 to 10 minutes Cycle rate: 2 cycles per hour (CPH) **Preconditioning:** JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Unbiased highly accelerated stress test: JESD22-A118 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	231	231	231	231	Passed [1]
Biased highly accelerated stress test: JESD22-A110 130°C/85% RH and 96 hour duration or 110°C/85% RH and 264 hour duration Preconditioning: JESD22-A113-F MSL 3, reflow temperature: 260°C+0/-5°C Total samples from three different assembly lots	96	96	96	96	Passed [1]
High-temperature storage life: JESD22-A103-C Temperature 150°C, 500, 1000 hours Total samples from three different assembly lots	231	231	231	231	Passed [1]
Flammability UL-STD-94 **Note**: Flammability test – not required QTI ICs are exempt from the flammability requirements due to their sizes per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QTI ICs mounted are rated V-0 (better than V-1).	–	–	–	–	N/A (see note)
Physical dimensions: JESD22-B100-A (Total samples from three different assembly lots at each SAT)	30	30	30	30	Passed [1]
Die shear MIL-STD-883E, Method 2019 (Total samples from three different assembly lots at each SAT)	15	15	15	15	Passed [1]
Solder ball shear: JESD22-B117 Total samples from three different assembly lots at each SAT	30	30	30	30	30
Internal/external visual Total samples from three different assembly lots at each SAT	75	75	75	75	75

1. Data is leveraged from other previously qualified NSP packages that are similar to this configuration.

7.3 Qualification sample description

Device characteristics

Device name:	MSM8953
Package type:	857 NSP
Package body size:	14 mm × 14 mm × 0.84 mm
Lead count:	857
Lead composition:	SAC125/Ni
Fab process:	14 nm FinFET
Fab sites:	Samsung, GLOBALFOUNDRIES
Assembly sites:	JCET STATS ChipPAC, Korea Amkor, China ASE, Taiwan SPIL, Taiwan
Solder ball pitch:	0.4 mm

8 Revision history

Revision	Date	Description
A	October 2015	Initial release
B	December 2015	■ Global: □ Updated the frequency from 2.0+ GHz to 2.0 GHz □ Updated the maximum height of the package dimension from 0.9 to 0.83 mm ■ Figure 1-1, MSM8953 functional block diagram and example application: Updated the block diagram ■ Table 1-1, MSM8953 features: □ Updated the secondary and tertiary CSI support from 13 MP and 8 MP to 24 MP respectively □ Updated the package dimension from 0.9 mm to 0.83 mm □ Updated DSDA feature to DSDS □ Updated noise cancellation technology support to Fluence 6.1 and Fluence Pro V2.2 ■ Table 2.2.1, Pin map: Provided CreatePoint link to MSM8953 pin assignment spreadsheet ■ Table 2-8, Pin descriptions: internal functions: Updated the functional description of a few GPIOs ■ Section 3.3, Power delivery network specification: Added PDN tables, Table 3-5, Power distribution network impedance vs. frequency and Table 3-6, VDD_P1 and VDD_EBI PDN specification ■ Section 4.1, Device physical dimensions: Updated CreatePoint link to the outline diagram ■ Added Section 4.2, Part marking and Section 4.3, Device ordering information ■ Added information in Chapter 4, Mechanical information and Chapter 5, Carrier, storage, and handling information
C	May 12, 2016	■ Global: □ Updated the maximum height of the package dimension from 0.83 mm to 0.84 mm □ Updated CreatePoint links throughout the document ■ Figure 1-1, MSM8953 functional block diagram and example application: Updated the block diagram

Revision	Date	Description
C (contd.)	May 12, 2016	■ Figure 2-2, MSM8953 pin assignments: □ Corrected pin AC5 pin name from MIPI_CSI0_LANE3_M to MIPI_CSI1_CLK_P □ Corrected pin J25 from VDDPX_CK to VDDPX_1 ■ Table 2-5, Pin descriptions: connectivity functions: Changed the BLSP order assignment for BLSP 1 to BLSP4 ■ Table 2-9, Pin descriptions: chipset interface functions: Updated the functional description for GPIO_81 and GPIO_82 under FM signals ■ Table 2-13, Pin descriptions: power-supply pins: □ Pad name for Pin J25 changed from VDDPX_CK to VDDPX_1 and moved to pad group 1 EBI pads □ Pad name changed for Pin AD40 ■ Chapter 3, Electrical specifications: Updated with electrical specifications, review in entirety ■ Table 4-1, MSM8953 marking line definitions: Corrected the assembly site information ■ Figure 4-3, Device identification code: Added the device identification figure ■ Table 4-3, Device identification details: Updated the ES2/CS sample information ■ Table 4-4, Date code information for MSM8953 devices: Added table with date code information ■ Chapter 7, Part reliability: Added MSM8953 reliability information
D	May 24, 2016	■ Global: □ Corrected pin name from VDD_USBPHY_3P3 to VDD_USB_HS1_3P1 and VDDA_DSI_CSI to VDD_DSI_CSI □ Added the lead composition information as SAC125/Ni □ Corrected document to remove Hexagon vector processor HVX-512 support ■ Table 2-4, Pin descriptions: multimedia functions: Pad rails updated for Camera-timing and CCI signals, and SDE vertical sync ■ Table 2-5, Pin descriptions: connectivity functions: Pad rails updated for USB and SDC1 interfaces ■ Table 2-11, Pin descriptions: general-purpose input/output ports: Updated the functional description for GPIO_81 and GPIO_82 ■ Table 2-14, Pin descriptions: ground pins: Added pin BB38 ■ Chapter 6, PCB mounting guidelines: □ Updated chapter as per latest device specification template □ Added the CreatePoint link to the Daisy chain PCB routing recommendation document
E	June 20, 2016	Table 7-1, Silicon reliability results – Samsung: Updated the TBDs with the result

Revision	Date	Description
F	June 27, 2016	■ Global: Updated the document to add the MSM8953 2.2 GHz SKU ■ Table 2-4, Pin descriptions: multimedia functions: Corrected the pin direction for the camera interface ■ Chapter 3, Electrical specifications: Added a note on the MSM8953 2.2 GHz parts ■ Section 3.3, Power delivery network (PDN) specification: Added a note on the MSM8953 2.2 GHz parts ■ Table 4-3, Device identification details: Updated to add two new SKUs with feature code AC
G	August 2016	■ Global: □ Changed all instances of EBI1 to EBI0 □ Updated pad names to match the reference schematic □ Updated the document to add CS information for the MSM8953 2.2 GHz parts □ Removed PCM references in Audio section □ Removed UICC references □ Updated the version of Bluetooth supported ■ Figure 1-1, <Product_Name> functional block diagram and example application: □ Removed QPA4351 from the list of front end components □ Updated WCD9326 and WSA8810/WSA8815 interface connection ■ Table 2-1, I/O description (pad type) parameters: Corrected description of pad group 7 to 1.8 V ■ Table 2-5, Pin descriptions: connectivity functions: □ Corrected the functional description for four pins under SDC2 interface □ Corrected pad names for the six pins under Audio codec interface and added rows for pads CDC_PDM_RX1_DRE and CDC_PDM_RX0_DRE □ Added pins E47 and G43 for MI2S_1_D2 and MI2_1_D3 □ Updated table subheading from Configurable I/O to BAM based low speed peripheral interface 3–BLSP 3 for the BLSP3 pins ■ Table 2-8, Pin descriptions: internal functions: □ Corrected functional description of pins BE9, AY46, BF6, L45, BB44, AH46, AE45, AE43, AE47, AF46, AG47, AH46, AT42, D46, and G45 to general-purpose wake interrupt □ Updated functional description of pins SDC1_DATA_3, SDC1_DATA_3, SDC2_DATA_1, and SDC2_DATA_3 ■ Table 2-11, Pin descriptions: general-purpose input/output ports: □ Corrected the bit numbers in the functional description □ Updated the configurable function for GPIO_67 and GPIO_68 □ Added configurable function MI2S_1_D2 and MI2S_1_D3 for GPIO_94 and GPIO_95 respectively

Revision	Date	Description
G (contd.)		■ Table 3-2, Operating conditions: Updated the max value for VDD_WLAN from 1.33.V to 1.377 V ■ Section 3.3, Power delivery network (PDN) specification: Updated the note with reference to the design guidelines document ■ Table 3-7, VDDPX_1 and VDD_EBI PDN specification: □ Updated the column heading of maximum impedance from DC to 10 Hz to DCR □ Added a footnote on PDN specification at 1 MHz ■ Table 3-8, Dhrystone and rock bottom maximum power for MSM8953 devices: □ Updated the column heading to octa core Dhrystone □ Updated table footnote to latest template ■ Table 3-9, Digital I/O characteristics for VDDPX_1 (1.2 V): Added table ■ Table 3-10, DC specification of VDDPX_3 = 1.8 V GPIOs: Updated description for IIH , IIL ,IOZH, and IOZL parameters. ■ Table 3-12, Digital I/O characteristics for VDDPX_2 = 2.95 V nominal (SDC2): Updated description for IIH , IIL , IOZH, and IOZL parameters. ■ Table 3-13, Digital I/O characteristics for VDDPX_2 = 1.8 V nominal (SDC2): Updated description for IIH , IIL , IOZH, and IOZL parameters. ■ Table 3-14, Digital I/O characteristics for VDDPX_2 = 1.8 V nominal (SDC2): Updated description for IIH , IIL , IOZH, and IOZL parameters. ■ Table 3-15, Digital I/O characteristics for VDDPX_X = 1.8 V nominal (UIM1 and UIM2 – Class B): Updated description for IIH , IIL , IOZH, and IOZL parameters. ■ Table 3-20, Supported USB standards and exceptions: Removed UTMI + ULTI specification from applicable standards ■ Table 4-3, Device identification details: Added CS information for the MSM8953 2.2 GHz parts ■ Table 4-4, Date code information for <Product_Name> devices: Added the date code for MSM8953 2.2 GHz CS samples ■ Section 4.3.2, Daisy chain devices: Added section ■ Section 4.4, Device moisture sensitivity level: Added section ■ Section 4.5, Thermal characteristics: Added section ■ Figure 5-1, Carrier tape drawing with part orientation: Updated pocket pitch and hub diameter
H	September 2016	■ Table 1-1, MSM8953 features: Updated the audio interface section in the features ■ Table 3-8, Dhrystone and rock bottom maximum power for MSM8953 devices: Updated the Dhrystone and rock bottom values for the 2.2 GHz parts ■ Table 3-10, DC specification of VDDPX_3 = 1.8 V GPIOs: The DC specification for 1.8 V GPIO is updated for Pull-up and Pull-down resistors
Revision I was omitted in accordance with QTI document conventions.		

Revision	Date	Description
J	January 2017	■ Table 2-9 Pin descriptions: multimedia functions: Updated the descriptions of CAM_MCLK0, CAM_MCLK1, and (8888) CAM_MCLK2 ■ Table 3-9 Digital I/O characteristics for VDDPX_1 (1.2 V): Updated the description and the value for VIH and VIL ■ Table 3-10 DC specification of VDDPX_3 = 1.8 V GPIOs: Added the pull-up, pull-down, keeper-up, and keeper-down resistance information for the RFFE pins ■ Table 3-11 Digital I/O characteristics for VDDPX_7 = 1.8 V nominal (SDC1): Added a description for each parameter in this table ■ Table 4-1 MSM8953 marking line definitions: Updated the foundry code for GLOBALFOUNDRIES ■ Table 4-3 Device identification details: Updated the source code information ■ Table 4-4 Date code information for MSM8953 devices: Updated the source code for GLOBALFOUNDRIES ■ Section 7.2 Reliability qualifications summary: Added the reliability data for GLOBALFOUNDRIES ■ Section 7.3 Qualification sample description: Added the fab site for GLOBALFOUNDRIES
K	July 2017	■ Table 2-11 Pin descriptions: general-purpose input/output ports: Changed the pad type to B-PD:nppukp for various GPIO pad numbers
L	March 2018	Global: Removed all the FHD values across the document
M	May 2018	■ Updated the block diagram to support PMI632 ■ Updated the GNSS support
N	September 2018	■ Figure 3-11 I2S timing diagram: Updated the 1^2S timing diagram ■ Table 3-24 I2S interface timing: □ Added a new column to show the x% of T □ Updated the max value of t(dtr) SD and WS output delay
Rev O is omitted as per QTI guidelines		
P	October 2018	■ Section 1.1 Functional block diagram: Updated the notes

For additional information or to submit technical questions, go to https://createpoint.qti.qualcomm.com

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