极景微半导体

LVDS 1:10 Ultra-Low Additive Jitter Differential Clock Buffer

US5D210
Datasheet

Description

The US5D210 is a 2.1-Ghz,10-output differential high-performance clock fanout buffer.

The fanout from a differential input to ten LVDS outputs reduces loading on the preceding driver and provides an efficient clock distribution network. TheUS5D210 can act as a translator from a differential HSTL, eHSTL, LVEPECL (2.5V), LVPECL (3.3V), CML, or LVDS input to LVDS outputs. A single-ended 3.3V / 2.5V LVTTL input can also be used to translate to LVDS outputs. The redundant input capability allows for an asynchronous change-over from a primary clock source to a secondary clock source. Selectable reference inputs are controlled by SEL.

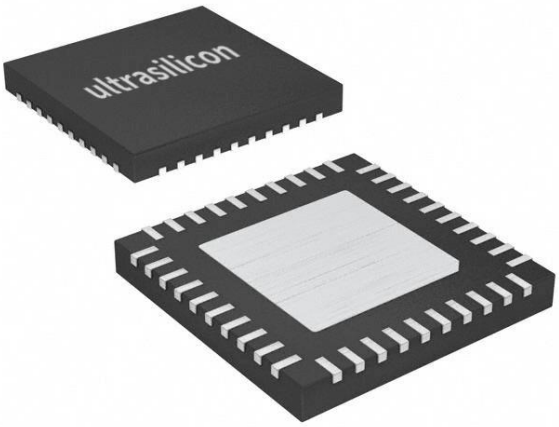
The US5D210 outputs can be asynchronously enabled/disabled. When disabled, the outputs will drive to the value selected by the GL pin. Multiple power and grounds reduce noise.

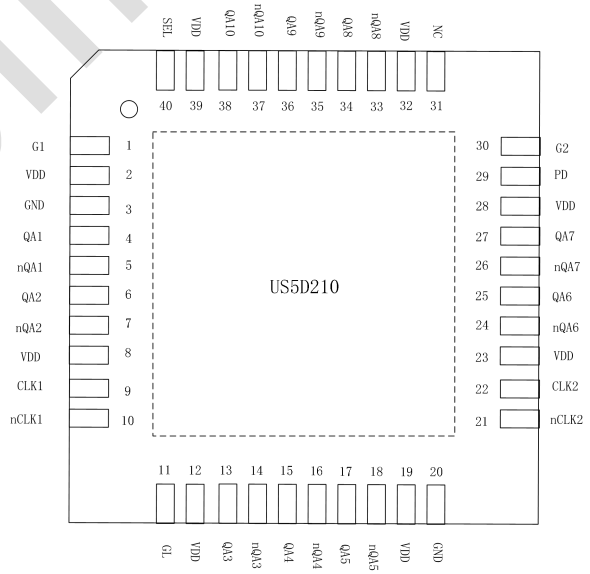
Features

- Two differential reference clock input pairs
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL, HSTL or Single Ended
- Ten LVDS outputs
- Maximum Output Frequency up to 2.1GHz
- Output skew: 20ps (typical)
- Part-to-part skew: 200ps (typical)
- Additive RMS phase jitter @ 156.25MHz:
  12.5 fs RMS (10kHz - 1 MHz), typical @ 3.3V/ 3.3V
  50.5 fs RMS (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Power-down mode
- Supply voltage: 3.3V, 2.5V
- Industrial Temperature Range:-40°C to 85°C
- Pin-to-Pin Compatible to the 5T9310
- Available in a 40-pin, 6mm*6mm WQFN package

Applications

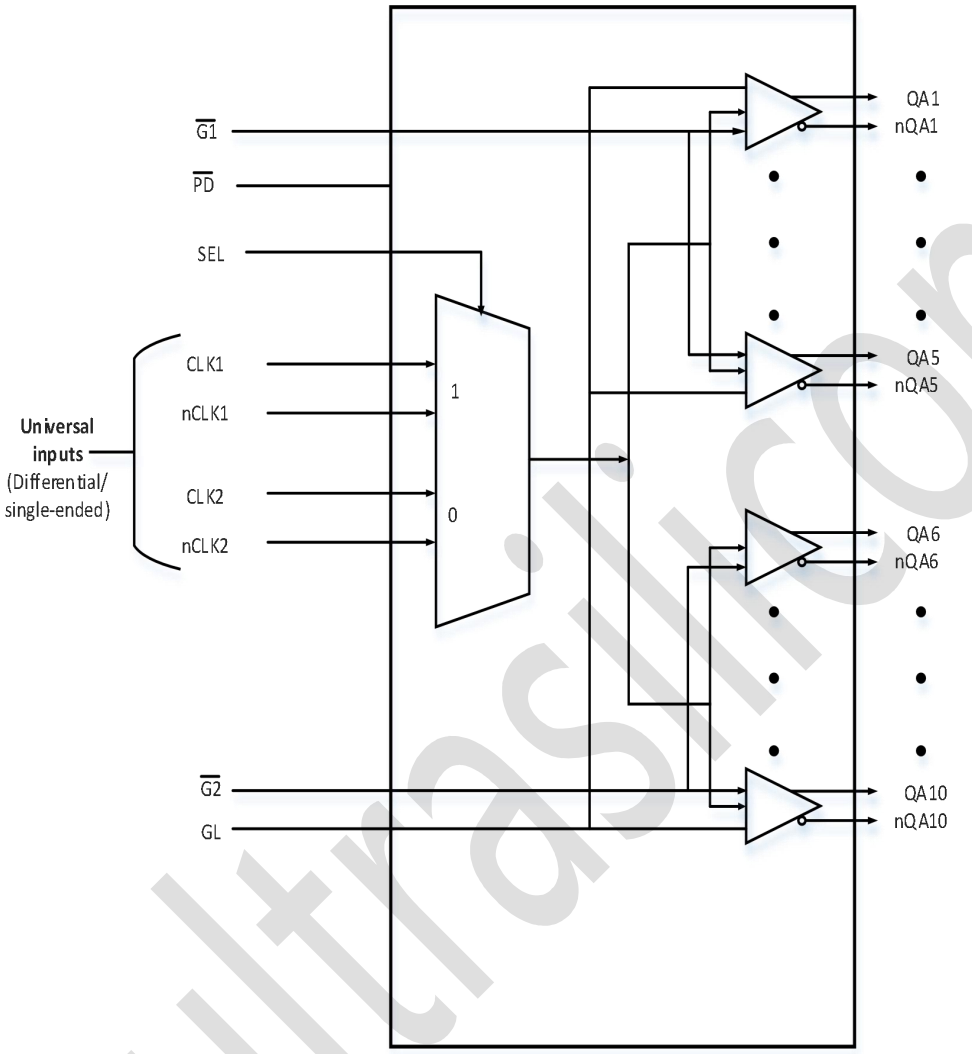
- Clock distribution





E-mail: sales@ultrasilicon.com.cn

Block Diagram

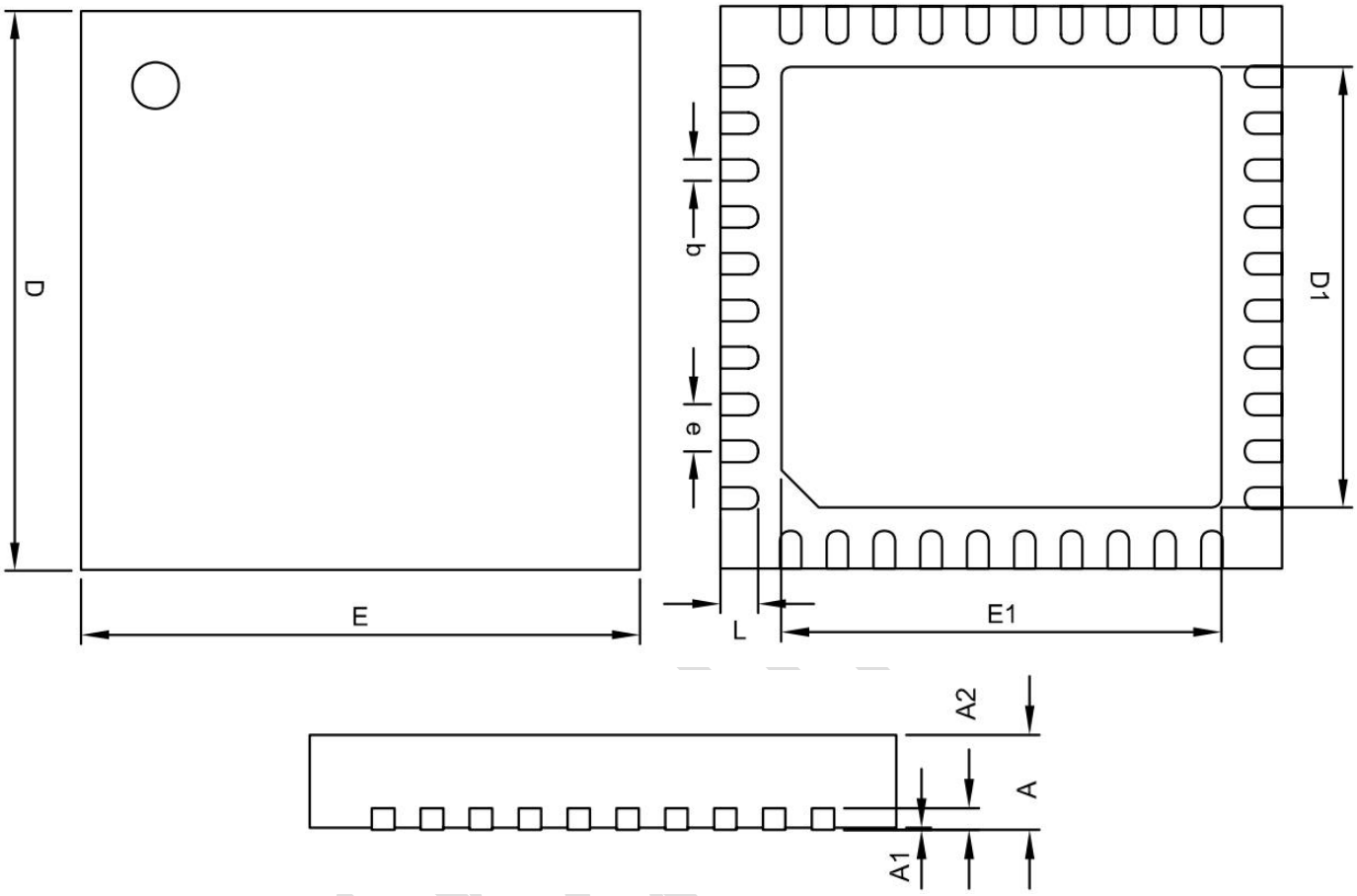


Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions[1]

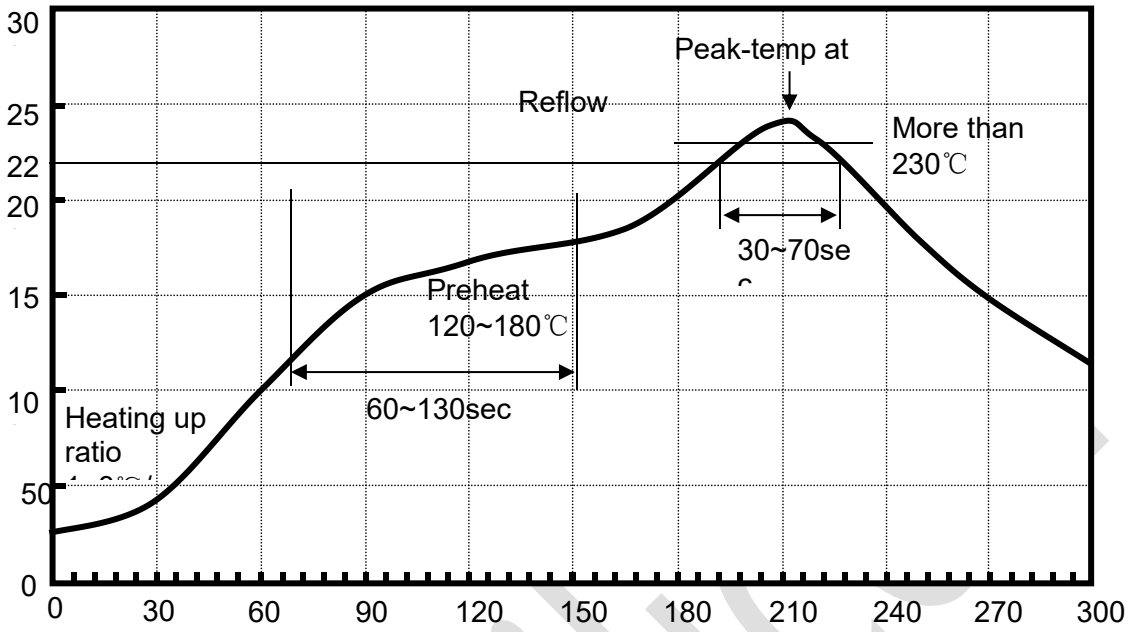
Number	Type		Description
CLK[1:2]	Input	Adjustable	Clock input. CLK[1:2] is the "true" side of the differential clock input.
nCLK[1:2]	Input	Adjustable	Complementary clock inputs. nCLK[1:2] is the complementary side of CLK[1:2]. For LVTTL single-ended operation, n[1:2] should be set to the desired toggle voltage for CLK[1:2]: 3.3V LVTTL VREF = 1650mV 2.5V LVTTL VREF = 1250mV
$\overline{G}$1	Input		Gate control for differential outputs QA1 and nQA1 through QA5 and nQA5. When $\overline{G}$1 is LOW, the differential outputs are active. When $\overline{G}$1 is HIGH, the differential outputs are asynchronously driven to the level designated by GL.
$\overline{G}$2	Input		Gate control for differential outputs QA6 and nQA6 through QA10 and nQA10. When $\overline{G}$2 is LOW, the differential outputs are active. When $\overline{G}$2 is HIGH, the differential outputs are asynchronously driven to the level designated by GL.
GL	Input		Specifies output disable level. If HIGH, "true" outputs disable HIGH and "complementary" outputs disable LOW. If LOW, "true" outputs disable LOW and "complementary" outputs disable HIGH.
QA[1:10]	Output	LVDS	Clock outputs.
nQA[1:10]	Output	LVDS	Complementary clock outputs.
SEL	Input		Reference clock select. When LOW, selects CLK2 and nCLK2. When HIGH, selects CLK1 and nCLK1.
$\overline{P}$D	Input		Power-down control. Shuts off entire chip. If LOW, the device goes into low power mode. Inputs and outputs are disabled. Both "true" and "complementary" outputs will pull to VDD. Set HIGH for normal operation.
VDD	Power		Power supply for the device core and inputs.
GND	Power		Power supply return for all power.
NC	Output		No connect

PACKAGE DIMENSIONS



Symble	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.00	- - -	0.05	0.0000	- - -	0.0020
A2	0.19	0.20	0.21	0.0075	0.0079	0.0083
D	5.95	6.00	6.05	0.2343	0.2362	0.2382
E	5.95	6.00	6.05	0.2343	0.2362	0.2382
D1	4.55	4.65	4.75	0.1791	0.1831	0.1870
E1	4.55	4.65	4.75	0.1791	0.1831	0.1870
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
e	0.50 BSC			0.0197 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177

Reflow profile



Recommended Temperature Sn95.5Ag4.0Cu0.5