Ultra-Low Quiescent (ULQ™) Dual Synchronous Step-Down Controller with 5V and 3.3V LDOs

Check for Samples: TPS51285A, TPS51285B

FEATURES

- **Input Voltage Range: 5 V to 24 V**
- **Output Voltages: 5 V and 3.3 V (Adjustable Range ±10%)**
- **Built-in, 100-mA, 5-V and 3.3-V LDOs**
- **Clock Output for Charge-Pump**
- **±1% Reference Accuracy**
- **Adaptive On-Time D-CAP™ Mode Control Architecture with 400 kHz (CH1) and 475 kHz (CH2) Frequency**
- **Auto-skip and ULQ™ modes for long battery life in system stand-by mode**
- **Internal 0.8-ms Voltage Servo Soft-Start**
- **Low-Side $R_{DS(on)}$ Current Sensing Scheme**
- **Built-In Output Discharge Function**
- **Separate Enable Input for Switchers**
- **Dedicated OC Setting Terminals**
- **Power Good Indicator**
- **OVP, UVP and OCP Protection**
- **Non-Latch UVLO and OTP Protection**
- **20-Pin, 3 mm x 3 mm, QFN (RUK)**

APPLICATIONS

- **Notebook Computers**
- **Tablet Computers**

DESCRIPTION

The TPS51285A and TPS51285B are cost-effective, dual synchronous buck controllers with 5-V and 3.3-V LDOs, targeted for notebook system-power supply solutions. The device achieves low power consumption by the use of auto-skip and ULQ™ modes, which is beneficial for long battery life in system stand-by mode. The 256-kHz VCLK output is provided to drive an external charge pump, generating gate drive voltage for the load switches with minimum power consumption in the main converter. The device employs adaptive on-time D-CAP™ mode control which enables fast load transient response without external compensation network. The TPS51285A/B operates with supply input voltage ranging from 5V to 24V and supports output voltages of 5 V and 3.3 V. The TPS51285A and TPS51285B are available in a 20-pin 3 x 3 (mm) QFN package and is specified from -40°C to 85°C.

ORDERING INFORMATION(1)

ORDERABLE DEVICE NUMBER	ALWAYS On-LDO	OUTPUT SUPPLY	QUANTITY
TPS51285ARUKR	VREG3	Tape and Reel	3000
TPS51285ARUKT		Mini reel	250
TPS51285BRUKR	VREG3 and VREG5	Tape and Reel	3000
TPS51285BRUKT		Mini reel	250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

D-CAP, ULQ are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION DIAGRAMS

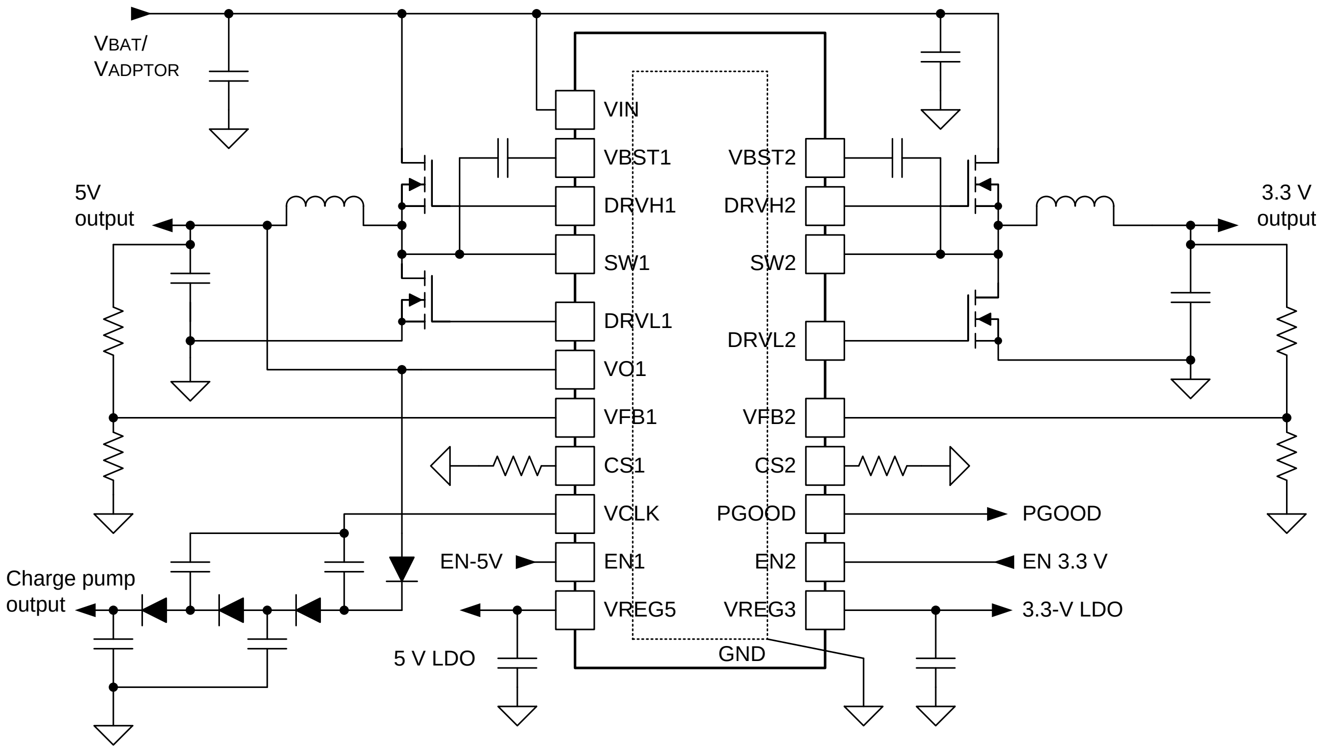


Figure 1. TYPICAL APPLICATION DIAGRAM (With Charge Pump)

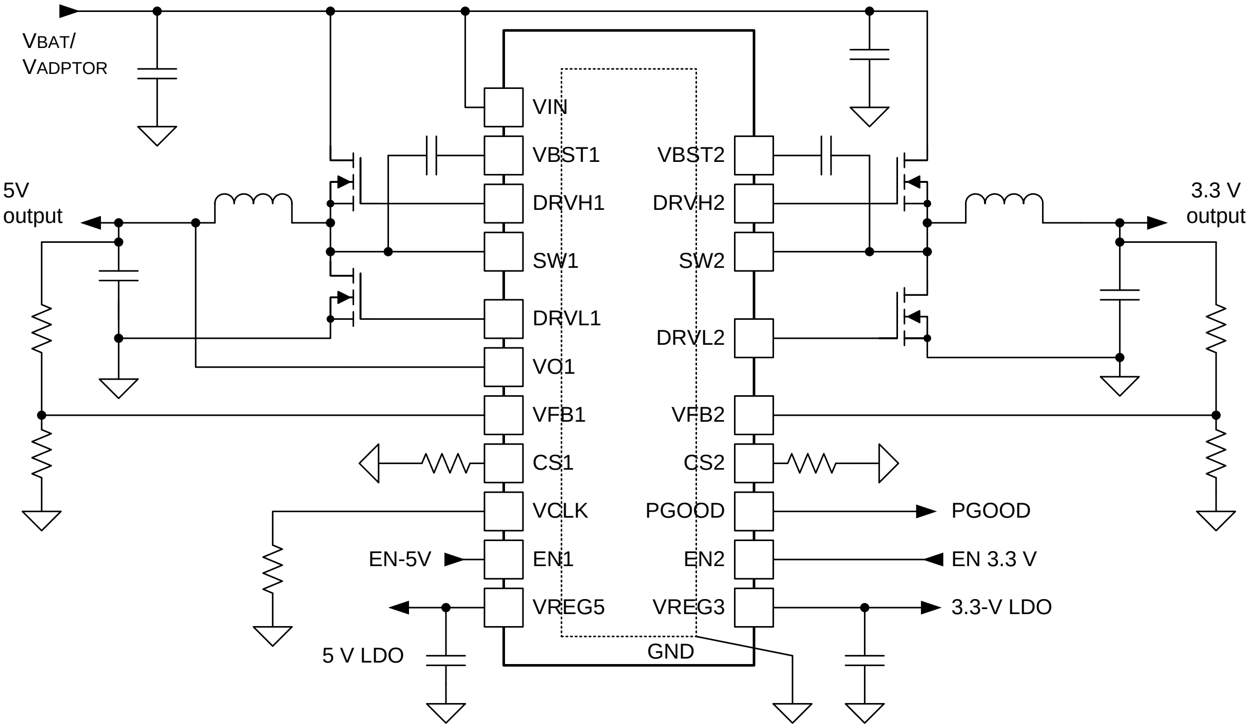


Figure 2. TYPICAL APPLICATION DIAGRAM (Without Charge Pump)

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Input voltage(2)	VBST1, VBST2	–0.3	32	V
	VBST1, VBST2(3)	–0.3	6	
	SW1, SW2	–6	26	
	VIN	–0.3	26	
	EN1, EN2	–0.3	6	
	VFB1, VFB2	–0.3	3.6	
	VO1	–0.3	6	
Output voltage(2)	DRVH1, DRVH2	–6.0	32	V
	DRVH1, DRVH2(3)	–0.3	6	
	DRVH1, DRVH2(3) (duty cycle < 1%)	–2.5	6	
	DRVL1, DRVL2	–0.3	6	
	DRVL1, DRVL2 (duty cycle < 1%)	–2.5	6	
	PGOOD, VCLK, VREG5	–0.3	6	
	VREG3, CS1, CS2	–0.3	3.6	
Electrostatic discharge (ESD) ratings (4)	Human Boby Model (HBM)		2	kV
	Charged Device Model (CDM)		0.5	
Junction temperature, T_J			150	°C
Storage temperature, T_{ST}		–55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted
(3) Voltage values are with respect to SW terminals.
(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51285A TPS51285B	UNITS
		20-PIN RUK	
θ_{JA}	Junction-to-ambient thermal resistance	46.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.6	
θ_{JB}	Junction-to-board thermal resistance	19.2	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	19.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.6	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Supply voltage	VIN	5		24	V
Input voltage(1)	VBST1, VBST2	–0.1		30	
	VBST1, VBST2(2)	–0.1		5.5	
	SW1, SW2	–5.5		24	
	EN1, EN2	–0.1		5.5	
	VFB1, VFB2	–0.1		3.5	
	VO1	–0.1		5.5	
Output voltage(1)	DRVH1, DRVH2	–5.5		30	V
	DRVH1, DRVH2(2)	–0.1		5.5	
	DRVL1, DRVL2	–0.1		5.5	
	PGOOD, VCLK, VREG5	–0.1		5.5	
	VREG3, CS1, CS2	–0.1		3.5	
Operating free-air temperature, T_A		–40		85	°C

(1) All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) Voltage values are with respect to the SW terminal.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{VIN} = 12 V, V_{VO1} = 5 V, V_{VFB1} = V_{VFB2} = 2 V, V_{EN1} = V_{EN2} = 3.3 V, VCLK: 200 Ω to GND
(unless otherwise noted)

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VIN1}	VIN supply current-1		T_A = 25°C, No load, V_{VO1} = 0 V, V_{VFB1} = V_{VFB2} = 2.06V		84		μA
I_{VIN2}	VIN supply current-2		T_A = 25°C, No load, V_{VFB1} = V_{VFB2} = 2.06 V		10		μA
I_{VO1}	VO1 supply current		T_A = 25°C, No load, V_{VFB1} = V_{VFB2} = 2.06 V		70		μA
$I_{VIN(STBY)}$	VIN stand-by current	TPS51285A	T_A = 25°C, No load, V_{VO1} = 0 V, V_{EN1}= V_{EN2}= 0 V		25		μA
		TPS51285B			28		
INTERNAL REFERENCE							
V_{FBx}	VFB regulation voltage		T_A = 25°C	1.99	2	2.01	V
				1.98	2	2.02	V
I_{FBx}	VFB Leakage Current		T_A = 25°C			0.1	μA
VREG5 OUTPUT							
V_{VREG5}	VREG5 output voltage		T_A = 25°C, No load, V_{VO1} = 0 V	4.9	5	5.1	V
			V_{VIN} > 7 V , V_{VO1}= 0 V, I_{VREG5} < 100 mA	4.85	5	5.1	
			V_{VIN} > 5.5 V , V_{VO1}= 0 V, I_{VREG5} < 35 mA	4.85	5	5.1	
			V_{VIN} > 5 V, V_{VO1}= 0 V, I_{VREG5} < 20 mA	4.55	4.75	5.1	
I_{VREG5}	VREG5 current limit		V_{VO1} = 0 V, V_{VREG5}= 4.5 V, V_{VIN} = 7 V	100	140		mA
R_{V5SW}	5-V switch resistance		T_A = 25°C, V_{VO1}= 5 V, I_{VREG5}= 50 mA		1.8		Ω
VREG3 OUTPUT							
V_{VREG3}	VREG3 output voltage		V_{VIN} > 7 V , V_{VO1}= 0 V, I_{VREG3} < 100 mA	3.217	3.3	3.383	V
			V_{VIN} > 5.5 V , V_{VO1}= 0 V, I_{VREG3} < 35 mA	3.234	3.3	3.366	
			0°C ≤ T_A ≤ 85°C, V_{VIN} > 5.5 V, V_{VO1}= 0 V, I_{VREG3} < 35 mA	3.267	3.3	3.333	
			0°C ≤ T_A ≤ 85°C, V_{VIN} > 5.5 V, I_{VREG3}< 35 mA	3.267	3.3	3.333	
			V_{VIN} > 5 V , V_{VO1}= 0 V, I_{VREG3} < 35 mA	3.217	3.3	3.366	
$I_{VREG3-1}$	VREG3 current limit-1		V_{VO1} = 0 V, V_{VREG3}= 3.15 V, V_{VIN}= 7 V	100	200		mA
$I_{VREG3-2}$	VREG3 current limit-2		V_{VREG3} = 3.15 V, V_{VIN}= 7 V	100	200		
DUTY CYCLE and FREQUENCY CONTROL							
f_{sw1}	CH1 frequency(1)		T_A = 25°C, V_{VIN}= 20 V		400		kHz
f_{SW2}	CH2 frequency(1)		T_A = 25°C, V_{VIN}= 20 V		475		kHz
$t_{OFF(MIN)}$	Minimum off-time		T_A = 25°C	200	300	400	ns
MOSFET DRIVERS							
R_{DRVH}	DRVH resistance		Source, I_{DRVH} = –50 mA, (V_{VBST} – V_{SW}) = 5 V		3		Ω
			Sink, I_{DRVH} = 50 mA, (V_{VBST} – V_{SW}) = 5 V		1.9		
R_{DRVL}	DRVL resistance		Source, I_{DRVL} = –50 mA, V_{VREG5} = 5 V		3		Ω
			Sink, I_{DRVL} = 50 mA, V_{VREG5}= 5 V		0.9		
t_D	Dead time		DRVH-off to DRVL-on		12		ns
			DRVL-off to DRVH-on		20		
INTERNAL BOOT STRAP SWITCH							
$R_{VBST\ (ON)}$	Boost switch on-resistance		T_A = 25°C, I_{VBST} = 10 mA		13		Ω
I_{VBSTLK}	VBST leakage current		T_A = 25°C			1	μA
CLOCK OUTPUT							
R_{VCLK}	VCLK on-resistance (pull-up)		T_A = 25°C, VCLK: Open		10		Ω
	VCLK on-resistance (pull-down)		T_A = 25°C, VCLK: Open		10		
f_{CLK}	Clock frequency		T_A = 25°C, VCLK: Open		256		kHz

(1) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

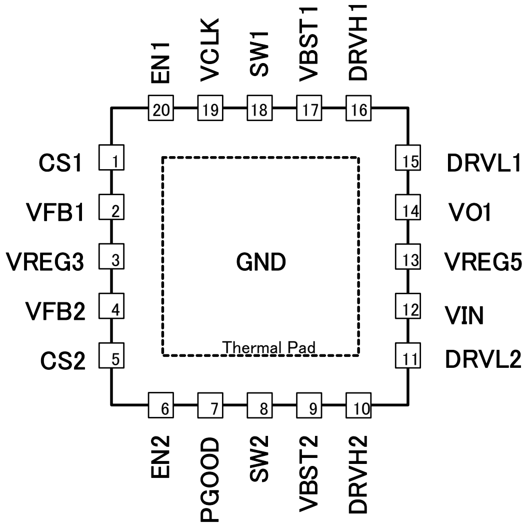
over operating free-air temperature range, V_{VIN} = 12 V, V_{VO1} = 5 V, V_{VFB1} = V_{VFB2} = 2 V, V_{EN1} = V_{EN2} = 3.3 V, VCLK: 200 Ω to GND
(unless otherwise noted)

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
OUTPUT DISCHARGE							
R_{DIS1}	CH1 discharge resistance		T_A = 25°C, V_{VO1} = 0.5 V V_{EN1} = V_{EN2} = 0 V		35		Ω
R_{DIS2}	CH2 discharge resistance	TPS51285A	T_A = 25°C, V_{SW2} = 0.5 V, V_{EN1} = V_{EN2} = 0 V		75		Ω
		TPS51285B			70		
SOFT START							
t_{SS}	Soft-start time (From ENx Hi)		From ENx="Hi" and V_{VREG5} > V_{UVLO5} to V_{OUT} = 95%		0.91		ms
t_{SSRAMP}	Soft-start time (ramp-up)		V_{OUT}= 0% to V_{OUT} = 95%, V_{VREG5} = 5 V		0.78		ms
POWER GOOD							
t_{PGDEL}	PG start-up delay		From EN1 = "Hi", EN2 = "Hi", and V_{VREG5} > V_{UVLO5}		1.65		ms
V_{PGTH}	PG threshold		PGOOD in from lower (start-up)	87.5%	90%	92.5%	
I_{PGMAX}	PG sink current		V_{PGOOD} = 0.5 V		6.5		mA
I_{PGLK}	PG leak current		V_{PGOOD} = 5.5 V			1	µA
CURRENT SENSING							
I_{CS}	CS source current		T_A = 25°C, V_{CS} = 0.4 V	45	50	55	µA
TC_{CS}	CS current temperature coefficient (2)		On the basis of 25°C		4500		ppm/°C
V_{CS}	CS Current limit setting range			0.2		2	V
V_{AZCADJ}	Adaptive zero cross adjustable range		Positive	5	10		mV
			Negative		–10	–5	
LOGIC THRESHOLD							
$V_{ENX(ON)}$	EN threshold high-level		SMPS on level			1.6	V
$V_{ENX(OFF)}$	EN threshold low-level		SMPS off level	0.3			V
I_{EN}	EN input current		V_{ENx}= 3.3 V			1	µA
OUTPUT OVERVOLTAGE PROTECTION							
V_{OVP}	OVP trip threshold			112.5%	115%	117.5%	
t_{OVPDLY}	OVP propagation delay		T_A = 25°C		0.5		µs
OUTPUT UNDERVOLTAGE PROTECTION							
V_{UVP}	UVP trip Threshold			55%	60%	65%	
$V_{UVP\text{-}ST}$	UVP trip Threshold		Start Up	87.5%	90%	92.5%	
t_{UVPDLY}	UVP prop delay				250		µs
$t_{UVPENDLY}$	UVP enable delay		From ENx ="Hi", V_{VREG5} = 5V		1.1		ms
UVLO							
$V_{UVL0VIN}$	VIN UVLO Threshold		Wake up	4.2	4.58	4.95	V
			Shutdown	3.75	4.1	4.45	V
V_{UVLO5}	VREG5 UVLO Threshold		Wake up	4.08	4.38	4.55	V
			Shutdown	3.7	4	4.3	V
V_{UVLO3}	VREG3 UVLO Threshold		Wake up	3	3.15	3.26	V
			Shutdown	2.75	3	3.21	V

(2) Specified by design. Not production tested.

DEVICE INFORMATION

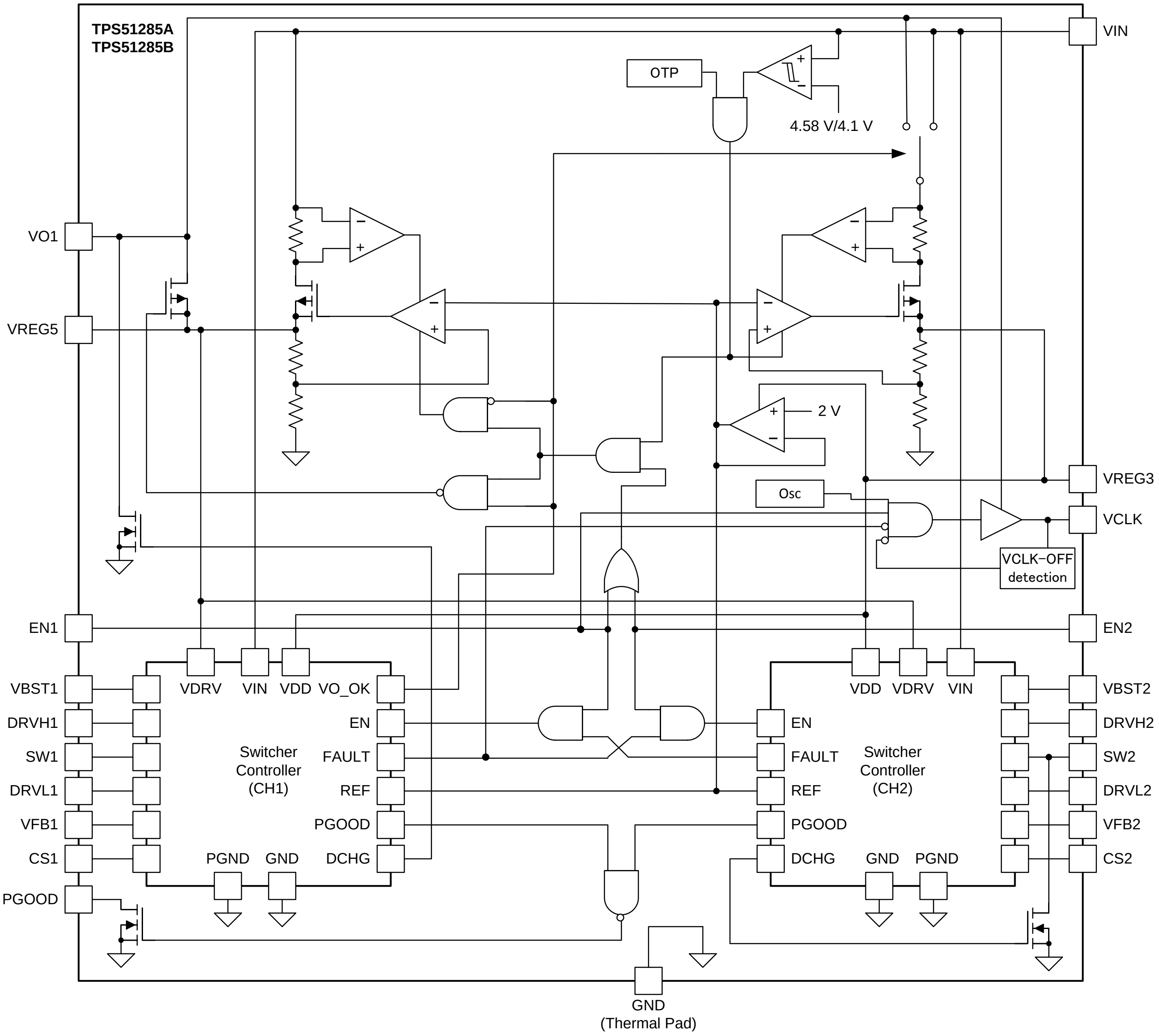
RUK PACKAGE
20 PINS
(TOP VIEW)



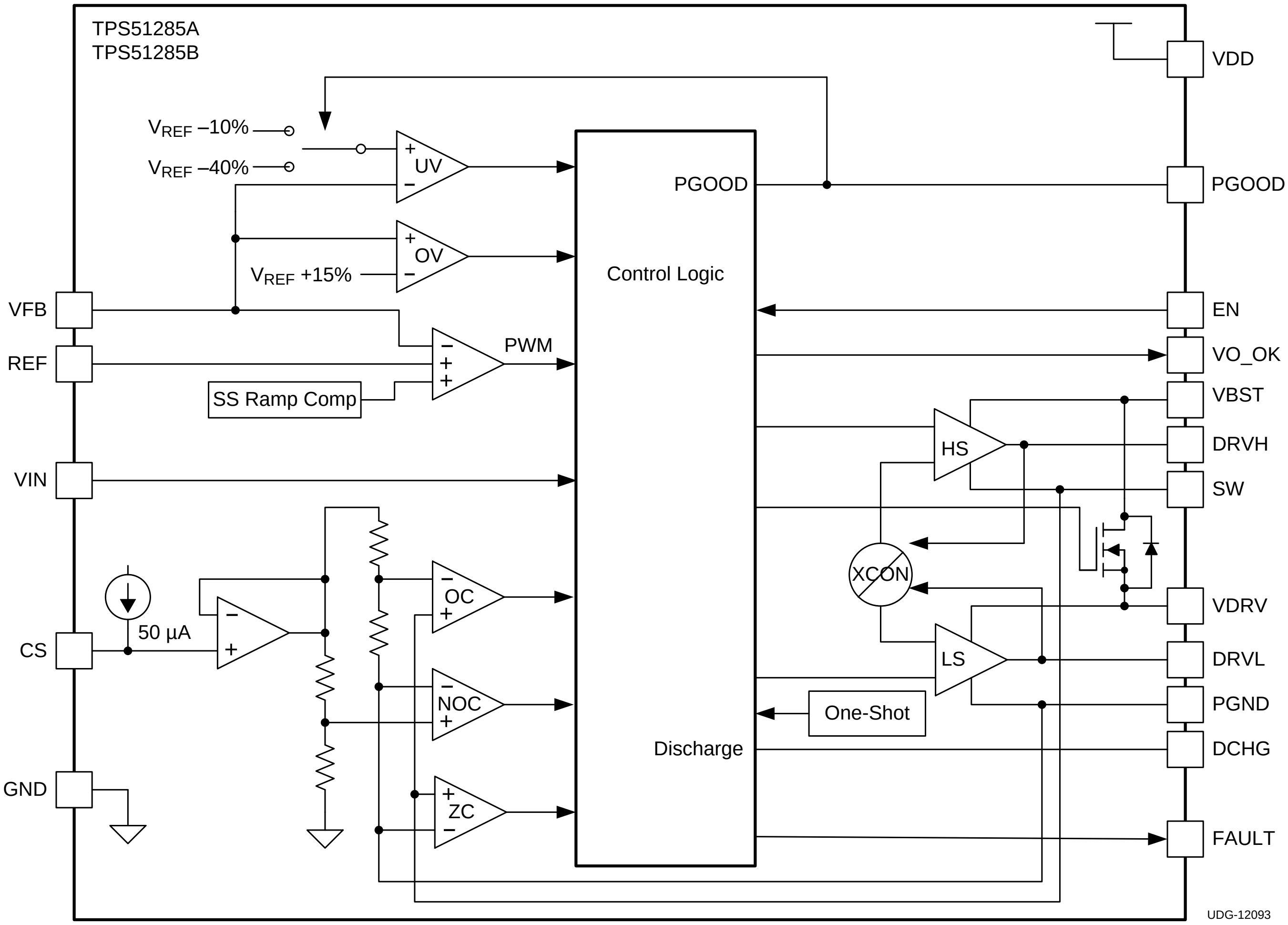
PIN FUNCTIONS

NAME	PIN NO.	I/O	DESCRIPTION
CS1	1	O	Sets the channel 1 OCL trip level.
CS2	5	O	Sets the channel 2OCL trip level.
DRVH1	16	O	High-side driver output
DRVH2	10	O	High-side driver output
DRVL1	15	O	Low-side driver output
DRVL2	11	O	Low-side driver output
EN1	20	I	Channel 1 enable.
EN2	6	I	Channel 2 enable.
PGOOD	7	O	Power good output flag. Open drain output. Pull up to external rail via a resistor
SW1	18	O	Switch-node connection.
SW2	8	O	Switch-node connection.
VBST1	17	I	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
VBST2	9	I	
VCLK	19	O	Clock output for charge pump.
VFB1	2	I	Voltage feedback Input
VFB2	4	I	
VIN	12	I	Power conversion voltage input. Apply the same voltage as drain voltage of high-side MOSFETs of channel 1 and channel 2.
VO1	14	I	Output voltage input, 5-V input for switch-over.
VREG3	3	O	3.3-V LDO output.
VREG5	13	O	5-V LDO output.
Thermal pad (GND)			GND terminal, solder to the ground plane

FUNCTIONAL BLOCK DIAGRAM



SWITCHER CONTROLLER BLOCK DIAGRAM



DETAILED DESCRIPTION

PWM Operations

The main control loop of the switch mode power supply (SMPS) is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP™ mode. D-CAP™ mode does not require external compensation circuits and is suitable for low external component count configuration when used with appropriate amount of ESR at the output capacitor(s).

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or enters the ON state. This MOSFET is turned off, or enters the ‘OFF state, after the internal, one-shot timer expires. The MOSFET is turned on again when the feedback point voltage, V_{VFB}, decreased to match the internal 2-V reference. The inductor current information is also monitored and should be below the overcurrent threshold to initiate this new cycle. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side (rectifying) MOSFET is turned on at the beginning of each OFF state to maintain a minimum of conduction loss. The low-side MOSFET is turned off before the high-side MOSFET turns on at next switching cycle or when the detecting inductor current decreases to zero. This enables seamless transition to the reduced frequency operation during light-load conditions so that high efficiency is maintained over a broad range of load current.

Adaptive On-Time/ PWM Frequency Control

Because the device does not have a dedicated oscillator for control loop on board, switching cycle is controlled by the adaptive on-time circuit. The on-time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. To achieve higher duty operation for lower input voltage application (2-cell battery), the target switching frequency is varied according to the input voltage. The switching frequency of CH1 (5-V output) is 400kHz during continuous conduction mode (CCM) operation when V_{IN} = 20 V. The CH2 (3.3-V output) is 475 kHz during CCM when V_{IN} = 20 V.

To improve load transient performance and load regulation in lower input voltage condition, device can extend the on-time. The maximum on-time extension of CH1 is 5 times. For CH2, it is 2 times. To maintain a reasonable inductor ripple current during on-time extension, the inductor ripple current should be set to less than half of the OCL (valley) threshold. The on-time extension function provides high duty cycle operation and shows better DC (static) performance. AC performance is determined mostly by the output LC filter and resistive factor in the loop.

Light Load Condition in Auto-Skip Operation

The device automatically reduces switching frequency during light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly. A more detailed description of this operation is as follows. As the output current decreases from heavy-load condition, the inductor current is also reduced and eventually approaches valley zero current, which is the boundary between continuous conduction mode and discontinuous conduction mode. The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires the next ON cycle. In reverse, when the output current increase from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches to the continuous conduction. The transition load point to the light load operation $I_{OUT(LL)}$ (that is, the threshold between continuous and discontinuous conduction mode) can be calculated as shown in n Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f_{SW} is the PWM switching frequency (1)

Switching frequency versus output current during light-load conditions is a function of inductance (L), input voltage (V_{IN}) and output voltage (V_{OUT}), but it decreases almost proportional to the output current from the $I_{OUT(LL)}$.

ULQ™ Mode

To achieve longer battery life in system stand-by mode of mobile devices, the device implements Ultra Low Quiescent (ULQ) mode. In the ULQ mode, the device consumes low quiescent current (see the ELECTRICAL CHARACTERISTICS table). Therefore, high efficiency can be obtained in the system stand-by mode. The TPS51285A/B enters the ULQ mode automatically (no control input signal is required) when both high-side and low-side MOSFET drivers are OFF state in discontinuous conduction operation. It exits from the ULQ mode when the PWM comparator detects VFB drops to the internal 2-V VREF and turns on the high-side MOSFET. In the ULQ mode, all protection functions are active.

D-CAP™ Mode

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in Figure 3.

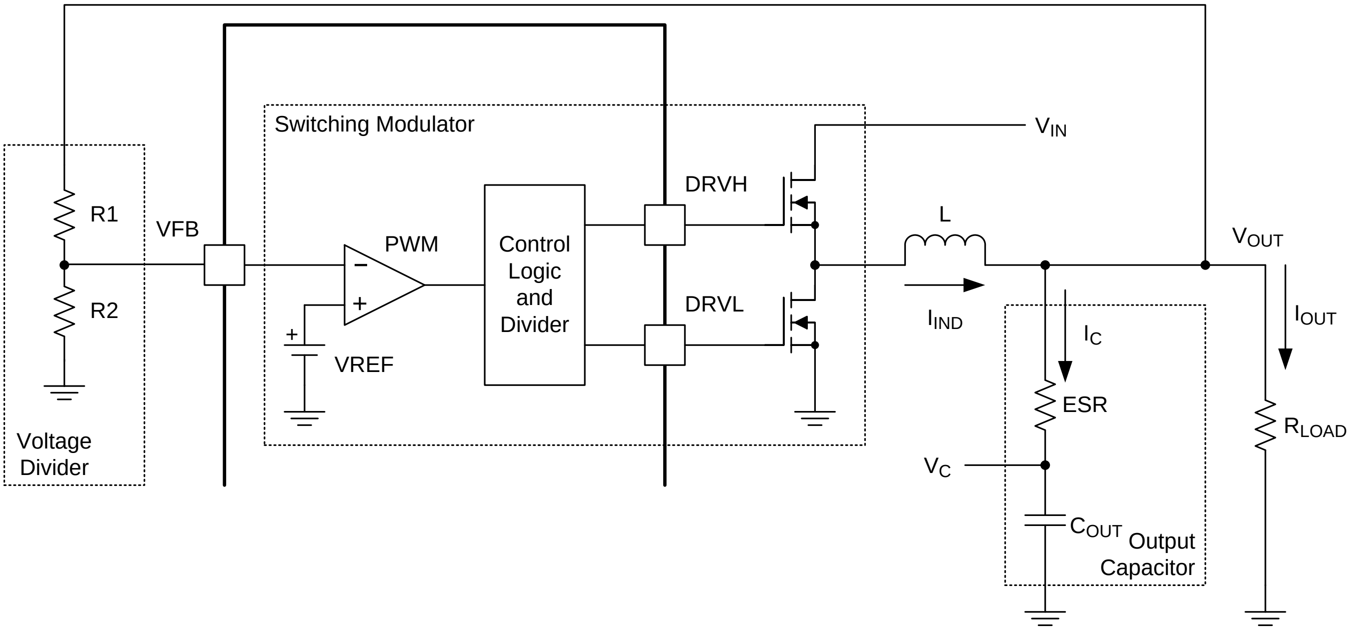


Figure 3. Simplifying the Modulator

The output voltage is compared with internal reference voltage after divider resistors, R1 and R2. The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each ON cycle substantially constant. For the loop stability, the 0 dB frequency, f_0, defined in Equation 2 must be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{4} \tag{2}$$

As f_0 is determined solely by the output capacitor characteristics, the loop stability during D-CAP™ mode is determined by the capacitor chemistry. For example, specialty polymer capacitors have output capacitance in the order of several hundred micro-Farads and ESR in range of 10 milli-ohms. These yield an f_0 value on the order of 100 kHz or less and the loop is stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

Enable and Power Good

VREG3 is an always-on regulator (TPS51285A and TPS1285B), For TPS51285B, VREG5 is an always-on LDO, too (See Table 1 and Table 2). When VIN exceeds the VIN-UVLO threshold VREG3 turns on. For TPS51285B, VREG5 turns on when VREG3 exceeds 2.4V. For TPS51285A, VREG5 turns on when either EN1 or EN2 enters ON state in addition to the above VREG3 threshold. CH1’s or CH2’s output starts ramping up when the corresponding EN pin is in the ON state and VREG5 is larger than the VREG5-UVLO. VCLK initiates switching when EN1 enters ON state. The state controls are shown in Table 1 and Table 2.

TPS51285A and TPS51285B have a PGOOD open drain output. During the start-up, if the feedback voltages for both CH1 and CH2 exceed 90% of the reference voltage, the PGOOD becomes high with defined PGOOD delay time. During the operation, if the feedback voltage rise beyond 115%(typ) for either switching regulator, PGOOD turns low. If the feedback voltage falls below 60%(typ), the PGOOD turns low.

Table 1. Enabling and PGOOD State (TPS51285A; Always-on VREG3)

EN1	EN2	VREG5	VREG3	CH1 (5Vout)	CH2 (3.3Vout)	VCLK	PGOOD
OFF	OFF	OFF	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High

Table 2. Enabling and PGOOD State (TPS51285B; Always-on VREG3 and VREG5)

EN1	EN2	VREG5	VREG3	CH1 (5Vout)	CH2 (3.3Vout)	VCLK	PGOOD
OFF	OFF	ON	ON	OFF	OFF	OFF	Low
ON	OFF	ON	ON	ON	OFF	ON	Low
OFF	ON	ON	ON	OFF	ON	OFF	Low
ON	ON	ON	ON	ON	ON	ON	High

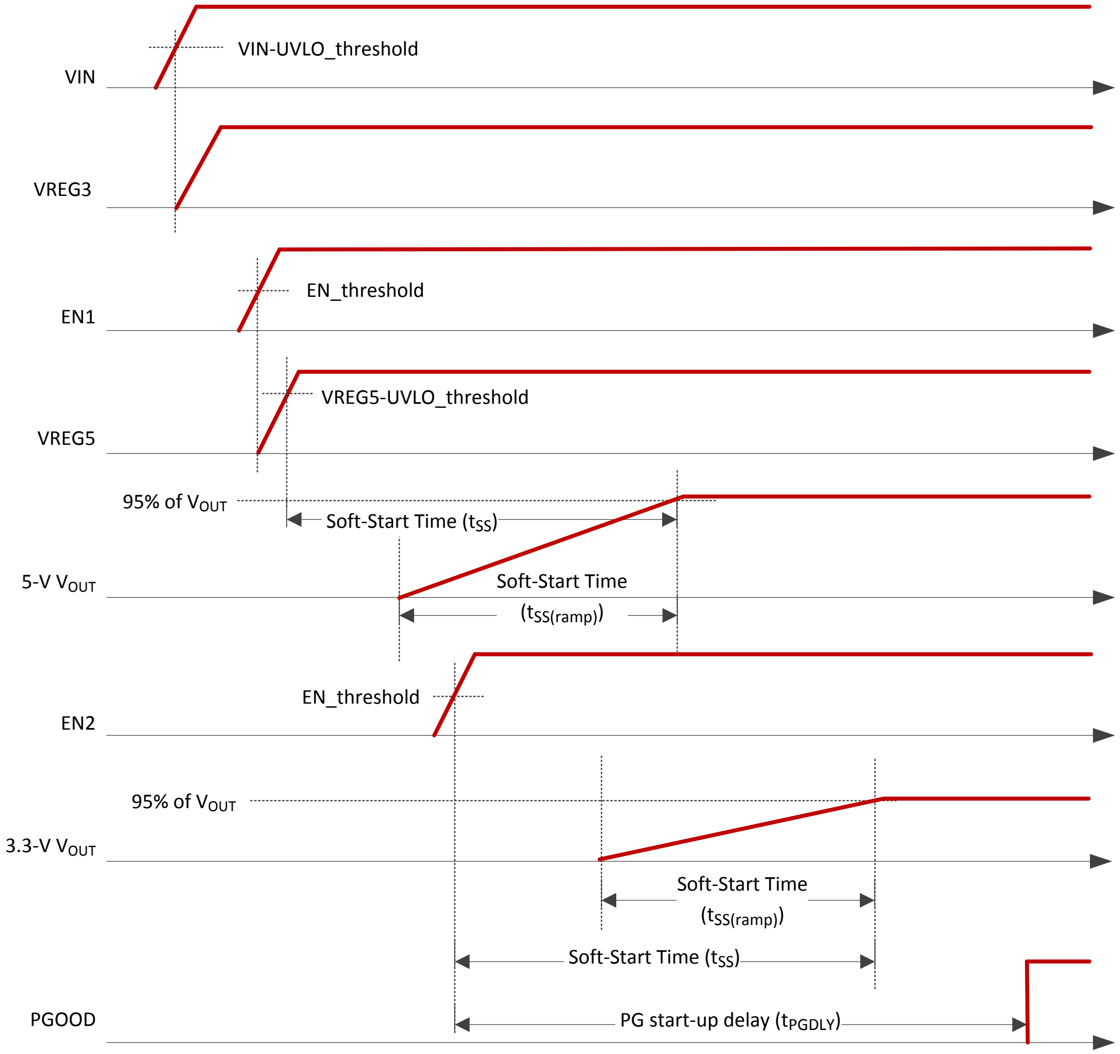


Figure 4. TPS51285A Timing Diagram of Start-up

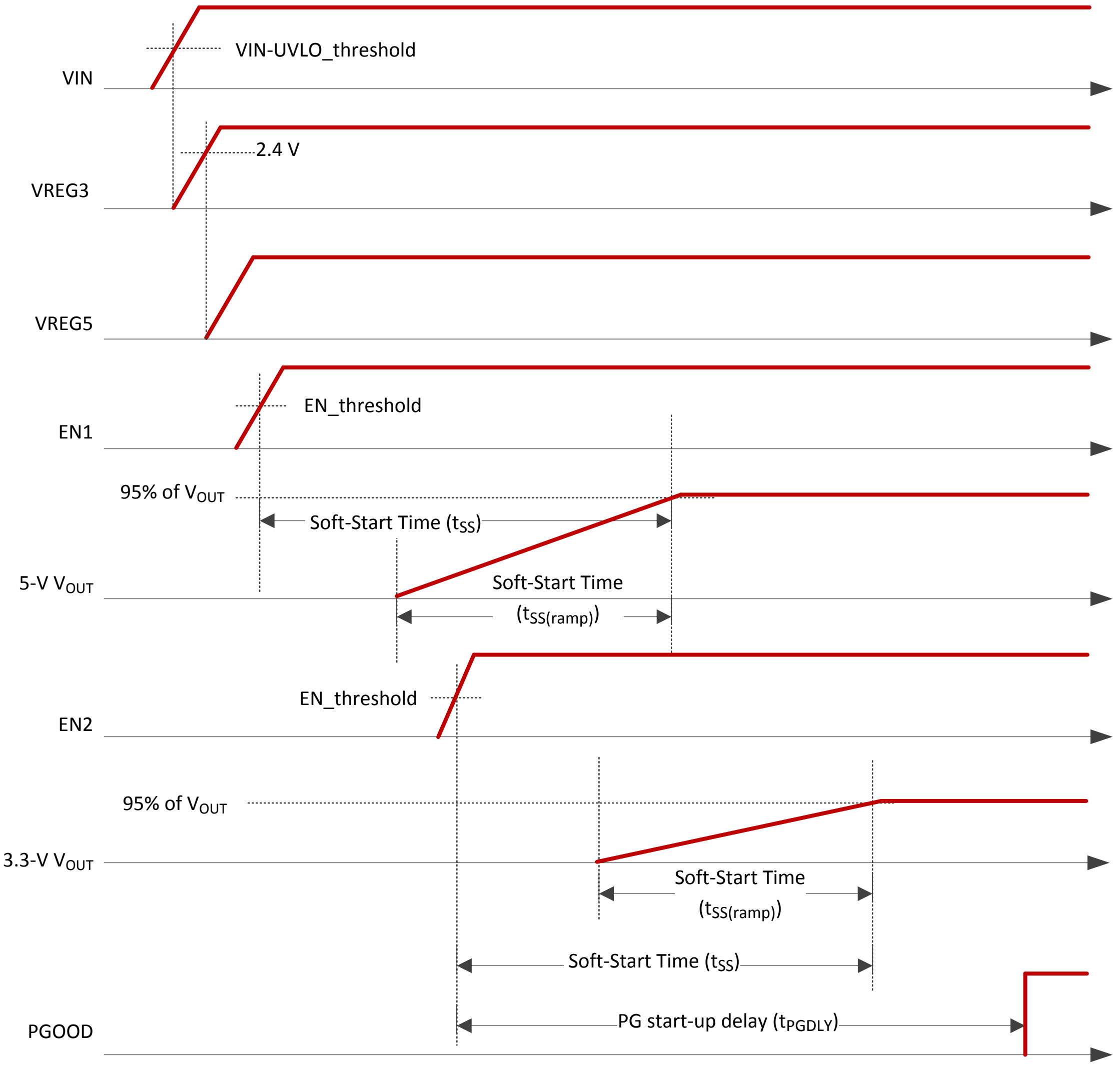


Figure 5. TPS51285B Timing Diagram of Start-up

Soft-Start and Discharge

The TPS51285A and TPS51285B operates an internal, 0.8-ms, voltage servo soft-start for each channel. When the ENx pin becomes higher than the enable threshold voltage, an internal DAC begins ramping up the reference voltage to the target (2 V). Smooth control of the output voltage is maintained during start-up. When ENx becomes lower than the lower level of threshold voltage, the device discharges outputs using internal MOSFETs through VO1 (CH1) and SW2 (CH2).

VREG5 and VREG3 Linear Regulators

There are two 100-mA standby linear regulators that output 5 V and 3.3 V, respectively. The VREG5 provides the current for gate drivers. VREG3 functions as the main power supply for the analog circuitry of the device.

A ceramic capacitor with a value of 4.7 µF or larger (X5R grade or better) is required for each of VREG5 and VREG3. It should be placed close to the VREG5 pin and the VREG3 pin respectively to stabilize the LDOs.

The VREG5 pin switchover function is asserted when three conditions are present:

- CH1 is not in UVP/OVP condition
- CH1 is not in OCL condition
- VO1 voltage is higher than (VREG5 -1V)

In this switchover condition three things occur:

- the internal 5-V LDO regulator is shut off
- the VREG5 output is connected to VO1 by internal switchover MOSFET
- VREG3 input pass is changed from VIN to VO1

VCLK for Charge Pump

A 256 kHz VCLK signal can be used for the external charge pump circuit. The VCLK signal becomes available when EN1 enters ON state. VCLK driver circuit is driven by VO1 voltage. In a design that does not require VCLK output, tie 200 Ω between VCLK pin and GND so that VCLK is turned off.

Overcurrent Protection

TPS51285A and TPS51285B have cycle-by-cycle over current limiting control. The inductor current is monitored during the OFF state and the controller maintains the OFF state during the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, the device supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The CSx pin should be connected to GND through the CS voltage setting resistor, R_{CS}. The CSx pin sources CS current (I_{CS}) which is 50 µA typically at room temperature, and the CSx terminal voltage ($V_{CS} = R_{CS} \times I_{CS}$) should be in the range of 0.2 V to 2 V over all operation temperatures. The trip level is set to the OCL trip voltage (V_{TRIP}) as shown in Equation 3.

$$V_{TRIP} = \frac{R_{CS} \times I_{CS}}{8} + 1\,\text{mV} \tag{3}$$

The inductor current is monitored by the voltage between GND pin and SWx pin so that SWx pin should be connected to the drain terminal of the low-side MOSFET properly.The CS pin current has a 4500 ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the source terminal of the low-side MOSFET.

As the comparison is done during the OFF state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, $I_{OCL(DC)}$, can be calculated as shown in Equation 4.

$$I_{OCL(DC)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{4}$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. Eventually, it ends up with crossing the undervoltage protection threshold and shutdown both channels.

Output Overvoltage and Undervoltage Protection

TPS51285A and TPS51285B assert the overvoltage protection (OVP) when VFBx voltage reaches OVP trip threshold level. When an OVP event is detected, the controller changes the output target voltage to 0 V. This usually turns off DRVH and forces DRVL to be on. When the inductor current begins to flow through the low-side MOSFET and reaches the negative OCL, DRVL is turned off and DRVH is turned on. After the on-time expires, DRVH is turned off and DRVL is turned on again. This action minimizes the output node undershoot due to LC resonance. When the VFBx reaches 0 V, the driver output is latched as DRVH off and DRVL on. The undervoltage protection (UVP) latch is set when the VFBx voltage remains lower than UVP trip threshold voltage for 250 μs or longer. In this fault condition, the controller latches DRVH low and DRVL low and discharges the outputs through VO1(CH1) and SW2 (CH2). UVP detection function is enabled after 1.1 ms of SMPS operation to ensure startup. Toggle ENx to clear the fault latch.

Undervoltage Lockout (UVLO) Protection

TPS51285A and B have undervoltage lock out protection at VIN, VREG5 and VREG3. When each voltage is lower than their UVLO threshold voltage, both SMPS are shut-off. They are non-latch protections.

Over-Temperature Protection

TPS51285A and TPS51285B features an internal temperature monitor. If the temperature exceeds the threshold value (typically 140°C), the device is shut off including LDOs. This is non-latch protection.

REFERENCE DESIGN

Application Schematic

This session describes a simplified design procedure for 5 V and 3.3 V outputs application using TPS1285A and TPS1285B. Figure 6 shows the application schematic.

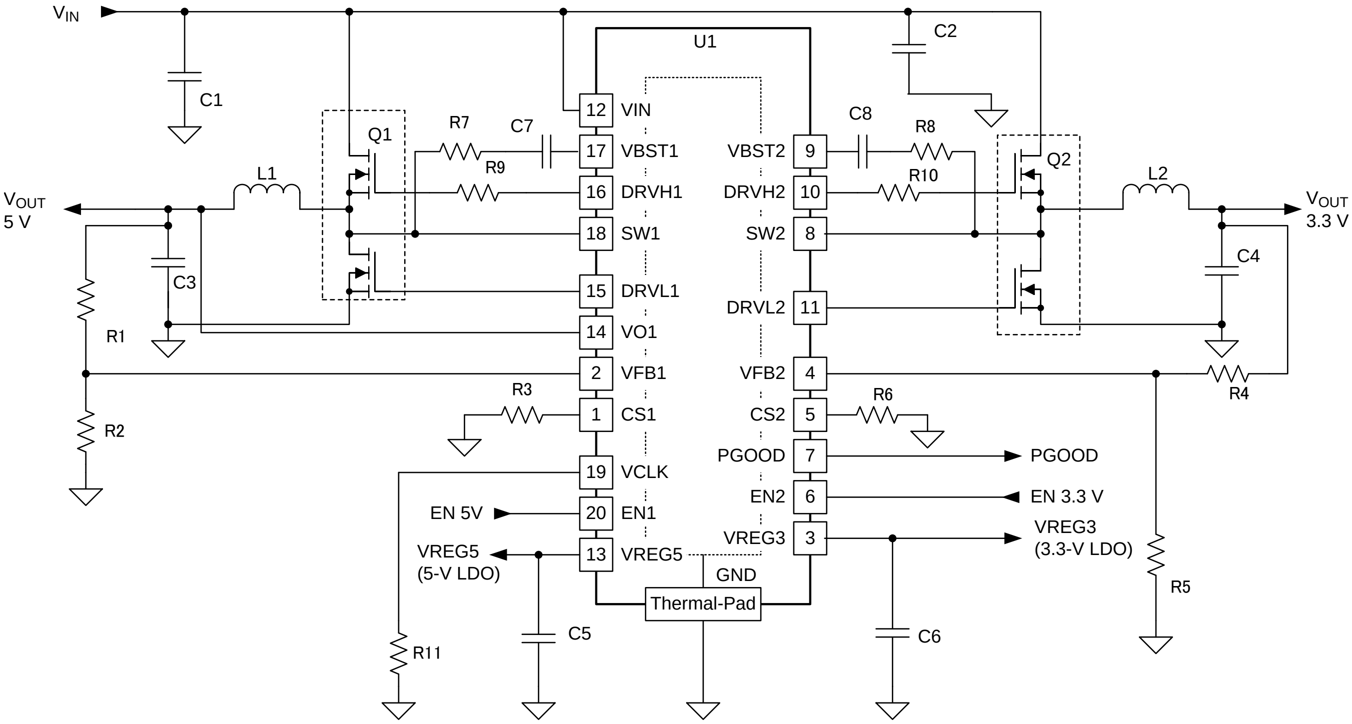


Figure 6. Application Schematic

Table 3. Key External Components

REFERENCE DESIGNATOR	FUNCTION	MANUFACTURER	PART NUMBER
L1	Output Inductor (5-Vout)	ALPS	GLMC3R303A
L2	Output Inductor (3.3-Vout)	ALPS	GLMC2R203A
C3	Output Capacitor (5-Vout)	SANYO	6TPS220MAZB x 2
C4	Output Capacitor (3.3-Vout)	SANYO	6TPS220MAZB x 2
Q1	MOSFET (5-Vout)	TI	CSD87330Q3D
Q2	MOSFET (3.3-Vout)	TI	CSD87330Q3D
C5	Decoupling Capacitance (VREG5)	MURATA	GRM188B30J475ME84
C6	Decoupling Capacitance (VREG3)	MURATA	GRM188B30J475ME84

Design Procedure

Step 1. Determine the Specifications:

- VIN range = 5.5 V to 20 V
- CH1 output: Vout1 = 5 V and Iout1 = 6 A
- CH2 output: Vout2 = 3.3 V and Iout2 = 7 A

Step 2. Determine the Value of Voltage Divider Resistors

The output voltage is determined by 2-V internal voltage reference and the resistor dividers (R1 and R2/ R4 and R5). To achieve higher efficiency at light load condition, for 5 V output, select R2 = 100 kΩ and R1 = 150kΩ for 3.3V output R5 = 200 kΩ and R4 = 130 kΩ. Determine R1 using Equation 5. (for 3.3 V, replace R1 with R4 and R2 with R5). For applications where signal-to-noise performance is more valuable than light load efficiency, set R2 (R5) to 10kΩ.

$$R1 = \frac{\left(V_{OUT} - 0.5 \times V_{RIPPLE} - 2.0\right)}{2.0} \times R2 \tag{5}$$

Step 3. Determine Inductance and Choose the Inductor

Smaller inductance yields better transient performance but the consequence is larger ripple and lower efficiency. Larger value has the opposite characteristics. It is the common practice to limit the inductor ripple current to 25% to 50% of the maximum output current. In this case, use 50% at V_{IN} = 20 V.

$$L1 = \frac{1}{I_{IND(ripple)} \times f_{SW(CH1)}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = 3.13\ \mu H \tag{6}$$

Where

- $I_{IND(ripple)}$ = 6 A x 0.5, V_{OUT} = 5 V. $V_{IN(MAX)}$ = 20 V, $f_{SW(CH2)}$ = 400 kHz

$$L2 = \frac{1}{I_{IND(ripple)} \times f_{SW(CH2)}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = 1.66\ \mu H \tag{7}$$

Where

- $I_{IND(ripple)}$ = 7 A x 0.5, V_{OUT} = 3.3 V. $V_{IN(MAX)}$ = 20 V, $f_{SW(CH2)}$ = 475 kHz

For this design, L1 = 3.3 µH and L2 = 2.2 µH are chosen.

Step 4. Choose Output Capacitor(s)

For the loop stability, the 0 dB frequency, f_0, defined in Equation 8 must be lower than 1/4 of the switching frequency (entire V_{IN} range).

$$f_0 = \frac{1}{2\pi \times ESR \times C_O} \le \frac{f_{sw}}{4} \quad (8)$$

Determine ESR to meet required ripple voltage below for better jitter performance. A quick approximation is as shown in Equation 9.

$$ESR = \frac{V_{OUT} \times 20[mV] \times (1-D)}{2[V] \times I_{IND(Ripple)}} = \frac{20[mV] \times L \times f_{SW}}{2[V]} \quad (9)$$

where

- D as the duty-cycle factor
- the required output ripple voltage slope is approximately 20 mV per t_{SW} (switching period) in terms of VFB terminal

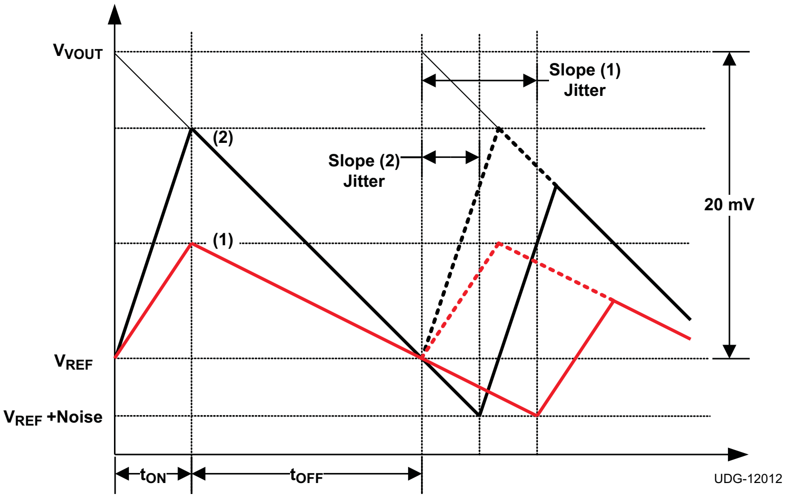


Figure 7. Ripple Voltage Slope and Jitter Performance

This design uses 2 x 220 µF (35 mΩ) for each output.

Step 5. Determine Over Current Limit (OCL) Setting Resistors

Use Equation 10 to determine the over current limit setting resistor (R3/ R6) which is connected from CS1/CS2 to GND.

$$R_{CS} = \frac{8}{I_{CS}} \times \left[\left(I_{OCL(DC)} - I_{IND(ripple)} \times 0.5\right) \times R_{DS(ON)} - 1mV \right] \quad (10)$$

Confirm CS voltage is within the range of 0.2 V to 2 V over all operation temperature using Equation 11.

$$V_{CS} = R_{CS} \times I_{CS} \left[(25^{o}C - T_A) \times TC_{CS} \times 10^{-6} + 1 \right] \quad (11)$$

Where

- T_A is an operation temperature

Confirm inductor ripple current is less than half of OCL (valley) using Equation 12

$$I_{IND(ripple)} < \frac{I_{OCL(VALLEY)}}{2} = \frac{\left(\frac{R_{CS} \times I_{CS}}{8} + 1mV \right)}{2 \times R_{DS(ON)}} \quad (12)$$

This design uses CSD87330Q3D (low-side $R_{DS(ON)}$ typ = 4.7 mΩ) and R3 (R_{CS} - CH1) = 6.19 kΩ, R6 (R_{CS} - CH2) = 6.65 kΩ.

Step 6. Select Decoupling Capacitors

Use ceramic capacitors with a value of 4.7 µF or larger (X5R grade or better) for C5 (VREG5) and C6 (VREG3). For the V_{IN} input capacitors (C1 and C2), 2 x 10 µF (1206, 25V, X5R) MLCC per channel is used in the design. Tighter tolerances and higher voltage ratings are always appreciated.

Step 7. Peripheral Components

For high-side N-channel MOSFET drive circuit, connect boot strap capacitor between VBSTx and SWx. To control gate driver strength, adding a resistor (reserved space) is recommended. This design uses 0.1 µF (C7 and C8), 0 Ω (R7 and R8), 6.8 Ω (R9) and 8.2 Ω (R10).

Step 8. Charge Pump Design

Figure 6 shows a circuit design without an external charge pump. Add R11 = 200Ω from VCLK to GND to disable VCLK signal. Figure 8 shows the design with an external charge pump. D1 (4-in 1 Diode: BAS40DW-04) should be tied to the 5V switcher output and 4 x 0.1 µF (C9, C10, C11 and C12) is used.

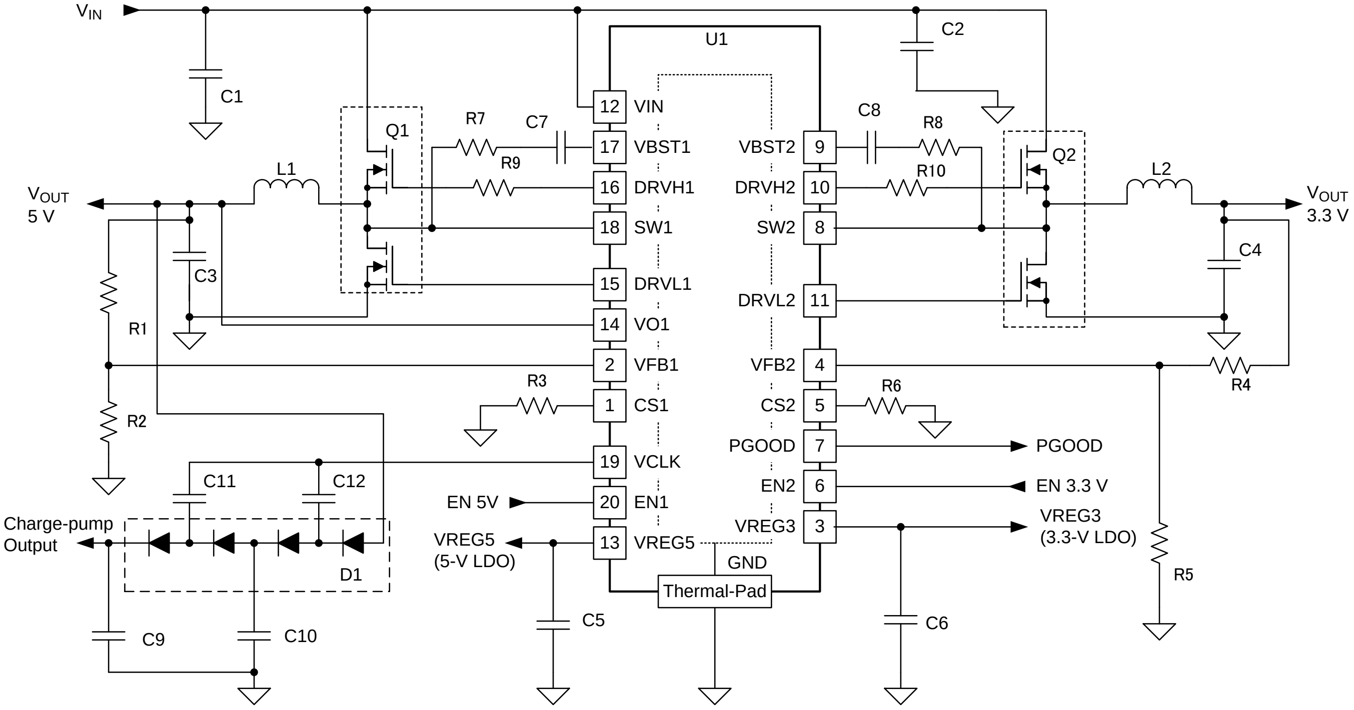


Figure 8. Application Schematic (with Charge pump)

Layout Considerations

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout.

Placement

- Place voltage setting resistors close to the device pins.
- Place bypass capacitors for VREG5 and VREG3 close to the device pins.

Routing (Sensitive analog portion)

- Use small copper space for VFBx. There are short and narrow traces to avoid noise coupling.
- Connect VFB resistor trace to the positive node of the output capacitor. Routing inner layer away from power traces is recommended.
- Use short and wide trace from VFB resistor to vias to GND (internal GND plane).

Routing (Power portion)

- Use wider/shorter traces of DRVL for low-side gate drivers to reduce stray inductance.
- Use the parallel traces of SW and DRVH for high-side MOSFET gate drive in a same layer or on adjoin layers, and keep them away from DRVL.
- Use wider/ shorter traces between the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET
- Thermal pad is the GND terminal of this device. Five or more vias with 0.33-mm (13-mils) diameter connected from the thermal pad to the internal GND plane should be used to have strong GND connection and help heat dissipation.

TYPICAL CHARACTERISTICS

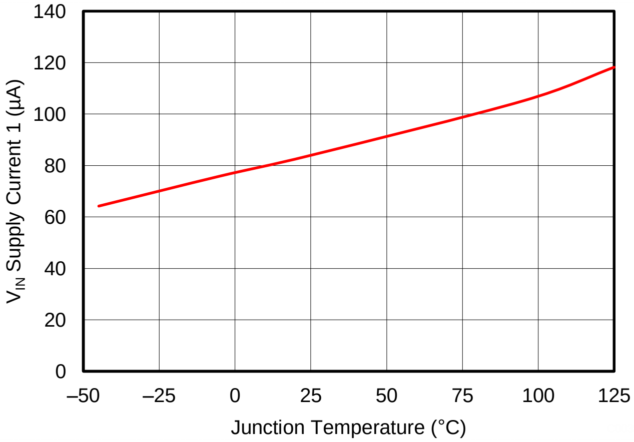


Figure 9. VIN Supply Current 1 vs. Junction Temperature

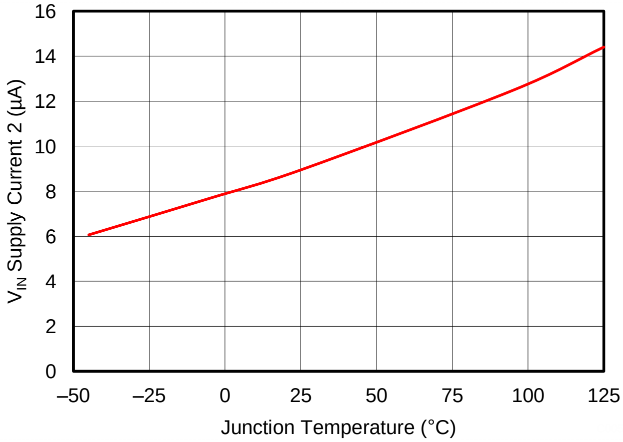


Figure 10. VIN Supply Current 2 vs. Junction Temperature

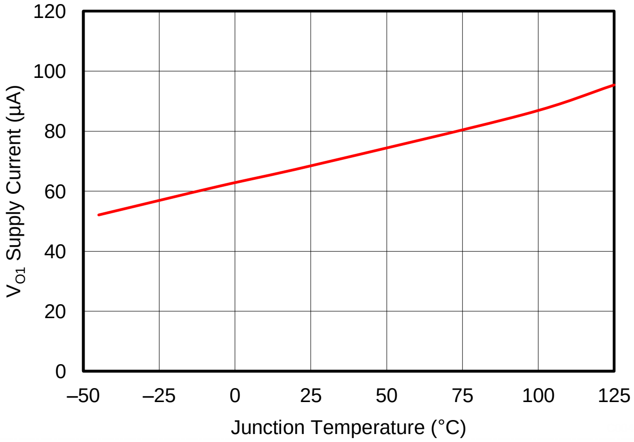


Figure 11. VO1 Supply Current 1 vs. Junction Temperature

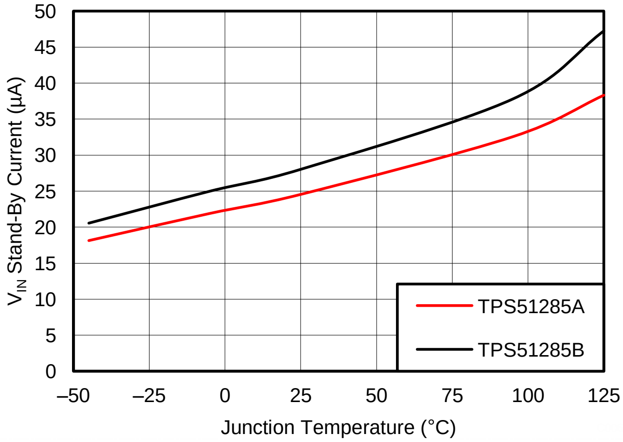


Figure 12. VIN Stand-By Current vs. Junction Temperature

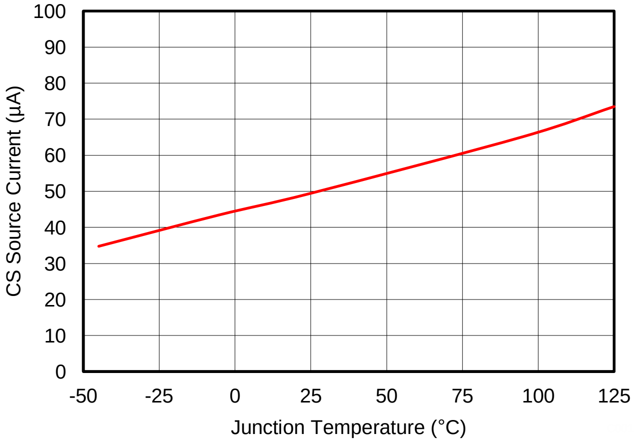


Figure 13. CS Source Current vs. Junction Temperature

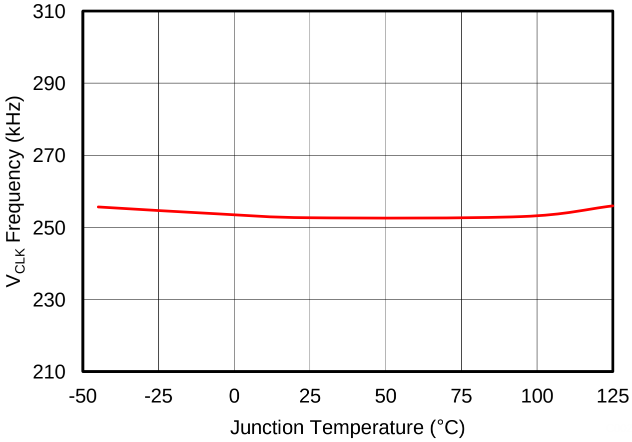


Figure 14. Clock Frequency vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

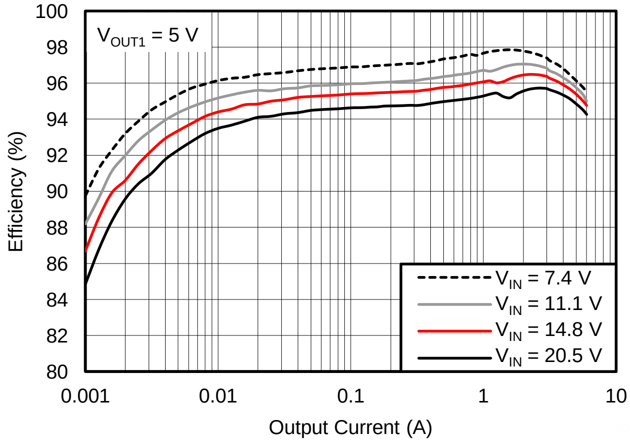


Figure 15. Efficiency vs. Output Current

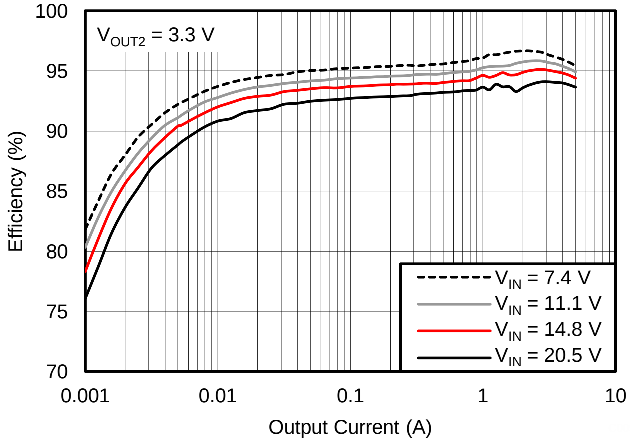


Figure 16. Efficiency vs. Output Current

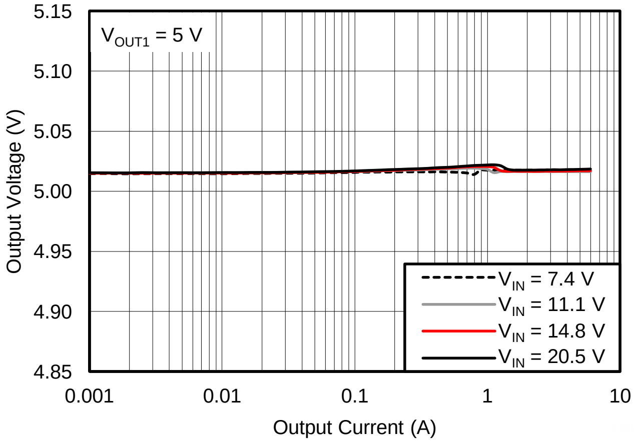


Figure 17. Load Regulation

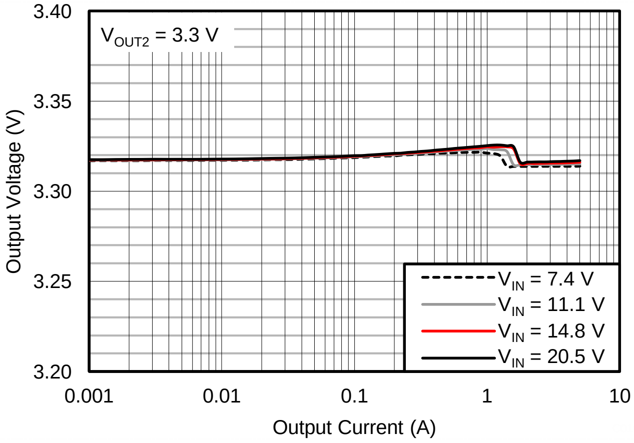


Figure 18. Load Regulation

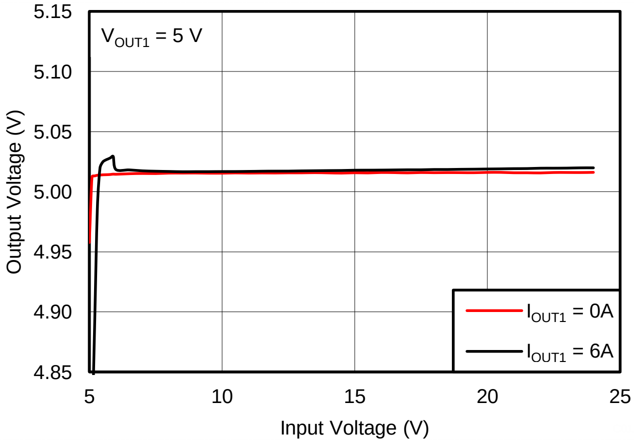


Figure 19. Line Regulation

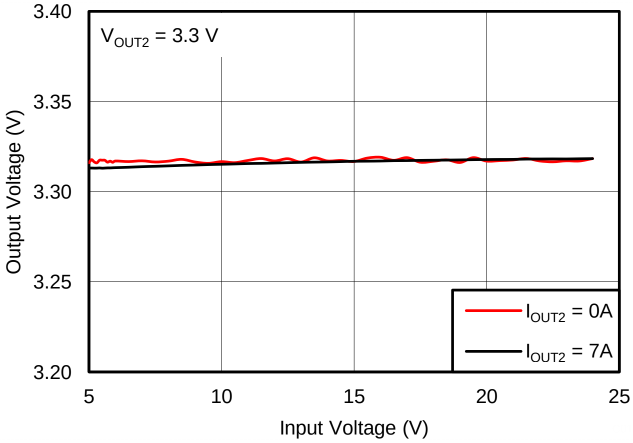


Figure 20. Line Regulation

TYPICAL CHARACTERISTICS (continued)

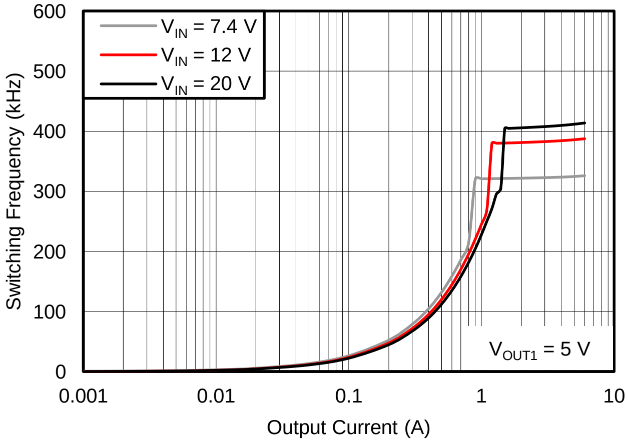


Figure 21. Switching Frequency vs. Output Current

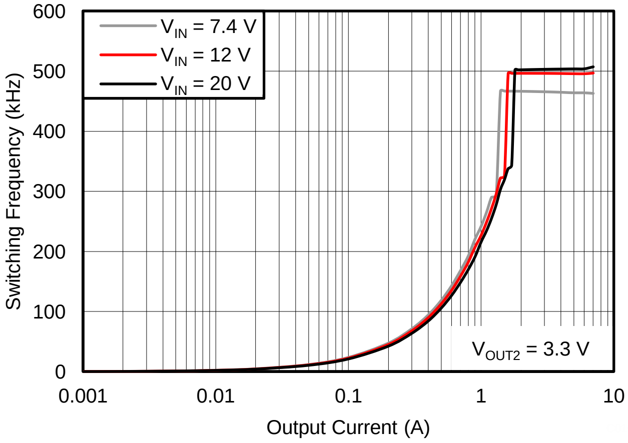


Figure 22. Switching Frequency vs. Output Current

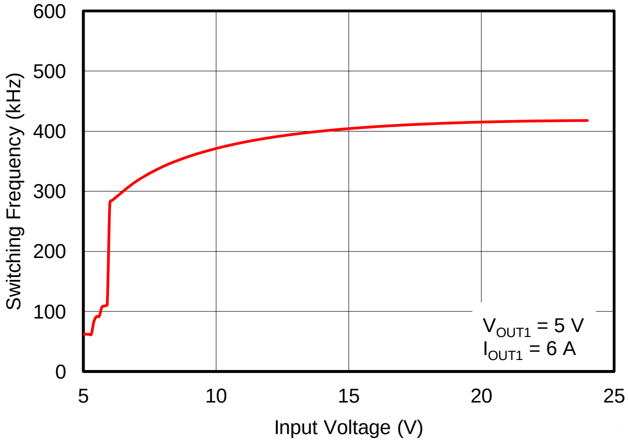


Figure 23. Switching Frequency vs. Input Voltage

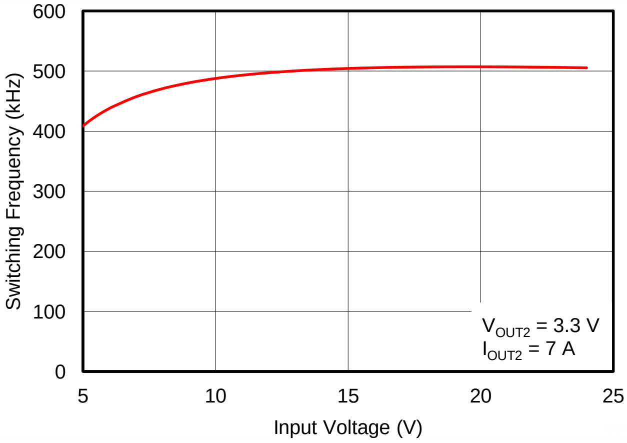


Figure 24. Switching Frequency vs. Input Voltage

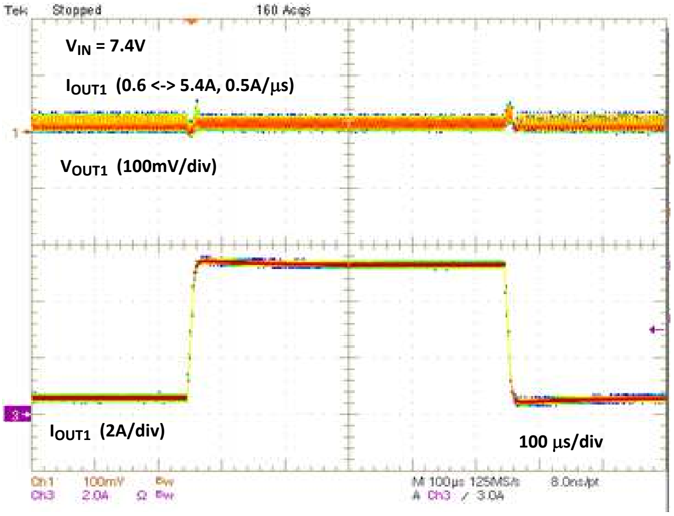


Figure 25. Load Transient

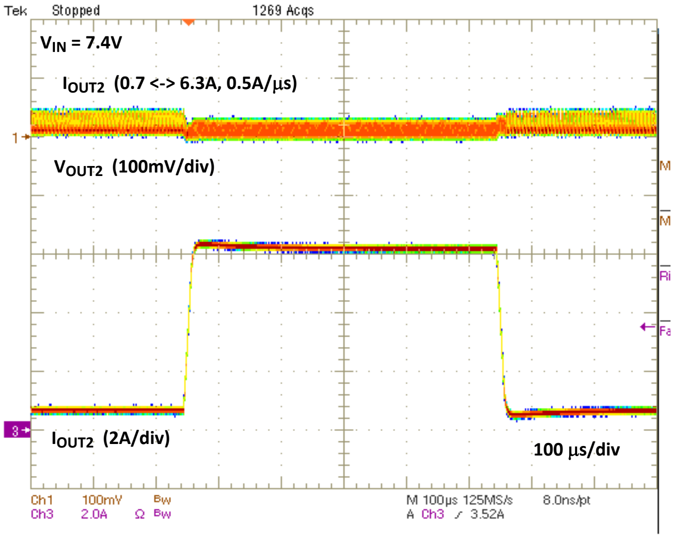


Figure 26. Load Transient

TYPICAL CHARACTERISTICS (continued)

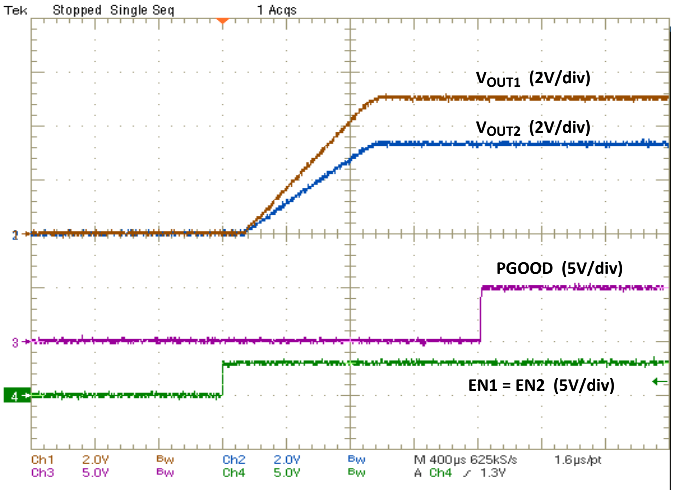


Figure 27. Start-Up

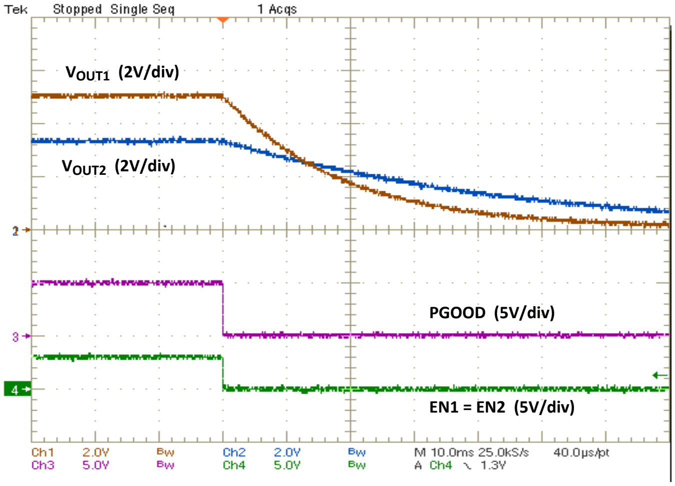


Figure 28. Output Discharge

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS51285ARUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1285A	Samples
TPS51285ARUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1285A	Samples
TPS51285BRUKR	ACTIVE	WQFN	RUK	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1285B	Samples
TPS51285BRUKT	ACTIVE	WQFN	RUK	20	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	1285B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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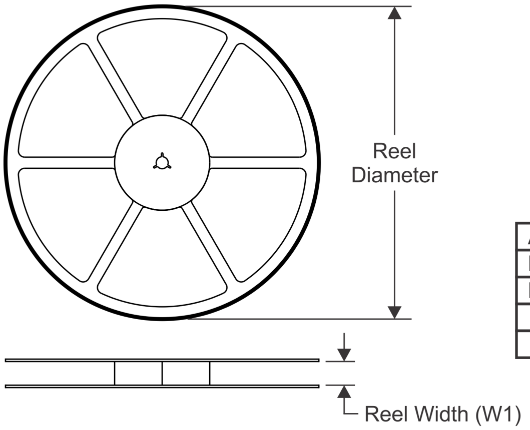
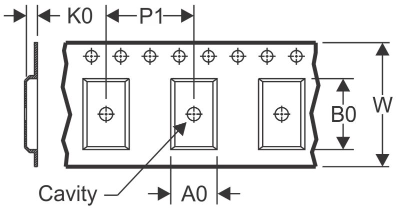
TAPE AND REEL INFORMATION

REEL DIMENSIONS

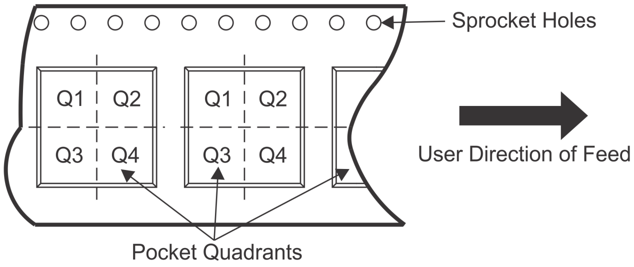


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

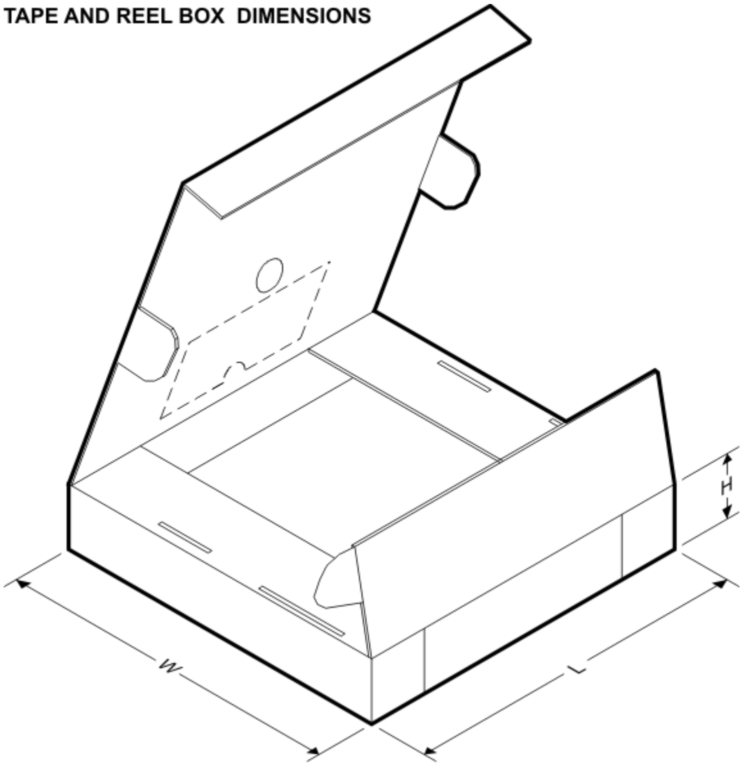
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51285ARUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51285ARUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51285BRUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS51285BRUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

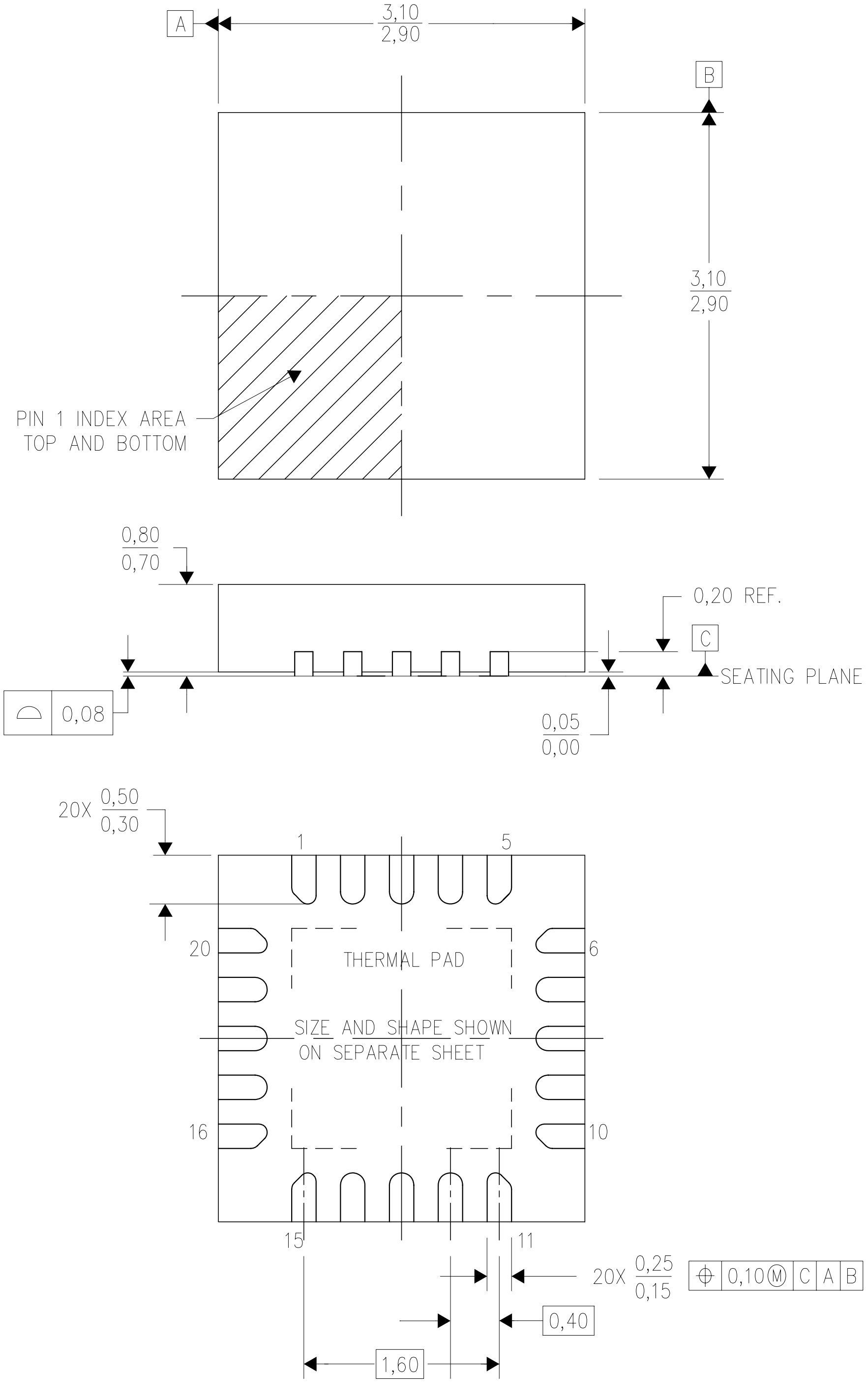
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51285ARUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS51285ARUKT	WQFN	RUK	20	250	210.0	185.0	35.0
TPS51285BRUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
TPS51285BRUKT	WQFN	RUK	20	250	210.0	185.0	35.0

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



4208637/C 01/12

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

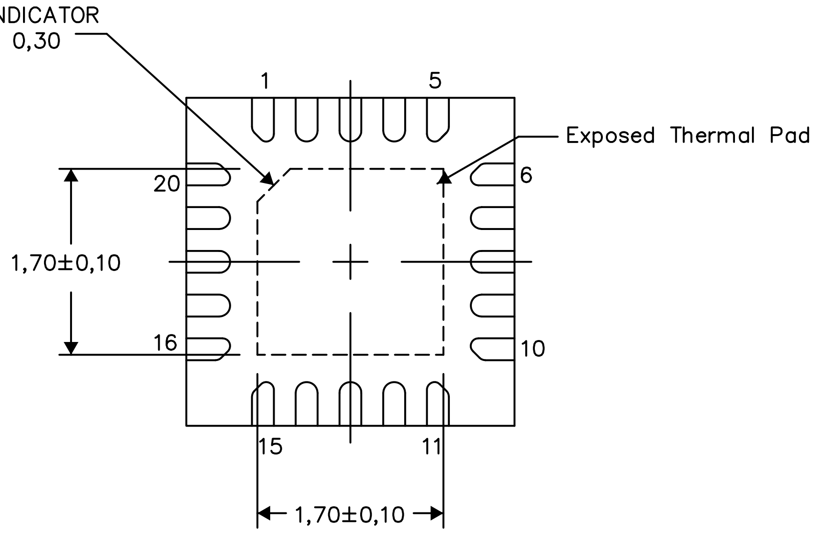
RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



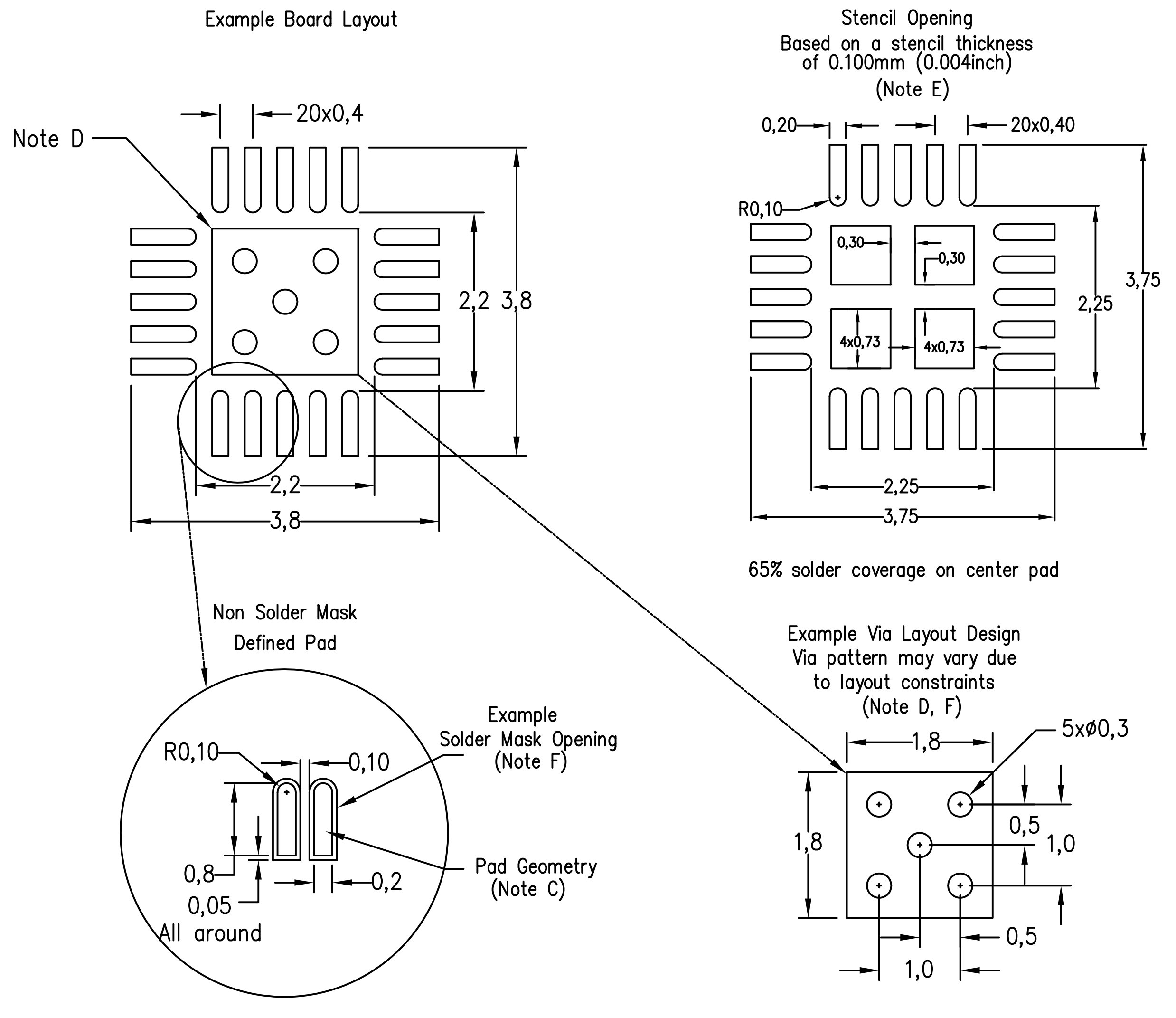
Bottom View

Exposed Thermal Pad Dimensions

4209762/E 12/12

NOTE: All linear dimensions are in millimeters

RUK (S-PWQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



4211052/D 12/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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