AW5808TR

5GHz Module (MA)

Data Sheet

Version: 0.1

Subject to change without further notice.

2019/07/25

INDEX

1. Features

The MA is a module based on ETK52L 32PIN RF controller, providing premium-quality audio for stereo audio applications operating in the 5.8/5.2GHz bands.

The wireless audio link supports up to two 24-bit quality audio streams and comes with additional features such as data encryption, pairing functionality, bi-directional data messages, enhanced RF interference detection, and automatic frequency allocation.

Brief features include:

- ☐ **Radio Frequency: 5.8/5.2GHz unlicensed bands**
- ☐ **Near Lossless Compressed Audio**
- ☐ **Link Distance: up to 40 Meters (Application depends)**
- ☐ **Advanced RF Selection Algorithm**
- ☐ **Small RF Foot Print**
- ☐ **Best Coexistence with Wi-Fi/Bluetooth**
- ☐ **Highly Integrated SoC: RF/PA/CPU/Flash Embedded**
- ☐ **Short RBOM List**
- ☐ **RF Modulation: FSK**
- ☐ **Digital I2S (master or slave) Audio Interface**
- ☐ **Low Power Consumption**
- ☐ **Supply Voltage: 2.7~3.6V**
- ☐ **Support I2C master/slave mode**
- ☐ **Two version for flexible system design, one RF connector / two RF connector**
- ☐ **Compliant with EMC Regulations (FCC/CE)**

2. Application

- ☐ **Wireless Surround Speakers**
- ☐ **Wireless Headphone / Headset**
- ☐ **Wireless HTiB**
- ☐ **Wireless microphone**

3. Electrical Specifications

RF Specification

Item	Min	Typ	Max	Unit	Note
RF Carrier Frequency	5725	—	5850	MHz	For 5.8GHz
	5135	—	5260		For 5.2GHz
-20dB bandwidth	—	2	—	MHz	
Output Power		7		dBm	
RF Sensitivity	—	-85		dBm	

Operation Condition

Item	Min	Typ	Max	Unit	Note
VDD	2.7	3.3	3.6	V	Power Supply Voltage
Operating Temperature	-5	25	60	℃	Ambient temperature

Electrical Specification (MCU+RF)

Item	Min	Typ	Max	Unit	Note
Transmitter current		80		mA	Output power 7dBm
Receiver current		50		mA	
sleep mode		2		mA	Crystal enable, timer or interrupt wake up system

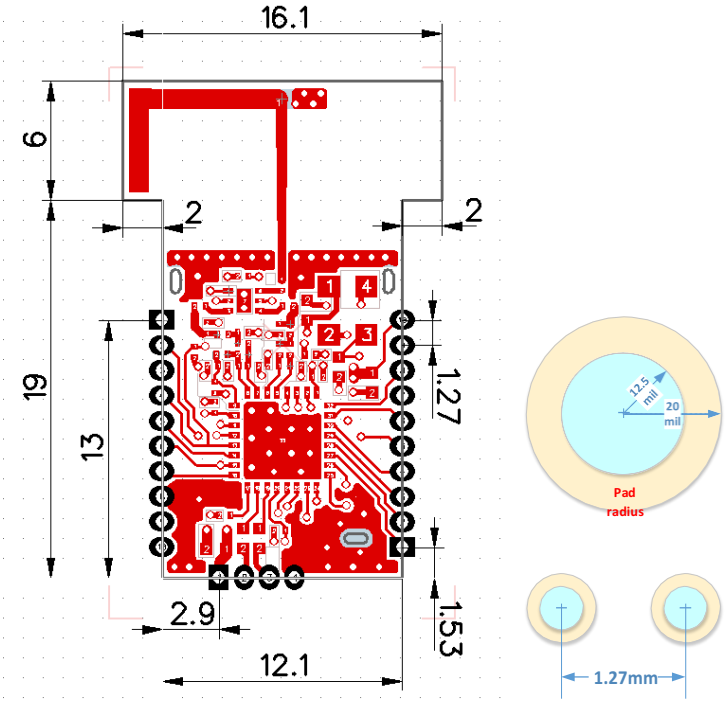
Note: power consumption varies on different applications.

Digital interface

Item	Min	Typ	Max	Unit	Note
VIH	0.7VDD		VDD+0.2	V	Input High Threshold
VIL	VSS		0.3VDD	V	Input Low Threshold
VOH	VDD-0.3		VDD	V	Output High Threshold
VOL	0		0.3	V	Output Low Threshold

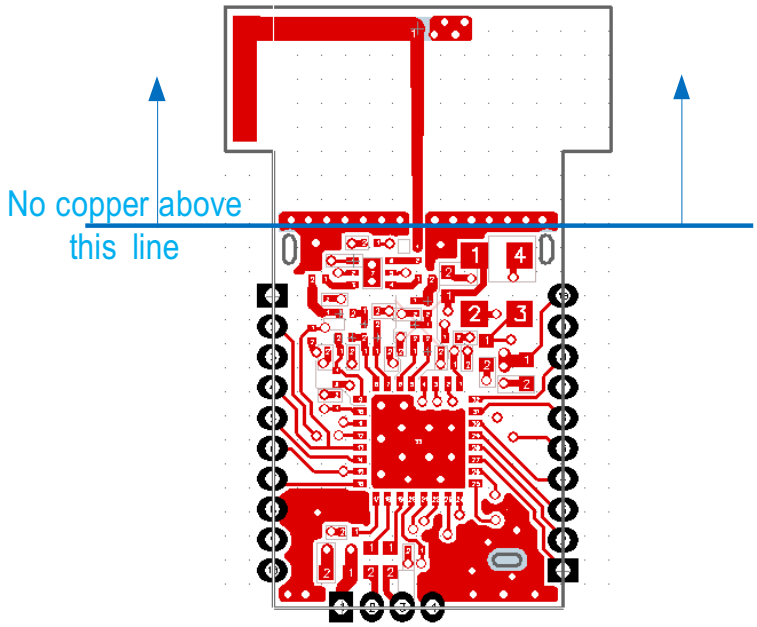
4. Mechanical Specification and Connection Notice

1. Dimension：16.1 mm x 25 mm
2. PCB 4 Layers
3. Mechanical Drawing:

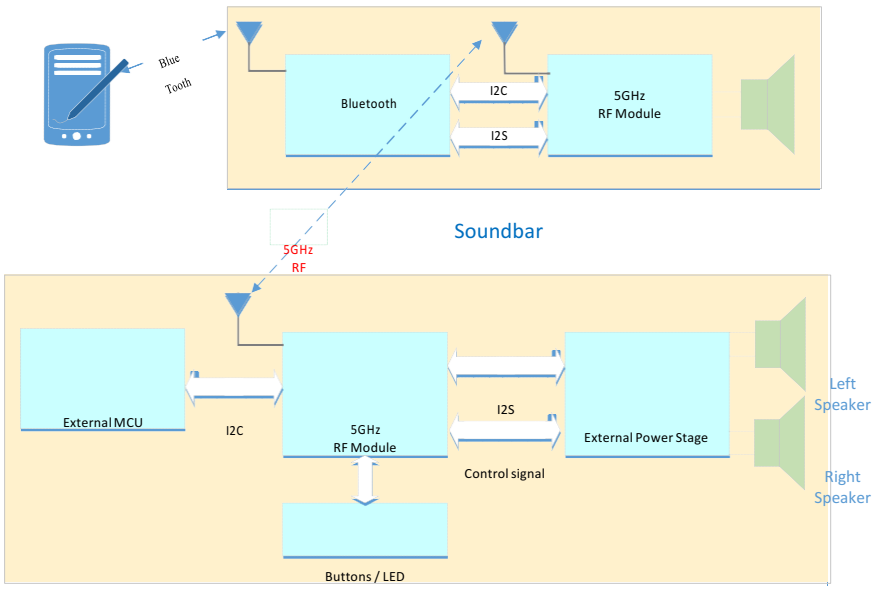


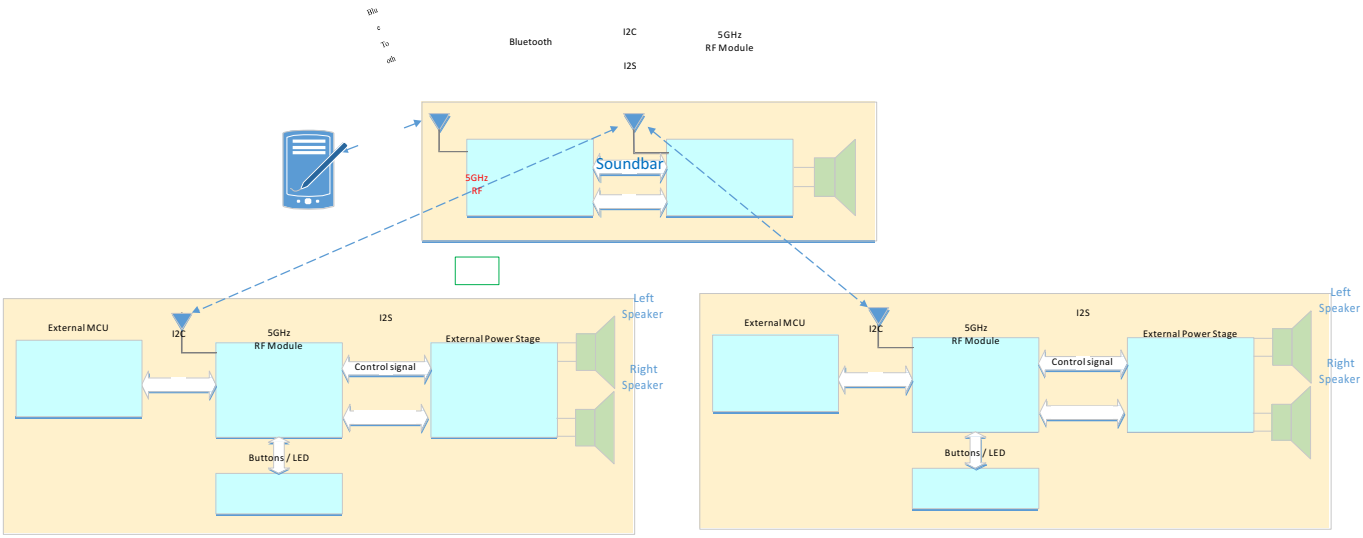
Note: Detail mechanical drawing DXF file, please contact FAE.

The no copper area is showed below in pink color. The main board layout should no copper, no trace underneath this area.

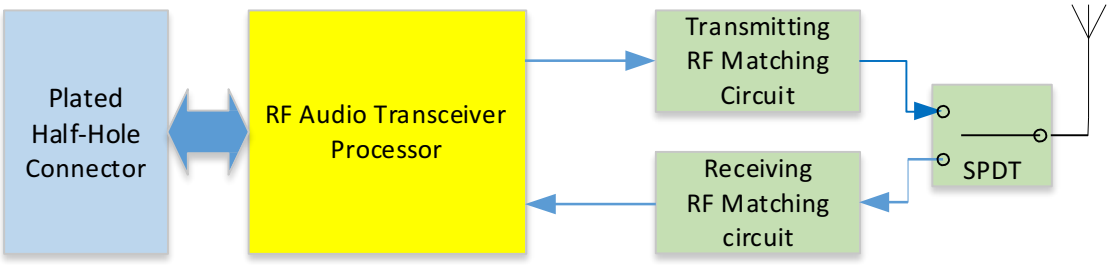


5. Application



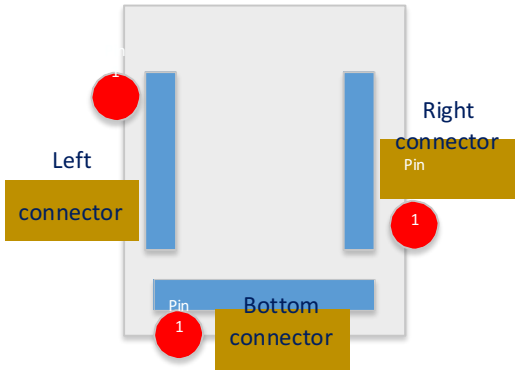


6. Block Diagram



7. Module Pin Definition

The first pin location (top view) have highlighted as the chart below,



J1(Left 10 pins):

Pin	Name	I/O	Function Definition
1	P3.2	I/O, A	GPIO
2	P0.0_SCL	I/O	General I/O, I2C clock
3	P0.1 _SDA	I/O	General I/O, I2C data
4	P0.7_CS	I/O, C	General I/O If DPDT is mounted on module, this GPIO is used for RF DPDT control. So please don't use this pin. SPI chip select for programming internal flash mode
5	P0.6_ SCK	I/O	General I/O SPI SCK for SPI in programming internal flash mode
6	P0.5_ MISO	I/O, C	SPI MISO for SPI in programming internal flash mode
7	P0.4_MOSI	I/O, C	General I/O SPI MOSI for SPI in programming internal flash mode
8	DGND	A	System ground
9	P2.7_PWM	P	Tx if module operate in, I2S slave mode: internal clock synchronization use only I2S master mode: GPIO Rx module: GPIO
10	P1.7	I/O	General I/O

J3(Bottom 4 pins):

Pin	Name	I/O	Function Definition
1	5V	P	USB 5V power in
2	D-	A	USB D- signal
3	D+	A	USB D+ signal
4	DGND	A	System ground

J2(Right 10 pins):

Pin	Name	I/O	Function Definition
1	P1.3_BCK	I/O	I2S BCK(input for I2S slave, output for I2S master)
2	P1.2_LRCK	I/O	I2S LRCK(input for I2S slave, output for I2S master)
3	P1.1_DIN	I/O	I2S Data in(from audio codec)
4	P1.0_DOUT	I/O	I2S Data out(to audio codec)
5	P2.1	A	GPIO If DPDT is mounted on module, this GPIO is used for RF DPDT control. So please don't use this pin.
6	PROG	C	Program mode select, active high, default pull low

			For programming internal flash memory Please leave this pin float for normal operation.
7	P2.0	I	General GPIO Second I2S data output
8	MCLK	O	For audio codec system clock(12.288MHz or 11.2896MHz)
9	DGND	P	System ground
10	VDD	P	VDD (2.7V~3.6V)

Note: P:Power, I/O:GPIO, S:System use only, A:DAC/ADC/USB differential signal, C:control

8. Ordering Information

Module Name: AW5808TR

9. Revision History

Version	Description	date
0.1	Initial version	2019/07/25