USBF4100

USB Firmware Memory

Features

- Firmware Memory Companion for the USB491X Family of USB Controllers
- Targeted for USB 2.0 High-Speed Infotainment Applications Including:
  - Integration with head unit systems
  - First, second, and third row USB media hubs
- Memory Size:
  - 512 KByte (4 Mbit)
- Single Voltage Read and Write Operations:
  - 2.7-3.6V
- Serial Interface Architecture:
  - SPI Compatible: Mode 0 and Mode 3
- High Speed Clock Frequency:
  - 40 MHz
- READ Support:
  - Fast-Read Dual-Output
  - Fast-Read Single I/O
- Superior Reliability:
  - Endurance: 100,000 Cycles
  - Greater than 20 years Data Retention
- Ultra-Low Power Consumption:
  - Active Read Current: 5 mA (typical)
  - Standby Current: 5 µA (typical)
  - Power-down Mode Standby Current: 3 µA (typical)
- Flexible Erase Capability:
  - Uniform 4 KByte sectors
  - Uniform 64 KByte overlay blocks
- Page Program Mode:
  - 256 Bytes/Page
- Fast Erase and Page-Program:
  - Chip Erase Time: 250 ms (typical)
  - Sector Erase Time: 40 ms (typical)
  - Block Erase Time: 80 ms (typical)
  - Page-Program Time: 4 ms/ 256 bytes (typical)
- End-of-Write Detection:
  - Software polling the BUSY bit in Status Register
- Hold Pin (HOLD#):
  - Suspend a serial sequence without deselecting the device
- Write Protection (WP#):
  - Enables/Disables the Lock-Down function of the status register
- Software Write Protection:
  - Write protection through Block-Protection bits in status register
- Temperature Range:
  - Automotive Grade 1: -40°C to 125°C
  - Automotive Grade 2: -40°C to 105°C
  - Automotive Grade 3: -40°C to 85°C
- Packages Available:
  - 8-lead SOIC (150 mils)
  - 8-contact USON (2x3 mm)
- All Devices are RoHS Compliant

Product Description

USBF4100, a USB Firmware memory chip, is a companion to the Microchip Automotive USB Smart Hub devices: USB491X. Factory pre-programming is available for custom firmware and configurations. The USBF4100 memory function assures proper functionality, providing for decreased development time and engineering resource, and overall faster time to market.

The USB Firmware memory family features a four-wire, SPI-compatible interface that allows for a low pin count package, which occupies less board space and ultimately lowers total system costs. It is manufactured with proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches ideal for applications requiring high quality and reliability.

USBF4100 is offered in 8-lead SOIC and 8-contact USON. See Figure 1-1 for the pin assignments.

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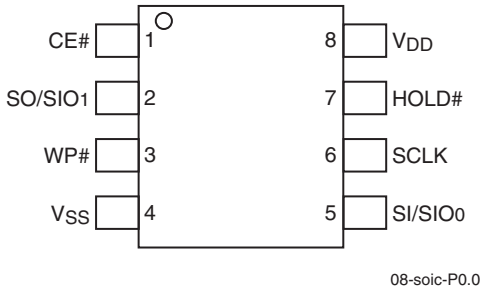
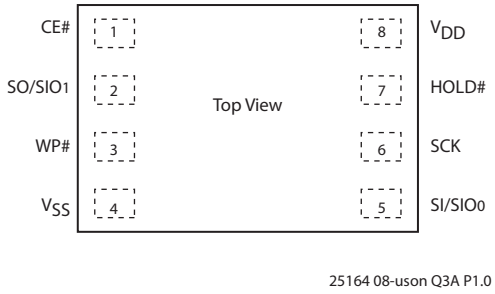
1.0 PIN ASSIGNMENTS

FIGURE 1-1: PIN ASSIGNMENTS



8-Lead SOIC



8-Contact USON

TABLE 1-1: PIN DESCRIPTION

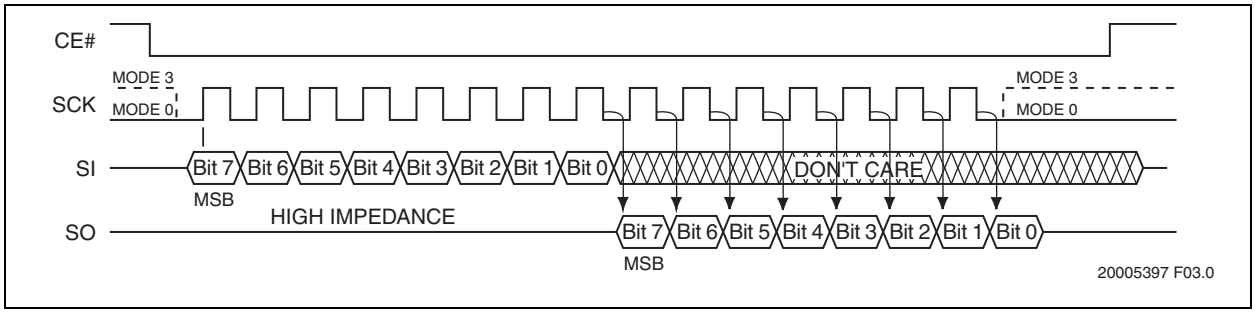
Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the input/output timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
$SIO_{[0:1]}$	Serial Data Input/ Output for Dual I/O Mode	To transfer commands, addresses, or data serially into the device, or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. These pins are used in Dual I/O mode
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence. The device is deselected and placed in Standby mode when CE# is high.
WP#	Write-Protect	The Write-Protect (WP#) pin is used to enable/disable BPL bit in the STATUS register.
HOLD#	Hold	To temporarily stop serial communication with USB Firmware memory while device is selected.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	

2.0 DEVICE OPERATION

USBF4100 is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consist of four control lines: Chip Enable (CE#) is used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The USBF4100 supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 2-1, is the state of the SCK signal when the bus master is in Standby mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

FIGURE 2-1: SPI PROTOCOL



3.0 INSTRUCTIONS

Instructions are used to read, write (Erase and Program), and configure the USBF4100 devices. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. The Write-Enable (WREN) instruction must be executed prior to Sector Erase, Block Erase, Page-Program, Write-Status-Register, or Chip Erase instructions. The complete instructions are provided in Table 3-1. All instructions are synchronized off a high-to-low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the Most Significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read-Status-Register instructions). Any low-to-high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to Standby mode. Instruction commands (Op Code), addresses, and data are all input from the Most Significant bit (MSB) first.

TABLE 3-1: DEVICE OPERATION INSTRUCTIONS

Instruction	Description	Op Code Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)	Maximum Frequency
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞	25 MHz
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞	40 MHz
Fast-Read Dual-Output	Read Memory with Dual Output	0011 1011b (3BH)	3	1[3]	1 to ∞[3]	
Fast-Read Dual I/O	Read Memory with Dual Address Input and Data Output	1011 1011b (BBH)	3[3]	1[3]	1 to ∞[3]	
4 KByte Sector Erase[4]	Erase 4 KByte of memory array	0010 0000b (20H) 1101 0111b (D7H)	3	0	0	
64 KByte Block Erase[5]	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0	
Chip Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0	
Page-Program	To program up to 256 Bytes	0000 0010b (02H)	3	0	1 to 256	
RDSR[6]	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞	
WRSR	Write-Status-Register	0000 0001b (01H)	0	0	1	
WREN	Write-Enable	0000 0110b (06H)	0	0	0	
WRDI	Write-Disable	0000 0100b (04H)	0	0	0	
RDID[7, 8]	Read-ID	1010 1011b (ABH)	3	0	1 to ∞	
JEDEC-ID	JEDEC ID Read	1001 1111b (9FH)	0	0	4 to ∞	
DPD	Deep Power-Down Mode	1011 1001b (B9H)	0	0	0	
RDPD[8]	Release from Deep Power-Down or Read ID	1010 1011b (ABH)	0	0	0	

1. One bus cycle is eight clock periods.
2. Address bits above the Most Significant bit of each density can be V_{IL} or V_{IH}.
3. One bus cycle is four clock periods in Dual Operation
4. 4 KByte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
5. 64 KByte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
6. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
7. Device ID = 6EH is read after three dummy address bytes. The Device ID output stream is continuous until terminated by a low-to-high transition on CE#.
8. The instructions Release from Deep Power-Down and Read-ID are similar instructions (ABH). Executing Read-ID requires the ABH instruction, followed by 24 dummy address bits to retrieve the Device ID. Release from Deep Power-Down only requires the instruction ABH. JEDEC-ID data = 62H 06H 13H 00H.

4.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -55°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[1] . . . . . 50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 4-1: OPERATING RANGE

Range	Ambient Temp	V_{DD}
Automotive Grade 1	-40°C to +125°C	2.7 - 3.6V
Automotive Grade 2	-40°C to +105°C	2.7 - 3.6V
Automotive Grade 3	-40°C to +85°C	2.7 - 3.6V

TABLE 4-2: AC CONDITIONS OF TEST

Input Rise/Fall Time	Output Load
5ns	C_L = 30 pF

4.1 Power-Up Specifications

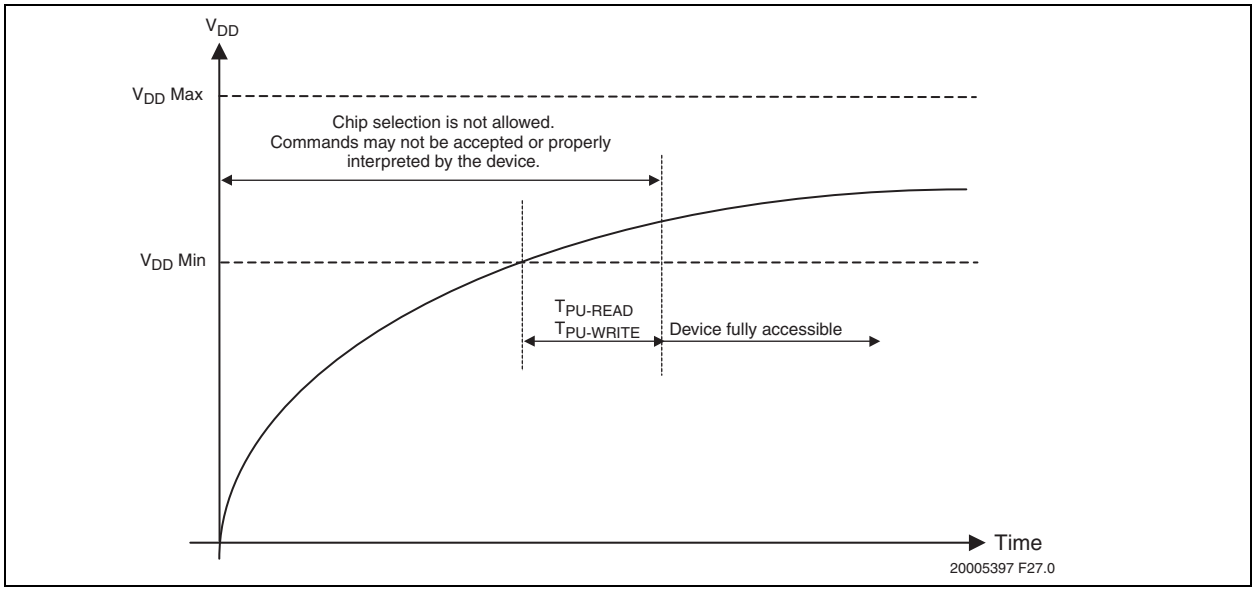
All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.3V in less than 330 ms). See Table 4-3 and Figure 4-2 for more information.

TABLE 4-3: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$ [1]	V_{DD} Min to Read Operation	100	µs
$T_{PU-WRITE}$ [1]	V_{DD} Min to Write Operation	100	µs

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 4-1: POWER-UP TIMING DIAGRAM



4.2 Hardware Data Protection

USBF4100 provides a power-up reset function. To ensure that the power reset circuit will operate correctly, the device must meet the conditions shown in Figure 4-2 and Table 4-4. Microchip does not guarantee the data in the event of an instantaneous power failure that occurs during a Write operation.

FIGURE 4-2: POWER-DOWN TIMING DIAGRAM

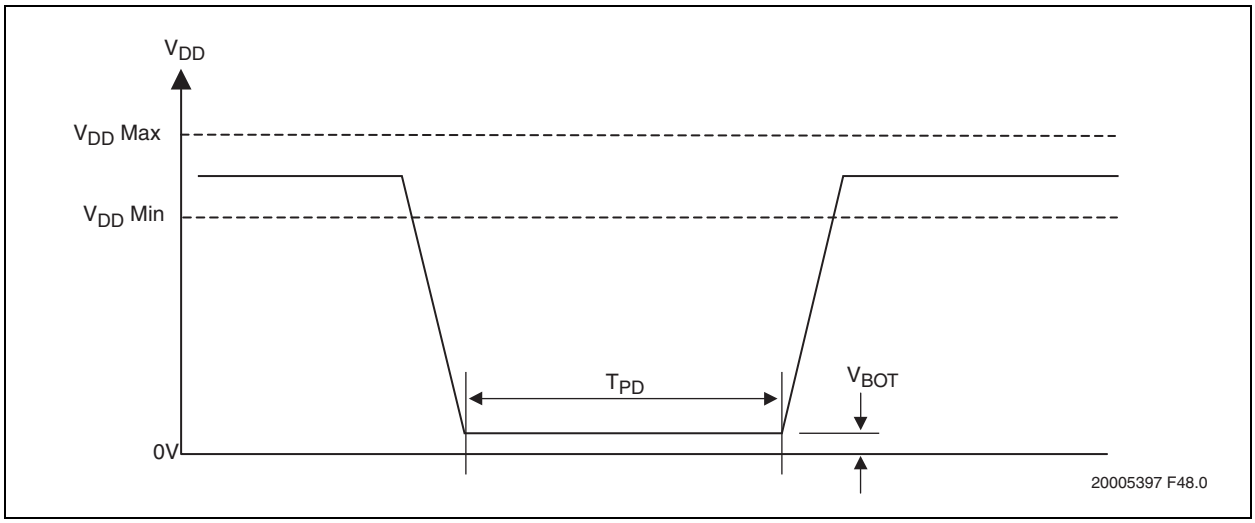


TABLE 4-4: RECOMMENDED SYSTEM POWER-DOWN TIMINGS

Symbol	Parameter	Min	Max	Units
T_{PD}	Power-down time	10		ms
V_{BOT}	Power-down voltage		0.2	V

4.3 Software Data Protection

USBF4100 prevents unintentional operations by not recognizing commands under the following conditions:

- After inputting a Write command, if the rising CE# edge timing is not in a bus cycle (8 CLK units of SCK)
- When the Page-Program data is not in 1-byte increments
- If the Write Status Register instruction is input for two bus cycles or more.

4.4 Decoupling Capacitor

A 0.1µF ceramic capacitor must be provided for each device and connected between V_{DD} and V_{SS} to ensure that the device will operate correctly.

4.5 DC Characteristics

TABLE 4-5: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits				Test Conditions
		Min	Typ[1]	Max	Units	
I_{DDR}	Read Current			6	mA	CE#=0.1 V_{DD}/0.9 V_{DD}@25 MHz, SO=open; Single I/O
I_{DDR2}	Read Current			10	mA	CE#=0.1 V_{DD}/0.9V_{DD}@40 MHz, SO=open
I_{DDR3}	Read Current			12	mA	CE#=0.1 V_{DD}/0.9V_{DD}@40 MHz, SO=open; Dual I/O;
I_{DDW}	Program and Erase Current			15	mA	CE#=V_{DD}
I_{SB}	Standby Current			50	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{DPD}	Deep Power-Down			10	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current			2	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			2	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage	-0.3		0.3	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD}+0.3	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage			0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2			V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

1. Value characterized, not fully tested in production.

TABLE 4-6: CAPACITANCE (T_A = 25°C, F=1 MHz, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 4-7: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	100,000	Cycles	JEDEC Standard A117
	Status Register Write Cycle	100,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	20	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

4.6 AC Characteristics

TABLE 4-8: AC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits - 25 MHz			Limits - 40 MHz			Units
		Min	Typical	Max	Min	Typical	Max	
F_{CLK}[1]	Serial Clock Frequency			25			40	MHz
T_{SCKH}	Serial Clock High Time	18			11.5			ns
T_{SCKL}	Serial Clock Low Time	18			11.5			ns
T_{SCKR}	Serial Clock Rise Time			5			5	ns
T_{SCKF}	Serial Clock Fall Time			5			5	ns
T_{CES}[2]	CE# Active Setup Time	8			8			ns
T_{CEH}[2]	CE# Active Hold Time	8			8			ns
T_{CHS}[2]	CE# Not Active Setup Time	8			8			ns
T_{CHH}[2]	CE# Not Active Hold Time	8			8			ns
T_{CPH}	CE# High Time	25			25			ns
T_{CHZ}	CE# High to High-Z Output			8			8	ns
T_{CLZ}	SCK Low to Low-Z Output	0			0			ns
T_{DS}	Data In Setup Time	2			2			ns
T_{DH}	Data In Hold Time	5			5			ns
T_{HLS}	HOLD# Low Setup Time	5			5			ns
T_{HHS}	HOLD# High Setup Time	5			5			ns
T_{HLH}	HOLD# Low Hold Time	5			5			ns
T_{HHH}	HOLD# High Hold Time	5			5			ns
T_{HZ}	HOLD# Low to High-Z Output			9			9	ns
T_{LZ}	HOLD# High to Low-Z Output			9			9	ns
T_{OH}	Output Hold from SCK Change	1			1			ns
T_{V}	Output Valid from SCK			11			11	ns
T_{WPS}	WP# Setup Time	20			20			ns
T_{WPH}	WP# Hold Time	20			20			ns
T_{WRSR}	Status Register Write Time			10			15	ms
T_{DPD}	CE# High to Deep Power-Down			3			3	µs
T_{SBR}	Deep Power-Down (CE# High) to Standby Mode			3			3	µs
T_{SE}	Sector Erase		40	150		40	150	ms
T_{BE}	Block Erase		80	250		80	250	ms
T_{CE}	Chip Erase		0.25	2		0.25	2	s
T_{PP}	Page-Program (256 Byte)		4	5		4	5	ms

1. Maximum clock frequency for Read instruction, 03H, is 25 MHz
2. Relative to SCK

FIGURE 4-3: SERIAL OUTPUT TIMING DIAGRAM

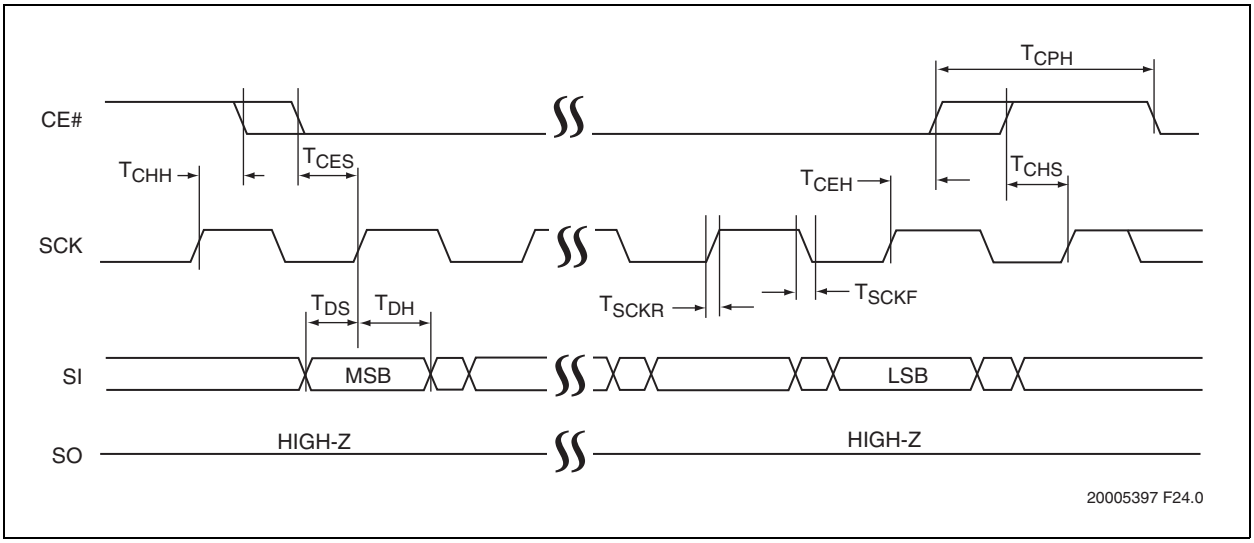


FIGURE 4-4: SERIAL INPUT TIMING DIAGRAM

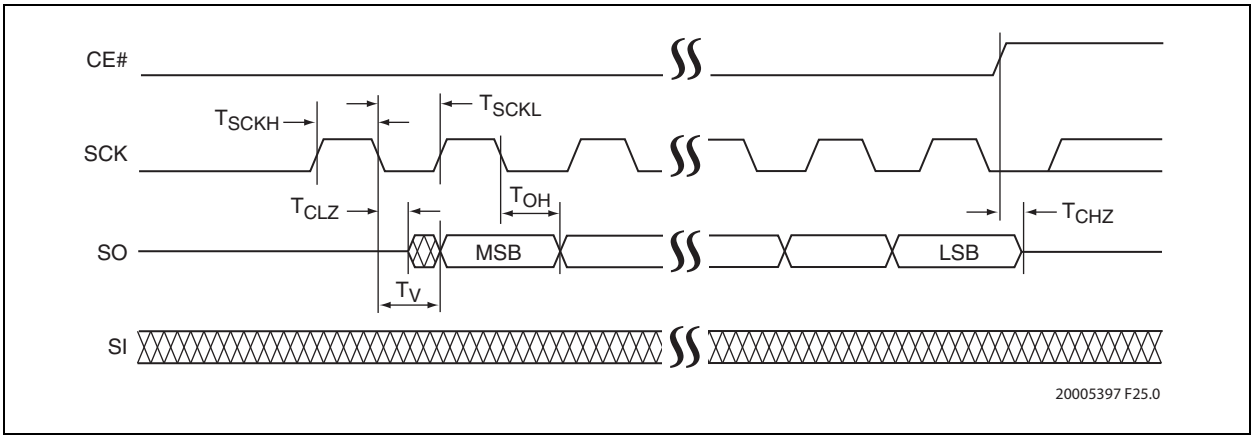


FIGURE 4-5: HOLD TIMING DIAGRAM

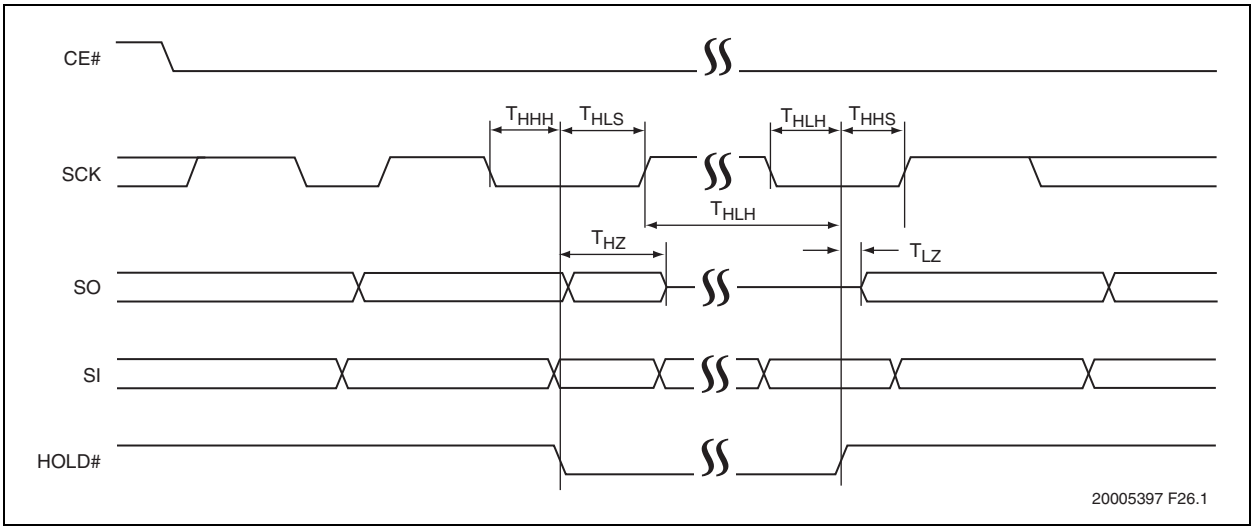


FIGURE 4-6: STATUS REGISTER WRITE TIMING

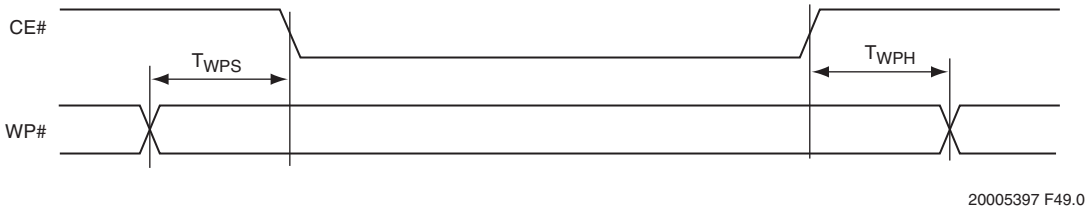
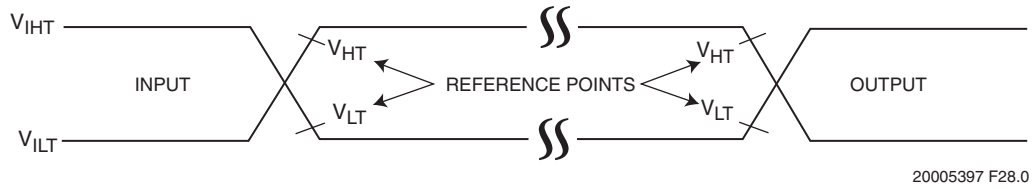


FIGURE 4-7: AC INPUT/OUTPUT REFERENCE WAVEFORMS



AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic '1' and V_{ILT} ($0.1V_{DD}$) for a logic '0'. Measurement reference points for inputs and outputs are V_{HT} ($0.5V_{DD}$) and V_{LT} ($0.5V_{DD}$). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 4-8: PAGE-PROGRAM FLOW CHART

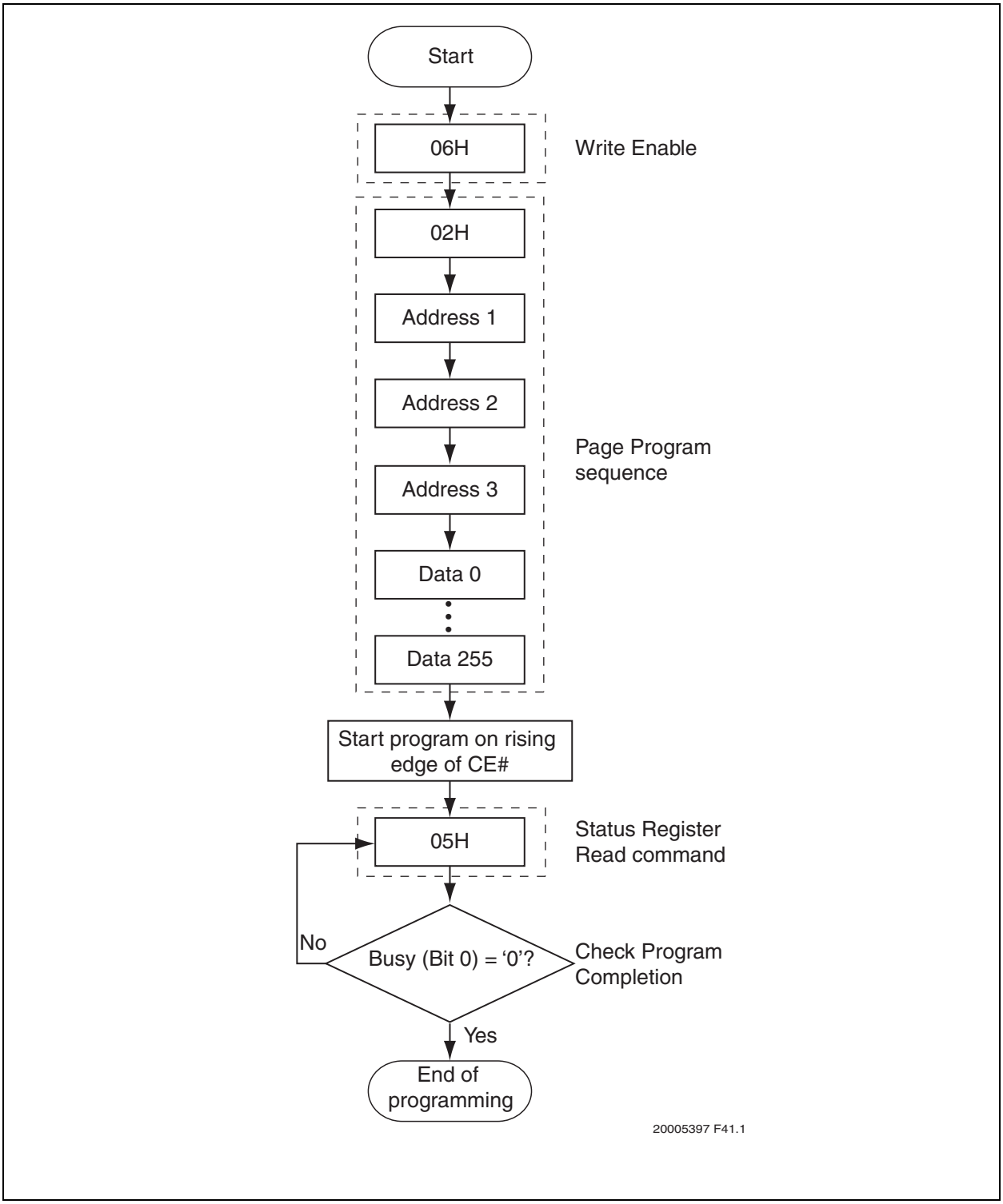


FIGURE 4-9: SECTOR ERASE OR 64-KBYTE BLOCK ERASE FLOW CHART

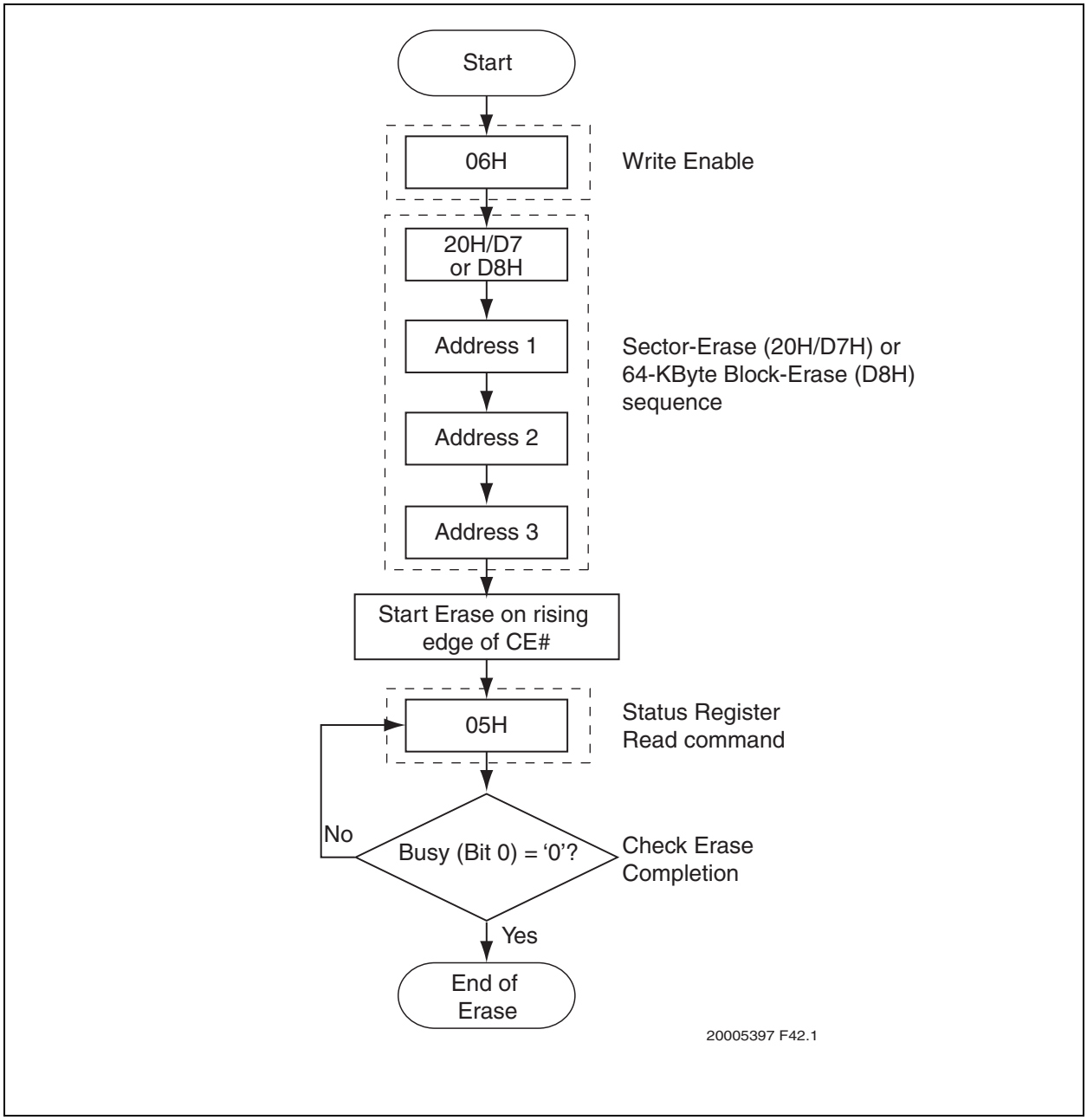


FIGURE 4-10: CHIP ERASE FLOW CHART

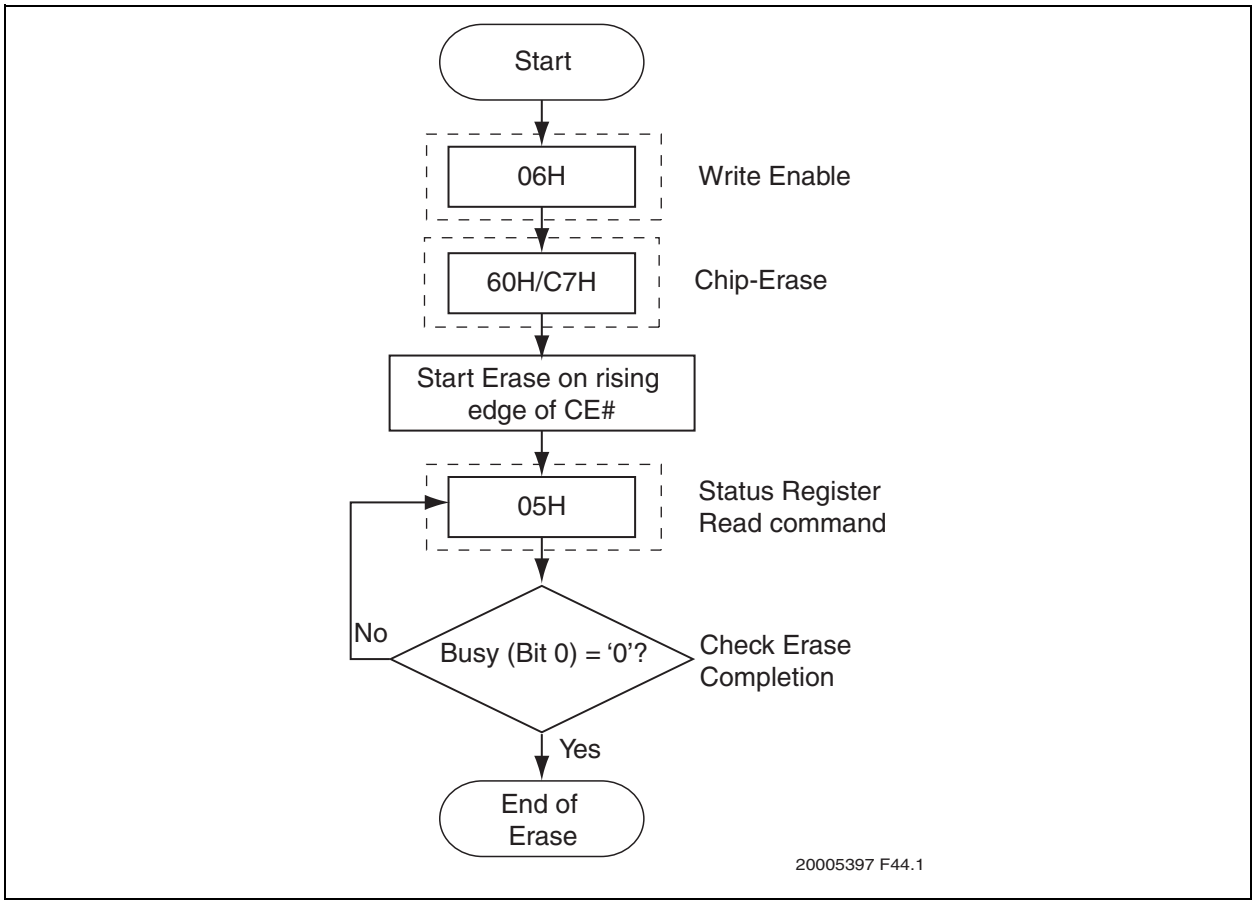
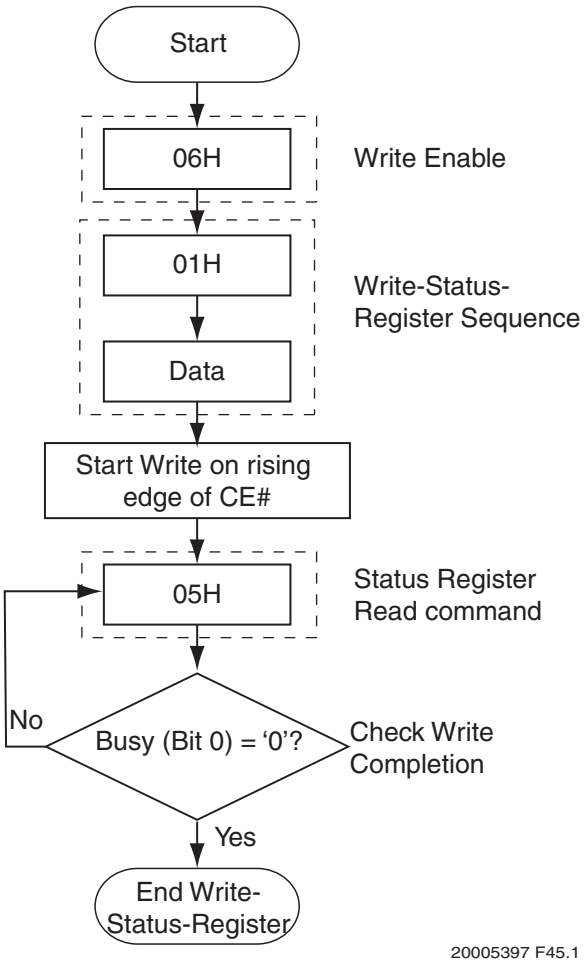


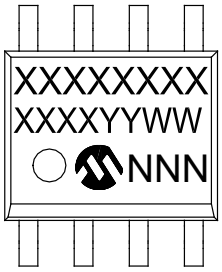
FIGURE 4-11: WRITE-STATUS-REGISTER (WRSR) FLOW CHART



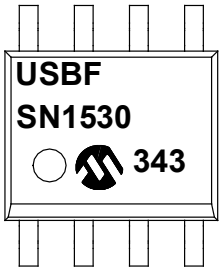
5.0 PACKAGING DIAGRAMS

5.1 Package Marking

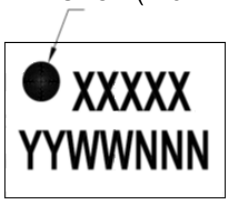
8-Lead SOIC (3.90 mm)



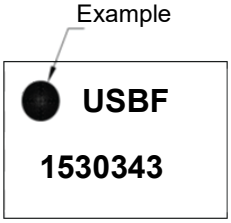
Example



8-Lead USON (2x3 mm)



Example



Part Number	Package Type	1st Line Marking Codes
USBF4100	SOIC	USBF
USBF4100	USON	USBF

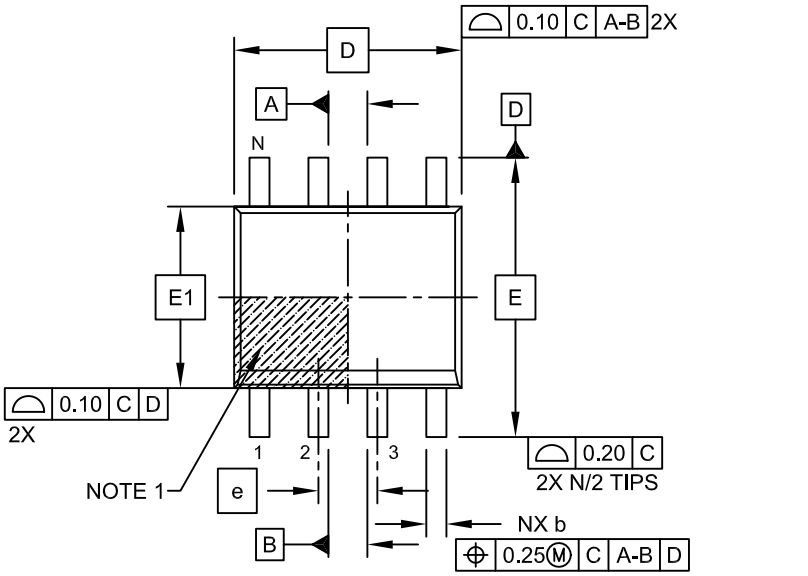
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC® designator (e3) , the marking will only appear on the outer carton or reel label.

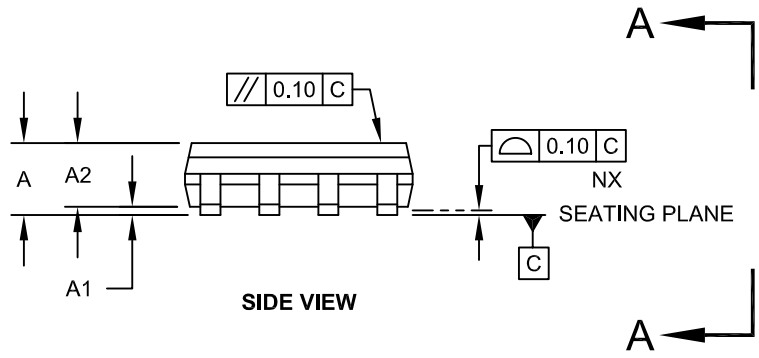
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

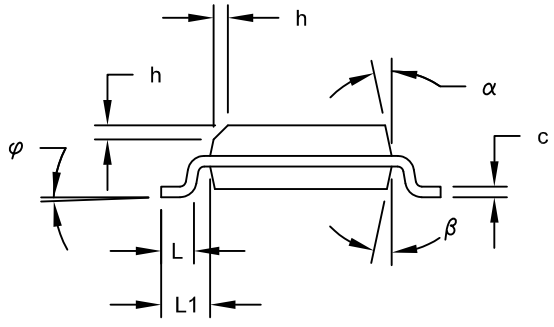
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

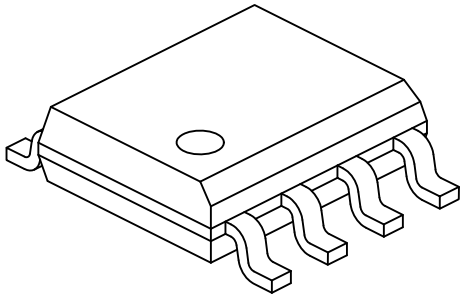


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

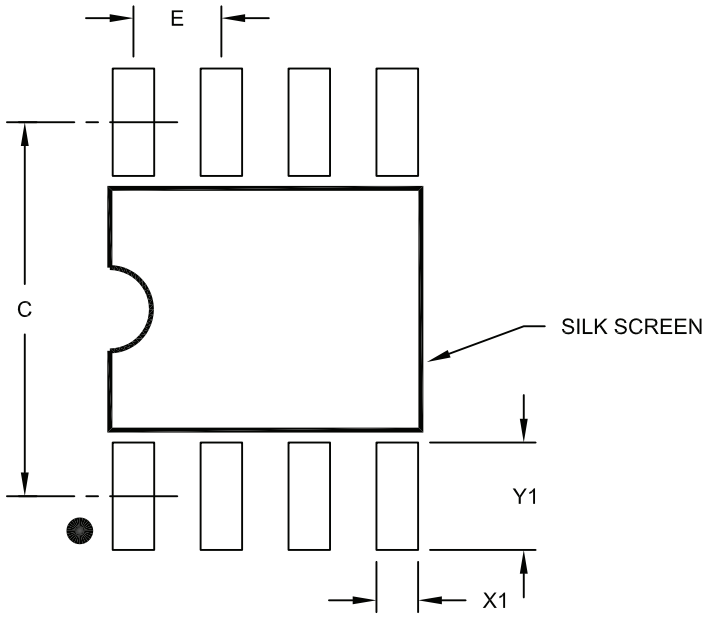
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

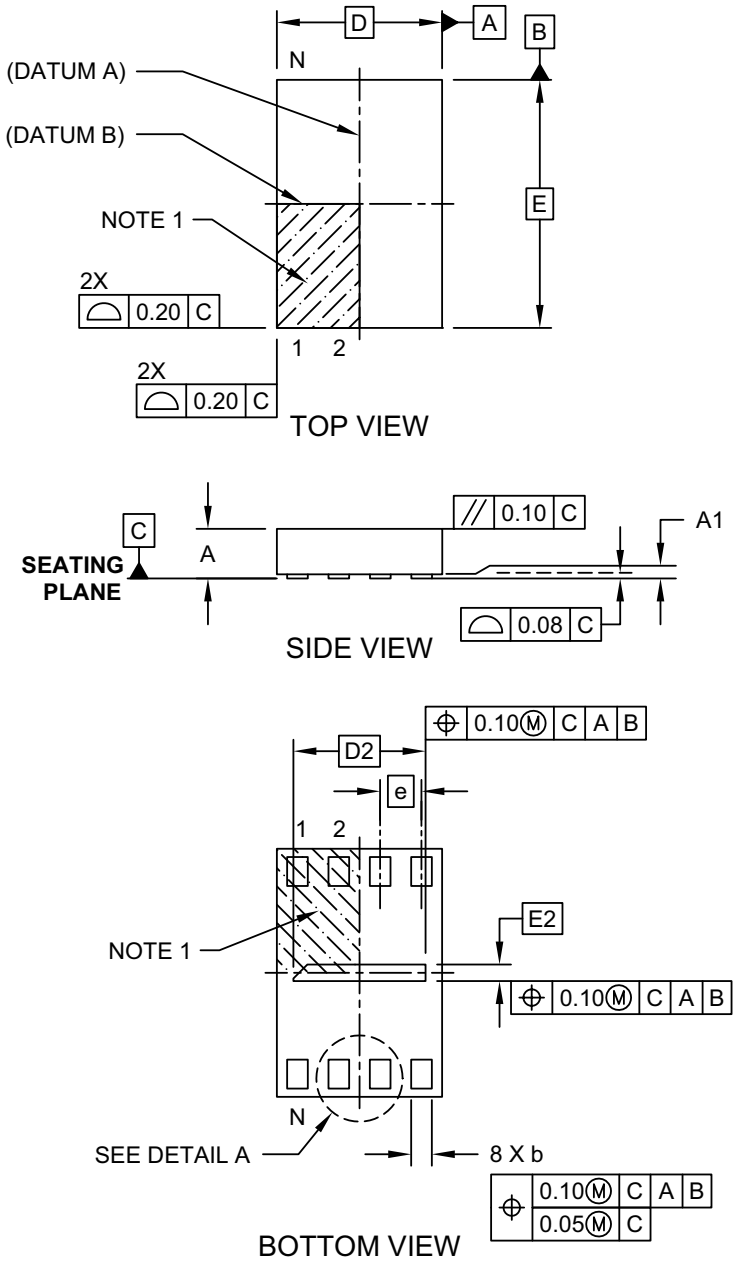
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Ultra Thin Small Outline No Lead Package (NP) - 2x3 mm Body [USON] [Also called UDFN]

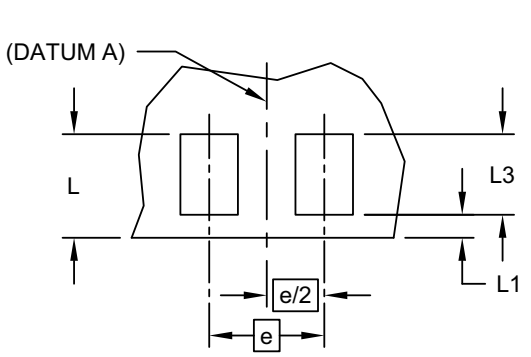
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



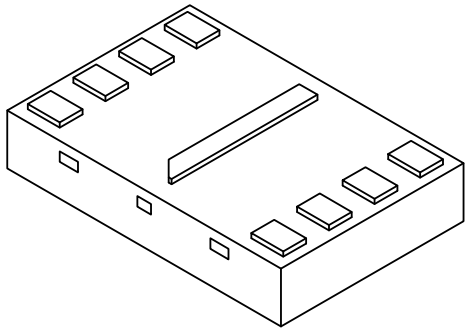
Microchip Technology Drawing C04-203C [NP] Sheet 1 of 2

8-Lead Plastic Ultra Thin Small Outline No Lead Package (NP) - 2x3 mm Body [USON] [Also called UDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.45	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Overall Width	D		2.00 BSC	
Exposed Pad Width	D2	1.50	1.60	1.70
Overall Length	E		3.00 BSC	
Exposed Pad Length	E2	0.10	0.20	0.30
Terminal Width	b	0.20	0.25	0.30
Package Edge to Terminal Edge	L	0.40	0.45	0.50
Package Edge to Terminal Edge	L1	—	0.10	—
Terminal Length	L3	0.30	0.35	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

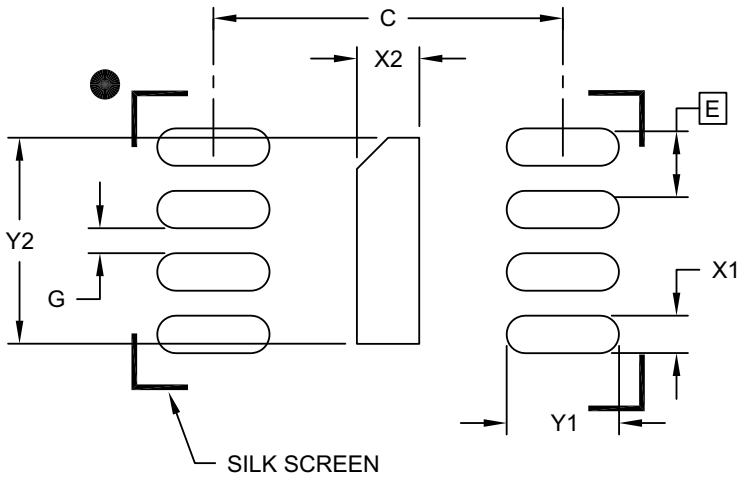
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-203C [NP] Sheet 2 of 2

8-Lead Plastic Ultra Thin Small Outline No Lead Package (NP) - 2x3 mm Body [USON] [Also called UDFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Terminal Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			0.25
Optional Center Pad Length	Y2			1.65
Terminal Pad Spacing	C		2.80	
Terminal Pad Width (X8)	X1			0.30
Terminal Pad Length (X8)	Y1			0.90
Mininum Between Terminal Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2203B [NP]

APPENDIX A: REVISION HISTORY

April 2020

- Added automotive grade 1/extended temperature.

June 2018

- Initial release.

6.0 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XX	XXX
Device	Tape/Reel Indicator	Temperature	Package	Grade

Device:	USBF4100	= USB Firmware Memory
Tape and Reel Flag:	T	= Tape and Reel
Temperature:	I	= -40°C to +85°C
	V	= -40°C to +105°C
	E	= -40°C to +125°C
Package:	SN	= SOIC (3.90 mm Body), 8-lead
	NP	= USON (2x3 mm Body), 8-contact
Grade:	VAO	= Automotive Grade

Valid Combinations:

USBF4100-I/SNVAO
USBF4100T-I/SNVAO
USBF4100T-I/NPVAO
USBF4100-V/SNVAO
USBF4100T-V/SNVAO
USBF4100T-V/NPVAO
USBF4100-E/SNVAO
USBF4100T-E/SNVAO

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