USBF1600

USB Firmware Memory

Features

- Read and Write Operations
  - 2.7-3.6V
- x1/x2/x4 Serial Peripheral Interface (SPI) Protocol
- Firmware memory companion for the USB491X family of USB controllers
- Targeted for USB 2.0 High-Speed infotainment applications including:
  - Integration with head unit systems
  - First, second and third row USB media hubs
  - Power delivery
- Memory Size:
  - 2 MByte (16 Mbit)
- High Speed Clock Frequency
  - 104 MHz max
- Superior Reliability
  - Endurance: 100,000 Cycles (min)
  - Greater than 100 years Data Retention
- Low Power Consumption:
  - Active Read current: 15 mA (typical @ 104 MHz)
  - Standby Current: 15 µA (typical)
- Fast Erase Time
  - Sector/Block Erase: 18 ms (typ), 25 ms (max)
  - Chip Erase: 35 ms (typ), 50 ms (max)
- Page-Program
  - 256 Bytes per page in x1 or x4 mode
- End-of-Write Detection
  - Software polling the BUSY bit in status register
- Flexible Erase Capability
  - Uniform 4 KByte sectors
  - Four 8 KByte top and bottom parameter overlay blocks
  - One 32 KByte top and bottom overlay blocks
  - Uniform 64 KByte overlay blocks
- Write-Suspend
  - Suspend Program or Erase operation to access another block/sector
- Software Reset (RST) mode
- Software Write Protection
  - Individual-Block Write Protection with permanent lock-down capability
    - 64 KByte blocks, two 32 KByte blocks, and eight 8 KByte parameter blocks
  - Read Protection on top and bottom 8 KByte parameter blocks
  - Security ID
  - One-Time Programmable (OTP) 2 KByte, Secure ID
    - 64 bit unique, factory pre-programmed identifier
    - User-programmable area
- Temperature Range
  - Industrial: -40°C to +85°C
  - Industrial +: -40°C to +105°C
- Packages Available
  - 8-contact WDFN (6mm x 5mm)
  - 8-lead SOIC (3.90 mm)
- All devices are RoHS compliant
- Automotive AECQ-100 Grade 2 and Grade 3 qualified

Product Description

USBF1600, a USB Firmware memory chip, is a companion to the Microchip Automotive USB Smart Hub devices: USB491X. Factory pre-programming is available for custom firmware and configurations. The USBF1600 memory function assures proper functionality, providing for decreased development time and engineering resources, and overall faster time to market.

The USB Firmware memory features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin count package.

USBF1600 is manufactured with proprietary, high-performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturing compared with alternate approaches.

USBF1600 is offered in 8-contact WDFN (6 mm x 5 mm), and 8-lead SOIC (3.90 mm). See Figures 1-1 through 1-2 for pin assignments.

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1.0 PIN DESCRIPTIONS

FIGURE 1-1: PIN DESCRIPTION FOR 8-CONTACT WDFN

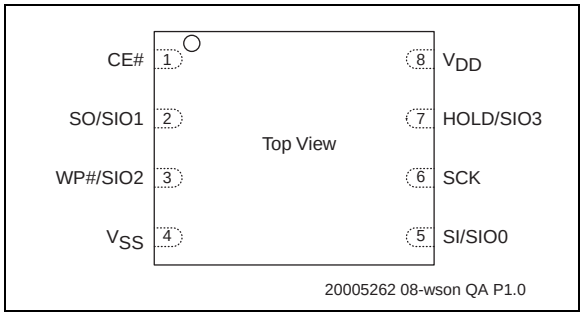


FIGURE 1-2: PIN DESCRIPTION FOR 8-LEAD SOIC

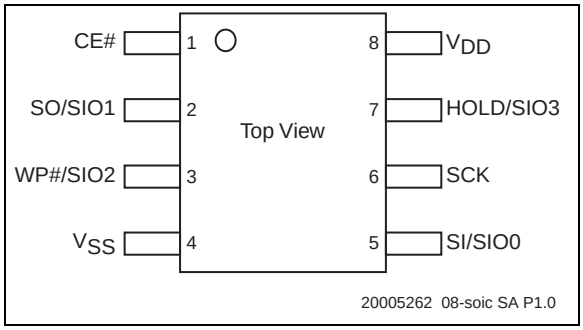


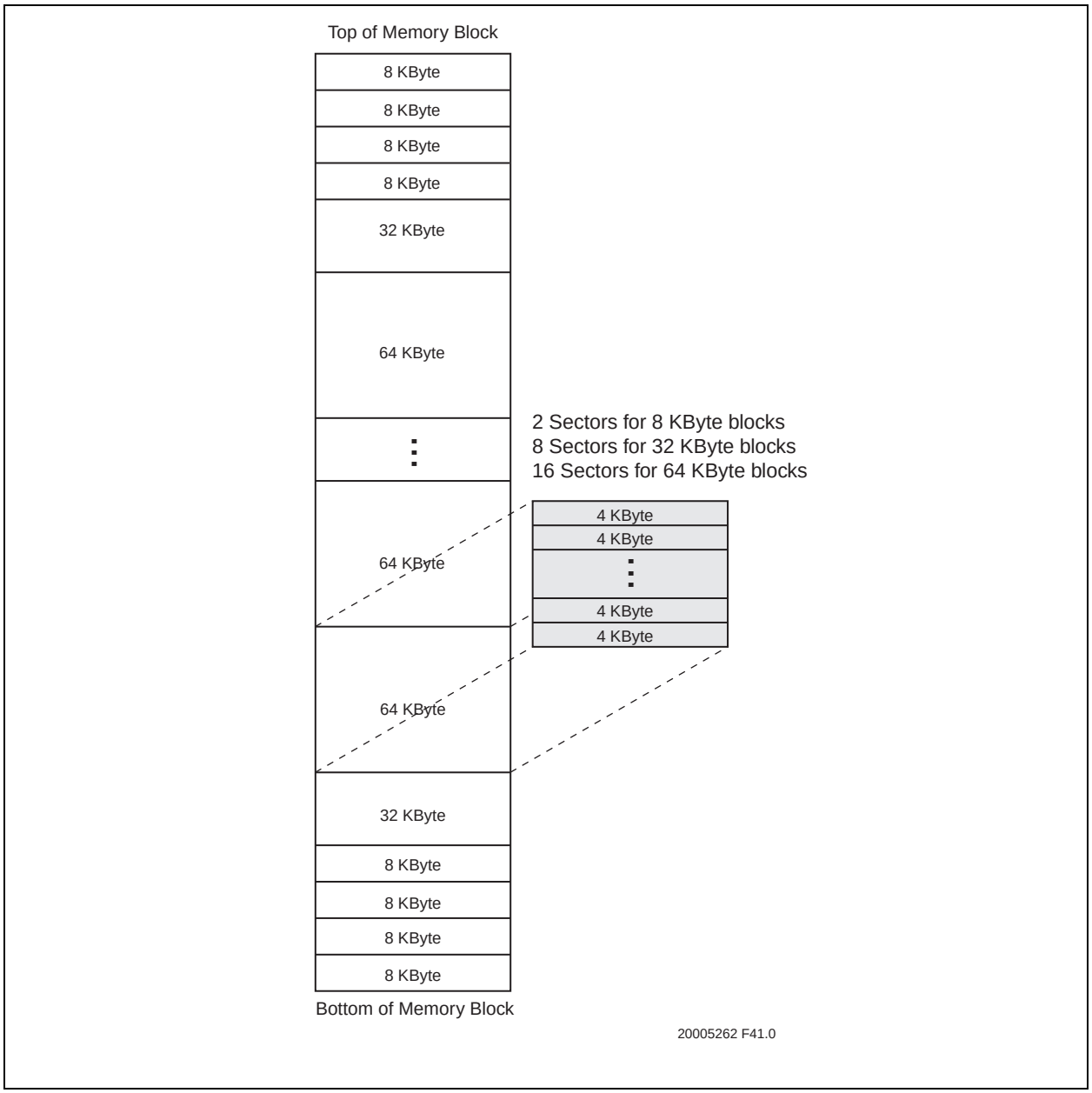
TABLE 1-1: PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SIO[3:0]	Serial Data Input/Output	To transfer commands, addresses, or data serially into the device or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. The Enable Quad I/O (EQIO) command instruction configures these pins for Quad I/O mode.
SI	Serial Data Input for SPI mode	To transfer commands, addresses or data serially into the device. Inputs are latched on the rising edge of the serial clock. SI is the default state after a Power-on Reset.
SO	Serial Data Output for SPI mode	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock. SO is the default state after a power on reset.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence; or in the case of Write operations, for the command/data input sequence.
WP#	Write Protect	The WP# is used in conjunction with the WPEN and IOC bits in the Configuration register to prohibit write operations to the Block-Protection register. This pin only works in SPI, single-bit and dual-bit Read mode.
HOLD#	Hold	Temporarily stops serial communication with the SPI Flash memory while the device is selected. This pin only works in SPI, single-bit and dual-bit Read mode and must be tied high when not in use.
V_{DD}	Power Supply	To provide power supply voltage.
V_{SS}	Ground	

2.0 MEMORY ORGANIZATION

The USBF1600 SQI memory array is organized in uniform, 4 KByte erasable sectors with the following erasable blocks: eight 8 KByte parameter, two 32 KByte overlay, and thirty 64 KByte overlay blocks. See Figure 2-1.

FIGURE 2-1: MEMORY MAP



3.0 DEVICE OPERATION

USBF1600 supports both Serial Peripheral Interface (SPI) bus protocol and a 4-bit multiplexed SQI bus protocol. To provide backward compatibility to traditional SPI Serial Flash devices, the device's initial state after a power-on reset is SPI mode which supports multi-I/O (x1/x2/x4) Read/Write commands. A command instruction configures the device to SQI mode. The dataflow in the SQI mode is similar to the SPI mode, except it uses four multiplexed I/O signals for command, address, and data sequence.

The device supports both Mode 0 (0,0) and Mode 3 (1,1) bus operations. The difference between the two modes is the state of the SCK signal when the bus master is in stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data I/O (SIO[3:0]) is sampled at the rising edge of the SCK clock signal for input, and driven after the falling edge of the SCK clock signal for output. The traditional SPI protocol uses separate input (SI) and output (SO) data signals as shown in Figure 3-1. The SQI protocol uses four multiplexed signals, SIO[3:0], for both data in and data out, as shown in Figure 3-2. This means the SQI protocol quadruples the traditional bus transfer speed at the same clock frequency, without the need for more pins on the package.

FIGURE 3-1: SPI PROTOCOL

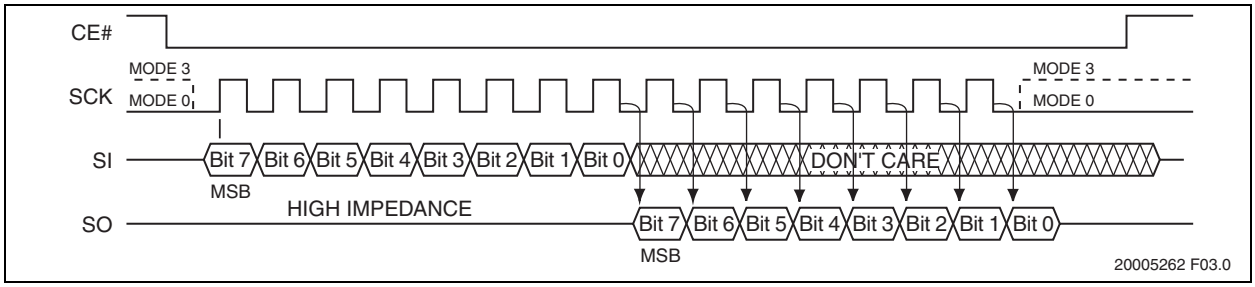
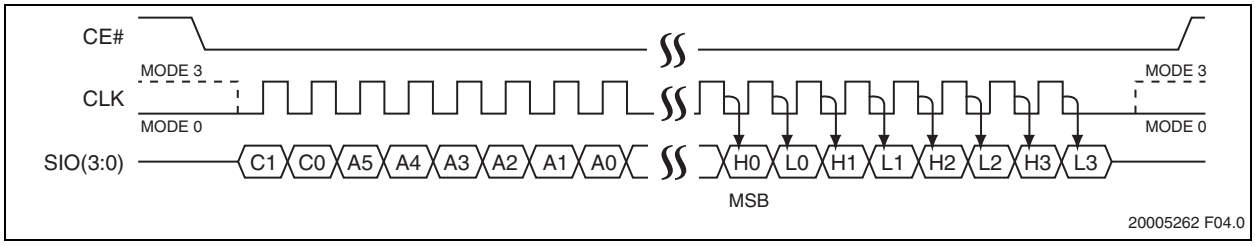


FIGURE 3-2: SERIAL QUAD I/O PROTOCOL



4.0 INSTRUCTIONS

Instructions are used to read, write (erase and program), and configure the USBF1600. The complete list of the instructions is provided in Table 4-1.

TABLE 4-1: DEVICE OPERATION INSTRUCTIONS FOR USBF1600

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq
			SPI	SQI				
Configuration								
NOP	No Operation	00H	X	X	0	0	0	104 MHz
RSTEN	Reset Enable	66H	X	X	0	0	0	
RST[4]	Reset Memory	99H	X	X	0	0	0	
EQIO	Enable Quad I/O	38H	X		0	0	0	
RSTQIO[5]	Reset Quad I/O	FFH	X	X	0	0	0	
RDSR	Read Status Register	05H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
WRSR	Write Status Register	01H	X	X	0	0	2	
RDCR	Read Configuration Register	35H	X		0	0	1 to ∞	
				X	0	1	1 to ∞	
Read								
Read	Read Memory	03H	X		3	0	1 to ∞	40 MHz
High-Speed Read	Read Memory at Higher Speed	0BH		X	3	3	1 to ∞	104 MHz
			X		3	1	1 to ∞	
SQOR[6]	SPI Quad Output Read	6BH	X		3	1	1 to ∞	
SQIOR[7]	SPI Quad I/O Read	EBH	X		3	3	1 to ∞	
SDOR[8]	SPI Dual Output Read	3BH	X		3	1	1 to ∞	
SDIOR[9]	SPI Dual I/O Read	BBH	X		3	1	1 to ∞	
SB	Set Burst Length	C0H	X	X	0	0	1	
RBSQI	SQI Read Burst with Wrap	0CH		X	3	3	n to ∞	
RBSPI[7]	SPI Read Burst with Wrap	ECH	X		3	3	n to ∞	
Identification								
JEDEC-ID	JEDEC-ID Read	9FH	X		0	0	3 to ∞	104 MHz
Quad J-ID	Quad I/O J-ID Read	AFH		X	0	1	3 to ∞	
SFDP	Serial Flash Discoverable Parameters	5AH	X		3	1	1 to ∞	
Write								
WREN	Write Enable	06H	X	X	0	0	0	104 MHz
WRDI	Write Disable	04H	X	X	0	0	0	
SE[10]	Erase 4 KBytes of Memory Array	20H	X	X	3	0	0	
BE[11]	Erase 64, 32 or 8 KBytes of Memory Array	D8H	X	X	3	0	0	
CE	Erase Full Array	C7H	X	X	0	0	0	
PP	Page Program	02H	X	X	3	0	1 to 256	
SPI Quad PP[6]	SQI Quad Page Program	32H	X		3	0	1 to 256	

TABLE 4-1: DEVICE OPERATION INSTRUCTIONS FOR USBF1600

Instruction	Description	Command Cycle[1]	Mode		Address Cycle(s)[2, 3]	Dummy Cycle(s)[3]	Data Cycle(s)[3]	Max Freq
			SPI	SQI				
WRSU	Suspends Program/Erase	B0H	X	X	0	0	0	104 MHz
WRRE	Resumes Program/Erase	30H	X	X	0	0	0	
Protection								
RBPR	Read Block-Protection Register	72H	X		0	0	1 to 6	104 MHz
				X	0	1	1 to 6	
WBPR	Write Block-Protection Register	42H	X	X	0	0	1 to 6	
LBPR	Lock Down Block-Protection Register	8DH	X	X	0	0	0	
nVWLDR	non-Volatile Write Lock-Down Register	E8H	X	X	0	0	1 to 6	
ULBPR	Global Block Protection Unlock	98H	X	X	0	0	0	
RSID	Read Security ID	88H	X		2	1	1 to 2048	
				X	2	3	1 to 2048	
PSID	Program User Security ID area	A5H	X	X	2	0	1 to 256	
LSID	Lockout Security ID Programming	85H	X	X	0	0	0	
Power Saving								
DPD	Deep Power-down Mode	B9H	X	X	0	0	0	104 MHz
RDPD	Release from Deep Power-down and Read ID	ABH	X	X	3	0	1 to ∞	

1. Command cycle is two clock periods in SQI mode and eight clock periods in SPI mode.
2. Address bits above the most significant bit of each density can be V_{IL} or V_{IH}.
3. Address, Dummy/Mode bits, and Data cycles are two clock periods in SQI and eight clock periods in SPI mode.
4. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
5. Device accepts eight-clock command in SPI mode, or two-clock command in SQI mode.
6. Data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
7. Address, Dummy/Mode bits, and data cycles are two clock periods. IOC bit must be set to '1' before issuing the command.
8. Data cycles are four clock periods.
9. Address, Dummy/Mode bits, and Data cycles are four clock periods.
10. Sector Addresses: Use A_{MS} - A_{12}, remaining address are don't care, but must be set to V_{IL} or V_{IH}.
11. Blocks are 64 KByte, 32 KByte, or 8KByte, depending on location. Block Erase Address: A_{MS} - A_{16} for 64 KByte; A_{MS} - A_{15} for 32 KByte; A_{MS} - A_{13} for 8 KByte. Remaining addresses are don't care, but must be set to V_{IL} or V_{IH}.

5.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[1] . . . . . 50 mA

1. Output shorted for no more than one second. No more than one output shorted at a time.

TABLE 5-1: OPERATING RANGE

Range	Ambient Temp	V_{DD}
Industrial	-40°C to +85°C	2.3V-3.6V
Industrial Plus	-40°C to +105°C	

TABLE 5-2: AC CONDITIONS OF TEST[1]

Input Rise/Fall Time	Output Load
3ns	C_L = 30 pF

1. See Figure 7-5

5.1 Power-Up Specifications

All functionalities and DC specifications are specified for a V_{DD} ramp rate of greater than 1V per 100 ms (0V to 3.0V in less than 300 ms). See Table 5-3 and Figure 5-1 for more information.

When V_{DD} drops from the operating voltage to below the minimum V_{DD} threshold at power-down, all operations are disabled and the device does not respond to commands. Data corruption may result if a power-down occurs while a Write-Registers, program, or erase operation is in progress. See Figure 5-2.

TABLE 5-3: RECOMMENDED SYSTEM POWER-UP/DOWN TIMINGS

Symbol	Parameter	Minimum	Max	Units	Condition
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	100		µs	
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	100		µs	
T_{PD}[1]	Power-down Duration	100		ms	
V_{OFF}	V_{DD} off time		0.3	V	0V recommended

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

FIGURE 5-1: POWER-UP TIMING DIAGRAM

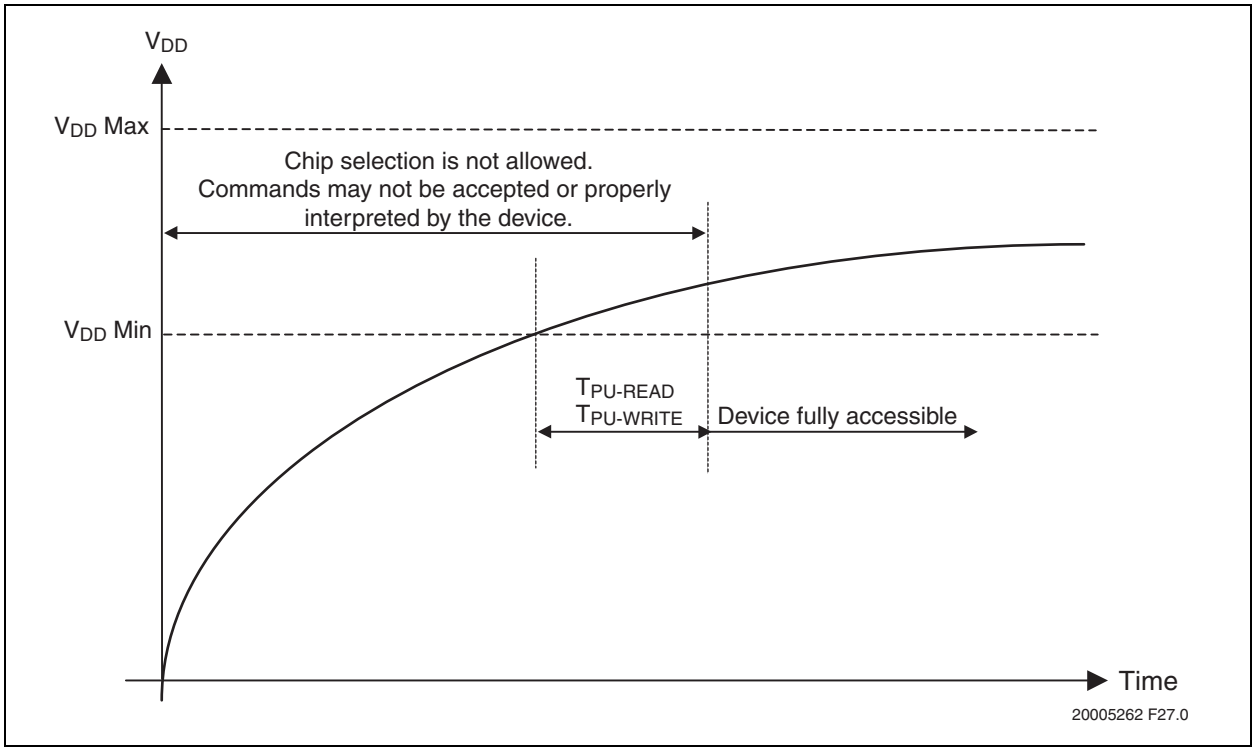
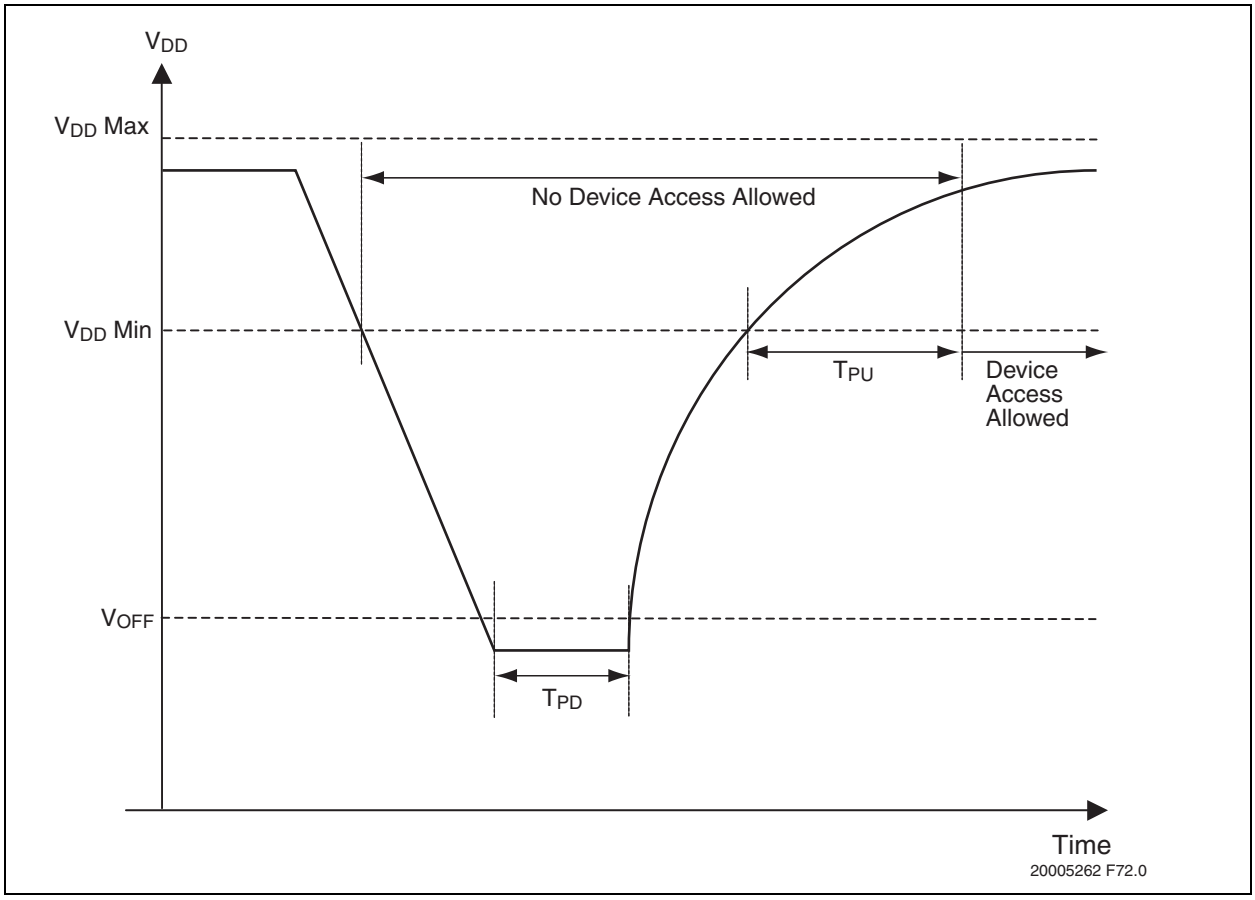


FIGURE 5-2: POWER-DOWN AND VOLTAGE DROP DIAGRAM



6.0 DC CHARACTERISTICS

TABLE 6-1: DC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits				Test Conditions
		Min	Typ	Max	Units	
I_{DDR1}	Read Current		8	15	mA	$V_{DD=}V_{DD}$ Max, CE#=0.1 V_{DD}/0.9 V_{DD}@40 MHz, SO=open
I_{DDR2}	Read Current			20	mA	V_{DD} = V_{DD} Max, CE#=0.1 V_{DD}/0.9 V_{DD}@104 MHz, SO=open
I_{DDW}	Program and Erase Current			25	mA	V_{DD} Max
I_{SB}	Standby Current		15	45	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{DPD}	Deep Power-down Current		8	25	µA	CE#=V_{DD}, V_{IN}=V_{DD} or V_{SS}
I_{LI}	Input Leakage Current			2	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			2	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage			0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.7 V_{DD}			V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage			0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	V_{DD}-0.2			V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

TABLE 6-2: CAPACITANCE (TA = 25°C, F=1 MHZ, OTHER PINS OPEN)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	8 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-3: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	100,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 6-4: WRITE TIMING PARAMETERS

Symbol	Parameter	Minimum	Maximum	Units
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms
T_{PP}[1]	Page-Program		1.5	ms
T_{PSID}	Program Security-ID		1.5	ms
T_{WS}	Write-Suspend Latency		25	µs
T_{Wpen}	Write-Protection Enable Bit Latency		25	ms

1. Estimate for typical conditions less than 256 bytes: Programming Time (µs) = 55 + (3.75 x # of bytes)

7.0 AC CHARACTERISTICS

TABLE 7-1: AC OPERATING CHARACTERISTICS

Symbol	Parameter	Limits - 40 MHz		Limits - 80 MHz		Limits - 104 MHz		Units
		Min	Max	Min	Max	Min	Max	
F_{CLK}	Serial Clock Frequency		40		80		104	MHz
T_{CLK}	Serial Clock Period		25		12.5		9.6	ns
T_{SCKH}	Serial Clock High Time	11		5.5		4.5		ns
T_{SCKL}	Serial Clock Low Time	11		5.5		4.5		ns
T_{SCKR} [1]	Serial Clock Rise Time (slew rate)	0.1		0.1		0.1		V/ns
T_{SCKF} [1]	Serial Clock Fall Time (slew rate)	0.1		0.1		0.1		V/ns
T_{CES} [2]	CE# Active Setup Time	8		5		5		ns
T_{CEH} [2]	CE# Active Hold Time	8		5		5		ns
T_{CHS} [2]	CE# Not Active Setup Time	8		5		5		ns
T_{CHH} [2]	CE# Not Active Hold Time	8		5		5		ns
T_{CPH}	CE# High Time	25		12.5		12		ns
T_{CHZ}	CE# High to High-Z Output		19		12.5		12	ns
T_{CLZ}	SCK Low to Low-Z Output	0		0		0		ns
T_{HLS}	HOLD# Low Setup Time	8		5		5		ns
T_{HHS}	HOLD# High Setup Time	8		5		5		ns
T_{HLH}	HOLD# Low Hold Time	8		5		5		ns
T_{HHH}	HOLD# High Hold Time	8		5		5		ns
T_{HZ}	HOLD# Low-to-High-Z Output		8		8		8	ns
T_{LZ}	HOLD# High-to-Low-Z Output		8		8		8	ns
T_{DS}	Data In Setup Time	3		3		3		ns
T_{DH}	Data In Hold Time	4		4		4		ns
T_{OH}	Output Hold from SCK Change	0		0		0		ns
T_V	Output Valid from SCK		8/5 [3]		8/5 [3]		8/5 [3]	ns

1. Maximum Rise and Fall time may be limited by T_{SCKH} and T_{SCKL} requirements
2. Relative to SCK.
3. 30 pF/10 pF

FIGURE 7-1: HOLD TIMING DIAGRAM

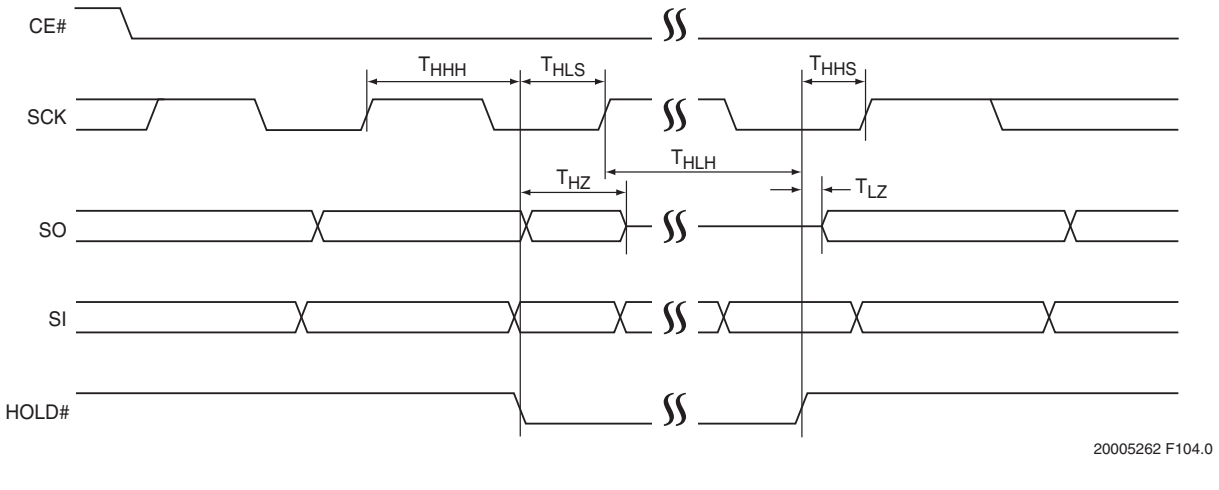


FIGURE 7-2: SERIAL INPUT TIMING DIAGRAM

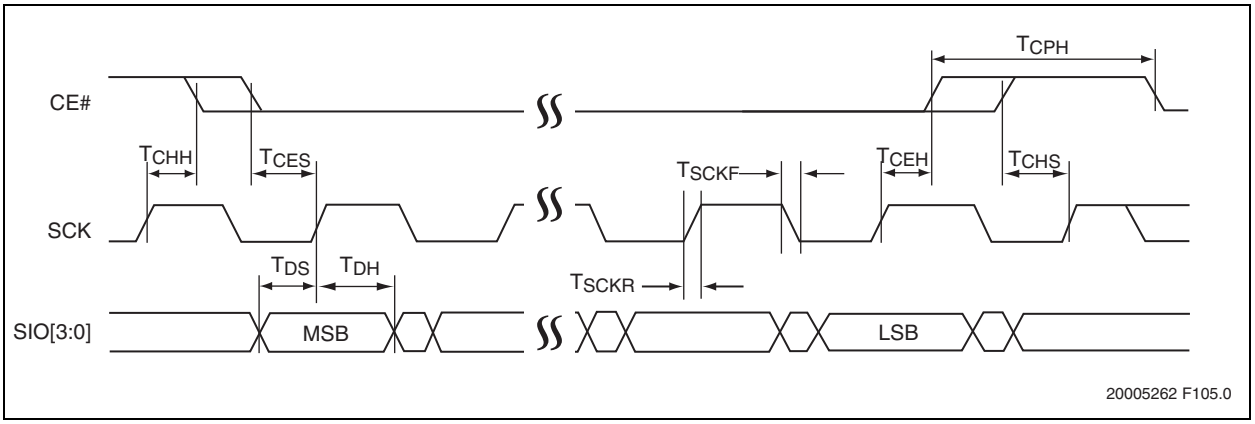


FIGURE 7-3: SERIAL OUTPUT TIMING DIAGRAM

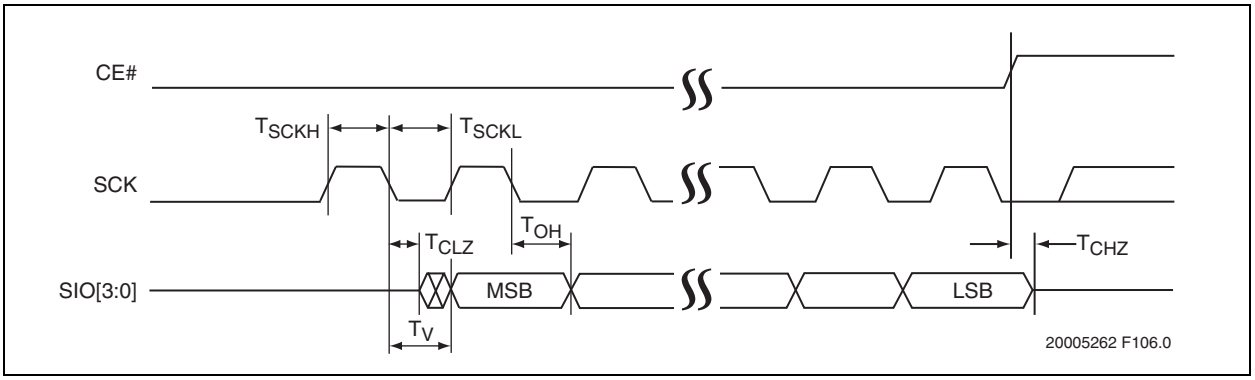
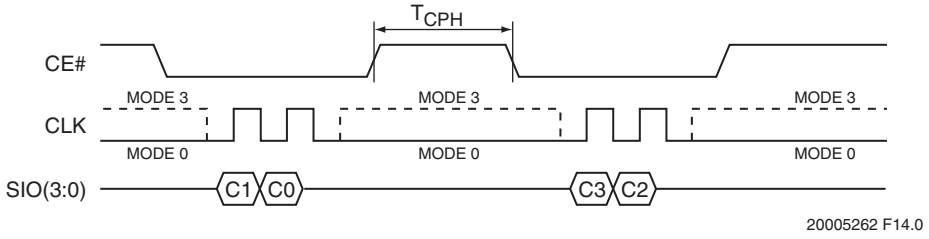


TABLE 7-2: RESET TIMING PARAMETERS

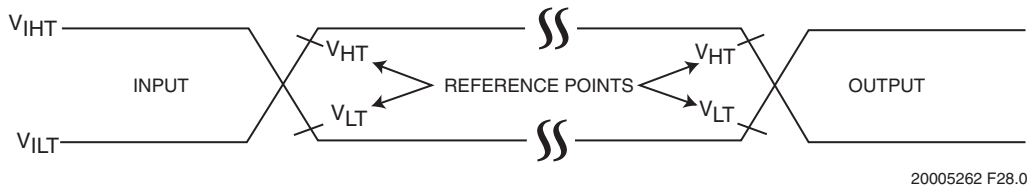
$T_{R(i)}$	Parameter	Minimum	Maximum	Units
$T_{R(o)}$	Reset to Read (non-data operation)		20	ns
$T_{R(p)}$	Reset Recovery from Program or Suspend		100	µs
$T_{R(e)}$	Reset Recovery from Erase		1	ms

FIGURE 7-4: RESET TIMING DIAGRAM



Note: C[1:0] = 66H; C[3:2] = 99H

FIGURE 7-5: AC INPUT/OUTPUT REFERENCE WAVEFORMS



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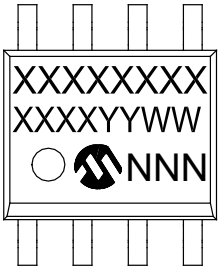
AC test inputs are driven at V_{IHT} ($0.9V_{DD}$) for a logic '1' and V_{ILT} ($0.1V_{DD}$) for a logic '0'. Measurement reference points for inputs and outputs are V_{HT} ($0.6V_{DD}$) and V_{LT} ($0.4V_{DD}$). Input rise and

Note: V_{HT} - V_{HIGH} Test
V_{LT} - V_{LOW} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

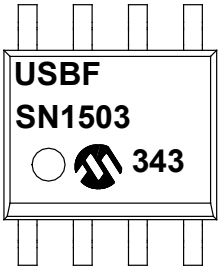
8.0 PACKAGING INFORMATION

8.1 Package Marking

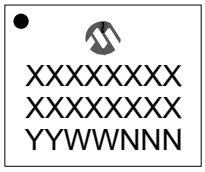
8-Lead SOIC (3.90 mm)



Example



8-Lead WDFN (5x6 mm)



Example

Part Number	1st Line Marking Codes	
	SOIC	WDFN
USBF1600	USBF	USBF

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)

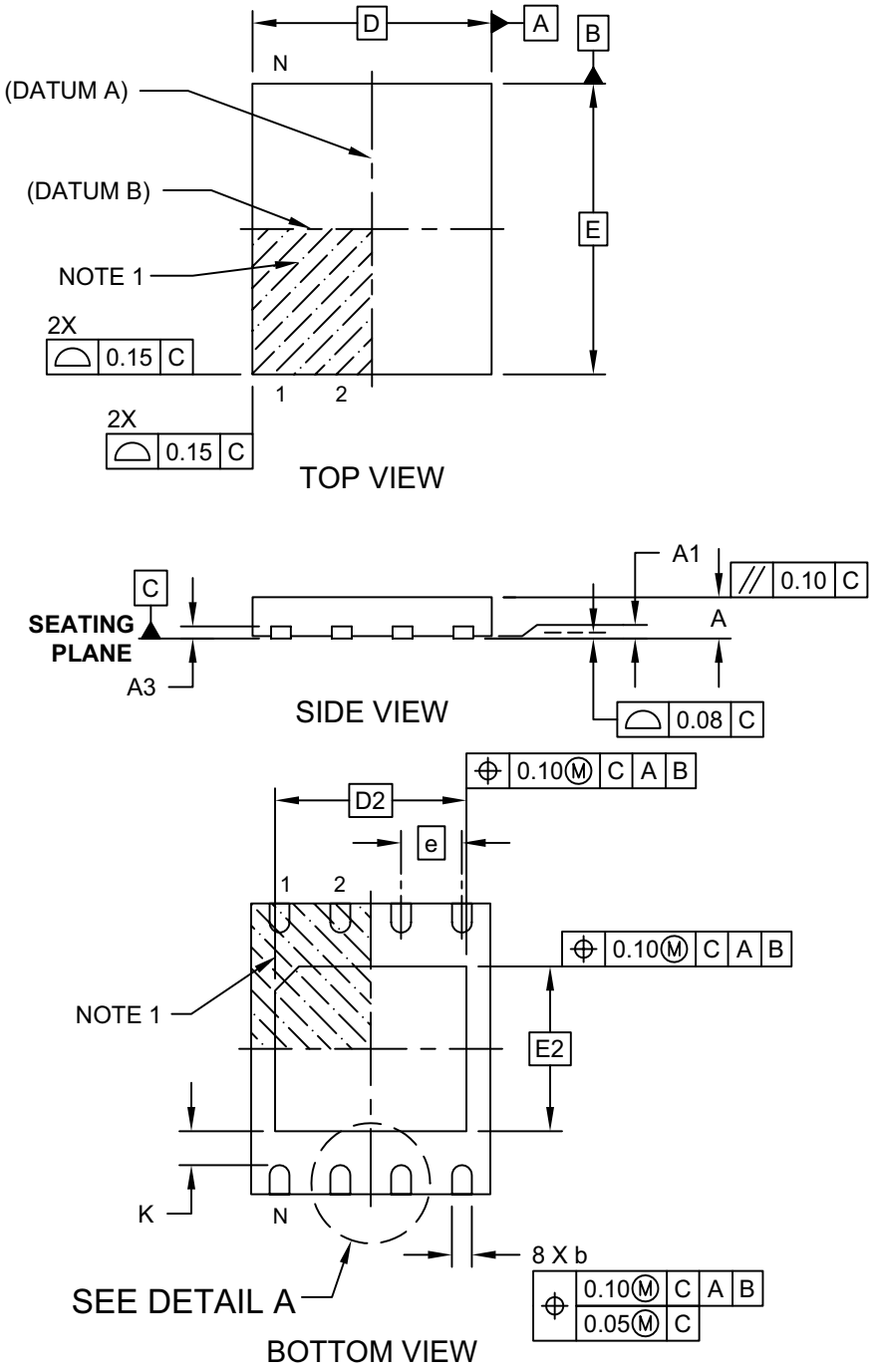
Note: For very small packages with no room for the Pb-free JEDEC® designator (e3) , the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8.2 Packaging Diagrams

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

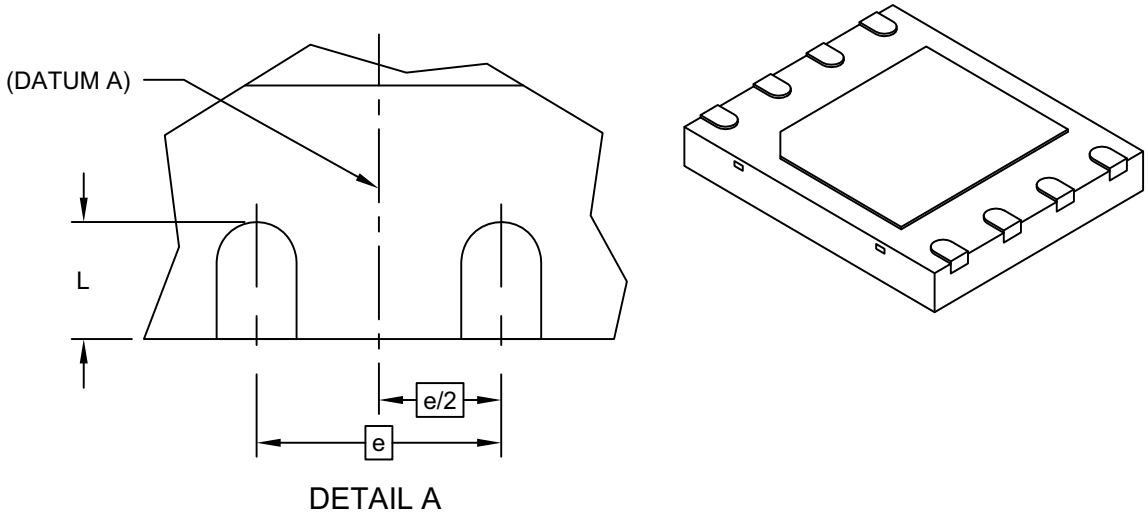
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-210B Sheet 1 of 2

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	D		5.00 BSC	
Exposed Pad Width	D2		4.00 BSC	
Overall Length	E		6.00 BSC	
Exposed Pad Length	E2		3.40 BSC	
Terminal Width	b	0.35	0.42	0.48
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

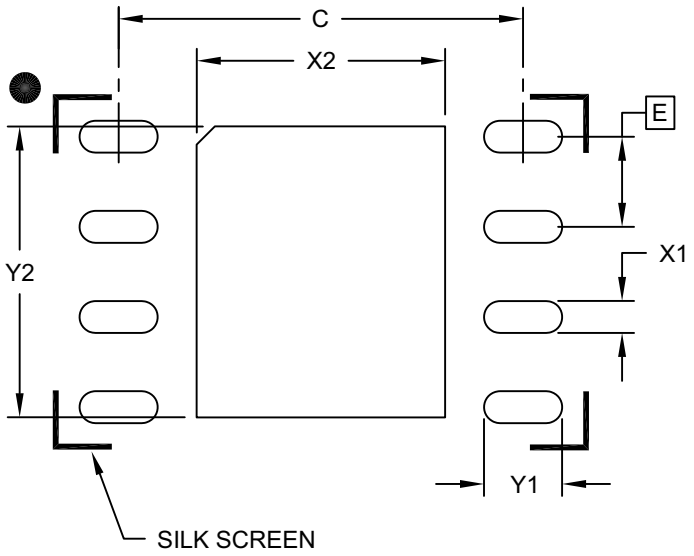
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-210B Sheet 2 of 2

8-Lead Plastic Very, Very Thin Small Outline No-Lead (MF) - 5x6 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Optional Center Pad Width	X2			3.50
Optional Center Pad Length	Y2			4.10
Contact Pad Spacing	C		5.70	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

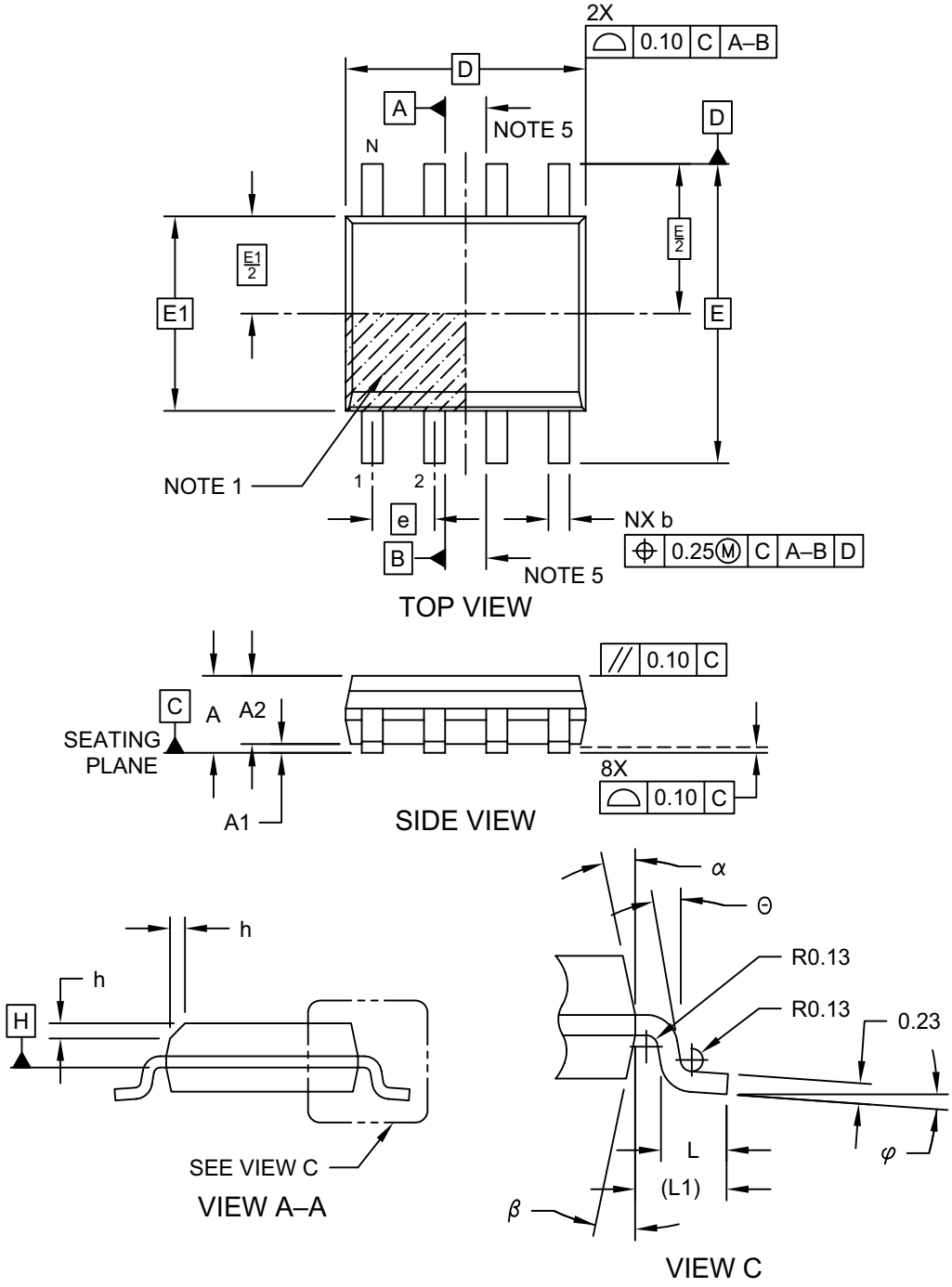
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2210A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

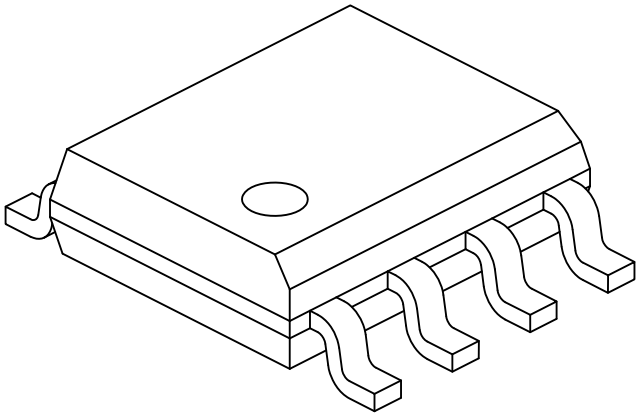
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

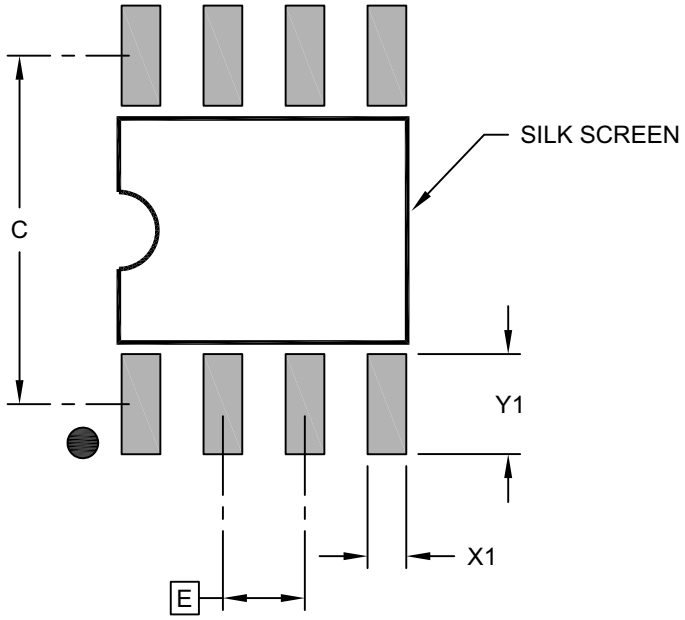
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B

TABLE 8-1: REVISION HISTORY

Revision	Description	Date
A	• Initial release of data sheet	Dec 2018

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
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Technical support is available through the web site at: http://microchip.com/support

9.0 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	–	XXX	X	/	XX
Device	Tape/Reel Indicator		Operating Frequency	Temperature		Package

Device:	USBF1600	= USB Firmware Memory
Tape and Reel Flag:	T	= Tape and Reel
	(blank)	= Tube or Tray
Operating Frequency:	104	= 104 MHz
Temperature:	I	= -40°C to +85°C
	V	= -40°C to +105°C
Package:	MF	= WDFN (6mm x 5mm Body), 8-lead
	SN	= SOIC (3.90 mm Body), 8-lead
Others:	VXX	= Automotive

Valid Combinations:

USBF1600-104I/SNVAO
USBF1600T-104I/SNVAO
USBF1600-104I/MFVAO
USBF1600T-104I/MFVAO

USBF1600-104V/SNVAO
USBF1600T-104V/SNVAO
USBF1600-104V/MFVAO
USBF1600T-104V/MFVAO

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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