

# TPS65982 USB Type-C 和 USB PD 控制器、电源开关和高速多路复用器

## 1 特性

- USB 电力输送 (PD) 控制器
  - 提供供电 (主机)、受电 (设备) 或供电-受电三种模式配置
  - 双相标记编码/解码 (BMC)
  - 物理层 (PHY) 协议
  - 策略引擎
  - 可配置为引导控制和主机控制
- 符合 USB Type-C 规范
  - 检测 USB 电缆插头连接状态
  - 电缆方向和角色检测
  - 分配 CC 和 VCONN 引脚
  - 为 5V USB Type-C 电源提供默认值、1.5A 或 3A 三种电流
- 端口电源开关
  - 5V、3A 开关，用于切换到 Type-C 电源的 VBUS
  - 5V 至 20V、3A 双向开关，用于与 USB PD 电源的 VBUS 之间进行切换
  - 用于 VCONN 的 5V、600mA 开关
  - 过流限制器、过压保护器
  - PD 压摆率控制和硬复位支持
- 端口数据多路复用器
  - USB 2.0 HS 数据、UART 数据和低速终点
  - 适用于交替模式 (DisplayPort 和 Thunderbolt) 的边带使用™数据
- 电源管理
  - 适用于外部 5V 至 20V、5A 双向 NFET 开关的栅极控制和电流检测
  - 由 3.3V 或 VBUS 电源供电
  - 3.3V LDO 输出，在电池电量耗尽时提供支持
- BGA MicroStar Junior 封装
  - 0.5mm 间距
  - 穿孔对于所有引脚均兼容
- 通过以下 UL 认证: E169910 和 E339631
  - 使用的标准: 2367
- IEC 认证: NO88109
  - 使用的标准: 60950-1(ed.2);am1;am2

## 2 应用

- 笔记本电脑、平板电脑和超极本
- 扩展坞系统、显示器和电视
- 交流/直流充电器适配器
- USB PD 拉电流、灌电流和双角色端口

## 3 说明

TPS65982 器件是一款独立式 USB Type-C 和供电 (PD) 控制器，可在 USB Type-C 连接器中提供电缆插头和方向检测。进行线缆检测时，TPS65982 器件会使用 USB PD 协议在 CC 线路上进行通信。在成功完成 USB PD 协商后，TPS65982 会启用合适的电源路径并为内部和 (可选) 外部多路复用器配置交替模式设置。

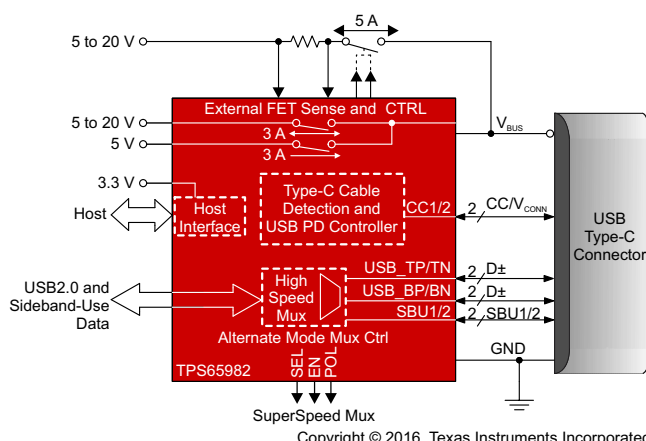
CC 引脚上的混合信号前端可为 USB Type-C 电源提供默认值、1.5A 或 3A 三种电流、检测电缆插入事件、确定 Type-C 电缆方向以及利用双相标记编码 (BMC) 和物理层 (PHY) 协议自主协商 USB PD 合约。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TPS65982	BGA MicroStar Junior (96)	6.00mm × 6.00mm
	NFBGA (96)	

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化图表



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (August 2016) to Revision D	Page
• 已添加 将 NFBGA 封装更改为器件信息表 .....	1
• Added NFBGA package to the <i>Pin Configuration and Functions</i> section .....	5
• Added NFBGA package to the <i>Thermal Information</i> table .....	11

Changes from Revision B (May 2016) to Revision C	Page
• Added the HRESET I/O voltage parameter to the <i>Absolute Maximum Ratings</i> table.....	10
• Changed the value for the HBM from $\pm 2000$ to $\pm 1500$ in the <i>ESD Ratings</i> table .....	10
• Changed the maximum values for the ILDO_3V3 (50 to 70 mA) and ILDO_3V3EX (10 to 30 mA) current parameters in the <i>Power Supply Requirements and Characteristics</i> .....	12
• Updated the GPIO_RPU parameter to show values for DEBUG_CTL1/2 separately in the <i>Input/Output (I/O) Characteristics</i> table .....	23
• Added parameters for HRESET in the <i>Input/Output (I/O) Characteristics</i> table .....	23

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• 完成了编辑性更改，以修复印刷错误并提高术语一致性 .....	1
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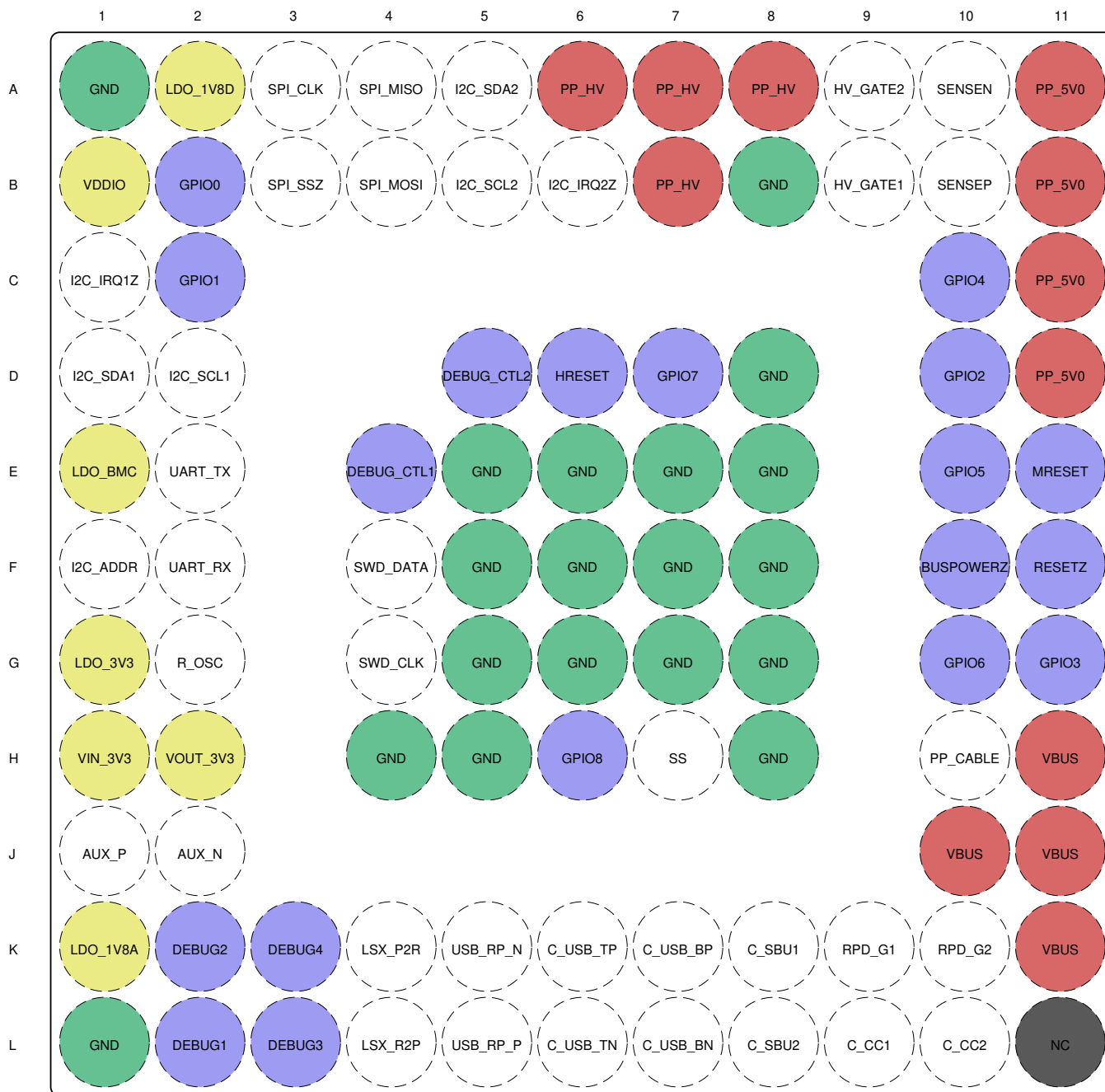
## 5 说明（续）

端口电源开关在 5V 电压下可为传统 USB 电源和 Type-C USB 电源提供高达 3A 的下行电流。当 USB PD 电源用作供电器件（主机）、受电器件（设备）或供电-受电器件时，附加的双向开关路径可在最高 20V 的电压下为其提供高达 3A 的电流。

此外，TPS65982 还可用作上行数据端口 (UFP)、下行数据端口 (DFP) 或者双角色数据端口。端口数据多路复用器可实现端口与顶部或底部 D+/D- 信号对之间的 USB 2.0 HS 数据传输；此外，还可以将边带使用 (SBU) 信号对用于交替模式。当 3.3V 电源不可用时，电源管理电路可将 VBUS 用作主电源，在电池电量耗尽或无电池的情况下运行。

## 6 Pin Configuration and Functions

**ZQZ and ZBH Package  
96-Pin BGA MicroStar Junior and NFBGA  
Top View**



**Legend for Pinout Drawing**



### Pin Functions

PIN		TYPE	CATEGORY	POR STATE	DESCRIPTION
NO.	NAME				
A1	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
A10	SENSEN	Analog input	External HV-FET control and sense pins and soft start	Analog input	Positive sense for external high-voltage power-path current-sense resistance. Short pin to VBUS when unused.
A11	PP_5V0	Power	High-current power pins	—	5-V supply for VBUS. Bypass with capacitance CPP_5V0 to GND. Tie pin to GND when unused.
A2	LDO_1V8D	Power	Low-current power pins	—	Output of the 1.8-V LDO for core digital circuits. Bypass with capacitance CLDO_1V8D to GND.
A3	SPI_CLK	Digital output	Digital core I/O and control pins	Digital input	SPI serial clock. Ground pin when unused
A4	SPI_MISO	Digital input	Digital core I/O and control pins	Digital input	SPI serial master input from slave. This pin is used during boot sequence to determine if the flash memory is valid. Refer to the <a href="#">Boot Code</a> section for more details. Ground pin when unused.
A5	I2C_SDA2	Digital I/O	Digital core I/O and control pins	Digital input	I <sup>2</sup> C port 2 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
A6	PP_HV	Power	High-current power pins	—	HV supply for VBUS. Bypass with capacitance CPP_HV to GND. Tie pin to GND when unused.
A7					
A8					
A9	HV_GATE2	Analog output	External HV-FET control and sense pins and soft start	Short to VBUS	External NFET gate control for high-voltage power path. Float pin when unused.
B1	VDDIO	Power	Low-current power pins	—	VDD for I/O. Some I/Os are reconfigurable to be powered from VDDIO instead of LDO_3V3. When VDDIO is not used, tie pin to LDO_3V3. When not tied to LDO_3V3 and used as a supply input, bypass with capacitance CVDDIO to GND.
B10	SENSEP	Analog input	External HV-FET control and sense pins and soft start	Analog input	Positive sense for external high-voltage power-path current-sense resistance. Short pin to VBUS when unused.
B11	PP_5V0	Power	High-current power pins	—	5-V supply for VBUS. Bypass with capacitance CPP_5V0 to GND. Tie pin to GND when unused.
B2	GPIO0	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 0. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
B3	SPI_SSZ	Digital output	Digital core I/O and control pins	Digital input	SPI slave select. Ground pin when unused.
B4	SPI_MOSI	Digital output	Digital core I/O and control pins	Digital input	SPI serial master output to slave. Ground pin when unused.
B5	I2C_SCL2	Digital I/O	Digital core I/O and control pins	Digital input	I <sup>2</sup> C port 2 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-kΩ resistance when used or unused.
B6	I2C_IRQ2Z	Digital output	Digital core I/O and control pins	Hi-Z	I <sup>2</sup> C port 2 interrupt. Active-low. Implement externally as an open-drain with a pullup resistance. Float pin when unused.
B7	PP_HV	Power	High-current power pins	—	HV supply for VBUS. Bypass with capacitance CPP_HV to GND. Tie pin to GND when unused.
B8	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
B9	HV_GATE1	Analog output	External HV-FET control and sense pins and soft start	Short to SENSEP	External NFET gate control for high-voltage power path. Float pin when unused.
C1	I2C_IRQ1Z	Digital output	Digital core I/O and control pins	Hi-Z	I <sup>2</sup> C port 1 interrupt. Active-low. Implement externally as an open-drain with a pullup resistance. Float pin when unused.
C10	GPIO4 (HPD TXRX)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 4. Configured as hot-plug detect (HPD) TX, HPD RX, or both when DisplayPort mode is supported. Ground pin with a 1-MΩ resistor when unused in the application.
C11	PP_5V0	Power	High-current power pins	—	5-V supply for VBUS. Bypass with capacitance CPP_5V0 to GND. Tie pin to GND when unused.

**Pin Functions (continued)**

PIN		TYPE	CATEGORY	POR STATE	DESCRIPTION
NO.	NAME				
C2	GPIO1	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 1. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
C3	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
C4					
C5					
C6					
C7					
C8					
C9					
D1	I2C_SDA1	Digital I/O	Digital core I/O and control pins	Digital input	I <sup>2</sup> C port 1 serial data. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-k $\Omega$ resistance when used or unused.
D10	GPIO2	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 2. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
D11	PP_5V0	Power	High-current power pins	—	5-V supply for VBUS. Bypass with capacitance CPP_5V0 to GND. Tie pin to GND when unused.
D2	I2C_SCL1	Digital I/O	Digital core I/O and control pins	Digital input	I <sup>2</sup> C port 1 serial clock. Open-drain output. Tie pin to LDO_3V3 or VDDIO (depending on configuration) through a 10-k $\Omega$ resistance when used or unused.
D3	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
D4					
D5	DEBUG_CTL2 (GPIO17, I <sup>2</sup> C ADDR B5)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 17. At power-up, pin state is sensed to determine bit 5 of the I <sup>2</sup> C address.
D6	HRESET	Digital I/O	Digital core I/O and control pins	Hi-Z	Active high hardware reset input. Will re-load settings from external flash memory. Ground pin when HRESET functionality is not used.
D7	GPIO7	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 7. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
D8	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
D9	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
E1	LDO_BMC	Power	Low-current power pins	—	Output of the USB-PD BMC transceiver output level LDO. Bypass with capacitance CLDO_BMC to GND.
E10	GPIO5 (HPD RX)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 5. Can be configured as Hot Plug Detect (HPD) RX when DisplayPort mode supported. Must be tied high or low through a 1-k $\Omega$ pullup or pulldown resistor when used as a configuration input. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
E11	MRESET (GPIO11)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 11. Forces RESETZ to assert. By default, this pin asserts RESETZ when pulled high. The pin can be programmed to assert RESETZ when pulled low. Ground pin with a 1M $\Omega$ resistor when unused in the application.
E2	UART_TX	Digital output	Port multiplexer pins	UART_RX	UART serial transmit data. Connect pin to another TPS65982 UART_TX to share firmware. Connect UART_RX to UART_TX when not connected to another TPS65982.
E3	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
E4	DEBUG_CTL1 (GPIO16, I <sup>2</sup> C ADDR B4)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 16. At power-up, pin state is sensed to determine bit 4 of the I <sup>2</sup> C address.
E5	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
E6					
E7					
E8					
E9	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.

Pin Functions (continued)

PIN		TYPE	CATEGORY	POR STATE	DESCRIPTION
NO.	NAME				
F1	I2C_ADDR	Analog I/O	Digital core I/O and control pins	Analog input	Sets the I <sup>2</sup> C address for both I <sup>2</sup> C ports as well as determine the master and slave devices for memory code sharing.
F10	BUSPOWERZ (GPIO10)	Analog Input	Digital core I/O and control pins	Input (Hi-Z)	General purpose digital I/O 10. Sampled by ADC at boot. Tie pin to LDO_3V3 through a 100-kΩ resistor to disable PP_HV and PP_EXT power paths during dead-battery or no-battery boot conditions. Refer to the <a href="#">BUSPOWERZ</a> table for more details.
F11	RESETZ (GPIO9)	Digital I/O	Digital core I/O and control pins	Push-pull output (Low)	General purpose digital I/O 9. Active-low reset output when VOUT_3V3 is low (driven low on start-up). Float pin when unused.
F2	UART_RX	Digital input	Port multiplexer pins	Digital input	UART serial receive data. Connect pin to another TPS65982 UART_TX to share firmware. Connect UART_RX to UART_TX when not connected to another TPS65982 and ground pin through a 100-kΩ resistance.
F3	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
F4	SWD_DATA	Digital I/O	Port multiplexer pins	Resistive pull high	SWD serial data. Float pin when unused.
F5	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
F6					
F7					
F8					
F9	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
G1	LDO_3V3	Power	Low-current power pins	—	Output of the VBUS to 3.3-V LDO or connected to VIN_3V3 by a switch. Main internal supply rail. Used to power external flash memory. Bypass with capacitance CLDO_3V3 to GND.
G10	GPIO6	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 6. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
G11	GPIO3	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 3. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.
G2	R_OSC	Analog I/O	Digital core I/O and control pins	Hi-Z	External resistance setting for oscillator accuracy. Connect R_OSC to GND through resistance RR_OSC.
G3	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
G4	SWD_CLK	Digital input	Port multiplexer pins	Resistive pull high	SWD serial clock. Float pin when unused.
G5	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
G6					
G7					
G8					
G9	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
H1	VIN_3V3	Power	Low-current power pins	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.
H10	PP_CABLE	Power	High-current power pins	—	5-V supply for C_CC pins. Bypass with capacitance CPP_CABLE to GND when not tied to PP_5V0. Tie pin to PP_5V0 when unused.
H11	VBUS	Power	High-current power pins	—	5-V output from PP_5V0. Input or output from PP_HV up to 20 V. Bypass with capacitance CVBUS to GND.
H2	VOUT_3V3	Power	Low-current power pins	—	Output of supply switched from VIN_3V3. Bypass with capacitance COUT_3V3 to GND. Float pin when unused.
H3	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
H4	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
H5					
H6	GPIO8	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 8. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-MΩ resistor when unused in the application.



**Pin Functions (continued)**

PIN		TYPE	CATEGORY	POR STATE	DESCRIPTION
NO.	NAME				
H7	SS	Analog output	External HV-FET control and sense pins and soft start	Driven low	Soft Start. Tie pin to capacitance CSS to ground.
H8	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
H9	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
J1	AUX_P	Analog I/O	Port multiplexer pins	Hi-Z	System-side DisplayPort connection to port multiplexer. Ground pin with between 1-k $\Omega$ and 5-M $\Omega$ resistance when unused.
J10	VBUS	Power	High-current power pins	—	5-V output from PP_5V0. Input or output from PP_HV up to 20 V. Bypass with capacitance CVBUS to GND.
J11					
J2	AUX_N	Analog I/O	Port multiplexer pins	Hi-Z	System-side DisplayPort connection to port multiplexer. Ground pin with between 1-k $\Omega$ and 5-M $\Omega$ resistance when unused.
J3	No Ball	Blank	Ground and no connect pins	—	Unpopulated ball for A1 marker and unpopulated inner ring.
J4					
J5					
J6					
J7					
J8					
J9					
K1	LDO_1V8A	Power	Low-current power pins	—	Output of the 1.8-V LDO for core analog circuits. Bypass with capacitance CLDO_1V8A to GND.
K10	RPD_G2	Analog I/O	Type-C port pins	Hi-Z	Tie pin to C_CC2 when configured to receive power in dead-battery or no-power condition. Tie pin to GND otherwise.
K11	VBUS	Power	High-current power pins	—	5-V output from PP_5V0. Input or output from PP_HV up to 20 V. Bypass with capacitance CVBUS to GND.
K2	DEBUG2 (GPIO14)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 14. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
K3	DEBUG4 (GPIO12)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 12. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
K4	LSX_P2R	Digital output	Port multiplexer pins	Hi-Z	System side low speed RX to system from port. This pin is configurable to be an output from the digital core or the crossbar multiplexer from the port. Float pin when unused.
K5	USB_RP_N	Analog I/O	Port multiplexer pins	Hi-Z	System side USB2.0 high-speed connection to Port Multiplexer. Ground pin with between 1-k $\Omega$ and 5-M $\Omega$ resistance when unused.
K6	C_USB_TP	Analog I/O	Type-C port pins	Hi-Z	Port-side top USB D+ connection to port multiplexer.
K7	C_USB_BP	Analog I/O	Type-C port pins	Hi-Z	Port-side bottom USB D+ connection to port multiplexer.
K8	C_SBU1	Analog I/O	Type-C port pins	Hi-Z	Port-side Sideband Use connection of port multiplexer.
K9	RPD_G1	Analog I/O	Type-C port pins	Hi-Z	Tie pin to C_CC1 when configured to receive power in dead-battery or no-power condition. Tie pin to GND otherwise.
L1	GND	Ground	Ground and no connect pins	—	Ground. Connect all balls to ground plane.
L10	C_CC2	Analog I/O	Type-C port pins	Hi-Z	Output to Type-C CC or VCONN pin. Filter noise with capacitance CC_CC2 to GND.
L11	NC	Blank	Ground and no connect pins	—	Populated ball that must remain unconnected.
L2	DEBUG1 (GPIO15)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 15. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
L3	DEBUG3 (GPIO13)	Digital I/O	Digital core I/O and control pins	Hi-Z	General purpose digital I/O 13. Float pin if it is configured as a push-pull output in the application. Ground pin with a 1-M $\Omega$ resistor when unused in the application.
L4	LSX_R2P	Digital input	Port multiplexer pins	Digital input	System side low speed TX from system to port. This pin is configurable to be an input to the digital core or the crossbar multiplexer to the port. Ground pin with between 1-k $\Omega$ and 5-M $\Omega$ resistance when unused.
L5	USB_RP_P	Analog I/O	Port multiplexer pins	Hi-Z	System side USB2.0 high-speed connection to Port Multiplexer. Ground pin with between 1-k $\Omega$ and 5-M $\Omega$ resistance when unused.

Pin Functions (continued)

PIN		TYPE	CATEGORY	POR STATE	DESCRIPTION
NO.	NAME				
L6	C_USB_TN	Analog I/O	Type-C port pins	Hi-Z	Port-side top USB D– connection to port multiplexer.
L7	C_USB_BN	Analog I/O	Type-C port pins	Hi-Z	Port-side bottom USB D– connection to port multiplexer.
L8	C_SBU2	Analog I/O	Type-C port pins	Hi-Z	Port-side Sideband Use connection of port multiplexer.
L9	C_CC1	Analog I/O	Type-C port pins	Hi-Z	Output to Type-C CC or VCONN pin. Filter noise with capacitance CC_CC1 to GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>I</sub>	Input voltage <sup>(2)</sup>	PP_CABLE, PP_5V0	-0.3	6	V
		VIN_3V3	-0.3	3.6	
		SENSEP <sup>(3)</sup> , SENSEN <sup>(3)</sup>	-0.3	24	
		VDDIO, UART_RX	-0.3	LDO_3V3 + 0.3	
V <sub>IO</sub>	Output voltage <sup>(2)</sup>	LDO_1V8A, LDO_1V8D, LDO_BMC, SS	-0.3	2	V
		LDO_3V3	-0.3	3.45	
		VOUT_3V3, RESETZ, I2C_IRQ1Z, I2C_IRQ2Z, SPI_MOSI, SPI_CLK, SPI_SSZ, LSX_P2R, SWD_CLK, UART_TX	-0.3	LDO_3V3 + 0.3	
		HV_GATE1, HV_GATE2	-0.3	30	
		HV_GATE1 (relative to SENSEP), HV_GATE2 (relative to VBUS)	-0.3	6	
V <sub>IO</sub>	I/O voltage <sup>(2)</sup>	PP_HV, VBUS <sup>(3)</sup>	-0.3	24	V
		I2C_SDA1, I2C_SCL1, SWD_DATA, SPI_MISO, I2C_SDA2, I2C_SCL2, LSX_R2P, USB_RP_P, USB_RP_N, AUX_N, AUX_P, DEBUG1, DEBUG2, DEBUG3, DEBUG4, DEBUG_CTL1, DEBUG_CTL2, GPIO <sub>n</sub> , MRESET, BUSPOWERZ, GPIO0-8	-0.3	LDO_3V3 + 0.3	
		R_OSC, I2C_ADDR	-0.3	2	
		HRESET	-0.3	LDO_1V8D + 0.3	
		C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU2, C_SBU1 (switches open)	-2	6	
		C_USB_TP, C_USB_TN, C_USB_BP, C_USB_BN, C_SBU2, C_SBU1 (switches closed)	-0.3	6	
C_CC1, C_CC2, RPD_G1, RPD_G2	-0.3	6			
T <sub>J</sub>	Operating junction temperature		-10	125	°C
T <sub>stg</sub>	Storage temperature		-55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
- (3) The 24 V maximum is based on keeping HV\_GATE1/2 at or below 30 V. Fast voltage transitions (<100 ns) may occur up to 30 V.

7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1500
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	VIN_3V3	2.85	3.45	V
		PP_5V0	4.75	5.5	
		PP_CABLE	2.95	5.5	
		PP_HV	4.5	22	
		VDDIO	1.7	3.45	
V <sub>IO</sub>	I/O voltage range <sup>(1)</sup>	VBUS	4	22	V
		C_USB_PT, C_USB_NT, C_USB_PB, C_USB_NB, C_SBU1, C_SBU2	-2	5.5	
		C_CC1, C_CC2	0	5.5	
T <sub>A</sub>	Ambient operating temperature range	-10	85	°C	
T <sub>B</sub>	Operating board temperature range	-10	100	°C	
T <sub>J</sub>	Operating junction temperature range	-10	125	°C	

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65982		UNIT
		ZQZ (BGA)	ZBH (NFBGA)	
		96 BALLS	96 BALLS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	42.4	42.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	12.4	12.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	13	13	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13	13	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Power Supply Requirements and Characteristics

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>EXTERNAL</b>						
VIN_3V3	Input 3.3-V supply		2.85	3.3	3.45	V
PP_CABLE	Input voltage to power C_CC pins. This input is also available to power core circuitry and the VOUT_3V3 output		2.95	5	5.5	V
VBUS	Bi-direction DC bus voltage. Output from the TPS65982 or input to the TPS65982		4	5	22	V
PP_5V0	5V supply input to power VBUS. This supply does not power the TPS65982		4.75	5	5.5	V
VDDIO <sup>(1)</sup>	Optional supply for I/O cells		1.7		3.45	V
<b>INTERNAL</b>						
VLDO_3V3	DC 3.3V generated internally by either a switch from VIN_3V3, an LDO from PP_CABLE, or an LDO from VBUS		2.7	3.3	3.45	V
VDO_LDO3V3	Drop Out Voltage of LDO_3V3 from PP_CABLE	$I_{LOAD} = 50\text{ mA}$			250	mV
	Drop Out Voltage of LDO_3V3 from VBUS		250	500	750	mV
VLDO_1V8D	DC 1.8V generated for internal digital circuitry		1.7	1.8	1.9	V
VLDO_1V8A	DC 1.8V generated for internal analog circuitry		1.7	1.8	1.9	V
VLDO_BMC	DC voltage generated on LDO_BMC. Setting for USB-PD		1.05	1.125	1.2	V
ILDO_3V3	DC current supplied by the 3.3V LDOs. This includes internal core power and external load on LDO_3V3				70	mA
ILDO_3V3EX	External DC current supplied by LDO_3V3				30	mA
IOUT_3V3	External DC current supplied by VOUT_3V3				100	mA
ILDO_1V8D	DC current supplied by LDO_1V8D. This is intended for internal loads only but small external loads may be added				50	mA
ILDO_1V8DEX	External DC current supplied by LDO_1V8D				5	mA
ILDO_1V8A	DC current supplied by LDO_1V8A. This is intended for internal loads only but small external loads may be added				20	mA
ILDO_1V8AEX	External DC current supplied by LDO_1V8A				5	mA
ILDO_BMC	DC current supplied by LDO_BMC. This is intended for internal loads only				5	mA
ILDO_BMC EX	External DC current supplied by LDO_BMC				0	mA
VFWD_DROP	Forward voltage drop across VIN_3V3 to LDO_3V3 switch	$I_{LOAD} = 50\text{ mA}$	25	60	90	mV
RIN_3V3	Input switch resistance from VIN_3V3 to LDO_3V3	$V_{VIN\_3V3} - V_{LDO\_3V3} > 50\text{ mV}$	0.5	1.1	1.75	$\Omega$
ROUT_3V3	Output switch resistance from VIN_3V3 to VOUT_3V3			0.35	0.7	$\Omega$
TR_OUT3V3	10-90% rise time on VOUT_3V3 from switch enable	$C_{VOUT\_3V3} = 1\ \mu\text{F}$	35		120	$\mu\text{s}$

(1) I/O buffers are not fail-safe to LDO\_3V3. Therefore, VDDIO may power-up before LDO\_3V3. When VDDIO powers up before LDO\_3V3, the I/Os shall not be driven high. When VDDIO is low and LDO\_3V3 is high, the I/Os may be driven high.

## 7.6 Power Supervisor Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UV_LDO3V3	Undervoltage threshold for LDO_3V3. Locks out 1.8-V LDOs	LDO_3V3 rising	2.2	2.325	2.45	V
UVH_LDO3V3	Undervoltage hysteresis for LDO_3V3	LDO_3V3 falling	20	80	150	mV
UV_VBUS_LDO	Undervoltage threshold for VBUS to enable LDO	VBUS rising	3.35	3.75	3.95	V
UVH_VBUS_LDO	Undervoltage hysteresis for VBUS to enable LDO	VBUS falling	20	80	150	mV
UV_PCBL	Undervoltage threshold for PP_CABLE	PP_CABLE rising	2.5	2.625	2.75	V
UVH_PCBL	Undervoltage hysteresis for PP_PCABLE	PP_CABLE falling	20	50	80	mV
UV_5V0	Undervoltage threshold for PP_5V0	PP_5V0 rising	3.5	3.725	3.95	V
UVH_5V0	Undervoltage hysteresis for PP_P5V0	PP_5V0 falling	20	80	150	mV
OV_VBUS	Overvoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS rising	5		24	V
OVLSB_VBUS	Overvoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS rising		328		mV
OVH_VBUS	Overvoltage hysteresis for VBUS	VBUS falling, % of OV_VBUS	0.9%	1.3%	1.7%	
UV_VBUS	Undervoltage threshold for VBUS. This value is a 6-bit programmable threshold	VBUS falling	2.5		18.21	V
UVLSB_VBUS	Undervoltage threshold step for VBUS. This value is the LSB of the programmable threshold	VBUS falling		249		mV
UVH_VBUS	Undervoltage hysteresis for VBUS	VBUS rising, % of UV_VBUS	0.9%	1.3%	1.7%	
UVR_OUT3V3	Configurable undervoltage threshold for VOUT_3V3 rising. Deasserts RESETZ	Setting 0	2.019	2.125	2.231	V
		Setting 1	2.138	2.25	2.363	
		Setting 2	2.256	2.375	2.494	
		Setting 3	2.375	2.5	2.625	
		Setting 4	2.494	2.625	2.756	
		Setting 5	2.613	2.75	2.888	
		Setting 6	2.731	2.875	3.019	
		Setting 7	2.85	3	3.15	
UVRH_OUT3V3	Undervoltage hysteresis for VOUT_3V3 falling	OUT_3V3 falling		30	50	mV
TUVRASSERT	Delay from falling VOUT_3V3 or MRESET assertion to RESETZ asserting low				75	$\mu\text{s}$
TUVRDELAY	Configurable delay from VOUT_3V3 to RESETZ deassertion		0		161.3	ms

## 7.7 Power Consumption Characteristics<sup>(1)</sup>

Recommended operating conditions;  $T_A = 25^\circ\text{C}$  (Room temperature) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IVIN_3V3	Sleep <sup>(2)</sup>	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, PPCABLE = 0; 100-kHz oscillator running		58		$\mu\text{A}$
	Idle <sup>(3)</sup>	VIN_3V3 = VDDIO = 3.45 V, VBUS=0, PPCABLE = 0; 100-kHz oscillator running, 48-MHz oscillator running		1.66		mA
	Active <sup>(4)</sup>	VIN_3V3 = VDDIO = 3.45 V, VBUS = 0, PPCABLE = 0; 100-kHz Oscillator running, 48-MHz oscillator running		5.64		mA

(1) Application code can result in other power consumption measurements by adjusting enabled circuitry and clock rates. Application code also provisions the wake-up mechanisms (for example, I<sup>2</sup>C activity and GPIO activity).

(2) Sleep is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active.

(3) Idle is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active, and a selectable clock to the digital core of 3 MHz or 4 MHz.

(4) Active is defined as Type-C cable detect activated as DFP or UFP, internal power management and supervisory functions active, all core functionality active, and the digital core is clocked at 12 MHz.

## 7.8 Cable Detection Characteristics

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IH_CC_USB	Source Current through each C_CC pin when in a disconnected state and Configured as a DFP advertising Default USB current to a peripheral device		73.6	80	86.4	$\mu\text{A}$
IH_CC_1P5	Source Current through each C_CC pin when in a disconnected state when Configured as a DFP advertising 1.5 A to a UFP		169	180	191	$\mu\text{A}$
IH_CC_3P0	Source Current through each C_CC pin when in a disconnected state and Configured as a DFP advertising 3.0 A to a UFP.	VIN_3V3 $\geq$ 3.135 V	303	330	356	$\mu\text{A}$
VD_CCH_USB	Voltage Threshold for detecting a DFP attach when configured as a UFP and the DFP is advertising Default USB current source capability		0.15	0.2	0.25	V
VD_CCH_1P5	Voltage Threshold for detecting a DFP advertising 1.5 A source capability when configured as a UFP		0.61	0.66	0.7	V
VD_CCH_3P0	Voltage Threshold for detecting a DFP advertising 3 A source capability when configured as a UFP		1.169	1.23	1.29	V
VH_CCD_USB	Voltage Threshold for detecting a UFP attach when configured as a DFP and advertising Default USB current source capability	IH_CC = IH_CC_USB	1.473	1.55	1.627	V
VH_CCD_1P5	Voltage Threshold for detecting a UFP attach when configured as a DFP and advertising 1.5 A source capability	IH_CC = IH_CC_1P5	1.473	1.55	1.627	V
VH_CCD_3P0	Voltage Threshold for detecting a UFP attach when configured as a DFP and advertising 3 A source capability	IH_CC = IH_CC_3P0 VIN_3V3 $\geq$ 3.135 V	2.423	2.55	2.67	V
VH_CCA_USB	Voltage Threshold for detecting an active cable attach when configured as a DFP and advertising Default USB current capability		0.15	0.2	0.25	V
VH_CCA_1P5	Voltage Threshold for detecting active cables attach when configured as a DFP and advertising 1.5 A capability		0.35	0.4	0.45	V
VH_CCA_3P0	Voltage Threshold for detecting active cables attach when configured as a DFP and advertising 3 A capability		0.76	0.8	0.84	V
RD_CC	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP. LDO_3V3 powered	V = 1 V, 1.5 V	4.85	5.1	5.35	k $\Omega$
RD_CC_OPEN	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP. LDO_3V3 powered	V = 0 V to LDO_3V3	500			k $\Omega$
RD_DB	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP when configured for dead battery (RPD_Gn tied to C_CCn). LDO_3V3 unpowered	V = 1.5 V, 2.0 V RPD_Gn tied to C_CCn	4.08	5.1	6.12	k $\Omega$
RD_DB_OPEN	Pulldown resistance through each C_CC pin when in a disconnect state and configured as a UFP when not configured for dead battery (RPD_Gn tied to GND). LDO_3V3 unpowered	V = 1.5 V, 2.0 V RPD_Gn tied to GND	500			k $\Omega$
VTH_DB	Threshold Voltage of the pulldown FET in series with RD during dead battery	I_CC = 80 $\mu\text{A}$	0.5	0.9	1.2	V
R_RPD	Resistance between RPD_Gn and the gate of the pulldown FET		25	50	85	M $\Omega$

## 7.9 USB-PD Baseband Signal Requirements and Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>COMMON</b>						
PD_BITRATE	PD data bit rate		270	300	330	Kbps
UI <sup>(1)</sup>	Unit interval (1/PD_BITRATE)		3.03	3.33	3.7	$\mu\text{s}$
CCBLPLUG <sup>(2)</sup>	Capacitance for a cable plug (each plug on a cable may have up to this value)				25	pF
ZCABLE	Cable characteristic impedance		32		65	$\Omega$
CRECEIVER <sup>(3)</sup>	Receiver capacitance. Capacitance looking into C_CCn pin when in receiver mode		70		120	pF
<b>TRANSMITTER</b>						
ZDRIVER	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750kHz) while the source is driving the C_CCn line		33		75	$\Omega$
TRISE	Rise Time. 10% to 90% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask		300			ns
TFALL	Fall Time. 90% to 10% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask		300			ns
<b>RECEIVER</b>						
VRXTR	Rx Receive Rising Input threshold		605	630	655	mV
VRXTF	Rx Receive Falling Input threshold		450	470	490	mV
NCOUNT <sup>(4)</sup>	Number of transitions for signal detection (number to count to detect non-idle bus)		3			
TTRANWIN <sup>(4)</sup>	Time window for detecting non-idle bus		12		20	$\mu\text{s}$
ZBMCRX	Receiver input impedance	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z.	10			M $\Omega$
TRXFILTER <sup>(5)</sup>	Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingress		100			ns

- (1) UI denotes the time to transmit an un-encoded data bit not the shortest high or low times on the wire after encoding with BMC. A single data bit cell has duration of 1 UI, but a data bit cell with value 1 will contain a centrally placed 01 or 10 transition in addition to the transition at the start of the cell.
- (2) The capacitance of the bulk cable is not included in the CCBLPLUG definition. It is modeled as a transmission line.
- (3) CRECEIVER includes only the internal capacitance on a C\_CCn pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the [USB-PD Specifications](#). TI recommends to add capacitance to bring the total pin capacitance to 300 pF for improved TX behavior.
- (4) BMC packet collision is avoided by the detection of signal transitions at the receiver. Detection is active when a minimum of NCOUNT transitions occur at the receiver within a time window of TTRANWIN. After waiting TTRANWIN without detecting NCOUNT transitions, the bus is declared idle.
- (5) Broadband noise ingress is because of coupling in the cable interconnect.

## 7.10 USB-PD TX Driver Voltage Adjustment Parameter

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VTXP0	TX transmit peak voltage		1.615	1.7	1.785	V
VTXP1	TX transmit peak voltage		1.52	1.6	1.68	V
VTXP2	TX transmit peak voltage		1.425	1.5	1.575	V
VTXP3	TX transmit peak voltage		1.33	1.4	1.47	V
VTXP4	TX transmit peak voltage		1.235	1.3	1.365	V
VTXP5	TX transmit peak voltage		1.188	1.25	1.312	V
VTXP6	TX transmit peak voltage		1.14	1.2	1.26	V
VTXP7	TX transmit peak voltage		1.116	1.175	1.233	V
VTXP8	TX transmit peak voltage		1.092	1.15	1.208	V
VTXP9	TX transmit peak voltage		1.068	1.125	1.181	V

- (1) VTXP voltage settings are determined by application code and the setting used must meet the needs of the application and adhere to the [USB-PD Specifications](#).

## USB-PD TX Driver Voltage Adjustment Parameter (continued)

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VTXP10	TX transmit peak voltage		1.045	1.1	1.155	V
VTXP11	TX transmit peak voltage		1.021	1.075	1.128	V
VTXP12	TX transmit peak voltage		0.998	1.05	1.102	V
VTXP13	TX transmit peak voltage		0.974	1.025	1.076	V
VTXP14	TX transmit peak voltage		0.95	1	1.05	V
VTXP15	TX transmit peak voltage		0.903	0.95	0.997	V

## 7.11 Port Power Switch Characteristics

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
RPPCC	PP_CABLE to C_CCn power switch resistance				312	mΩ
RPP5V	PP_5V0 to VBUS power switch resistance			50	60	mΩ
RPPHV	PP_HV to VBUS power switch resistance			95	135	mΩ
IHVACT	Active quiescent current from PP_HV pin, EN_HV = 1				1	mA
IHVSD	Shutdown quiescent current from PP_HV pin, EN_HV = 0				100	μA
IHVEXTACT	Active quiescent current from SENSEP pin, EN_HV = 1	Configured as source			1	mA
	Active quiescent current from VBUS pin, EN_HV = 1	Configured as sink			3.5	mA
IHVEXTSD	Shutdown quiescent current from SENSEP pin, EN_HV = 0				40	μA
IPP5VACT	Active quiescent current from PP_5V0				1	mA
IPP5VSD	Shutdown quiescent current from PP_5V0				100	μA
ILIMHV <sup>(2)</sup>	PP_HV current limit, setting 0		1.007	1.118	1.330	A
	PP_HV current limit, setting 1		1.258	1.398	1.638	A
	PP_HV current limit, setting 2		1.51	1.678	1.945	A
	PP_HV current limit, setting 3		1.761	1.957	2.153	A
	PP_HV current limit, setting 4		2.013	2.237	2.46	A
	PP_HV current limit, setting 5		2.265	2.516	2.768	A
	PP_HV current limit, setting 6		2.516	2.796	3.076	A
	PP_HV current limit, setting 7		2.768	3.076	3.383	A
	PP_HV current limit, setting 8		3.02	3.355	3.691	A
	PP_HV current limit, setting 9		3.271	3.635	3.998	A
	PP_HV current limit, setting 10		3.523	3.914	4.306	A
	PP_HV current limit, setting 11		3.775	4.194	4.613	A
	PP_HV current limit, setting 12		4.026	4.474	4.921	A
	PP_HV current limit, setting 13		4.278	4.753	5.228	A
	PP_HV current limit, setting 14		4.529	5.033	5.536	A
PP_HV current limit, setting 15		5.033	5.592	6.151	A	

(1) Maximum capacitance on VBUS when configured as a source must not exceed 12 μF.

(2) Settings selected automatically by application code for the current limit needed in the application.



## Port Power Switch Characteristics (continued)

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
ILIMHVEXT <sup>(3)(2)</sup>	PP_EXT current limit, setting 0		0.986	1.12	1.254	A
	PP_EXT current limit, setting 1		1.231	1.399	1.567	A
	PP_EXT current limit, setting 2		1.477	1.678	1.879	A
	PP_EXT current limit, setting 3		1.761	1.957	2.153	A
	PP_EXT current limit, setting 4		2.012	2.236	2.46	A
	PP_EXT current limit, setting 5		2.263	2.515	2.767	A
	PP_EXT current limit, setting 6		2.514	2.794	3.074	A
	PP_EXT current limit, setting 7		2.765	3.073	3.381	A
	PP_EXT current limit, setting 8		3.016	3.352	3.688	A
	PP_EXT current limit, setting 9		3.267	3.631	3.995	A
	PP_EXT current limit, setting 10		3.519	3.91	4.301	A
	PP_EXT current limit, setting 11		3.77	4.189	4.608	A
	PP_EXT current limit, setting 12		4.021	4.468	4.915	A
	PP_EXT current limit, setting 13		4.272	4.747	5.222	A
	PP_EXT current limit, setting 14		4.523	5.026	5.529	A
	PP_EXT current limit, setting 15		5.025	5.584	6.143	A
ILIMPP5V <sup>(2)</sup>	PP_5V0 current limit, setting 0		1.006	1.118	1.330	A
	PP_5V0 current limit, setting 1		1.132	1.258	1.484	A
	PP_5V0 current limit, setting 2		1.258	1.398	1.638	A
	PP_5V0 current limit, setting 3		1.384	1.538	1.691	A
	PP_5V0 current limit, setting 4		1.51	1.677	1.845	A
	PP_5V0 current limit, setting 5		1.636	1.817	1.999	A
	PP_5V0 current limit, setting 6		1.761	1.957	2.153	A
	PP_5V0 current limit, setting 7		1.887	2.097	2.307	A
	PP_5V0 current limit, setting 8		2.013	2.237	2.46	A
	PP_5V0 current limit, setting 9		2.139	2.376	2.614	A
	PP_5V0 current limit, setting 10		2.265	2.516	2.768	A
	PP_5V0 current limit, setting 11		2.39	2.656	2.922	A
	PP_5V0 current limit, setting 12		2.516	2.796	3.075	A
	PP_5V0 current limit, setting 13		2.642	2.936	3.229	A
	PP_5V0 current limit, setting 14		2.768	3.075	3.383	A
	PP_5V0 current limit, setting 15		3.019	3.355	3.69	A
ILIMPPCC	PP_CABLE current limit (highest setting)		0.6	0.75	0.9	A
	PP_CABLE current limit (lowest setting)		0.35	0.45	0.55	A
IHV_ACC <sup>(4)</sup>	PP_HV current sense accuracy	I = 100 mA Reverse current blocking disabled	3.25	5	6.75	A/V
		I = 200 mA	4	5	6	A/V
		I = 500 mA	4.4	5	5.6	A/V
		I ≥ 1 A	4.5	5	5.5	A/V
IHVEXT_ACC	PP_EXT current sense accuracy (excluding RSENSE accuracy)	I = 100 mA, RSENSE = 10 mΩ Reverse current blocking disabled	3.5	5	6.5	A/V
		I = 200 mA, RSENSE = 10 mΩ	4	5	6	A/V
		I = 500 mA, RSENSE = 10 mΩ	4.4	5	5.6	A/V
		I ≥ 1 A, RSENSE = 10 mΩ	4.5	5	5.5	A/V

(3) Specified for a 10-mΩ RSENSE resistor and 10-mΩ RSENSE application code setting. Values will scale with a different RSENSE resistance and application code setting.

(4) The current sense in the ADC will not accurately read below the current VREV5V0/RPP5V or VREVHV/RPPHV because of the reverse blocking behavior. When reverse blocking is disabled, the values given for accuracy are valid.

## Port Power Switch Characteristics (continued)

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
IPP5V_ACC <sup>(4)</sup>	PP_5V0 current sense accuracy	I = 100 mA Reverse current blocking disabled	1.95	3	4.05	A/V
		I = 200 mA	2.4	3	3.6	A/V
		I = 500 mA	2.64	3	3.36	A/V
		I ≥ 1 A	2.7	3	3.3	A/V
IPPCBL_ACC	PP_CABLE current sense accuracy	I = 100 mA		1		A/V
		I = 200 mA		1		A/V
		I = 500 mA		1		A/V
IGATEEXT <sup>(5)</sup>	External Gate Drive Current on HV_GATE1 and HV_GATE2		4	5	6	μA
VGSEXT	VGS voltage driving external FETs		4.5		7.5	V
TON_HV	PP_HV path turn on time from enable to VBUS = 95% of PP_HV voltage	Configured as a source or as a sink with soft start disabled. PP_HV = 20 V, CVBUS = 10 μF, ILOAD = 100 mA			8	ms
TON_5V	PP_5V0 path turn on time from enable to VBUS = 95% of PP_5V0 voltage	Configured as a source or as a sink with soft start disabled. PP_5V0 = 5 V, CVBUS = 10 μF, ILOAD = 100 mA			2.5	ms
TON_CC	PP_CABLE path turn on time from enable to C_CCn = 95% of the PP_CABLE voltage	PP_CABLE = 5 V, C_CCn = 500 nF, ILOAD = 100 mA			2	ms
ISS	Soft start charging current		5.5	7	8.5	μA
RSS_DIS	Soft start discharge resistance		0.6	1	1.4	kΩ
VTHSS	Soft start complete threshold		1.35	1.5	1.65	V
TSSDONE	Soft start complete time	CSS = 220 nF	31.9	46.2	60.5	ms
VREVPHV	Reverse current blocking voltage threshold for PP_HV switch		2	6	10	mV
VREVPEXT	Reverse Current Blocking voltage Threshold for PP_EXT external switches		2	6	10	mV
VREV5V0	Reverse current blocking voltage threshold for PP_5V0 switches		2	6	10	mV
VHVDISPD	Voltage threshold above VIN at which the pulldown RHVDISPD on VBUS will disable during a transition from PHV to 5V0		45	200	250	mV
VSAFE0V	Voltage that is a safe 0 V per <a href="#">USB-PD Specifications</a>		0		0.8	V
TSAFE0V	Voltage transition time to VSAFE0V				650	ms
VSO_HV	Voltage on PP_HV or PP_HVEXT above which the PP_HV or PP_EXT to PP_5V0 transition on VBUS will meet transition requirements		9.9			V
SRPOS	Maximum slew rate for positive voltage transitions				0.03	V/μs
SRNEG	Maximum slew rate for negative voltage transitions		-0.03			V/μs
TSTABLE	EN to stable time for both positive and negative voltage transitions				275	ms
VSRCVALID	Supply output tolerance beyond VSRCNEW during time TSTABLE		-0.5		0.5	V
VSRCNEW	Supply output tolerance		-5		5	%

(5) Limit the resistance from the HV\_GATE1/2 pins to the external FET gate pins to < 1 Ω to provide adequate response time to short circuit events.

## 7.12 Port Data Multiplexer Switching Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SWD MULTIPLEXER PATH<sup>(1)</sup></b>						
SWD_RON_U	On resistance of SWD_DATA/CLK to C_USB_TP/TN/BP/BN	$V_i = 3.3\text{ V}, I_o = 20\text{ mA}$		35	55	$\Omega$
		$V_i = 1\text{ V}, I_o = 20\text{ mA}$		30	46	
SWD_ROND_U	On resistance difference between P and N paths of SWD_DATA/CLK to C_USB_TP/TN/BP/BN	$V_i = 1\text{ V to }3.3\text{ V}, I_o = 20\text{ mA}$	-2.5		2.5	$\Omega$
SWD_RON_S	On resistance of SWD_DATA/CLK to C_SBU1/2	$V_i = 3.3\text{ V}, I_o = 20\text{ mA}$		26	42	$\Omega$
		$V_i = 1\text{ V}, I_o = 20\text{ mA}$		24	37	
SWD_ROND_S	On resistance difference between P and N paths of SWD_DATA/CLK to C_SBU1/2	$V_i = 1\text{ V to }3.3\text{ V}, I_o = 20\text{ mA}$	-1.5		1.5	$\Omega$
SWD_TON	Switch on time from enable of SWD path	Time from enable bit with charge pump off			150	$\mu\text{s}$
		Time from enable bit at charge pump steady state			10	
SWD_TOFF	Switch off time from disable of SWD path	Time from disable bit at charge pump steady state			500	ns
SWD_BW	3 dB bandwidth of SWD path	$C_L = 10\text{ pF}$	200			MHz
<b>DEBUG1/2 MULTIPLEXER PATH<sup>(1)</sup></b>						
DB1_RON_U	On resistance DEBUG1/2 to C_USB_TP/TN/BP/BN	$V_i = 3.3\text{ V}, I_o = 20\text{ mA}$		14	26	$\Omega$
		$V_i = 1\text{ V}, I_o = 20\text{ mA}$		10	17	
DB1_ROND_U	On resistance difference between P and N paths of DEBUG1/2 to C_USB_TP/TN/BP/BN	$V_i = 1\text{ V to }3.3\text{ V}, I_o = 20\text{ mA}$	-2.5		2.5	$\Omega$
DB1_RON_S	On resistance of DEBUG1/2 to C_SBU1/2	$V_i = 3.3\text{ V}, I_o = 20\text{ mA}$		9.5	17	$\Omega$
		$V_i = 1\text{ V}, I_o = 20\text{ mA}$		6.5	12	
DB1_ROND_S	On resistance difference between P and N paths of Debug path DEBUG1/2 to C_SBU1/2	$V_i = 1\text{ V to }3.3\text{ V}, I_o = 20\text{ mA}$	-0.5		0.5	$\Omega$
DB1_TON	Switch on time from enable of DEBUG path	Time from enable bit with charge pump off			150	$\mu\text{s}$
		Time from enable bit at charge pump steady state			10	
DB1_TOFF	Switch off time from disable of DEBUG path	Time from disable bit at charge pump steady state			500	ns
DB1_BW	3dB bandwidth of DEBUG path	$C_L = 10\text{ pF}$	200			MHz
<b>DEBUG3/4 MULTIPLEXER PATH<sup>(1)</sup></b>						
DB3_RON_U	On resistance of DEBUG3/4 to C_USB_TP/TN/BP/BN	$V_i = 3.3\text{ V}, I_o = 20\text{ mA}$		14	24	$\Omega$
		$V_i = 1\text{ V}, I_o = 20\text{ mA}$		9	17	
DB3_ROND_U	On resistance difference between P and N paths of DEBUG3/4 to C_USB_TP/TN/BP/BN	$V_i = 1\text{ V to }3.3\text{ V}, I_o = 20\text{ mA}$	-1.5		1.5	$\Omega$
DB3_RON_S	On resistance of DEBUG3/4 to C_SBU1/2	$V_i = 3.3\text{ V}, I_o = 20\text{ mA}$		9.5	18	$\Omega$
		$V_i = 1\text{ V}, I_o = 20\text{ mA}$		6.5	12	
DB3_ROND_S	On resistance difference between P and N paths of DEBUG3/4 to C_SBU1/2	$V_i = 1\text{ V to }3.3\text{ V}, I_o = 20\text{ mA}$	-0.15		0.15	$\Omega$
DB3_TON	Switch on time from enable of DEBUG3/4 path	Time from enable bit with charge pump off			150	$\mu\text{s}$
		Time from enable bit at charge pump steady state			10	
DB3_TOFF	Switch off time from disable of DEBUG3/4 path	Time from disable bit at charge pump steady state			500	ns
DB3_BW	3dB bandwidth of DEBUG3/4 path	$C_L = 10\text{ pF}$	200			MHz

(1) All RON specified maximums are the maximum of either of the switches in a pair. All ROND specified maximums are the maximum difference between the two switches in a pair. ROND does not add to RON.

### Port Data Multiplexer Switching Characteristics (continued)

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LSX_R2P/P2R MULTIPLEXER PATH<sup>(1)</sup></b>						
LSX_RON	On resistance of LSX_P2R/R2P to C_SBU1/2	$V_i = 3.3\text{ V}, I_O = 20\text{ mA}$		8.5	17	$\Omega$
		$V_i = 1\text{ V}, I_O = 20\text{ mA}$		5.5	11	
LSX_ROND	On resistance difference between P and N paths of LSX path	$V_i = 1\text{ V to }3.3\text{ V}, I_O = 20\text{ mA}$	-0.3		0.3	$\Omega$
LSX_TON	Switch on time from enable of LSX path	Time from enable bit with charge pump off			150	$\mu\text{s}$
		Time from enable bit at charge pump steady state			10	
LSX_TOFF	Switch off time from disable of LSX path	Time from disable bit at charge pump steady state			500	ns
LSX_BW	3dB bandwidth of LSX path	$C_L = 10\text{ pF}$	200			MHz
<b>AUX MULTIPLEXER PATH<sup>(1)</sup></b>						
AUX_RON	On resistance of AUX_P/N to C_SBU1/2	$V_i = 3.3\text{ V}, I_O = 20\text{ mA}$		3.5	7	$\Omega$
		$V_i = 1\text{ V}, I_O = 20\text{ mA}$		2.5	5	
AUX_ROND	On resistance difference between P and N paths of AUX_P/N to C_SBU1/2	$V_i = 1\text{ V to }3.3\text{ V}, I_O = 20\text{ mA}$	-0.25		0.25	$\Omega$
AUX_TON	Switch on time from enable of AUX_P/N to C_SBU1/2	Time from enable bit with charge pump off			150	$\mu\text{s}$
		Time from enable bit at charge pump steady state			15	
AUX_TOFF	Switch off time from disable of AUX_P/N to C_SBU1/2	Time from disable bit at charge pump steady state			500	ns
AUX_BW	3dB bandwidth of AUX_P/N to C_SBU1/2 path	$C_L = 10\text{ pF}$	200			MHz
<b>UART MULTIPLEXER PATH (2<sup>nd</sup> STAGE ONLY)<sup>(1)(2)</sup></b>						
UART_RON	On resistance of UART buffers to C_USB_TP/TN/BP/BN or C_SBU1/2	$V_i = 3.3\text{ V}, I_O = 20\text{ mA}$		3.1	12	$\Omega$
UART_TON	Switch on time from enable of UART buffer C_USB_TP/TN/BP/BN or C_SBU1/2 path	Time from enable bit with charge pump off			150	$\mu\text{s}$
		Time from enable bit at charge pump steady state			10	
UART_TOFF	Switch off time from disable of UART buffer path	Time from disable bit at charge pump steady state			500	ns
UART_BW	3dB bandwidth of UART buffer path	$C_L = 10\text{ pF}$	200			MHz
<b>USB_RP MULTIPLEXER PATH<sup>(1)(3)</sup></b>						
USB_RON	On resistance of USB_RP to C_USB_TP/TN/BP/BN	$V_i = 3\text{ V}, I_O = 20\text{ mA}$		4.5	10	$\Omega$
		$V_i = 400\text{ mV}, I_O = 20\text{ mA}$		3	7	
USB_ROND	On resistance difference between P and N paths of USB_RP to C_USB_TP/TN/BP/BN	$V_i = 0.4\text{ V to }3\text{ V}, I_O = 20\text{ mA}$	-0.15		0.15	$\Omega$
USB_TON	Switch on time from enable of USB USB_RP path	Time from enable bit with charge pump off			150	$\mu\text{s}$
		Time from enable bit at charge pump steady state			15	
USB_TOFF	Switch off time from disable of USB_RP path	Time from disable bit at charge pump steady state			500	ns
USB_BW	3dB bandwidth of USB_RP path	$C_L = 10\text{ pF}$	850			MHz
USB_ISO	Off Isolation of USB_RP path	$R_L = 50\text{ }\Omega, V_i = 800\text{ mV}, f = 240\text{ MHz}$			-19	dB
USB_XTLK	Channel to Channel crosstalk of USB_RP path	$R_L = 50\text{ }\Omega, f = 240\text{ MHz}$			-26	dB
<b>C_SBU1/2 OUTPUT</b>						
R_SBU_OPEN	Resistance of the open C_SBU1/2 paths	$V_i = 0\text{ V to LDO}_3\text{V3}$		1		$\text{M}\Omega$
R_USB_OPEN	Resistance of the open C_USB_T/B/P/N paths	$V_i = 0\text{ V to LDO}_3\text{V3}$		1		$\text{M}\Omega$

(2) The UART switch path connects from the UART buffers to the port pins. See [Input/Output \(I/O\) Characteristics](#) for buffer specifications.

(3) See [Port Data Multiplexer USB Endpoint Characteristics](#) for the USB\_EP specifications.

### 7.13 Port Data Multiplexer Clamp Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCLMP_IND	Clamp voltage triggering indicator to digital core		3.8	3.95	4.1	V
ICLMP_IND	Clamp current at VCLMP_IND		10		250	$\mu\text{A}$
TCLMP_PRT <sup>(1)</sup>	Time from clamp current crossing ICLMP_IND to interrupt signal assertion	$I \geq \text{ICLMP\_IND}$ rising	0		4	$\mu\text{s}$
ICLMP	USB_EP and USB_RP port clamp current	$V = \text{LDO\_3V3}$			250	nA
		$V = \text{VCLMP\_IND} + 500 \text{ mV}$	3.5		15	mA

(1) The TCLMP\_PRT time includes the time through the digital synchronizers. When the clock speed is reduced, the signal assertion time may be longer.

### 7.14 Port Data Multiplexer SBU Detection Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIH_PORT	Port switch detect input high voltage	LDO_3V3 = 3.3 V	2			v
VIL_PORT	Port switch detect input low voltage	LDO_3V3 = 3.3 V			0.8	V

### 7.15 Port Data Multiplexer Signal Monitoring Pullup and Pulldown Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RPU05	500- $\Omega$ pullup and pulldown resistance	LDO_3V3 = 3.3 V	350	500	650	$\Omega$
RTPU5	5-k $\Omega$ pullup and pulldown resistance	LDO_3V3 = 3.3 V	3.5	5	6.5	k $\Omega$
RPU100	100-k $\Omega$ pullup and pulldown resistance	LDO_3V3 = 3.3 V	70	100	130	k $\Omega$

### 7.16 Port Data Multiplexer USB Endpoint Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TRANSMITTER<sup>(1)</sup></b>						
T_RISE_EP	Rising transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_FALL_EP	Falling transition time	Low-speed (1.5 Mbps) data rate only	75		300	ns
T_RRM_EP	Rise/fall time matching	Low-speed (1.5 Mbps) data rate only	-20%		25%	
V_XOVER_EP	Output crossover voltage		1.3		2	V
RS_EP	Source resistance of driver including 2nd stage port data multiplexer			34		$\Omega$
<b>DIFFERENTIAL RECEIVER<sup>(1)</sup></b>						
VOS_DIFF_EP	Input offset		-100		100	mV
VIN_CM_EP	Common mode range		0.8		2.5	V
RPU_EP	D- Bias Resistance	Receiving	1.425		1.575	k $\Omega$
<b>SINGLE ENDED RECEIVER<sup>(1)</sup></b>						
VTH_SE_EP	Single ended threshold	Signal rising and falling	0.8		2	V
VHYS_SE_EP	Single ended threshold hysteresis	Signal falling		200		mV

(1) The USB Endpoint PHY is functional across the entire VIN\_3V3 operating range, but parameter values are only verified by design for  $VIN\_3V3 \geq 3.135 \text{ V}$

### 7.17 Port Data Multiplexer BC1.2 Detection Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DATA CONTACT DETECT</b>						
IDP_SRC	DCD source current	LDO_3V3 = 3.3 V	7	10	13	$\mu\text{A}$
RDM_DWN	DCD pulldown resistance		14.25	20	24.8	$\text{k}\Omega$
VLGC_HI	Threshold for no connection	VC_USB_TP/BP $\geq$ VLGC_HILDO_3V3 = 3.3 V LDO_3V3 = 3.3 V	2			V
VLGC_LO	Threshold for connection	VC_USB_TP/BP $\leq$ VLGC_LO LDO_3V3 = 3.3 V			0.8	V
<b>PRIMARY AND SECONDARY DETECT</b>						
VDX_SRC	Source voltage		0.55	0.6	0.65	V
VDX_RSRC	Total series resistance because of port data multiplexer	VDX_SRC = 0.65 V			65	$\Omega$
VDX_ILIM	VDX_SRC current limit		250		400	$\mu\text{A}$
IDX_SNK	Sink current	VC_USB_TN/BN $\geq$ 250 mV	25	75	125	$\mu\text{A}$

### 7.18 Analog-to-Digital Converter (ADC) Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RES_ADC	ADC resolution			10		bits
F_ADC	ADC clock frequency		1.477	1.5	1.523	MHz
T_ENA	ADC enable time		42.14	43	43.86	$\mu\text{s}$
T_SAMPLEA	ADC input sample time		10.5	10.67	10.9	$\mu\text{s}$
T_CONVERTA	ADC conversion time		7.88	8	8.12	$\mu\text{s}$
T_INTA	ADC interrupt time		1.31	1.33	1.35	$\mu\text{s}$
LSB	Least significant bit		1.152	1.17	1.188	mV
DNL	Differential non-linearity		-0.65		0.65	LSB
INL	Integral non-linearity		-1.2		1.2	LSB
GAIN_ERR	Gain error (divider)		-1.5%		1.5%	
	Gain error (no divider)		-1		1	
VOS_ERR	Buffer offset error		-10		10	mV
THERM_ACC	Thermal sense accuracy		-8		8	$^\circ\text{C}$
THERM_GAIN	Thermal slope			3.095		$\text{mV}/^\circ\text{C}$
THERM_V0	Zero degree voltage			0.823		V

### 7.19 Input/Output (I/O) Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SPI</b>						
SPI_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SPI_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SPI_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SPI_ILKG	Leakage current	Output is Hi-Z, $V_{IN} = 0$ to LDO_3V3	-1		1	$\mu\text{A}$
SPI_VOH	SPI output high voltage	$I_O = -8$ mA, LDO_3V3=3.3 V	2.9			V
		$I_O = -15$ mA, LDO_3V3=3.3 V	2.5			
SPI_VOL	SPI output low voltage	$I_O = 10$ mA			0.4	V
		$I_O = 20$ mA			0.8	

## Input/Output (I/O) Characteristics (continued)

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SWDIO</b>						
SWDIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SWDIO_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SWDIO_ILKG	Leakage current	Output is Hi-Z, $V_{IN} = 0$ V to LDO_3V3	-1		1	$\mu\text{A}$
SWDIO_VOH	Output high voltage	$I_O = -8$ mA, LDO_3V3 = 3.3 V	2.9			V
		$I_O = -15$ mA, LDO_3V3 = 3.3 V	2.5			
SWDIO_VOL	Output low voltage	$I_O = 10$ mA			0.4	V
		$I_O = 20$ mA			0.8	
SWDIO_RPU	Pullup resistance		2.8	4	5.2	$\text{k}\Omega$
SWDIO_TOS	SWDIO output skew to falling edge SWDCLK		-5		5	ns
SWDIO_TIS	Input setup time required between SWDIO and rising edge of SWCLK		6			ns
SWDIO_TIH	Input hold time required between SWDIO and rising edge of SWCLK		1			ns
<b>SWDCLK</b>						
SWDCL_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SWDCL_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SWDCL_THI	SWDIOCLK HIGH period		0.05		500	$\mu\text{s}$
SWDCL_TLO	SWDIOCLK LOW period		0.05		500	$\mu\text{s}$
SWDCL_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
SWDCL_RPU	Pullup resistance		2.8	4	5.2	$\text{k}\Omega$
<b>GPIO (GPIO0-8, DEBUG1-4, DEBUG_CTL1/2, MRESET, RESETZ, BUSPOWERZ)</b>						
GPIO_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
		VDDIO = 1.8 V	1.25			
GPIO_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
		VDDIO = 1.8 V			0.63	
GPIO_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
		VDDIO = 1.8 V	0.09			
GPIO_ILKG	Leakage current	Pin is Hi-Z; $V_{IN} = 0$ V to VDD (VDDIO or LDO_3V3)	-1		1	$\mu\text{A}$
GPIO_RPU	Pullup resistance (GPIO0-8, DEBUG1-4, MRESET, RESETZ, BUSPOWERZ)	Pullup enabled	50	100	150	$\text{k}\Omega$
	Pullup resistance (DEBUG_CTL1/2)	Pullup enabled	2.5	5	7.5	
GPIO_RPD	Pulldown resistance (GPIO0-8, DEBUG1-4, MRESET, RESETZ, BUSPOWERZ) <sup>(1)</sup>	Pulldown enabled	50	100	150	$\text{k}\Omega$
GPIO_DG	Digital input path deglitch			20		ns
GPIO_VOH	Output high voltage	$I_O = -2$ mA, LDO_3V3 = 3.3 V	2.9			V
		$I_O = -2$ mA, VDDIO = 1.8 V	1.35			
GPIO_VOL	Output low voltage	$I_O = 2$ mA, LDO_3V3 = 3.3 V			0.4	V
		$I_O = 2$ mA, VDDIO = 1.8 V			0.45	
<b>HRESET</b>						
HRESET_VIH	High-level input voltage		1.25			V
HRESET_VIL	Low-level input voltage				0.63	V
HRESET_HYS	Input hysteresis Voltage		0.09			V
HRESET_ILKG	I/O leakage current	$V_{IN} = 0$ V to LDO_1V8D	-1		1	$\mu\text{A}$
HRESET_THIGH	HRESET minimum high time to assert a reset condition		2.0			ms
HRESET_TLOW	HRESET minimum low time to deassert a reset condition		2.0			
<b>UART_RX/TX, LSX_P2R/R2P</b>						

(1) DEBUG\_CTL1/2 do not have an internal pulldown resistance path.

## Input/Output (I/O) Characteristics (continued)

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UARTRX_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
		VDDIO = 1.8 V	1.25			
UARTRX_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
		VDDIO = 1.8 V			0.63	
UARTRX_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V
		VDDIO = 1.8 V	0.09			
UARTTX_VOH	GPIO output high voltage	$I_O = -2$ mA, LDO_3V3 = 3.3 V	2.9			V
		$I_O = -2$ mA, VDDIO = 1.8 V	1.35			
UARTTX_VOL	GPIO output low voltage	$I_O = 2$ mA, LDO_3V3 = 3.3 V			0.4	V
		$I_O = 2$ mA, VDDIO = 1.8 V			0.45	
UARTTX_RO	Output impedance, TX channel	LDO_3V3 = 3.3 V	35	70	115	$\Omega$
UARTTX_TRTF	Rise and fall time, TX channel	10%–90%, $C_L = 20$ pF	1		40	ns
UART_FMAX	Maximum UART baud rate				1.1	Mbps
<b>I2C_IRQ1Z, I2C_IRQ2Z</b>						
OD_VOL	Low level output voltage	$I_{OL} = 2$ mA			0.4	V
OD_LKG	Leakage current	Output is Hi-Z, $V_{IN} = 0$ to LDO_3V3	-1		1	$\mu\text{A}$
<b>SBU</b>						
SBU_VIH	High-level input voltage	LDO_3V3 = 3.3 V	2			V
SBU_VIL	Low-level input voltage	LDO_3V3 = 3.3 V			0.8	V
SBU_HYS	Input hysteresis voltage	LDO_3V3 = 3.3 V	0.2			V

## 7.20 I<sup>2</sup>C Slave Characteristics

Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SDA and SCL COMMON CHARACTERISTICS</b>						
ILEAK	Input leakage current	Voltage on Pin = LDO_3V3	-3		3	$\mu\text{A}$
VOL	SDA output low voltage	$I_{OL} = 3$ mA, LDO_3V3 = 3.3 V			0.4	V
		$I_{OL} = 3$ mA, VDDIO = 1.8 V			0.36	
IOL	SDA max output low current	VOL = 0.4 V	3			mA
		VOL = 0.6 V	6			
VIL	Input low signal	LDO_3V3 = 3.3 V			0.99	V
		VDDIO = 1.8 V			0.54	
VIH	Input high signal	LDO_3V3 = 3.3 V	2.31			V
		VDDIO = 1.8 V	1.26			
VHYS	Input Hysteresis	LDO_3V3 = 3.3 V	0.17			V
		VDDIO = 1.8 V	0.09			
TSP	I <sup>2</sup> C pulse width suppressed				50	ns
CI	Pin Capacitance				10	pF
<b>SDA and SCL STANDARD MODE CHARACTERISTICS</b>						
FSCL	I <sup>2</sup> C clock frequency		0		100	kHz
THIGH	I <sup>2</sup> C clock high time		4			$\mu\text{s}$
TLOW	I <sup>2</sup> C clock low time		4.7			$\mu\text{s}$
TSUDAT	I <sup>2</sup> C serial data setup time		250			ns
THDDAT	I <sup>2</sup> C serial data hold time		0			ns
TVDDAT	I <sup>2</sup> C Valid data time	SCL low to SDA output valid			3.4	$\mu\text{s}$
TVDACK	I <sup>2</sup> C Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			3.4	$\mu\text{s}$
TOCF	I <sup>2</sup> C output fall time	10 pF to 400 pF bus			250	ns
TBUF	I <sup>2</sup> C bus free time between stop and start		4.7			$\mu\text{s}$



## I<sup>2</sup>C Slave Characteristics (continued)

Recommended operating conditions; T<sub>A</sub> = –10 to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSTS	I <sup>2</sup> C start or repeated Start condition setup time		4.7			μs
TSTH	I <sup>2</sup> C Start or repeated Start condition hold time		4			μs
TSPS	I <sup>2</sup> C Stop condition setup time		4			μs
<b>SDA and SCL FAST MODE CHARACTERISTICS</b>						
FSCL	I <sup>2</sup> C clock frequency		0		400	kHz
THIGH	I <sup>2</sup> C clock high time		0.6			μs
TLOW	I <sup>2</sup> C clock low time		1.3			μs
TSUDAT	I <sup>2</sup> C serial data setup time		100			ns
THDDAT	I <sup>2</sup> C serial data hold time		0			ns
TVDDAT	I <sup>2</sup> C valid data time	SCL low to SDA output valid			0.9	μs
TVDACK	I <sup>2</sup> C valid data time of ACK condition	ACK signal from SCL low to SDA (out) low			0.9	μs
TOCF	I <sup>2</sup> C output fall time	10 pF to 400 pF bus, VDD = 3.3 V	12		250	ns
		10 pF to 400 pF bus, VDD = 1.8 V	6.5		250	
TBUF	I <sup>2</sup> C bus free time between stop and start		1.3			μs
TSTS	I <sup>2</sup> Cstart or repeated Start condition setup time		0.6			μs
TSTH	I <sup>2</sup> C Start or repeated Start condition hold time		0.6			μs
TSPS	I <sup>2</sup> C Stop condition setup time		0.6			μs

## 7.21 SPI Master Characteristics

Recommended operating conditions; T<sub>A</sub> = –10 to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSPI	Frequency of SPI_CLK		11.82	12	12.18	MHz
TPER	Period of SPI_CLK (1/F_SPI)		82.1	83.33	84.6	ns
TWHI	SPI_CLK High Width		30			ns
TWLO	SPI_CLK Low Width		30			ns
TDACT	SPI_SZZ falling to SPI_CLK rising delay time		30		50	ns
TDINACT	SPI_CLK falling to SPI_SSZ rising delay time		160		180	ns
TD MOSI	SPI_CLK falling to SPI_MOSI Valid delay time		–5		5	ns
TSUMISO	SPI_MISO valid to SPI_CLK falling setup time		21			ns
THDMSIO	SPI_CLK falling to SPI_MISO invalid hold time		0			ns
TRSPI	SPI_SSZ/CLK/MOSI rise time	10% to 90%, C <sub>L</sub> = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSPI	SPI_SSZ/CLK/MOSI fall time	90% to 10%, C <sub>L</sub> = 5 pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

## 7.22 BUSPOWERZ Configuration Characteristics

Recommended operating conditions; T<sub>A</sub> = –10 to 85°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBPZ_EXT	BUSPOWERZ Voltage for receiving VBUS Power through the PP_EXT path				0.8	V
VBPZ_HV	BUSPOWERZ Voltage for receiving VBUS Power through the PP_HV path		0.8		2.4	V
VBPZ_DIS	BUSPOWERZ Voltage for disabling system power from VBUS		2.4			V

## 7.23 Thermal Shutdown Characteristics

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TSD_MAIN	Thermal shutdown temperature of the main thermal shutdown	Temperature rising	145	160	175	$^\circ\text{C}$
TSDH_MAIN	Thermal shutdown hysteresis of the main thermal shutdown	Temperature falling		20		$^\circ\text{C}$
TSD_PWR	Thermal shutdown temperature of the power path block	Temperature rising	135	150	165	$^\circ\text{C}$
TSDH_PWR	Thermal shutdown hysteresis of the power path block	Temperature falling		37		$^\circ\text{C}$
TSD_DG	Programmable thermal shutdown detection deglitch time				0.1	ms

## 7.24 Oscillator Characteristics

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOSC_48M	48-MHz oscillator		47.28	48	48.72	MHz
FOSC_100K	100-kHz oscillator		95	100	105	kHz
RR_OSC	External oscillator set resistance (0.2%)		14.98 5	15	15.01 5	k $\Omega$

## 7.25 Single-Wire Debugger (SWD) Timing Requirements

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
FSWD	Frequency of SWD_CLK				10	MHz
TPER	Period of SWD_CLK (1 / FSWD)		100			ns
TWHI	SWD_CLK high width		35			ns
TWLO	SWD_CLK low width		35			ns
TDOUT	SWD_CLK rising to SWD_DATA valid delay time		2		25	ns
TSUIN	SWD_DATA valid to SWD_CLK rising setup time		9			ns
THDIN	SWD_DATA hold time from SWD_CLK rising		3			ns
TRSWD	SWD output rise time	10% to 90%, $C_L = 5$ pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns
TFSWD	SWD output fall time	90% to 10%, $C_L = 5$ pF to 50 pF, LDO_3V3 = 3.3 V	0.1		8	ns

## 7.26 HPD Timing Requirements

 Recommended operating conditions;  $T_A = -10$  to  $85^\circ\text{C}$  unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
<b>DP SOURCE SIDE (HPD TX)</b>						
T_IRQ_MIN	HPD IRQ minimum assert time		675	750	825	$\mu\text{s}$
T_3MS_MIN	HPD assert 3 ms minimum time		3	3.33	3.67	ms
<b>DP SINK SIDE (HPD RX)</b>						
T_HPDI_HDB	HPD high debounce time	HPDI_HDB_SEL = 0	300	375	450	$\mu\text{s}$
		HPDI_HDB_SEL = 1	100	111	122	ms
T_HPDI_LDB	HPD low debounce time		300	375	450	$\mu\text{s}$
T_HPDI_IRQ	HPD IRQ limit time		1.35	1.5	1.65	ms

## 7.27 Typical Characteristics

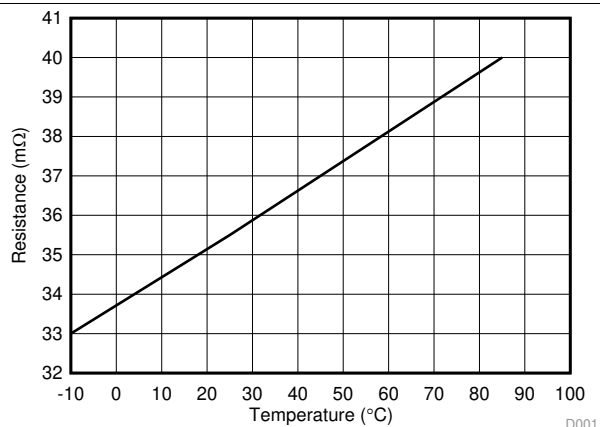


Figure 1. PP\_5V0 Switch On-Resistance vs. Temperature

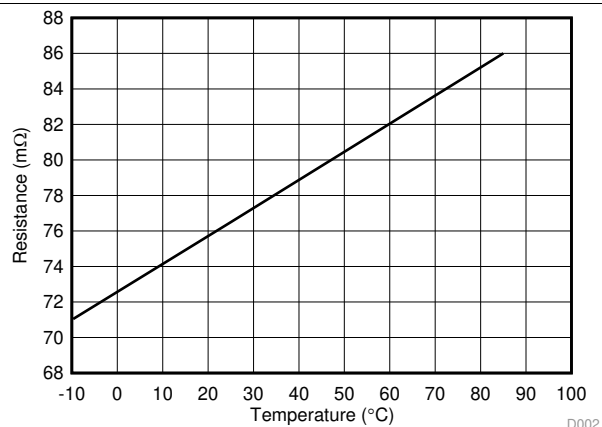


Figure 2. PP\_HV Switch On-Resistance vs. Temperature

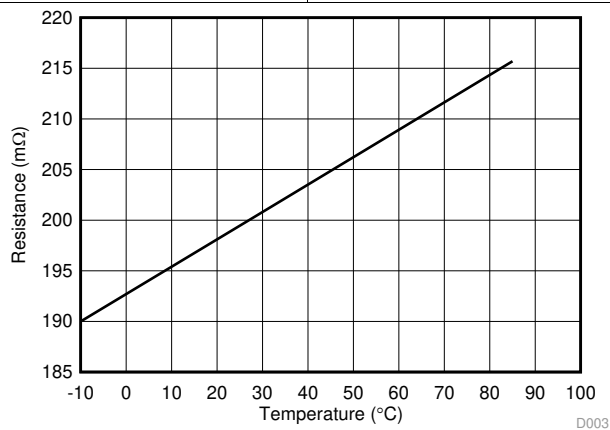
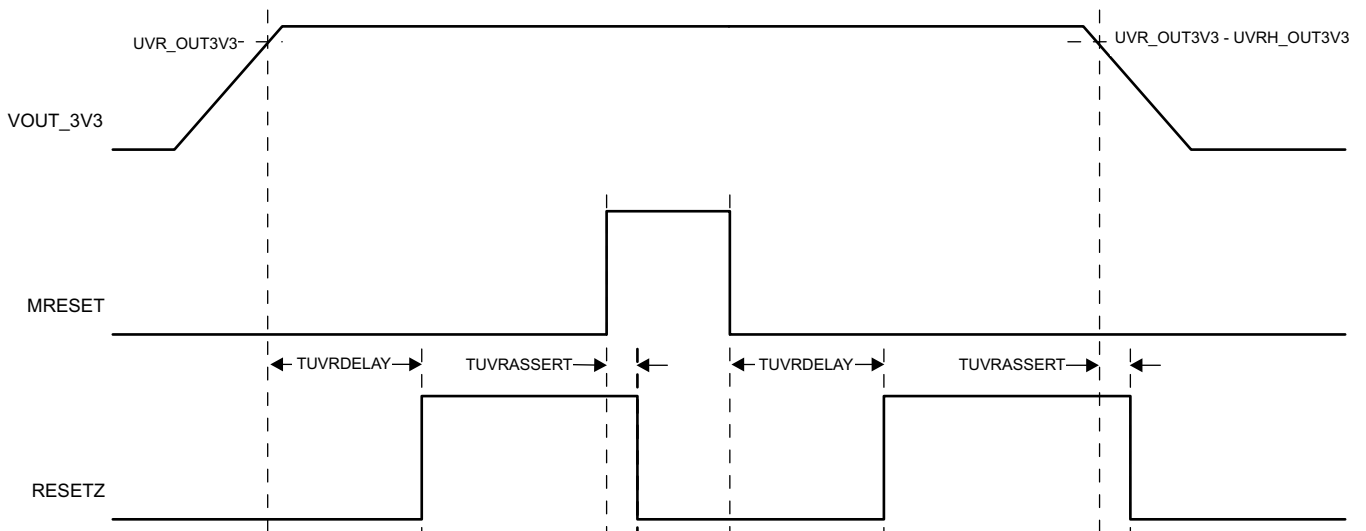
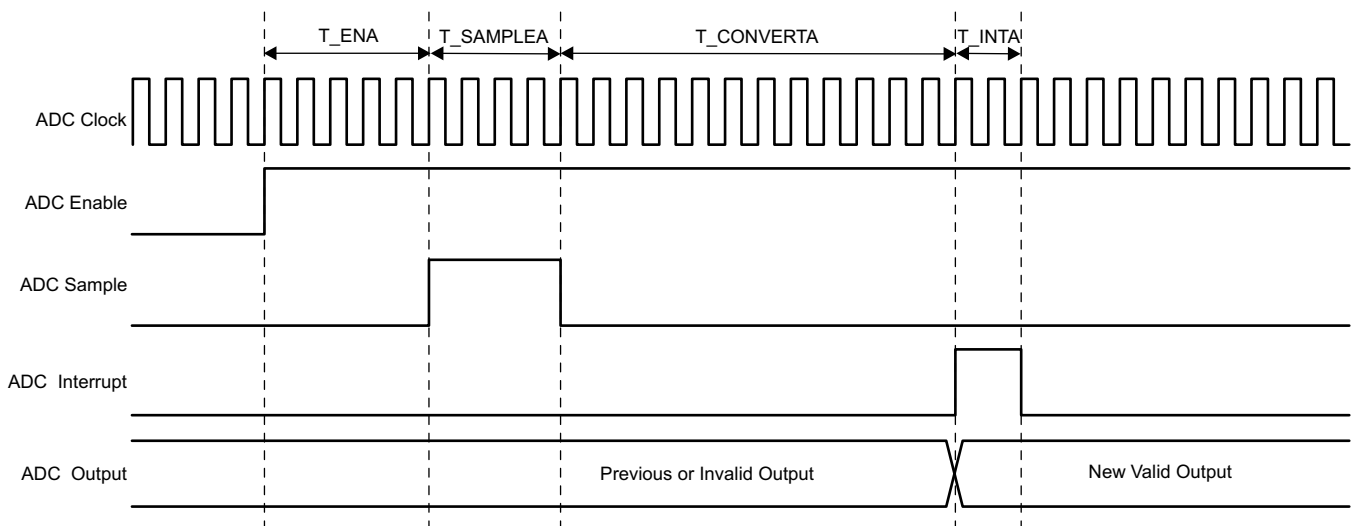


Figure 3. PP\_CABLE Switch On-Resistance vs. Temperature

## 8 Parameter Measurement Information



**Figure 4. RESETZ Assertion Timing**



**Figure 5. ADC Enable and Conversion Timing**

Parameter Measurement Information (continued)

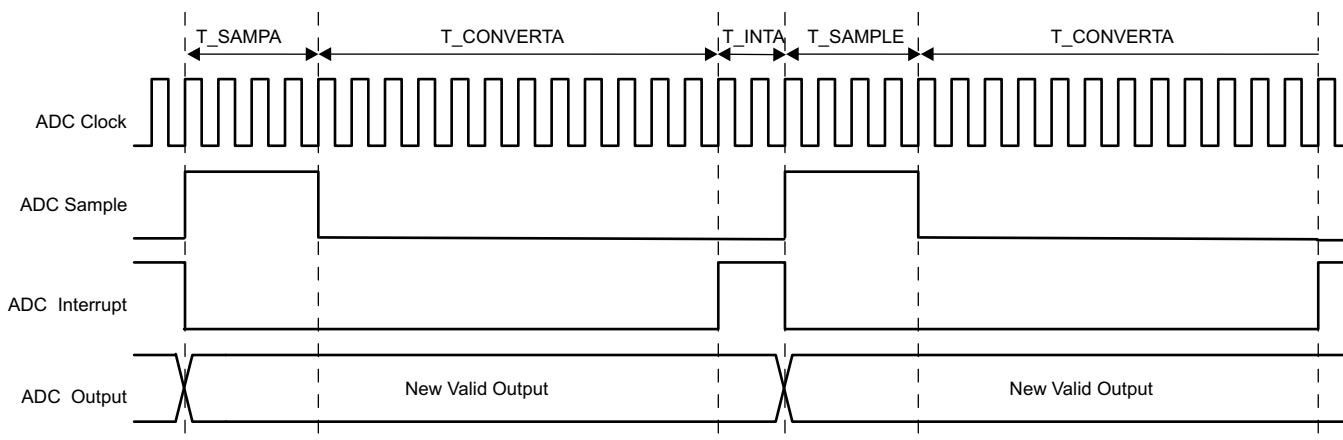


Figure 6. ADC Repeated Conversion Timing

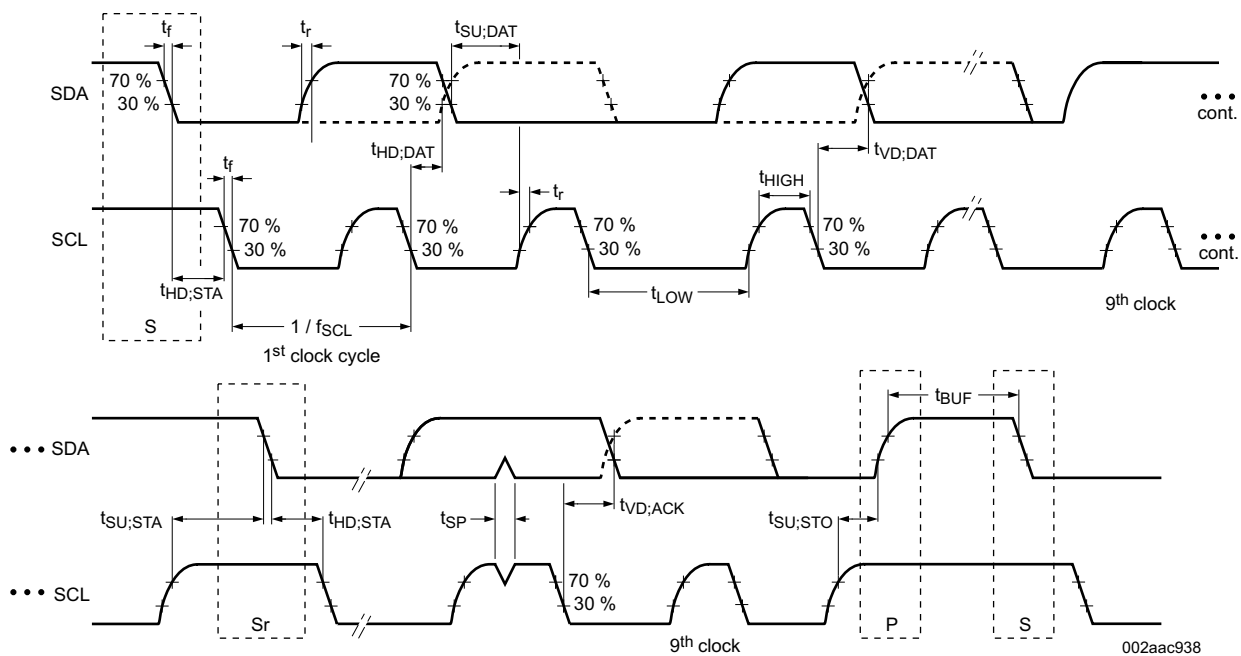
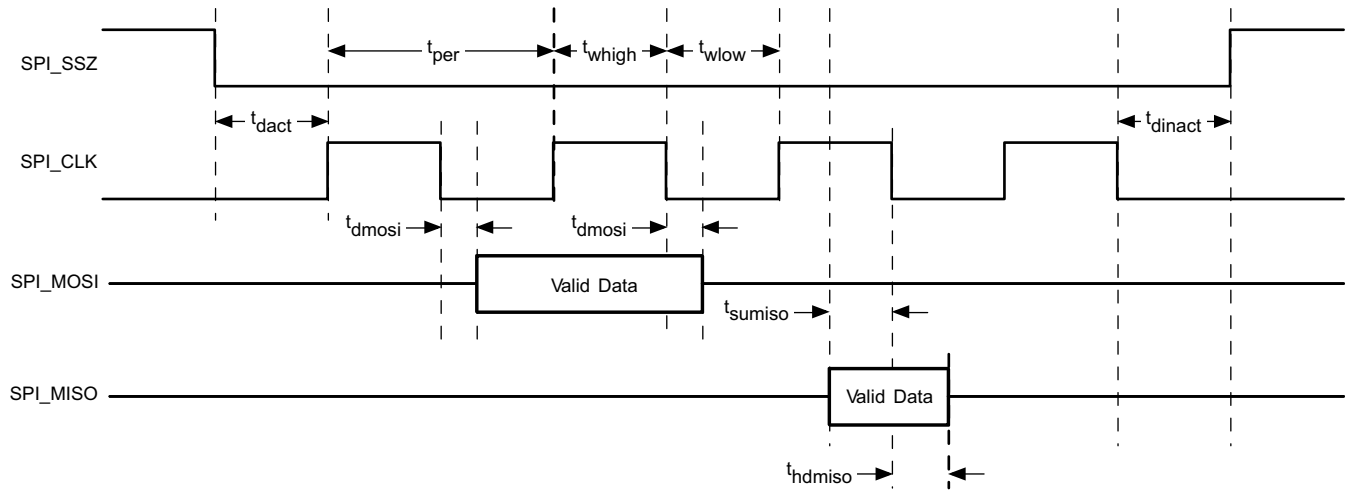
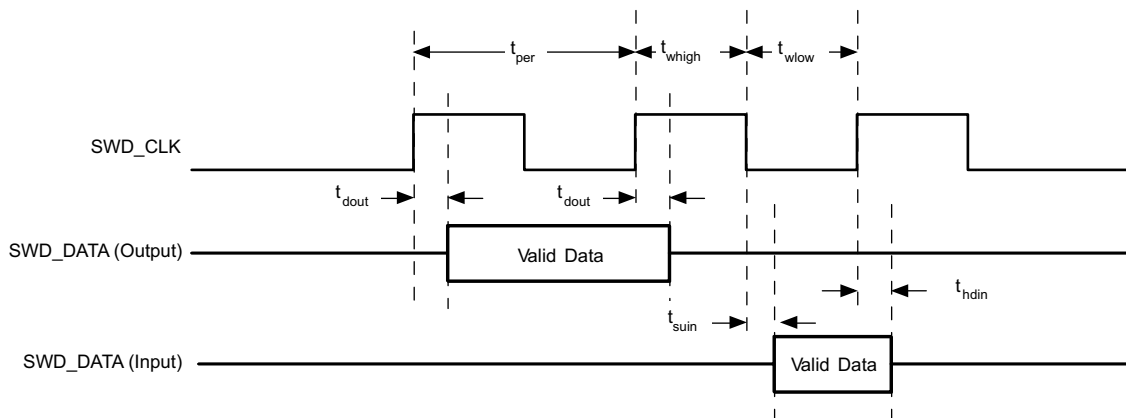


Figure 7. I<sup>2</sup>C Slave Interface Timing

**Parameter Measurement Information (continued)**



**Figure 8. SPI Master Timing**



**Figure 9. SWD Timing**

## 9 Detailed Description

### 9.1 Overview

The TPS65982 is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for a USB Type-C and PD plug or receptacle. The TPS65982 communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port power switches, controls an external high current port power switch, and multiplexes high-speed data to the port for USB2.0 and supported Alternate Mode sideband information. The TPS65982 also controls an attached super-speed multiplexer to simultaneously support USB3.0/3.1 data rates and DisplayPort video.

The TPS65982 is divided into six main sections: the USB-PD controller, the cable plug and orientation detection circuitry, the port power switches, the port data multiplexer, the power management circuitry, and the digital core.

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the C\_CC1 pin or the C\_CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features and more detailed circuitry, refer to the [USB-PD Physical Layer](#) section.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, refer to the [Cable Plug and Orientation Detection](#) section.

The port power switches provide power to the system port through the VBUS pin and also through the C\_CC1 or C\_CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, refer to the [Port Power Switches](#) section.

The port data multiplexer connects various input pairs to the system port through the C\_USB\_TP, C\_USB\_TN, C\_USB\_BP, C\_USB\_BN, C\_SBU1 and C\_SBU2 pins. For a high-level block diagram of the port data multiplexer, a description of its features and more detailed circuitry, refer to the [USB Type-C Port Data Multiplexer](#) section.

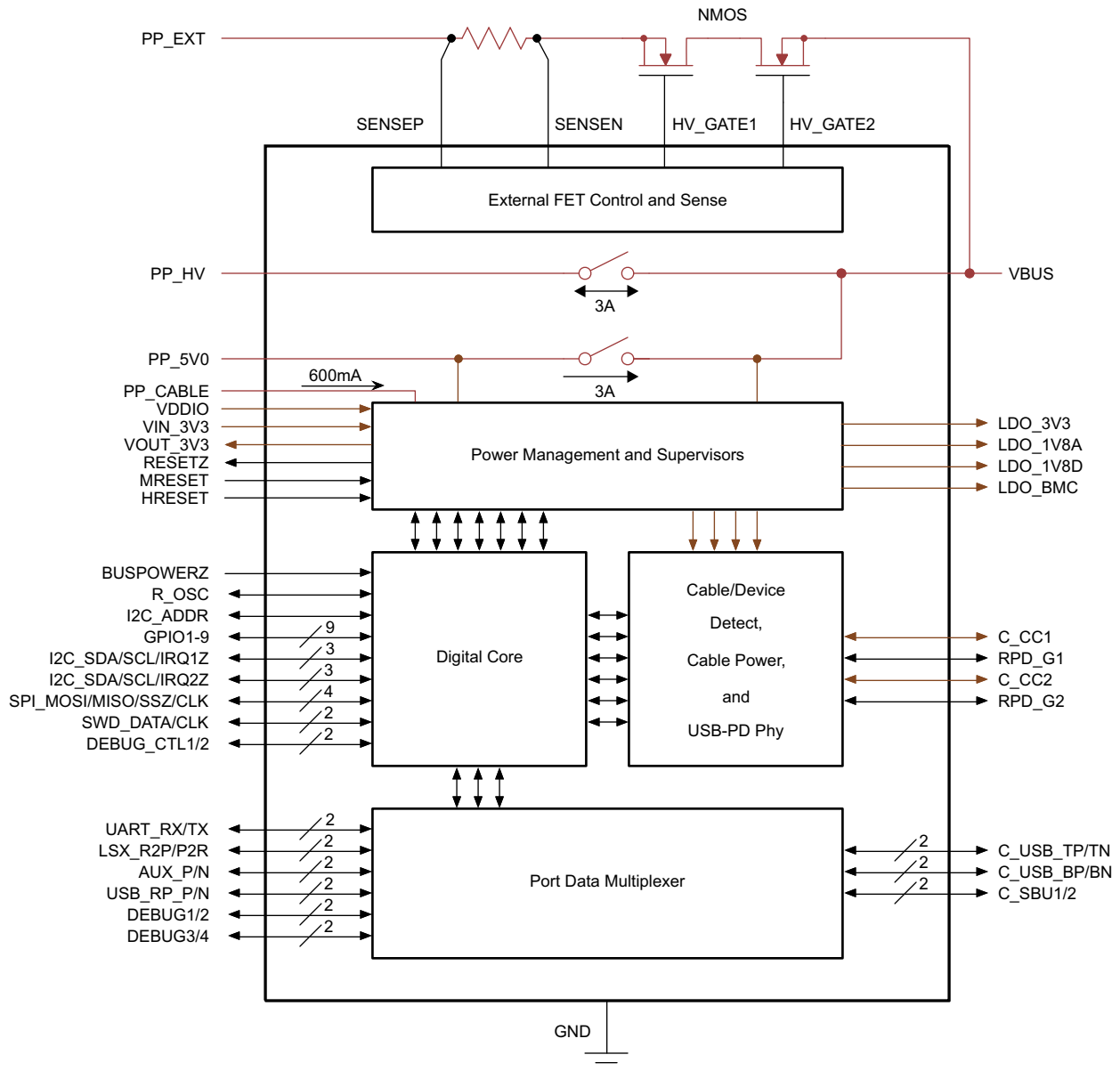
The power management circuitry receives and provides power to the TPS65982 internal circuitry and to the VOUT\_3V3 and LDO\_3V3 outputs. For a high-level block diagram of the power management circuitry, a description of its features and more detailed circuitry, refer to the [Power Management](#) section.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS65982 functionality. A small portion of the digital core contains non-volatile memory, called boot code, which is capable of initializing the TPS65982 and loading a larger, configurable portion of application code into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features and more detailed circuitry, refer to the [Digital Core](#) section.

The digital core of the TPS65982 also interprets and uses information provided by the analog-to-digital converter ADC (see the [ADC](#) section), is configurable to read the status of general purpose inputs and trigger events accordingly, and controls general outputs which are configurable as push-pull or open-drain types with integrated pullup or pulldown resistors and can operate tied to a 1.8 V or 3.3 V rail. The TPS65982 is an I<sup>2</sup>C slave to be controlled by a host processor (see the [I<sup>2</sup>C Slave Interface](#) section), an SPI master to write to and read from an external flash memory (see the [SPI Master Interface](#) section), and is programmed by a single-wire debugger (SWD) connection (see the [Single-Wire Debugger Interface](#) section).

The TPS65982 also integrates a thermal shutdown mechanism (see [Thermal Shutdown](#) section) and runs off of accurate clocks provided by the integrated oscillators (see the [Oscillators](#) section).

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 USB-PD Physical Layer

Figure 10 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.



Feature Description (continued)

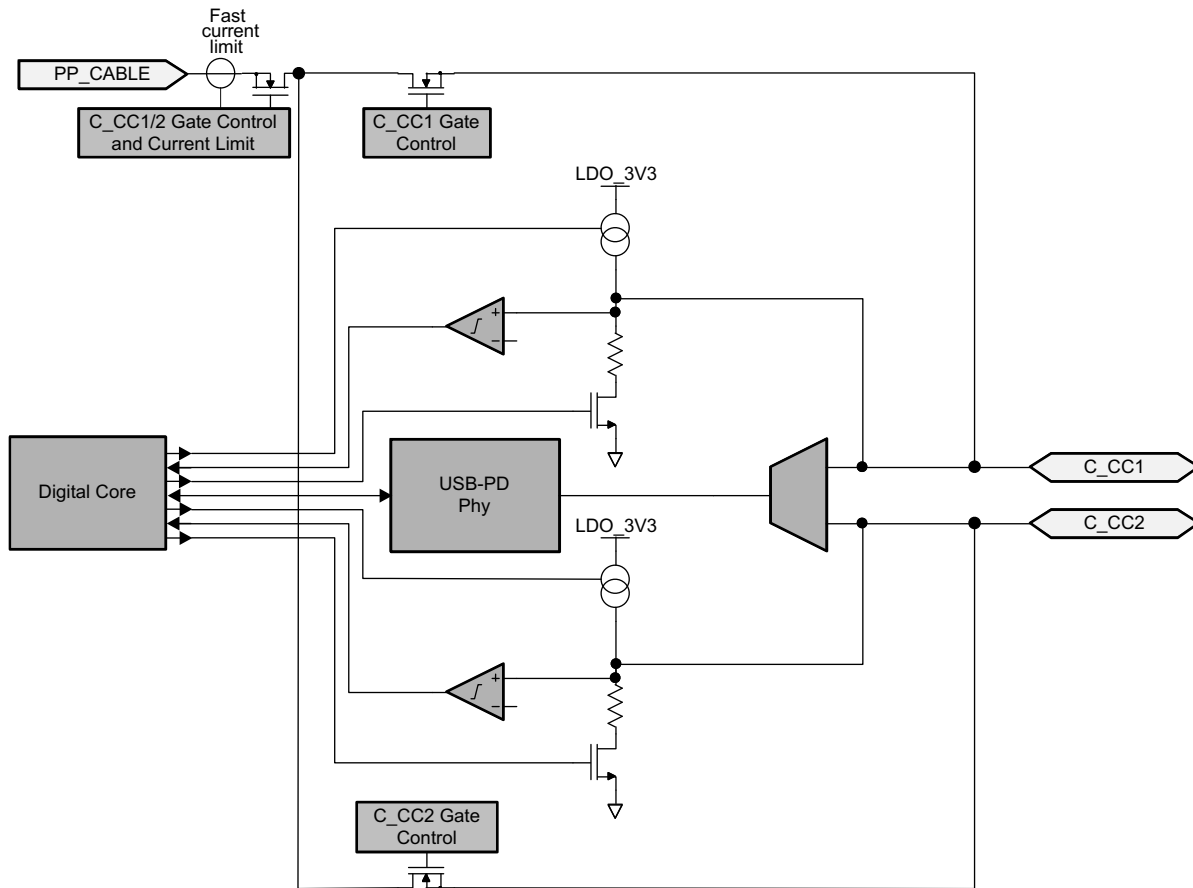


Figure 10. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (C\_CC1 or C\_CC2) that is DC biased because of the DFP (or UFP) cable attach mechanism discussed in the [Cable Plug and Orientation Detection](#) section.

9.3.1.1 USB-PD Encoding and Signaling

Figure 11 shows the high-level block diagram of the baseband USB-PD transmitter. Figure 12 shows the high-level block diagram of the baseband USB-PD receiver.

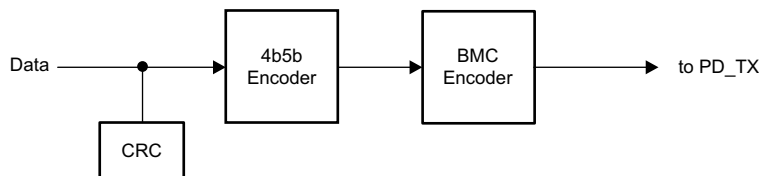
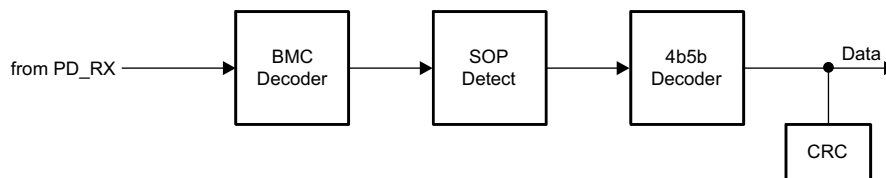


Figure 11. USB-PD Baseband Transmitter Block Diagram

## Feature Description (continued)

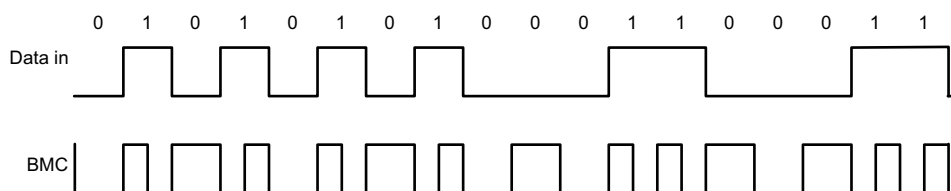


**Figure 12. USB-PD Baseband Receiver Block Diagram**

The USB-PD baseband signal is driven on the C\_CCn pins with a tri-state driver. The tri-state driver is slew rate limited to reduce the high frequency components imparted on the cable and to avoid interference with frequencies used for communication.

### 9.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS65982 is compliant to the [USB-PD Specifications](#). The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). [Figure 13](#) shows Biphase Mark Coding.



**Figure 13. Biphase Mark Coding Example**

The USB PD baseband signal is driven onto the C\_CC1 or C\_CC2 pins with a tri-state driver. The tri-state driver is slew rate limited to limit coupling to D+/D- and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter will start by transmitting a low level. The receiver at the other end will tolerate the loss of the first edge. The transmitter will terminate the final bit by an edge to ensure the receiver clocks the final bit of EOP.

### 9.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded 1 contains a signal edge at the beginning and middle of the UI, and the BMC coded 0 contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude because of the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that will have minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the [USB-PD Specifications](#) for more details.

### 9.3.1.4 USB-PD BMC Transmitter

The TPS65982 transmits and receives USB-PD data over one of the C\_CCn pins. The C\_CCn pin is also used to determine the cable orientation (see the [Cable Plug and Orientation Detection](#) section) and maintain cable/device attach detection. Thus, a DC bias will exist on the C\_CCn. The transmitter driver will overdrive the C\_CCn DC bias while transmitting, but will return to a Hi-Z state allowing the DC voltage to return to the C\_CCn pin when not transmitting. [Figure 14](#) shows the USB-PD BMC TX/Rx driver block diagram.

Feature Description (continued)

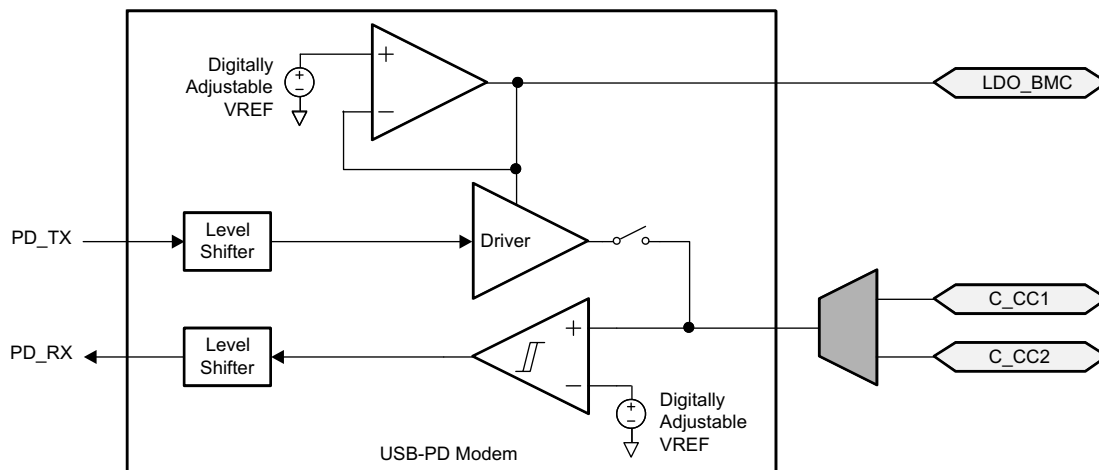


Figure 14. USB-PD BMC TX/Rx Block Diagram

Figure 15 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum threshold for detecting a UFP attach (VD\_CCH\_USB) and the maximum threshold for detecting a UFP attach to a DFP (VD\_CCH\_3P0) defined in the [Cable Plug and Orientation Detection](#) section. This means that the DC bias can be below VOH of the transmitter driver or above VOH.

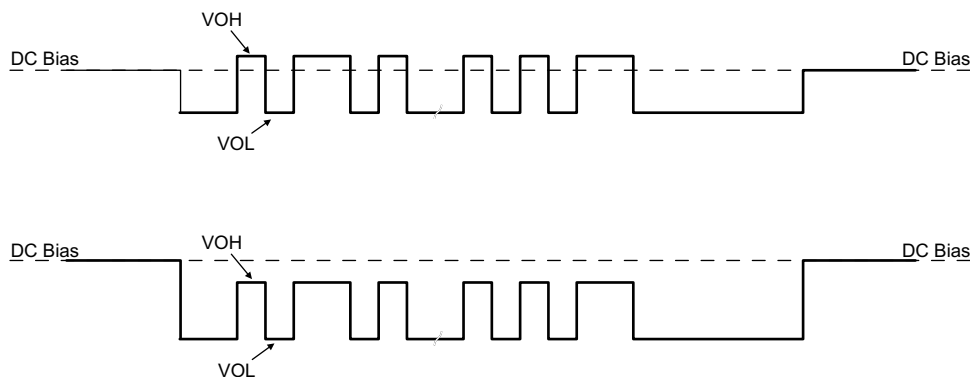


Figure 15. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the C\_CCn lines. The signal peak VTXP is adjustable by application code and sets the VOH/VOL for the BMC data that is transmitted, and is defined in [USB-PD TX Driver Voltage Adjustment Parameter](#). Keep in mind that the settings in a final system must meet the TX masks defined in the [USB-PD Specifications](#).

When driving the line, the transmitter driver has an output impedance of ZDRIVER. ZDRIVER is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. ZDRIVER impacts the noise ingress in the cable.

Figure 16 shows the simplified circuit determining ZDRIVER. It is specified such that noise at the receiver is bounded.

ZDRIVER is defined by [Equation 1](#).

$$ZDRIVER = \frac{R_{DRIVER}}{1 + s \times R_{DRIVER} \times C_{DRIVER}} \tag{1}$$

Feature Description (continued)

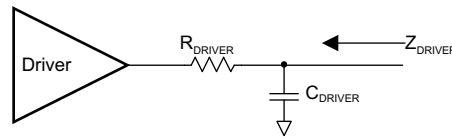


Figure 16. ZDRIVER Circuit

9.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS65982 receives a signal that falls within the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask. The values for VRXTR and VRXTF are listed in [USB-PD Baseband Signal Requirements and Characteristics](#).

Figure 17 shows an example of a multi-drop USB-PD connection. This connection has the typical UFP (device) to DFP (host) connection, but also includes cable USB-PD TX/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (ZBMC RX). The [USB-PD Specification](#) also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

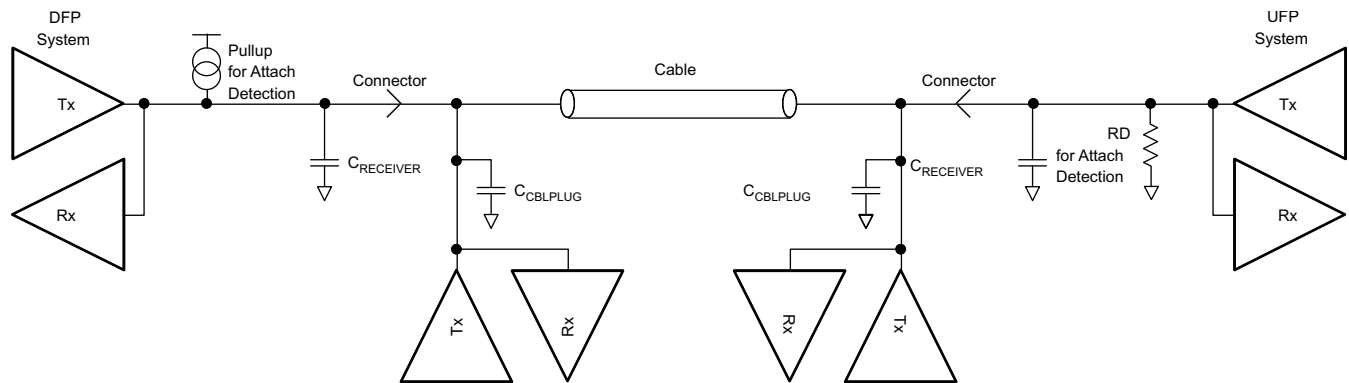


Figure 17. Example USB-PD Multi-Drop Configuration

9.3.2 Cable Plug and Orientation Detection

Figure 18 shows the plug and orientation detection block at each C\_CC pin (C\_CC1 and C\_CC2). Each pin has identical detection circuitry.

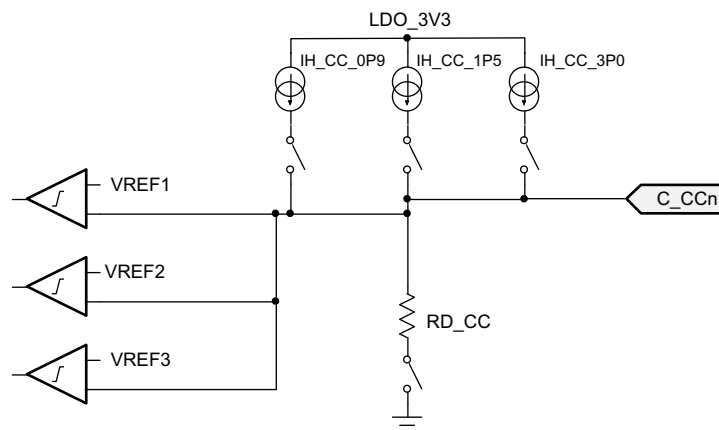


Figure 18. Plug and Orientation Detection Block

## Feature Description (continued)

### 9.3.2.1 Configured as a DFP

When configured as a DFP, the TPS65982 detects when a cable or a UFP is attached using the C\_CC1 and C\_CC2 pins. When in a disconnected state, the TPS65982 monitors the voltages on these pins to determine what, if anything, is connected. See the [USB Type-C Specification](#) for more information.

Table 1 shows the high-level detection results. Refer to the [USB Type-C Specification](#) for more information.

**Table 1. Cable Detect States for a DFP**

C_CC1	C_CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both C_CC pins for attach. Power is not applied to VBUS or VCONN until a UFP connect is detected.
Rd	Open	UFP attached	Monitor C_CC1 for detach. Power is applied to VBUS but not to VCONN (C_CC2).
Open	Rd	UFP attached	Monitor C_CC2 for detach. Power is applied to VBUS but not to VCONN (C_CC1).
Ra	Open	Powered Cable/No UFP attached	Monitor C_CC2 for a UFP attach and C_CC1 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Open	Ra	Powered Cable/No UFP attached	Monitor C_CC1 for a UFP attach and C_CC2 for cable detach. Power is not applied to VBUS or VCONN (C_CC1) until a UFP attach is detected.
Ra	Rd	Powered Cable/UFP Attached	Provide power on VBUS and VCONN (C_CC1) then monitor C_CC2 for a UFP detach. C_CC1 is not monitored for a detach.
Rd	Ra	Powered Cable/UFP attached	Provide power on VBUS and VCONN (C_CC2) then monitor C_CC1 for a UFP detach. C_CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either C_CC pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either C_CC pin for detach.

When the TPS65982 is configured as a DFP, a current IH\_CC is driven out each C\_CCn pin and each pin is monitored for different states. When a UFP is attached to the pin, a pulldown resistance of Rd to GND will exist. The current IH\_CC is then forced across the resistance Rd generating a voltage at the C\_CCn pin.

When configured as a DFP advertising Default USB current sourcing capability, the TPS65982 applies IH\_CC\_USB to each C\_CCn pin. When a UFP with a pulldown resistance Rd is attached, the voltage on the C\_CCn pin will pull below VH\_CCD\_USB. The TPS65982 can also be configured as a DFP to advertise default (500 mA), 1.5 A and 3 A sourcing capabilities.

When the C\_CCn pin is connected to an active cable VCONN (power to the active cable), the pulldown resistance will be different (Ra). In this case, the voltage on the C\_CCn pin will pull below VH\_CCA\_USB/1P5/3P0 and the system will recognize the active cable.

The VH\_CCD\_USB/1P5/3P0 thresholds are monitored to detect a disconnection from each of these cases respectively. When a connection has been recognized and the voltage on the C\_CCn pin rises above the VH\_CCD\_USB/1P5/3P0 threshold, the system will register a disconnection.

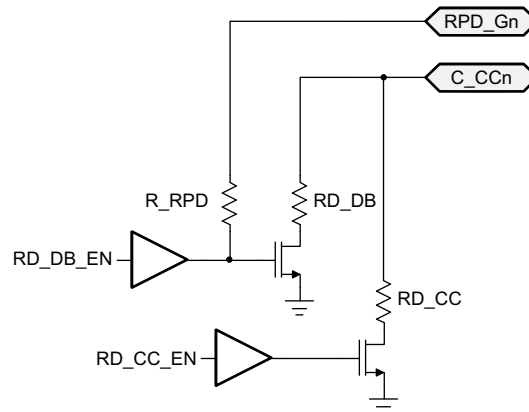
### 9.3.2.2 Configured as a UFP

When the TPS65982 is configured as a UFP, the TPS65982 presents a pulldown resistance RD\_CC on each C\_CCn pin and waits for a DFP to attach and pullup the voltage on the pin. The DFP will pullup the C\_CC pin by applying either a resistance or a current. The UFP detects an attachment by the presence of VBUS. The UFP determines the advertised current from the DFP by the pullup applied to the C\_CCn pin.

### 9.3.2.3 Dead-Battery or No-Battery Support

Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source will provide a voltage on VBUS. The TPS65982 is hardware-configurable to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd when the port is acting as a source. [Figure 19](#) shows the RPD\_Gn pin used to configure the behavior of the C\_CCn pins, and elaborates on the basic cable plug and orientation detection block shown in [Figure 18](#). RPD\_G1 and RPD\_G2 configure C\_CC1 and C\_CC2 respectively. A resistance R\_RPD is connected to the gate of the pulldown FET on each C\_CCn pin.

This resistance must be pin-strapped externally to configure the C\_CCn pin to behave in one of two ways: present an Rd pulldown resistance or present a Hi-Z when the TPS65982 is unpowered. During normal operation, RD will be RD\_CC; however, while dead-battery or no-battery conditions exist, the resistance is untrimmed and will be RD\_DB. When RD\_DB is presented during dead-battery or no-battery, application code will switch to RD\_CC.



**Figure 19. C\_CCn and RPD\_Gn pins**

When C\_CC1 is shorted to RPD\_G1 and C\_CC2 is shorted to RPD\_G2 in an application of the TPS65982, booting from dead-battery or no-battery conditions will be supported. In this case, the gate driver for the pulldown FET is Hi-Z at its output. When an external connection pulls up on C\_CCn (the case when connected to a DFP advertising with a pullup resistance Rp or pullup current), the connection through R\_RPD will pull up on the FET gate turning on the pulldown through RD\_DB. In this condition, the C\_CCn pin will act as a clamp VTH\_DB in series with the resistance RD\_DB.

When RPD\_G1 and RPD\_G2 are shorted to GND in an application and not electrically connected to C\_C1 and C\_CC2, booting from dead-battery or no-battery conditions is not possible. In this case, the TPS65982 will present a Hi-Z on the C\_CC1 and C\_CC2 pins and a USB Type-C source will never provide a voltage on VBUS.

### 9.3.3 Port Power Switches

Figure 20 shows the TPS65982 port power path including all internal and external paths. The port power path provides to VBUS from PP\_5V0, provides power to or from VBUS from or to PP\_HV, provides power to or from an external port power node (shown and referred to as PP\_EXT) from or to VBUS, and provides power from PP\_CABLE to C\_CC1 or C\_CC2. The PP\_CABLE to C\_CCn switches shown in Figure 20 are the same as in Figure 10, but are now shown without the analog USB Type-C cable plug and orientation detection circuitry.

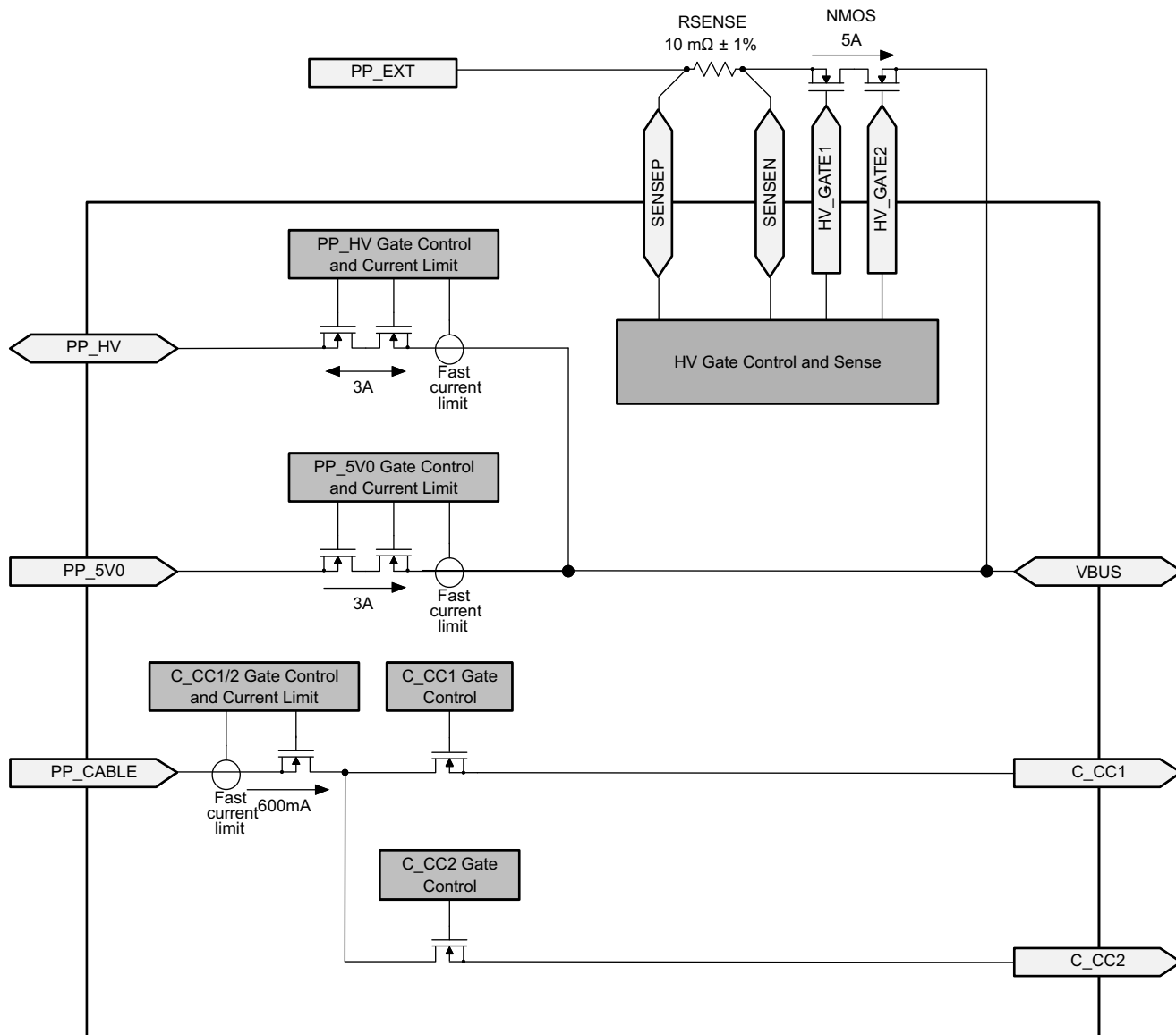


Figure 20. Port Power Paths

### 9.3.3.1 5V Power Delivery

The TPS65982 provides port power to VBUS from PP\_5V0 when a low voltage output is needed. The switch path provides 5 V at up to 3 A to from PP\_5V0 to VBUS. Figure 20 shows a simplified circuit for the switch from PP\_5V0 to VBUS.

### 9.3.3.2 5V Power Switch as a Source

The PP\_5V0 path is unidirectional, sourcing power from PP\_5V0 to VBUS only. When the switch is on, the protection circuitry limits reverse current from VBUS to PP\_5V0. Figure 21 shows the I-V characteristics of the reverse current protection feature. Figure 21 and the reverse current limit can be approximated using Equation 2.

$$I_{REV5V0} = V_{REV5V0} / R_{PP5V} \quad (2)$$

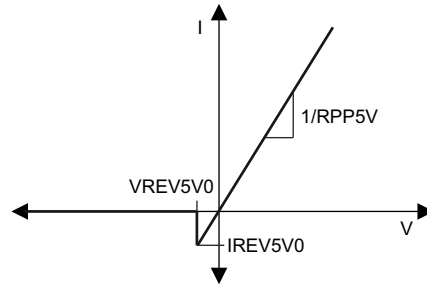


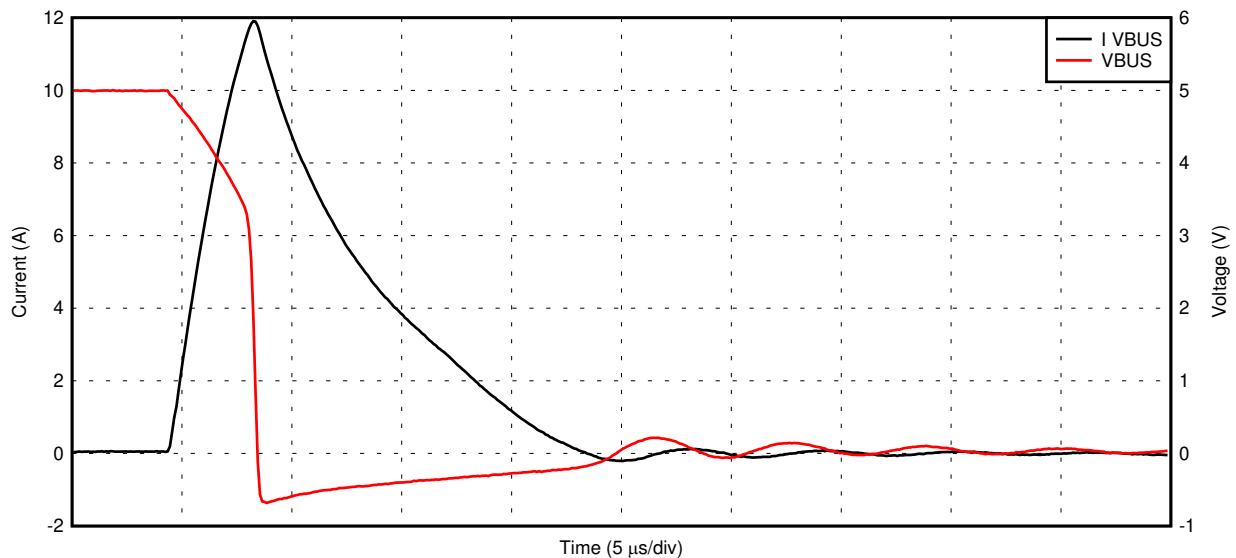
Figure 21. 5V Switch I-V Curve

9.3.3.3 PP\_5V0 Current Sense

The current from PP\_5V0 to VBUS is sensed through the switch and is available to be read digitally through the ADC.

9.3.3.4 PP\_5V0 Current Limit

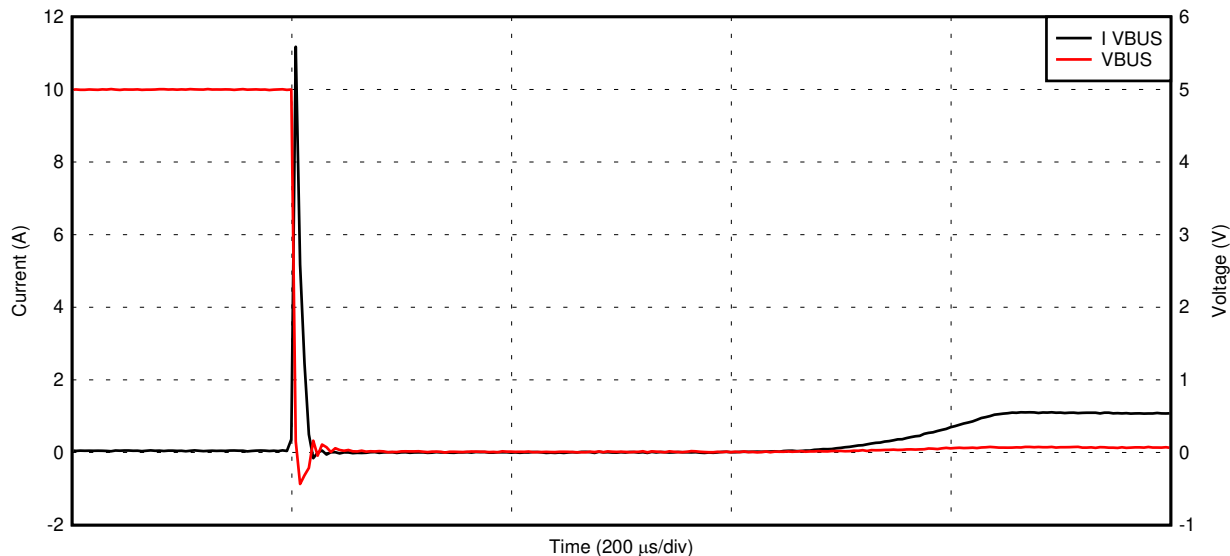
The current through PP\_5V0 to VBUS is limited to ILIMPP5V and is controlled automatically by the digital core. When the current exceeds ILIMPP5V, the current-limit circuit activates. Depending on the severity of the over-current condition, the transient response will react in one of two ways: Figure 22 and Figure 23 show the approximate response time and clamping characteristics of the circuit for a hard short while Figure 24 shows the approximate response time and clamping characteristics for a soft short with a load of 2 Ω.



D004

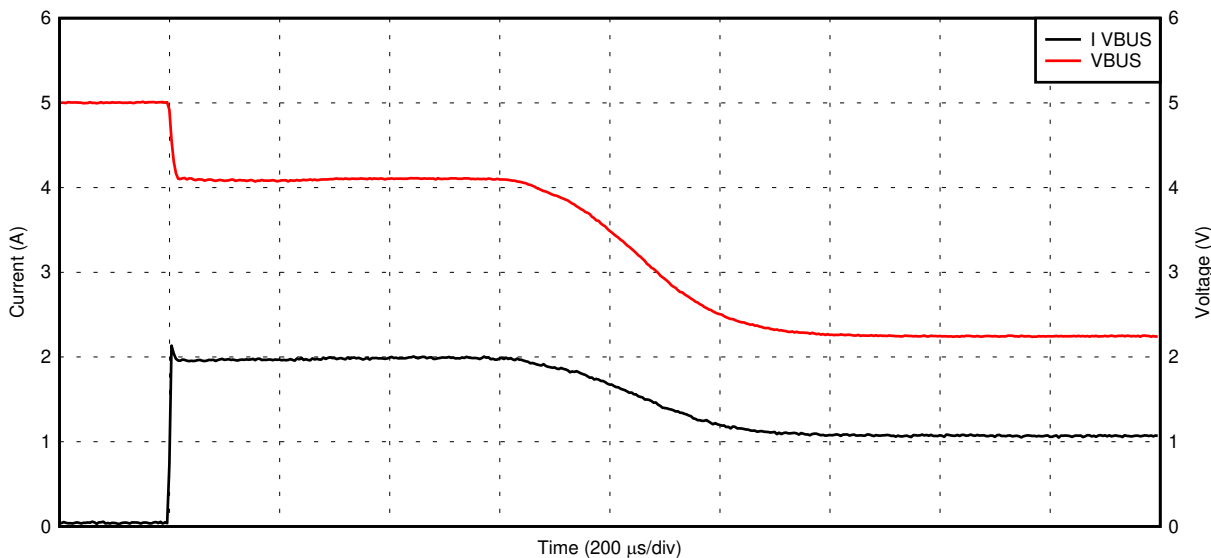
Figure 22. PP\_5V0 Current Limit with a Hard Short





D005

Figure 23. PP\_5V0 Current Limit with a Hard Short (Extended Time Base)



D006

Figure 24. PP\_5V0 Current Limit with a Soft Short (2 Ω)

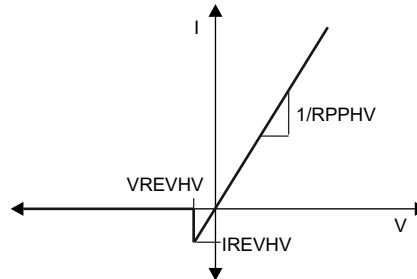
### 9.3.3.5 Internal HV Power Delivery

The TPS65982 has an integrated, bi-directional high-voltage switch that is rated for up to 3 Amps of current. The TPS65982 is capable of sourcing or sinking high-voltage power through an internal switch path designed to support USB-PD power up to 20 V at 3 A of current. VBUS and PP\_HV are both rated for up to 22 V as determined by [Recommended Operating Conditions](#), and operate down to 0 V as determined by [Absolute Maximum Ratings](#). In addition, VBUS is tolerant to voltages up to 22 V even when PP\_HV is at 0 V. Similarly, PP\_HV is tolerant up to 22 V while VBUS is at 0 V. The switch structure is designed to tolerate a constant operating voltage differential at either of these conditions. [Figure 20](#) shows a simplified circuit for the switch from PP\_HV to VBUS.

### 9.3.3.6 Internal HV Power Switch as a Source

The TPS65982 provides power from PP\_HV to VBUS at the USB Type-C port as an output when operating as a source. When the switch is on as a source, the path behaves resistively until the current reaches the amount calculated by Equation 3 and then blocks reverse current from VBUS to PP\_HV. Figure 25 shows the diode behavior of the switch as a source.

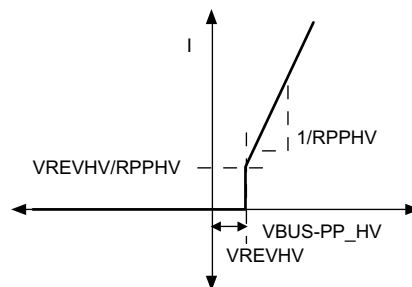
$$I_{REVHV} = V_{REVHV}/R_{PPHV} \quad (3)$$



**Figure 25. Internal HV Switch I-V Curve as a Source**

### 9.3.3.7 Internal HV Power Switch as a Sink

The TPS65982 can also receive power from VBUS to PP\_HV when operating as a sink. When the switch is on as a sink the path behaves as an ideal diode and blocks reverse current from PP\_HV to VBUS. Figure 26 shows the diode behavior of the switch as a sink.



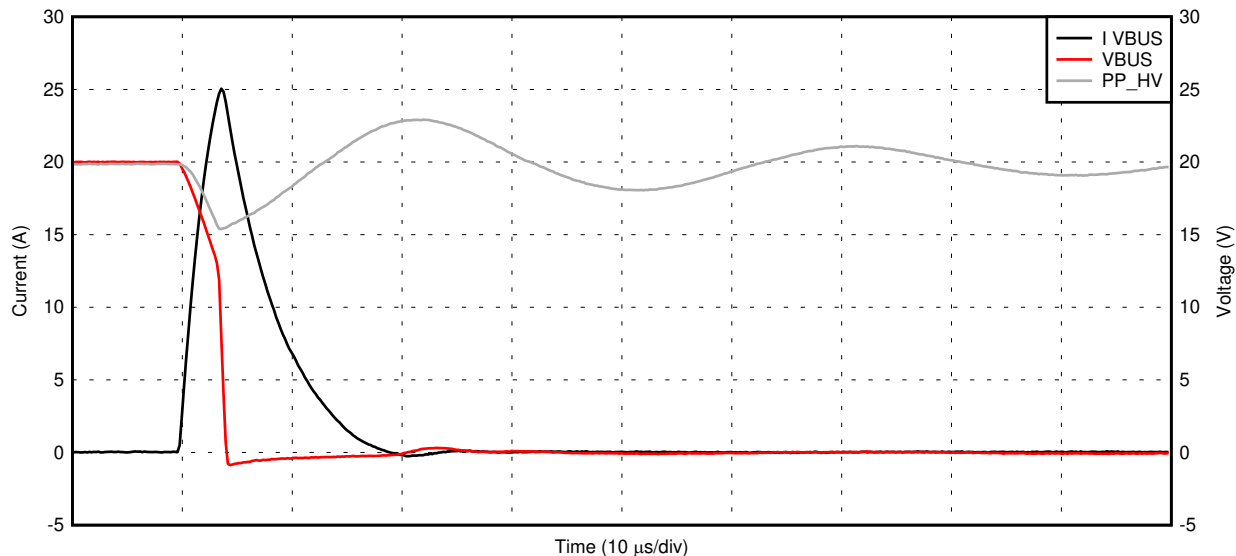
**Figure 26. Internal HV Switch I-V Curve as a Sink**

### 9.3.3.8 Internal HV Power Switch Current Sense

The current from PP\_HV to VBUS is sensed through the switch and is available to be read digitally through the ADC only when the switch is sourcing power. When sinking power, the readout from the ADC will not reflect the current.

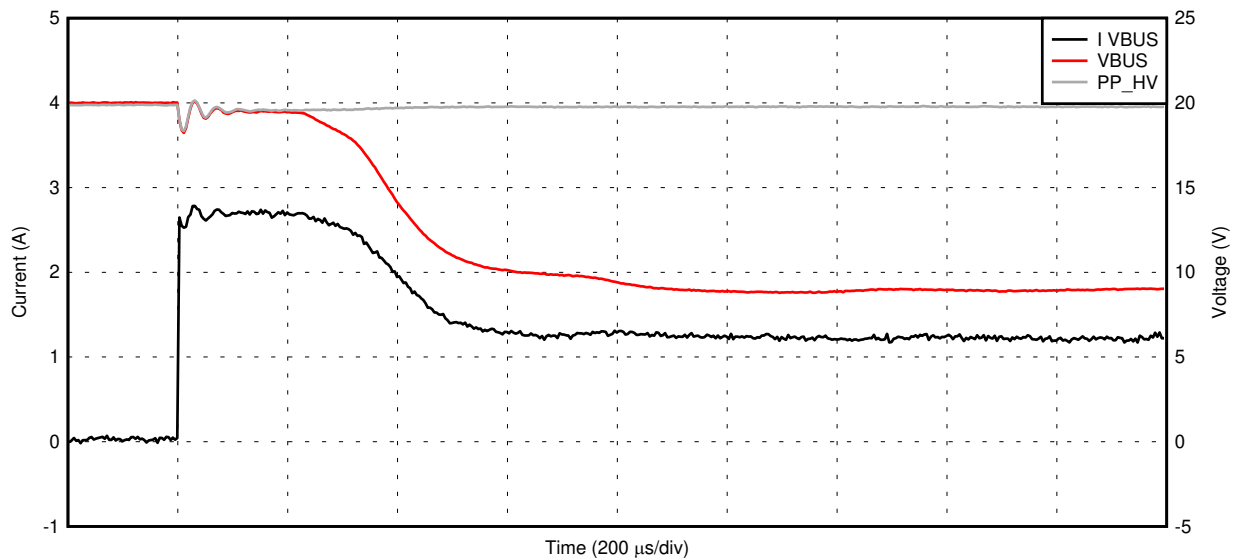
### 9.3.3.9 Internal HV Power Switch Current Limit

The current through PP\_HV to VBUS is current limited to ILIMPPHV (only when operating as a source) and is controlled automatically by the digital core. When the current exceeds ILIMPPHV, the current-limit circuit activates. Depending on the severity of the over-current condition, the transient response will react in one of two ways: Figure 27 shows the approximate response time and clamping characteristics of the circuit for a hard short while Figure 28 shows the approximate response time and clamping characteristics for a soft short of 7 Ω.



D007

Figure 27. PP\_HV Current Limit Response with a Hard Short



D008

Figure 28. PP\_HV Current Limit Response with a Soft Short (7 Ω)

9.3.3.10 External HV Power Delivery

The TPS65982 is capable of controlling an external high-voltage, common-drain back-to-back NMOS FET switch path to source or sink power up to the maximum limit of the USB PD specification: 20 V at 5 A of current. The TPS65982 provides external control and sense to external NMOS power switches for currents greater than 3 A. This path is bi-directional for either sourcing current to VBUS or sinking current from VBUS. The external NMOS switches are back-to-back to protect the system from large voltage differential across the FETs as well as blocking reverse current flow. Each NFET has a separate gate control. HV\_GATE2 is always connected to the VBUS side and HV\_GATE1 is always connected to the opposite side, referred to as PP\_EXT. Two sense pins, SENSEP and SENSEN, are used to implement reverse current blocking, over-current protection, and current sensing. The external path may be used in conjunction with the internal path. For example, the internal path may

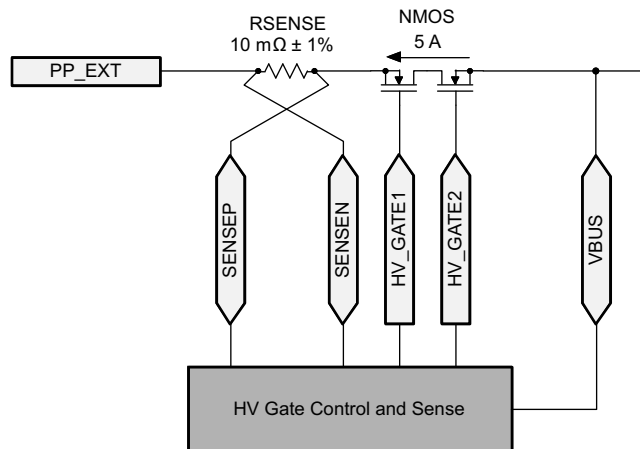
be used to source current from PP\_HV to VBUS when the TPS65982 is acting as a power source and the external path may be used to sink current from VBUS to PP\_EXT to charge a battery when the TPS65982 is acting as a sink. The internal and external paths must never be used in parallel to source current at the same time or sink current at the same time. The current limiting function will not function properly in this case and may become unstable.

### 9.3.3.11 External HV Power Switch as a Source with RSENSE

Figure 20 shows the configuration when the TPS65982 is acting as a source for the external switch path. The external FETs must be connected in a common-drain configuration and will not work in a common source configuration. In this mode, current is sourced to VBUS. RSENSE provides an accurate current measurement and is used to initiate the current limiting feature of the external power path. The voltage between SENSEP (PP\_EXT) and SENSEN (VBUS) is sensed to block reverse current flow. This measurement is also digitally readable via the ADC.

### 9.3.3.12 External HV Power Switch as a Sink with RSENSE

Figure 29 shows the configuration when the TPS65982 is acting as a sink for the external switch path with RSENSE used to sense current. Acting as a sink, the voltage between SENSEP (VBUS) and SENSEN (PP\_EXT) is sensed to provide an accurate current measurement and initiate the current limiting feature of the external power path. This measurement is also digitally readable via the ADC.



**Figure 29. External HV Switch as a Sink with RSENSE**

### 9.3.3.13 External HV Power Switch as a Sink without RSENSE

Figure 30 shows the configuration when the TPS65982 is acting as a sink for the external switch path without an RSENSE resistor. In this mode, current is sunk from VBUS to an internal system power node, referred to as PP\_EXT. This is used for charging a battery or for providing a supply voltage for a bus-powered device. To block reverse current, the VBUS and SENSEP pins monitor the voltage across the NFETs. To ensure that SENSEN does not float, tie SENSEP to SENSEN in this configuration. When configured in this mode, the digital readout from current from the ADC will be approximately zero.

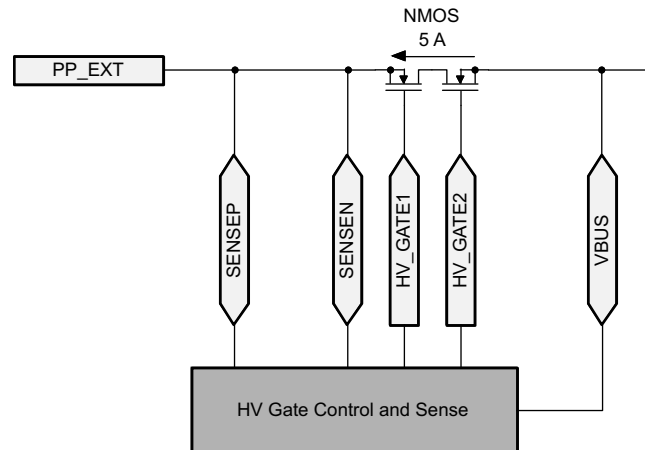


Figure 30. External HV Switch as a Sink without RSENSE

#### 9.3.3.14 External Current Sense

The current through the external NFETs to VBUS is sensed through the RSENSE resistor and is available to be read digitally through the ADC. When acting as a source, the readout from the ADC will only accurately reflect the current through the external NFETs when the connection of SENSEP and SENSEN adheres to Figure 20. When acting as a sink, the readout from the ADC will only accurately reflect the current through the external NFETs when the connection of SENSEP and SENSEN adheres to Figure 29.

#### 9.3.3.15 External Current Limit

The current through the external NFETs to VBUS is current limited when acting as a source or a sink. The current is sensed across the external RSENSE resistance. The current limit is set by a combination of the RSENSE magnitude and configuration settings for the voltage across the resistance. When the voltage across the RSENSE resistance exceeds the automatically set voltage limit, the current-limit circuit is activated.

#### 9.3.3.16 Soft Start

When configured as a sink, the SS pin provides a soft start function for each of the high-voltage power path supplies (P\_HV and external PP\_EXT path) up to 5.5 V. The SS circuitry is shared for each path and only one path will turn on as a sink at a time. The soft start is enabled by application code or via the host processor. The SS pin is initially discharged through a resistance RSS\_DIS. When the switch is turned on, a current ISS is sourced from the pin to a capacitance CSS. This current into the capacitance generates a slow ramping voltage. This voltage is sensed and the power path FETs turn on and the voltage follows this ramp. When the voltage reaches the threshold VTHSS, the power path FET will be near being fully turned on, the output voltage will be fully charged. At time TSSDONE, a signal to the digital core indicates that the soft start function has completed. The ramp rate of the supply is given by Equation 4:

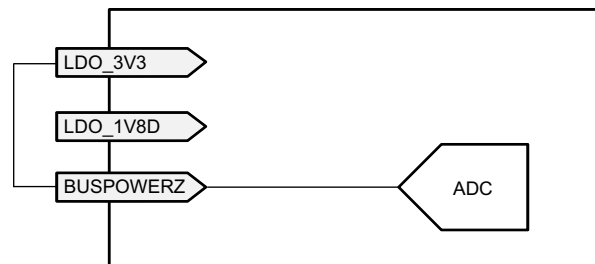
$$\text{Ramp Rate} = 9 \times \frac{\text{ISS}}{\text{CSS}} \quad (4)$$

The maximum ramp voltage for the supply is approximately 16.2 V. For any input voltage higher than this, the ramp will stop at 16.2 V until the firmware disables the soft start. At this point, the voltage will step to the input voltage at a ramp rate defined by approximately 7  $\mu\text{A}$  into the gate capacitance of the switch. The TSSDONE time is independent of the actual final ramp voltage.

### 9.3.3.17 BUSPOWERZ

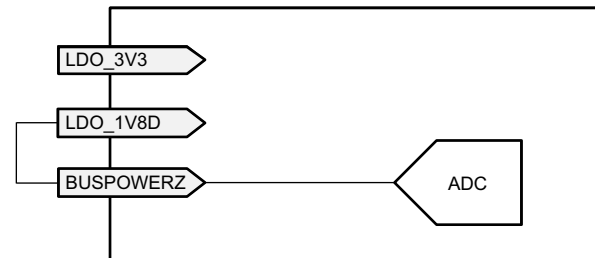
At power-up, when VIN\_3V3 is not present and a dead-battery condition is supported as described in [Dead-Battery or No-Battery Support](#), the TPS65982 will appear as a USB Type-C sink (device) causing a connected USB Type-C source (host) to provide 5 V on VBUS. The TPS65982 will power itself from the 5-V VBUS rail (see [Power Management](#)) and execute boot code (see [Boot Code](#)). The boot code will observe the BUSPOWERZ voltage, which will fall into one of three voltage ranges: VBPZ\_DIS, VBPZ\_HV, and VBPZ\_EXT (defined in [BUSPOWERZ Configuration Characteristics](#)). These three voltage ranges configure how the TPS65982 routes the 5 V present on VBUS to the system in a dead-battery or no-battery scenario.

When the voltage on BUSPOWERZ is in the VBPZ\_DIS range (when BUSPOWERZ is tied to LDO\_3V3 as in [Figure 31](#)), this indicates that the TPS65982 will not route the 5 V present on VBUS to the entire system. In this case, the TPS65982 will load SPI-connected flash memory and execute this application code. This configuration will disable both the PP\_HV and PP\_EXT high voltage switches and only use VBUS to power the TPS65982.



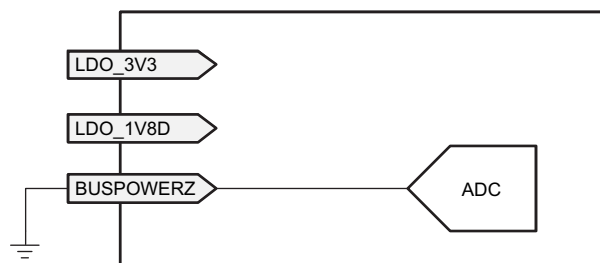
**Figure 31. BUSPOWERZ Configured to Disable Power from VBUS**

The BUSPOWERZ pin can alternately configure the TPS65982 to power the entire system through the PP\_HV internal load switch when the voltage on BUSPOWERZ is in the VBPZ\_HV range (when BUSPOWERZ is tied to LDO\_1V8D as in [Figure 32](#)).



**Figure 32. BUSPOWERZ Configured with PP\_HV as Input Power Path**

The BUSPOWERZ pin can also alternately configure the TPS65982 to power the entire system through the PP\_EXT external load switch when the voltage on BUSPOWERZ is in the VBPZ\_EXT range (when BUSPOWERZ is tied to GND as in [Figure 33](#)).



**Figure 33. BUSPOWERZ Configured with PP\_EXT as Input Power Path**

### 9.3.3.18 Voltage Transitions on VBUS through Port Power Switches

Figure 34 shows the waveform for a positive voltage transition. The timing and voltages apply to both a transition from 0 V to PP\_5V0 and a transition from PP\_5V0 to PP\_HV as well as a transition from PP\_5V0 to an PP\_EXT. A transition from PP\_HV to PP\_EXT is possible and vice versa, but does not necessarily follow the constraints in Figure 34. When a switch is closed to transition the voltage, a maximum slew-rate of SRPOS occurs on the transition. The voltage ramp will remain monotonic until the voltage reaches VSRCVALID within the final voltage. The voltage may overshoot the new voltage by VSRCVALID. After time TSTABLE from the start of the transition, the voltage will fall to within VSRCNEW of the new voltage. During the time TSTABLE, the voltage may fall below the new voltage, but will remain within VSRCNEW of this voltage.

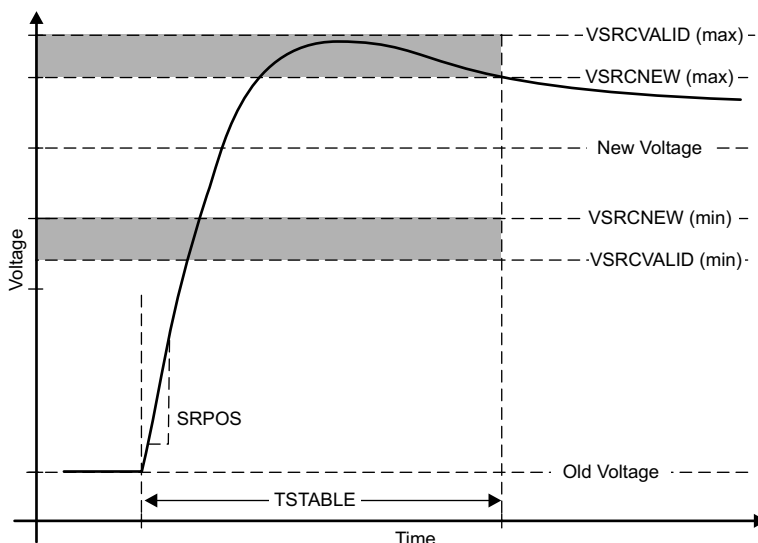


Figure 34. Positive Voltage Transition on VBUS

Figure 35 shows the waveform for a negative voltage transition. The timing and voltages apply to both a transition from PP\_HV to PP\_5V0 and a transition from PP\_5V0 to 0V as well as a transition from PP\_EXT to PP\_5V0. A transition from PP\_HV to PP\_EXT is possible and vice versa, but does not necessarily follow the constraints in Figure 35. When a switch is closed to transition the voltage, a maximum slew-rate of SRNEG occurs on the transition. The voltage ramp will remain monotonic until the voltage reaches TOLTRANUN within the final voltage. The voltage may overshoot the new voltage by TOLTRANLN. After time TSTABLE from the start of the transition, the voltage will fall to within VSRCNEW of the new voltage. During the time TSTABLE, the voltage may fall below the new voltage, but will remain within VSRCNEW of this voltage.

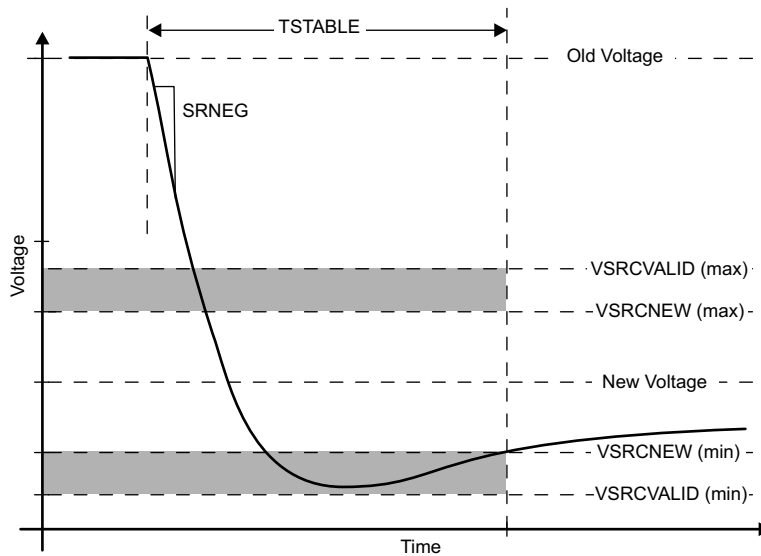


Figure 35. Negative Voltage Transition on VBUS

**9.3.3.19 HV Transition to PP\_RV0 Pull-Down on VBUS**

The TPS65982 has an integrated active pulldown on VBUS when transitioning from PP\_HV to PP\_5V0, shown in Figure 36. When the PP\_HV switch is disabled and  $VBUS > PP\_5V0 + VHVDISPD$ , amplifier turns on a current source and pulls down on VBUS. The amplifier implements active slew rate control by adjusting the pulldown current to prevent the slew rate from exceeding specification. When VBUS falls to within  $VHVDISPD$  of PP\_5V0, the pulldown is turned off. The load on VBUS will then continue to pull VBUS down until the ideal diode switch structure turns on connecting it to PP\_5V0. When switching from PP\_HV or PP\_EXT to PP\_5V0, PP\_HV or PP\_EXT must be above VSO\_HV to follow the switch-over shown in Figure 35.

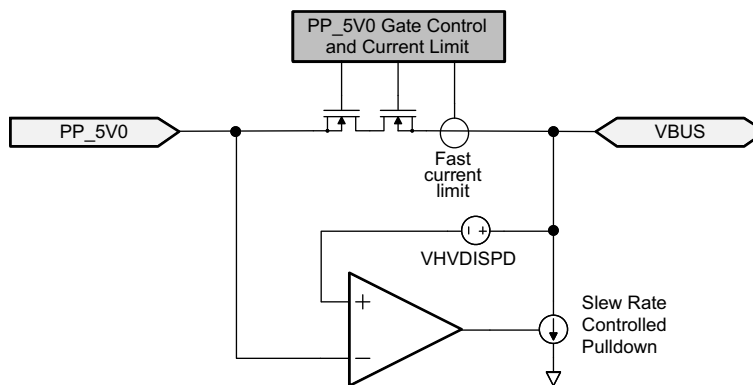


Figure 36. PP\_5V0 Slew Rate Control

**9.3.3.20 VBUS Transition to VSAFE0V**

When VBUS transitions to near 0 V (VSAFE0V), the pulldown circuit in Figure 36 is turned on until VBUS reaches VSAFE0V. This transition will occur within time TSAFE0V.

**9.3.3.21 C\_CC1 and C\_CC2 Power Configuration and Power Delivery**

The C\_CC1 and C\_CC2 pins are used to deliver power to active circuitry inside a connected cable and output USB-PD data to the cable and connected device. Figure 20 shows the C\_CC1, and C\_CC2 outputs to the port. Only one of these pins will be used to deliver power at a time depending on the cable orientation. The other pin will be used to transmit USB-PD data through the cable to a connected device.



Figure 37 shows a high-level flow of connecting these pins based on the cable orientation. See the *Cable Plug and Orientation Detection* section for more detailed information on plug and orientation detection.

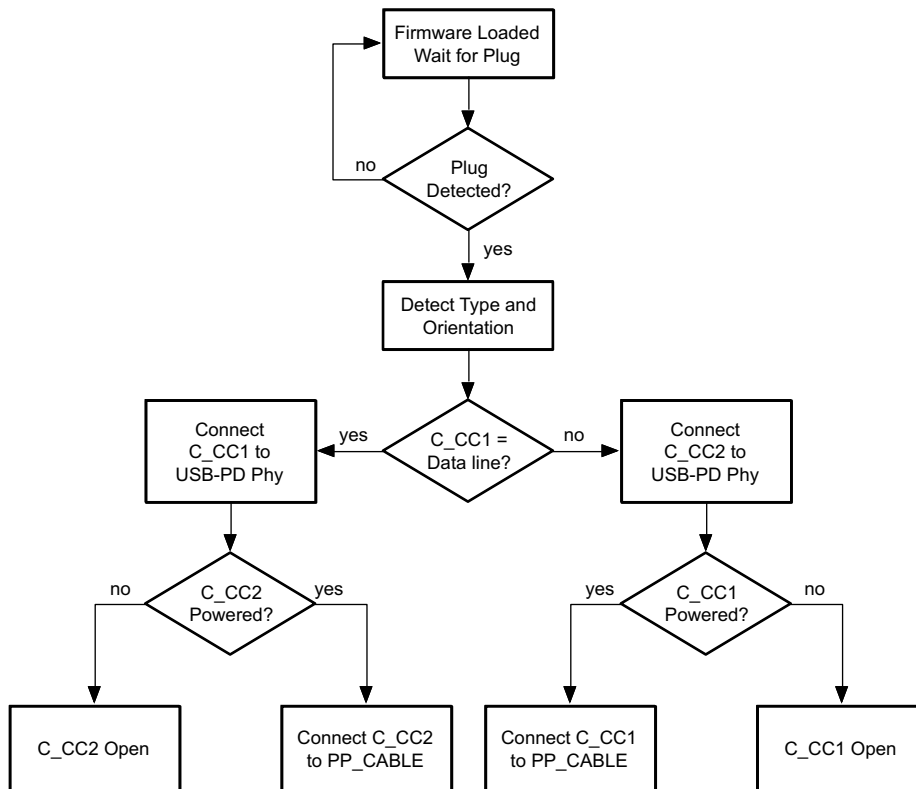


Figure 37. Port C\_CC and VCONN Connection Flow

Figure 38 and Figure 39 show the two paths from PP\_CABLE to the C\_CCn pins. When one C\_CCn pin is powered from PP\_CABLE, the other is connected to the USB-PD BMC modem. The red line shows the power path and the green line shows the data path.

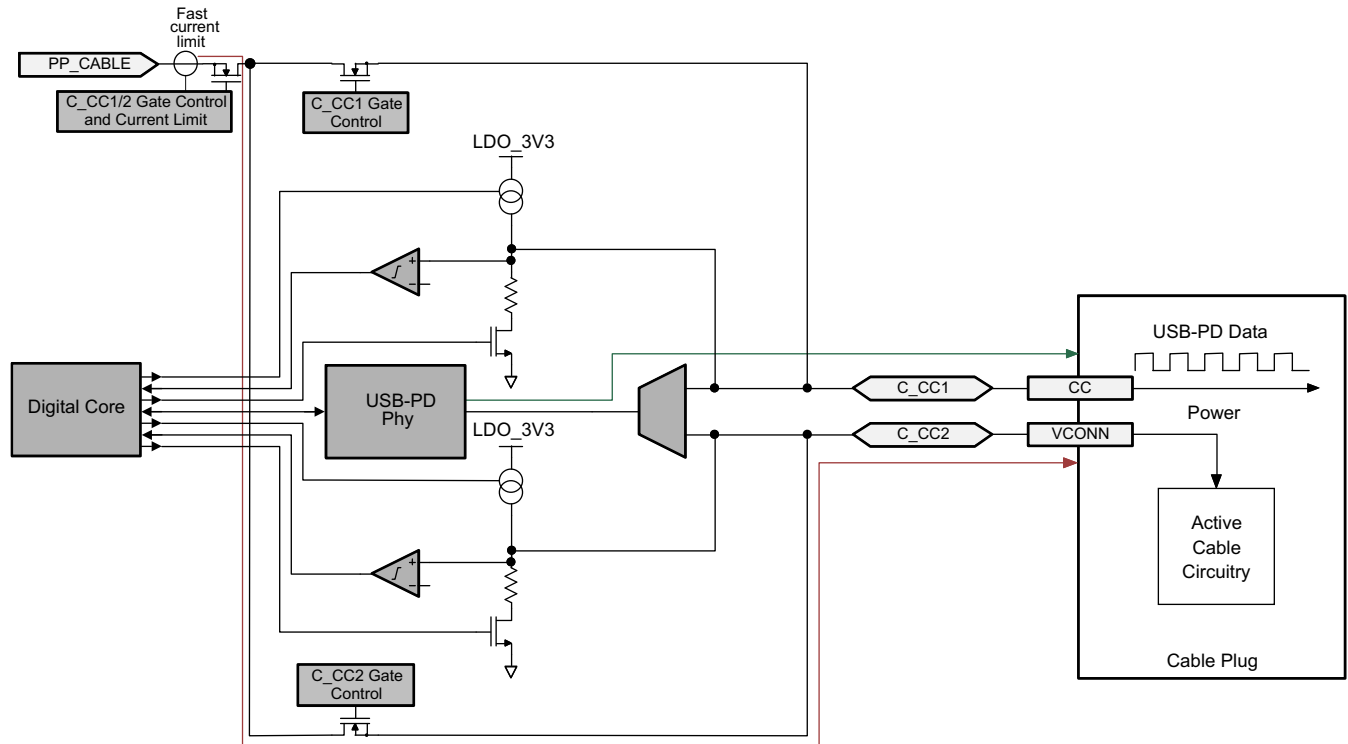


Figure 38. Port C\_CC1 and C\_CC2 Normal Orientation Power from PP\_CABLE

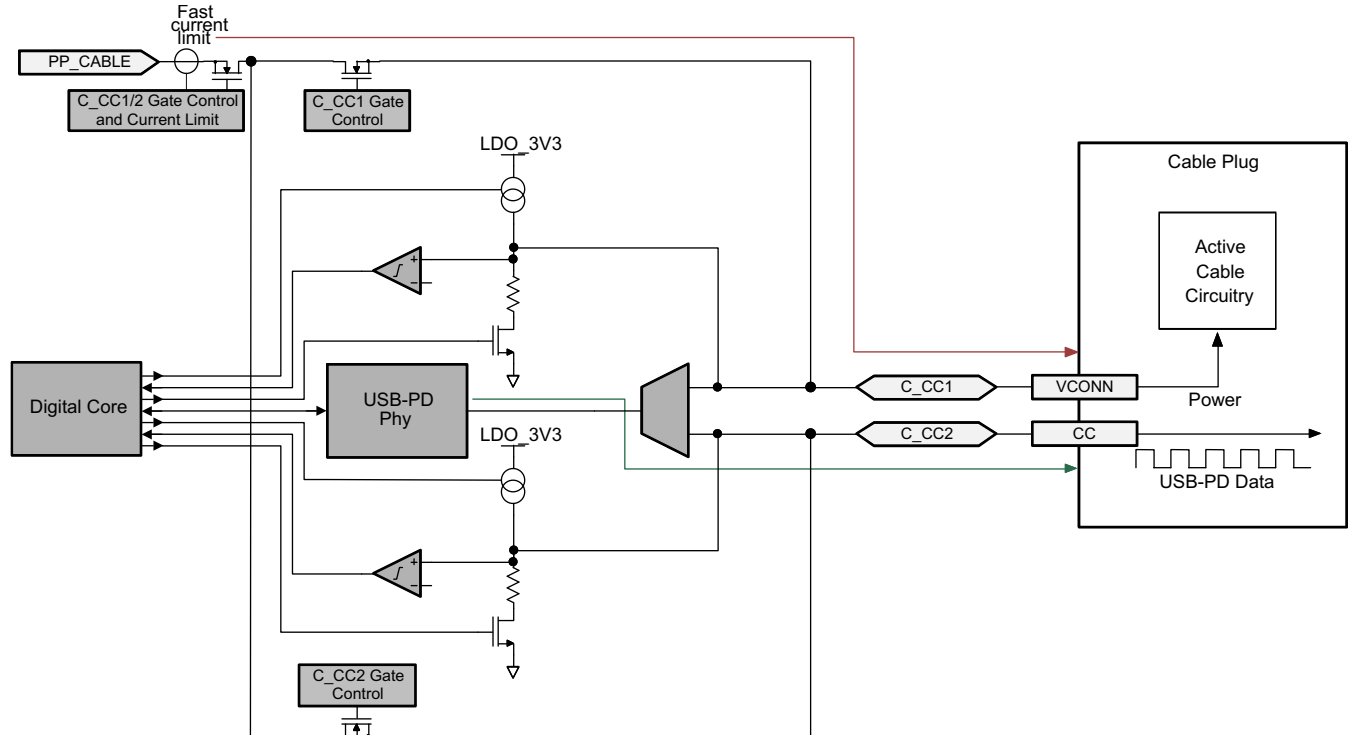


Figure 39. Port C\_CC1 and C\_CC2 Reverse Orientation Power from PP\_CABLE

### 9.3.3.22 PP\_CABLE to C\_CC1 and C\_CC2 Switch Architecture

Figure 20 shows the switch architecture for the PP\_CABLE switch path to the C\_CCc pins. Each path provides a unidirectional current from PP\_CABLE to C\_CC1 and C\_CC2. The switch structure blocks reverse current from C\_CC1 or C\_CC2 to PP\_CABLE.

### 9.3.3.23 PP\_CABLE to C\_CC1 and C\_CC2 Current Limit

The PP\_CABLE to C\_CC1 and C\_CC2 share current limiting through a single FET on the PP\_CABLE side of the switch. The current limit ILIMPPCC is adjustable between two levels. When the current exceeds ILIMPPCC, the current-limit circuit activates. Depending on the severity of the over-current condition, the transient response will react in one of two ways: Figure 40 and Figure 41 show the approximate response time and clamping characteristics of the circuit for a hard short while Figure 42 shows the approximate response time and clamping characteristics for a soft short. The switch does not have reverse current blocking when the switch is enabled and current is flowing to either C\_CC1 or C\_CC2.

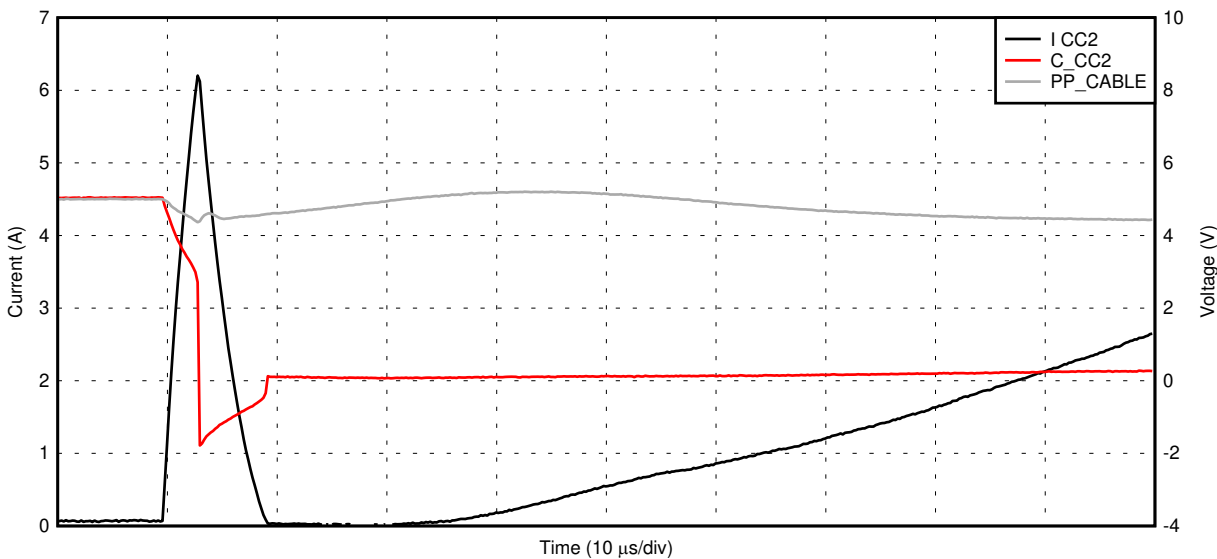


Figure 40. PP\_CABLE to C\_CCn Current Limit with a Hard Short

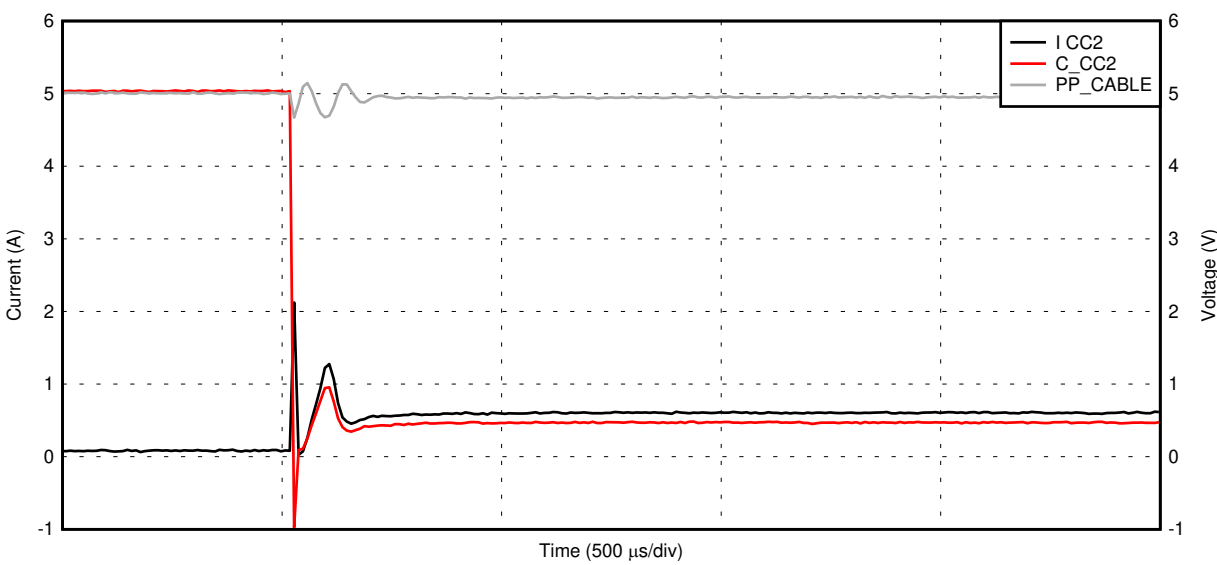


Figure 41. PP\_CABLE to C\_CCn Current Limit with a Hard Short (Extended Time Base)

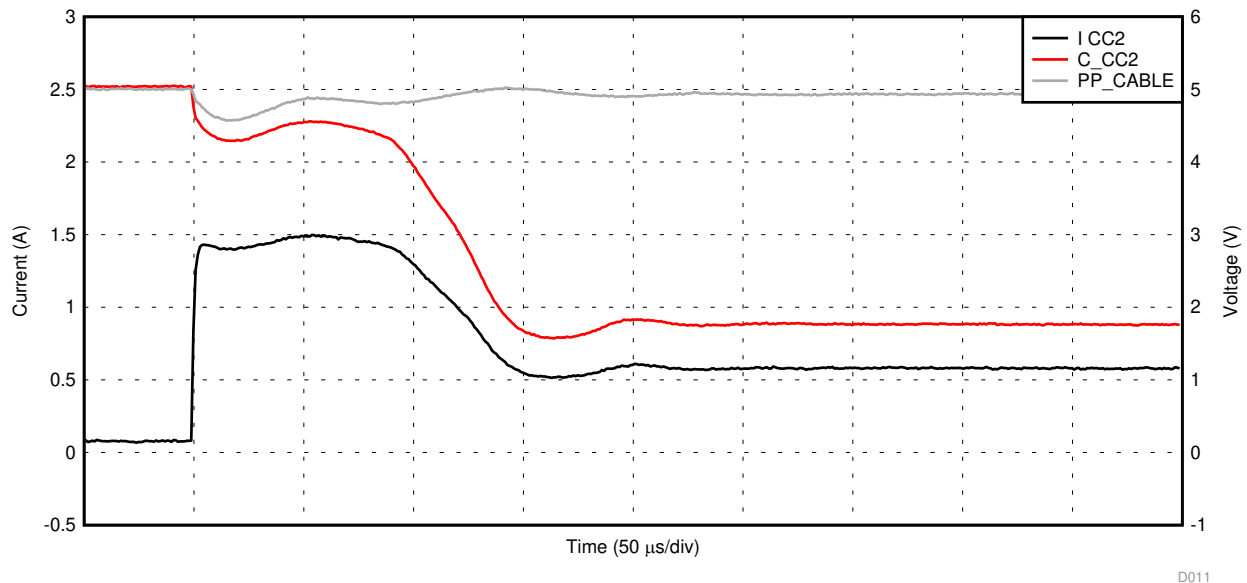


Figure 42. PP\_CABLE to C\_CCn Current Limit Response with a Soft Short (2 Ω)

### 9.3.4 USB Type-C Port Data Multiplexer

The USB Type-C receptacle pin configuration is shown in Figure 43. Not all signals shown are required for all platforms or devices. The basic functionality of the pins deliver USB 2.0 (D+ and D–) and USB 3.1 (TX and RX pairs) data buses, USB power (VBUS) and ground (GND). Configuration Channel signals (CC1 and CC2), and two Reserved for Future Use (SBU) signal pins. The data bus pins (Top and Bottom D+/D– and the SBU pins) are available to be used in non-USB applications as an Alternate Mode (i.e., DisplayPort, Thunderbolt™, etc.).

A1	A2	A3	A4	A5	A6	A7	A8	A9	A11	A11	A12
GND	TX1+	TX1–	VBUS	CC1	D+	D–	SBU1	VBUS	RX2–	RX2+	GND
GND	RX1+	RX1–	VBUS	SBU2	D–	D+	CC2	VBUS	TX2–	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 43. USB Type-C Receptacle Pin Configuration

The TPS65982 USB Type-C interface multiplexers are shown in Table 2. The outputs are determined based on detected cable orientation as well as the identified interface that is connected to the port. There are two USB output ports that may or may not be passing USB data. When an Alternate Mode is connected, these same ports may also pass that data (e.g. DisplayPort, Thunderbolt). Note, the TPS65982 pin to receptacle mapping is shown in Table 2. The high-speed RX and TX pairs are not mapped through the TPS65982 as this would place extra resistance and stubs on the high-speed lines and degrade signal performance.

Table 2. TPS65982 to USB Type-C Receptacle Mapping

DEVICE PIN	Type-C RECEPTACLE PIN
VBUS	VBUS (A4, A9, B4, B9)
C_CC1	CC1 (A5)
C_CC2	CC2 (B5)
C_USB_TP	D+ (A6)
C_USB_TN	D– (A7)
C_USB_BP	D+ (B6)
C_USB_BN	D– (B7)
C_SBU1	SBU1 (A8)
C_SBU2	SBU2 (B8)

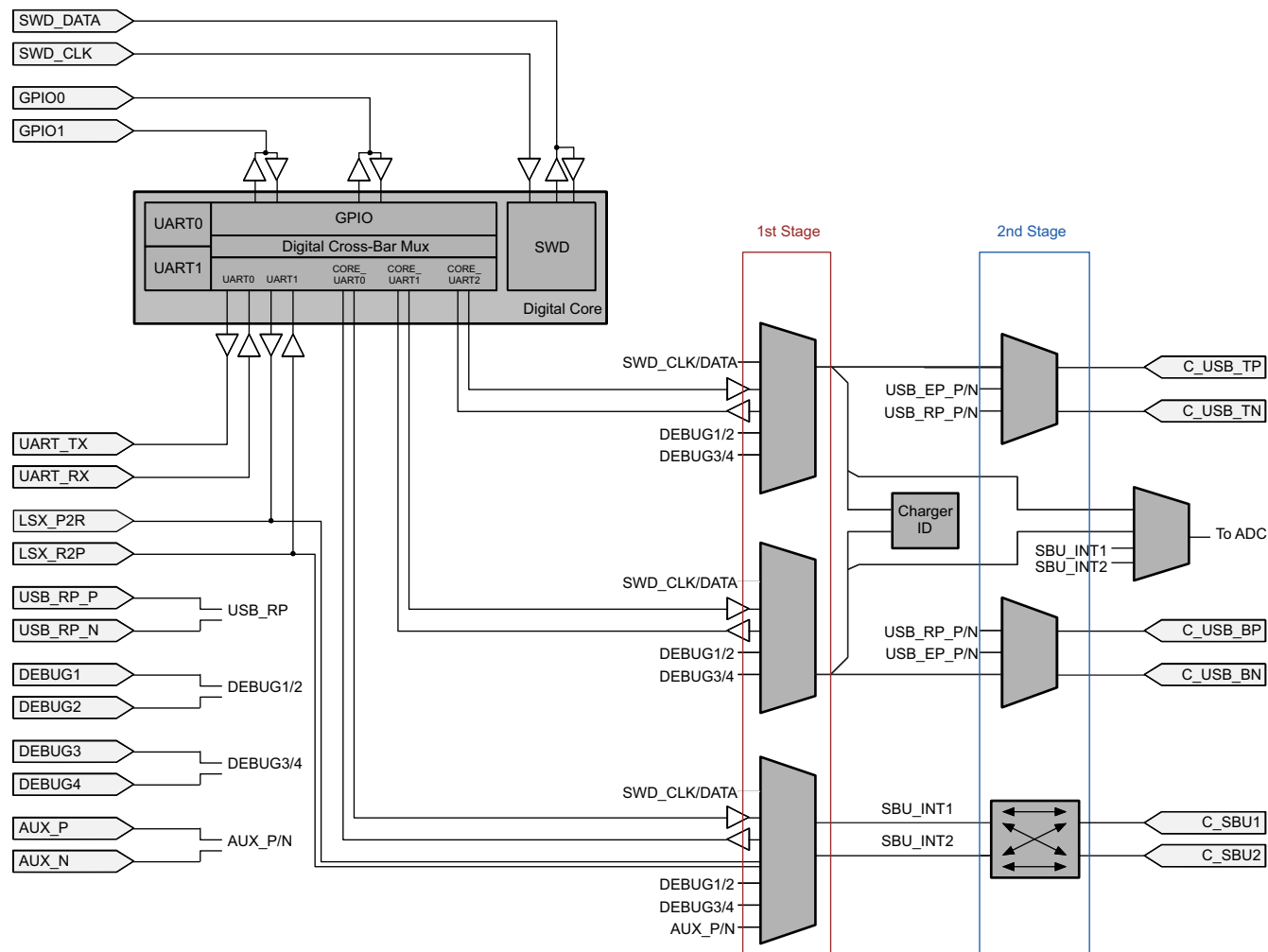


Figure 44. Port Data Multiplexers

Table 3 shows the typical signal types through the switch path. The UART\_RX/TX and LSX\_P2R/R2P paths are digitally buffered to allow tri-state control for these paths. All other switches are analog pass switches. The LSX\_P2R/R2P pair is also configurable to be analog pass switches as well. These switch paths are not limited to the specified signal type. For the signals that interface with the digital core, the maximum data rate is dictated by the clock rate at which the core is running.

Table 3. Typical Signals through Analog Switch Path

INPUT PATH	SIGNAL TYPE	SIGNAL FUNCTION
SWD_DATA/CLK	Single Ended	Data, Clock
UART_RX/TX	Single Ended TX/Rx	UART
LSX_P2R/R2P	Single Ended TX/Rx	UART
DEBUG1/2/3/4	Single Ended	Debug
AUX_P/N	Differential	DisplayPort and Thunderbolt AUX channel
USB_EP_P/N	Differential	USB 2.0 Low Speed Endpoint
USB_RP_P/N	Differential	USB 2.0 High Speed Data Root Port

### 9.3.4.1 USB Top and Bottom Ports

The Top (C\_USB\_TP and C\_USB\_TN) and Bottom (C\_USB\_BP and C\_USB\_BN) ports that correspond to the Type-C top and bottom USB D+/D– pairs are swapped based on the detected cable orientation. The symmetric pin order shown in [Figure 43](#) from the A-side to the B-side allows the pins to connect to equivalent pins on the opposite side when the cable orientation is reversed.

### 9.3.4.2 Multiplexer Connection Orientation

[Table 4](#) shows the multiplexer connection orientation. For the USB D+/D– pair top and bottom port connections, these connections are fixed. For the SBU port connections, the SBU crossbar multiplexer enables flipping of the signal pair and the connections shown are for the upside-up orientation. The CORE\_UARTn connections come from a digital crossbar multiplexer that allows the UART\_RX/TX, LSX\_P2R/R2P, and GPIO0/1 to be mapped to any of the 1<sup>st</sup> stage multiplexers.

**Table 4. Data Multiplexer Connections**

SYSTEM PIN	USB TOP PIN	USB BOTTOM PIN	SBU MULTIPLEXER PIN
USB_RP_P	C_USB_TP	C_USB_BP	
USB_RP_N	C_USB_TN	C_USB_BN	
USB_EP_P	C_USB_TP	C_USB_BP	
USB_EP_N	C_USB_TN	C_USB_BN	
SWD_CLK	C_USB_TP	C_USB_BP	SBU1
SWD_DATA	C_USB_TN	C_USB_BN	SBU2
DEBUG1	C_USB_TP	C_USB_BP	SBU1
DEBUG2	C_USB_TN	C_USB_BN	SBU2
DEBUG3	C_USB_TP	C_USB_BP	SBU1
DEBUG4	C_USB_TN	C_USB_BN	SBU2
AUX_P	C_USB_TP	C_USB_BP	SBU1
AUX_N	C_USB_TN	C_USB_BN	SBU2
LSX_R2P			SBU1
LSX_P2R			SBU2
CORE_UART0_TX	C_USB_TP		
CORE_UART0_RX	C_USB_TN		
CORE_UART1_TX		C_USB_BP	
CORE_UART1_RX		C_USB_BN	
CORE_UART2_TX			SBU1
CORE_UART2_RX			SBU2

### 9.3.4.3 Digital Crossbar Multiplexer

The TPS65982 UART paths (UART\_RX/TX and LSX\_P2R/R2P) and GPIO0/1 all have digital inputs that pass through a cross-bar multiplexer inside the digital core. Each of these pins is configurable as an input or output of the cross-bar multiplexer. The digital cross-bar multiplexer then connects to the port data multiplexers as shown in [Figure 44](#). The connections are configurable via firmware. The default state at power-up is to connect a buffered version of UART\_RX to UART\_TX providing a bypass through the TPS65982 for daisy chaining during power on reset.

### 9.3.4.4 SBU Crossbar Multiplexer

The SBU Crossbar Multiplexer provides pins (C\_SBU1 and C\_SBU2) for future USB functionality as well as Alternate Modes. The multiplexer swaps the output pair orientation based on the cable orientation. For more information on Alternate Modes, refer to the [USB PD Specification](#).

### 9.3.4.5 Signal Monitoring and Pullup/Pulldown

The TPS65982 has comparators that may be enabled to interrupt the core when a switching event occurs on any of the port inputs. The input parameters for the detection are listed in the [Port Data Multiplexer Signal Monitoring Pullup and Pulldown Characteristics](#) table. These comparators are disconnected by application code when these pins are not digital signals but an analog voltage.

The TPS65982 has pullups and pulldowns between the first and second stage multiplexers of the port switch for each port output: C\_SBU1/2, C\_USB\_TP/N, C\_USB\_BP/N. The configurable pullup and pulldown resistances between each multiplexer are shown in [Figure 45](#).

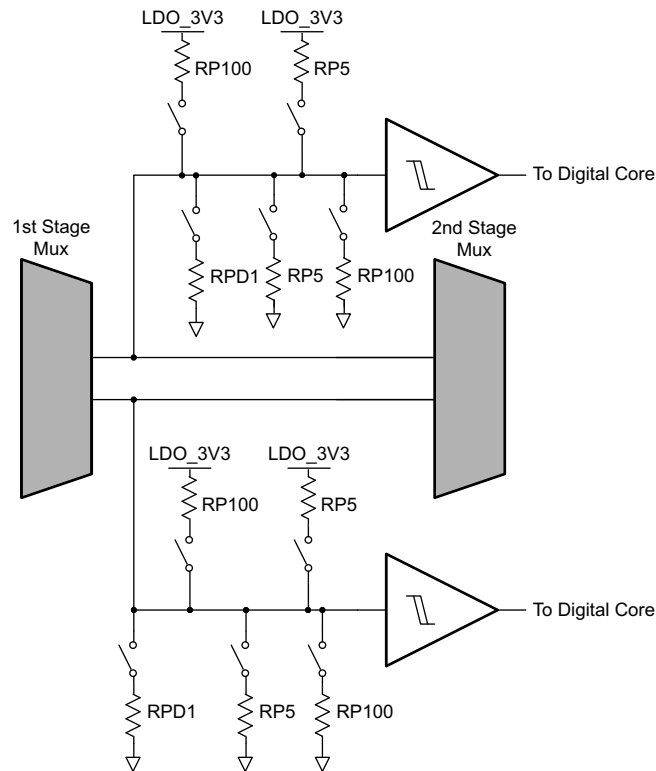


Figure 45. Port Detect and Pullup/Pulldown

### 9.3.4.6 Port Multiplexer Clamp

Each input to the 2<sup>nd</sup> stage multiplexer is clamped to prevent voltages on the port from exceeding the safe operating voltage of circuits attached to the system side of the Port Data Multiplexer. [Figure 46](#) shows the simplified clamping circuit. When a path through the 2<sup>nd</sup> stage multiplexer is closed, the clamp is connected to the one of the port pins (C\_USB\_TP/N, C\_USB\_BP/N, C\_SBU1/2). When a path through the 2<sup>nd</sup> stage multiplexer is not closed, then the port pin is not clamped. As the pin voltage rises above the VCLMP\_IND voltage, the clamping circuit activates, and sinks current to ground, preventing the voltage from rising further.

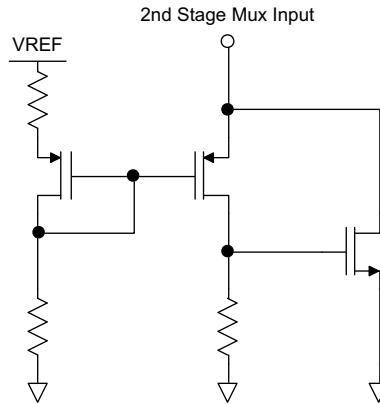


Figure 46. Port Mux Clamp

### 9.3.4.7 USB2.0 Low-Speed Endpoint

The USB low-speed Endpoint is a USB 2.0 low-speed (1.5 Mbps) interface used to support HID class based accesses. The TPS65982 supports control of endpoint EP0. This endpoint enumerates to a USB 2.0 bus to provide USB-Billboard information to a host system as defined in the USB Type-C standard. EP0 is used for advertising the Billboard Class. When a host is connected to a device that provides Alternate Modes which cannot be supported by the host, the Billboard class allows a means for the host to report back to the user without any silent failures.

Figure 47 shows the USB Endpoint physical layer. The physical layer consists of the analog transceiver, the Serial Interface Engine, and the Endpoint FIFOs and supports low speed operation.

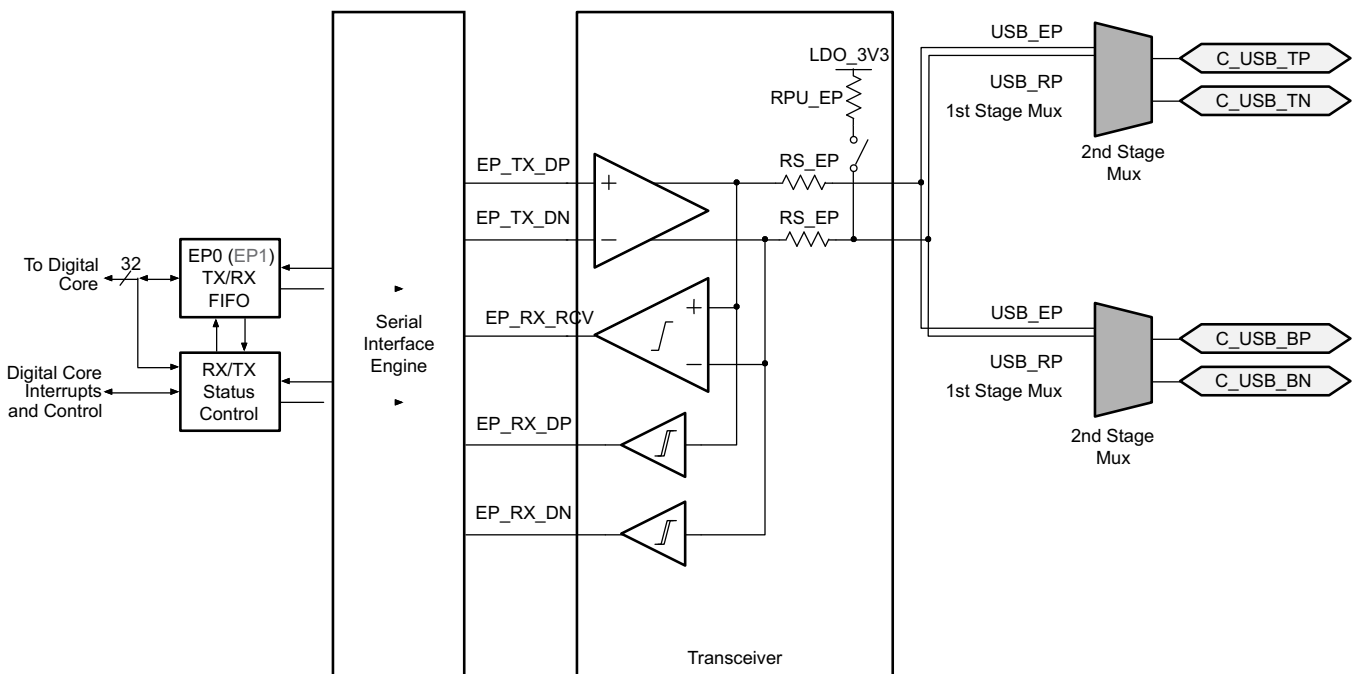


Figure 47. USB Endpoint Phy



The transceiver is made up of a fully differential output driver, a differential to single-ended receive buffer and two single-ended receive buffers on the D+/D– independently. The output driver drives the D+/D– of the selected output of the Port Multiplexer. The signals pass through the 2<sup>nd</sup> Stage Port Data Multiplexer to the port pins. When driving, the signal is driven through a source resistance RS\_EP. RS\_EP is shown as a single resistor in USB Endpoint Phy but this resistance also includes the resistance of the 2<sup>nd</sup> Stage Port Data Multiplexer defined in Port Data Multiplexer Requirements and Characteristics. RPU\_EP is disconnected during transmit mode of the transceiver.

When the endpoint is in receive mode, the resistance RPU\_EP is connected to the D– pin of the top or bottom port (C\_USB\_TN or C\_USB\_BN) depending on the detected orientation of the cable. The RPU\_EP resistance advertises low speed mode only.

### 9.3.4.8 Battery Charger (BC1.2) Detection Block

The battery charger (BC1.2) detection block integrates circuitry to detect when the connected entity on the USB D+/D– pins is a charger. To enable the required detection mechanisms, the block integrates various voltage sources, currents, and resistances to the Port Data Multiplexers. Figure 48 shows the connections of these elements to the Port Data Multiplexers.

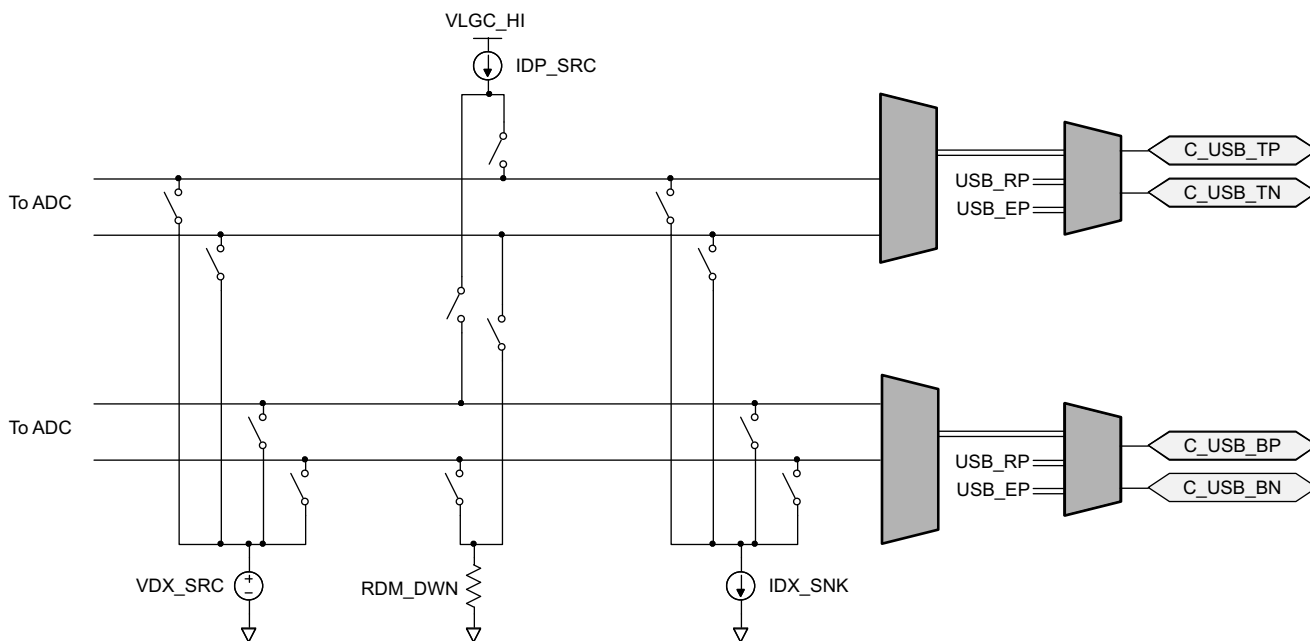


Figure 48. BC1.2 Detection Circuitry

### 9.3.4.9 BC1.2 Data Contact Detect

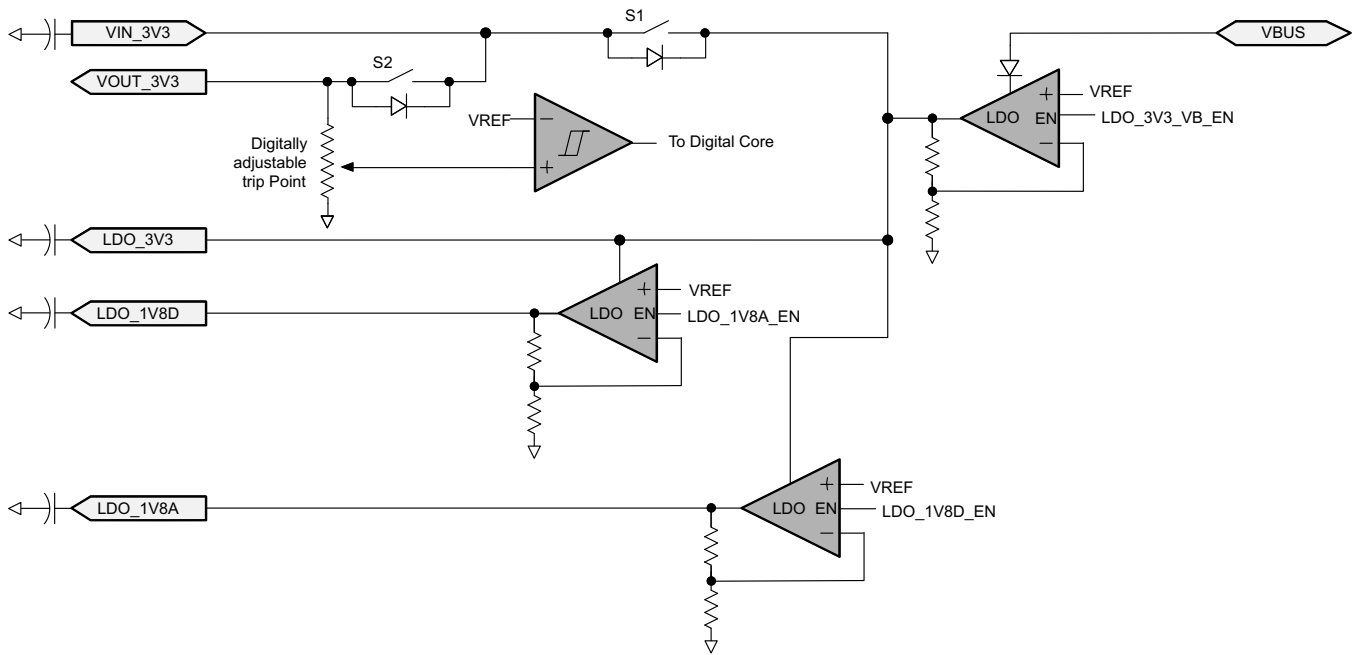
Data Contact Detect follows the definition in the USB BC1.2 specification. The detection scheme sources a current IDP\_SRC into the D+ pin of the USB connection. The current is sourced into either the C\_USB\_TP (top) or C\_USB\_BP (bottom) D+ pin based on the determined cable/device orientation. A resistance RDM\_DWN is connected between the D– pin and GND. Again, this resistance is connected to either the C\_USB\_TN (top) or C\_USB\_BN (bottom) D– pin based on the determined cable/device orientation. The middle section of Figure 48, the current source IDP\_SRC and the pull-down resistance RDM\_DWN, is activated during data contact detection.

### 9.3.4.10 BC1.2 Primary and Secondary Detection

The Primary and Secondary Detection follow the USB BC1.2 specification. This detection scheme looks for a resistance between D+ and D– lines by forcing a known voltage on the first line, forcing a current sink on the second line and then reading the voltage on the second line using the general purpose ADC integrated in the TPS65982. To provide complete flexibility, 12 independent switches are connected to allow firmware to force voltage, sink current, and read voltage on any of the C\_USB\_TP, C\_USB\_TN, C\_USB\_BP, and C\_USB\_BN. The left and right sections of Figure 48, the voltage source VDX\_SRC and the current sink IDX\_SNK, are activated during primary and secondary detection.

### 9.3.5 Power Management

The TPS65982 Power Management block receives power and generates voltages to provide power to the TPS65982 internal circuitry. These generated power rails are LDO\_3V3, LDO\_1V8A, and LDO\_1V8D. LDO\_3V3 is also a low power output to load flash memory. VOUT\_3V3 is a low power output that does not power internal circuitry that is controlled by application code and can be used to power other ICs in some applications. The power supply path is shown in [Figure 49](#).



**Figure 49. Power Supply Path**

The TPS65982 is powered from either VIN\_3V3 or VBUS. The normal power supply input is VIN\_3V3. In this mode, current flows from VIN\_3V3 to LDO\_3V3 to power the core 3.3 V circuitry and the 3.3 V I/Os. A second LDO steps the voltage down from LDO\_3V3 to LDO\_1V8D and LDO\_1V8A to power the 1.8 V core digital circuitry and 1.8 V analog circuits. When VIN\_3V3 power is unavailable and power is available on the VBUS, the TPS65982 will be powered from VBUS. In this mode, the voltage on VBUS is stepped down through an LDO to LDO\_3V3. Switch S1 in [Figure 49](#) is unidirectional and no current will flow from LDO\_3V3 to VIN\_3V3 or VOUT\_3V3. When VIN\_3V3 is unavailable, this is an indicator that there is a dead-battery or no-battery condition.

#### 9.3.5.1 Power-On and Supervisory Functions

A power-on-reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present. In addition to the POR and supervisory circuits for the internal supplies, a separate programmable voltage supervisor monitors the VOUT\_3V3 voltage.

#### 9.3.5.2 Supply Switch-Over

VIN\_3V3 takes precedence over VBUS, meaning that when both supply voltages are present the TPS65982 will power from VIN\_3V3. Refer to [The Figure 49](#) for a diagram showing the power supply path block. There are two cases in which a power supply switch-over will occur. The first is when VBUS is present first and then VIN\_3V3 becomes available. In this case, the supply will automatically switch-over to VIN\_3V3 and brown-out prevention is verified by design. The other way a supply switch-over will occur is when both supplies are present and VIN\_3V3 is removed and falls below 2.85 V. In this case, a hard reset of the TPS65982 occurs prompting a re-boot.

#### 9.3.5.3 RESETZ and MRESET

The VIN\_3V3 voltage is connected to the VOUT\_3V3 output by a single FET switch (S2 in [Figure 49](#)).

The enabling of the switch is controlled by the core digital circuitry and the conditions are programmable. A supervisor circuit monitors the voltage at VOUT\_3V3 for an undervoltage condition and sets the external indicator RESETZ. The RESETZ pin is active low (low when an undervoltage condition occurs). The RESETZ output is also asserted when the MRESET input is asserted. The MRESET input is active-high by default, but is configurable to be active low. Figure 4 shows the RESETZ timing with MRESET set to active high. When VOUT\_3V3 is disabled, a resistance of RPDOUT\_3V3 pulls down on the pin.

### 9.3.6 Digital Core

Figure 50 shows a simplified block diagram of the digital core. This diagram shows the interface between the digital and analog portions of the TPS65982.

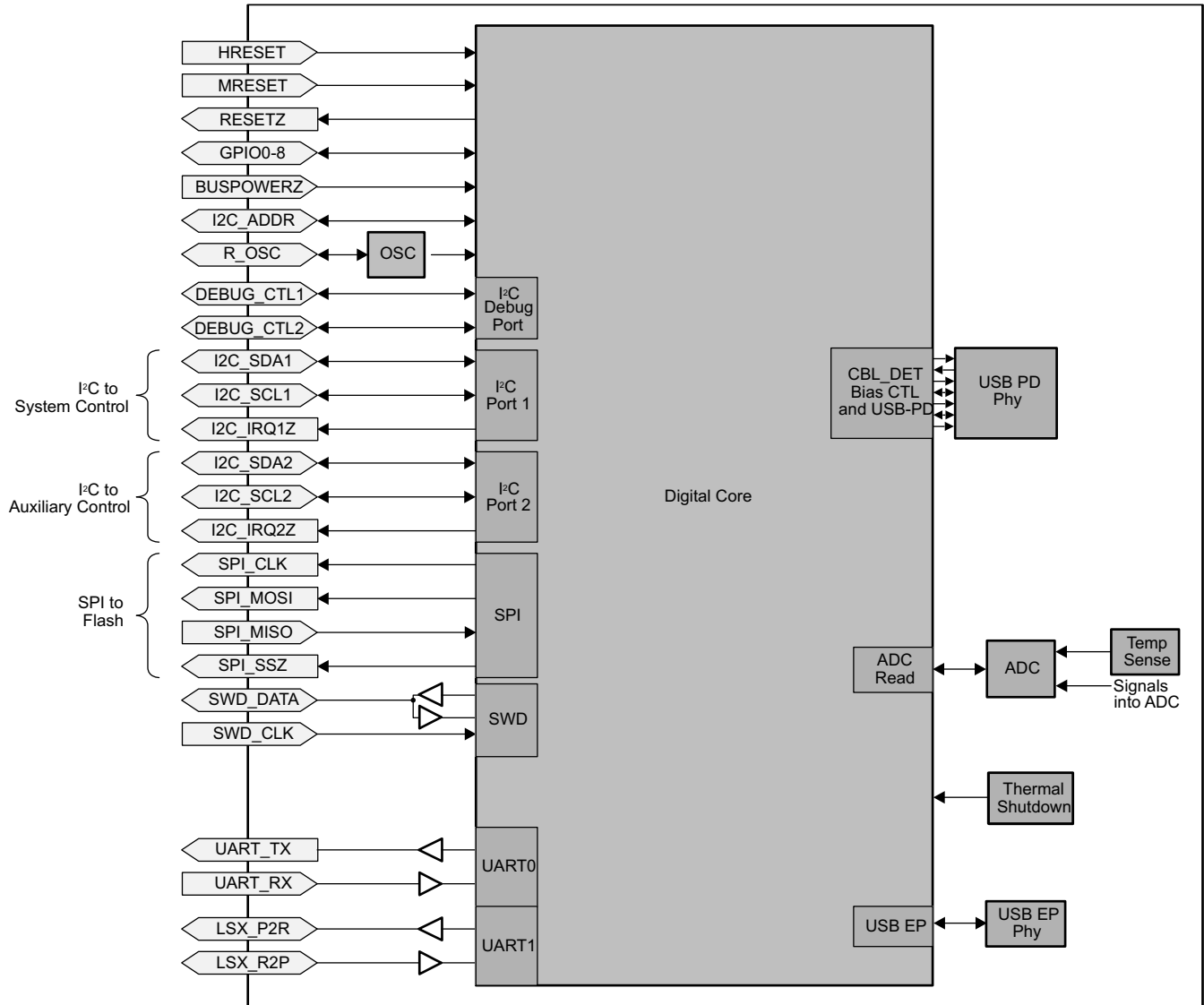


Figure 50. Digital Core Block Diagram

### 9.3.7 USB-PD BMC Modem Interface

The USB-PD BMC modem interface is a fully USB-PD compliant Type-C interface. The modem contains the BMC encoder/decoder, the TX/Rx FIFOs, the packet engine for construction/deconstruction of the USB-PD packet. This module contains programmable SOP values and processes all SOP headers.

### 9.3.8 System Glue Logic

The system glue logic module performs various system interface functions such as control of the system interface for RESETZ, MRESET, and VOUT\_3V3. This module supports various hardware timers for digital control of analog circuits.

### 9.3.9 Power Reset Congrol Module (PRCM)

The PRCM implements all clock management, reset control, and sleep mode control.

### 9.3.10 Interrupt Monitor

The Interrupt Control module handles all interrupt from the external GPIO as well as interrupts from internal analog circuits.

### 9.3.11 ADC Sense

The ADC Sense module is a digital interface to the SAR ADC. The ADC converts various voltages and currents from the analog circuits. The ADC converts up to 11 channels from analog levels to digital signals. The ADC can be programmed to convert a single sampled value.

### 9.3.12 UART

Two digital UARTS are provided for serial communication. The inputs to the UART are selectable by a programmable digital crossbar multiplexer. The UART may act as pass-through between the system and the Type-C port or may filter through the digital core. The UART\_RX/TX pins are typically used to daisy chain multiple TPS65982s in series to share application code at startup.

### 9.3.13 I<sup>2</sup>C Slave

Two I<sup>2</sup>C interfaces provide interface to the digital core from the system. These interfaces are master/slave configurable and support low-speed and full-speed signaling. See the [I<sup>2</sup>C Slave Interface](#) section for more information.

### 9.3.14 SPI Master

The SPI master provides a serial interface to an external flash memory. The recommended memory is the W25Q80DV 8 Mbit Serial Flash Memory. A memory of at least 2 Mbit is required when the TPS65982 is using the memory in an unshared manner. A memory of at least 8 Mbit is required when the TPS65982 is using the memory in a shared manner. See the [SPI Master Interface](#) section for more information.

### 9.3.15 Single-Wire Debugger Interface

The SWD interface provides a mechanism to directly master the digital core.

### 9.3.16 DisplayPort HPD Timers

To enable DisplayPort HPD signaling through PD messaging, two GPIO pins (GPIO4, GPIO5) are used as the HPD input and output. When events occur on this pins during a DisplayPort connection through the Type-C connector (configured in firmware), hardware timers trigger and interrupt the digital core to indicated needed PD messaging. [Table 5](#) shows each I/O function when GPIO4/5 are configured in HPD mode. When HPD is not enabled via firmware, both GPIO4 and GPIO5 remain generic GPIO and may be programmed for other functions. [Figure 51](#) and [Figure 52](#).

**Table 5. HPD GPIO Configuration**

HPD (Binary) Configuration	GPIO4	GPIO5
00	HPD TX	Generic GPIO
01	HPD RX	Generic GPIO
10	HPD TX	HPD RX
11	HPD TX/RX (bidirectional)	Generic GPIO

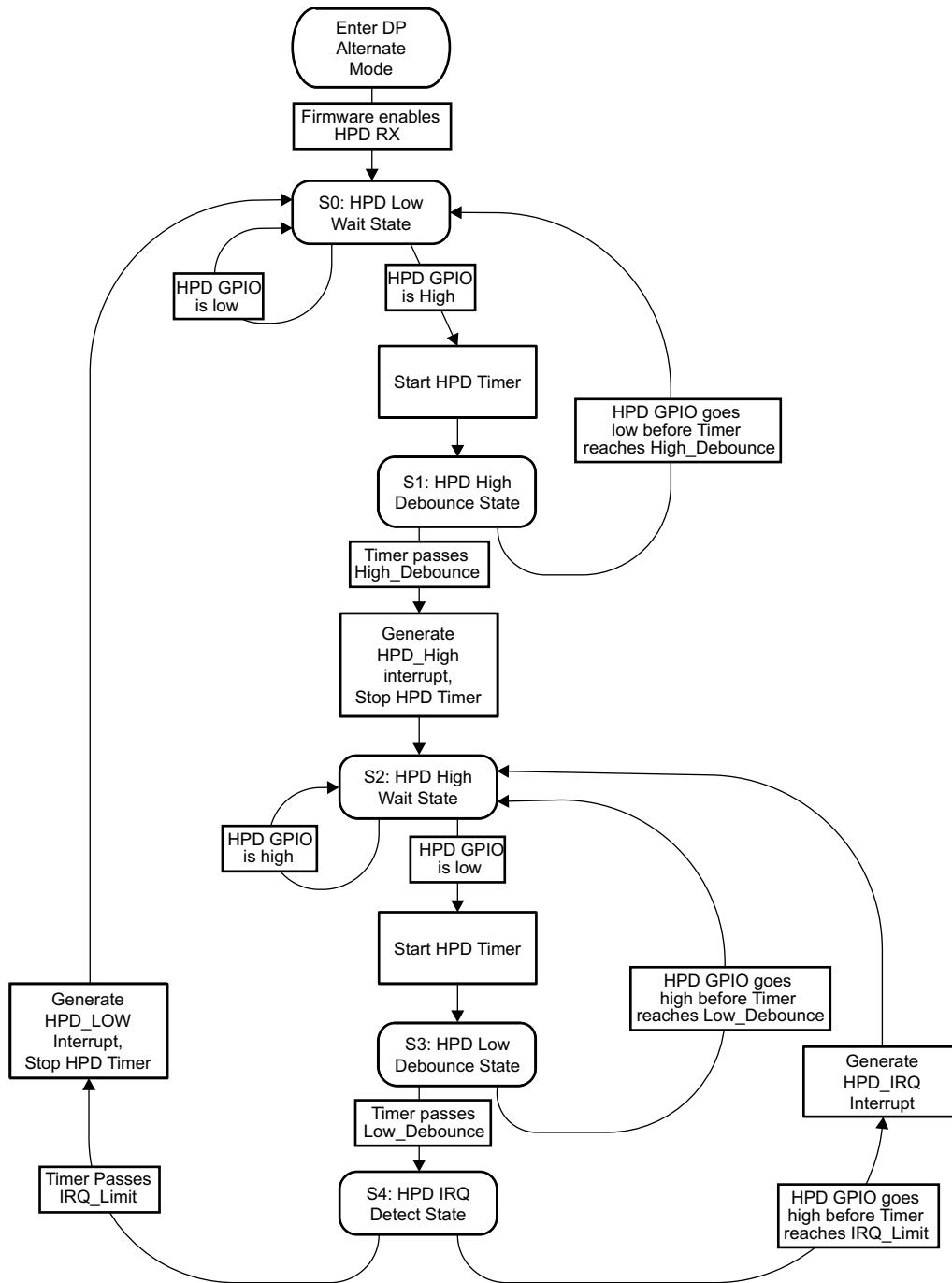


Figure 51. HPD RX Flow

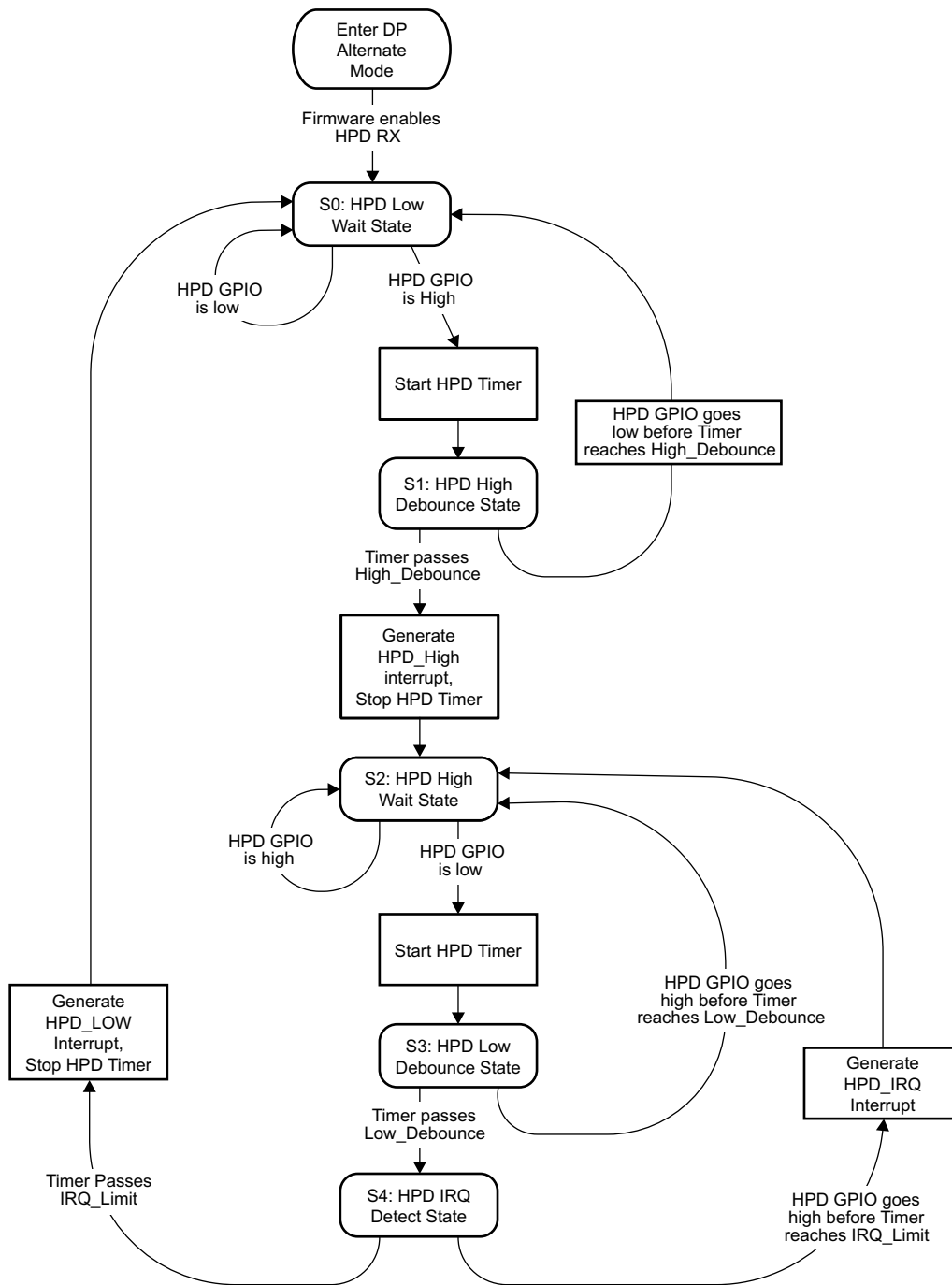


Figure 52. HPD TX Flow Diagram

### 9.3.17 ADC

The TPS65982 ADC is shown in Figure 53. The ADC is a 10-bit successive approximation ADC. The input to the ADC is an analog input multiplexer that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware. Each supply voltage into the TPS65982 is available to be converted including the port power path inputs and outputs. All GPIO, the C\_CCn pins, the charger detection voltages are also available for conversion. To read the port power path current sourced to VBUS, the high-voltage and low-voltage power paths are sensed and converted to voltages to be read by the ADC. For the external FET path, the difference in the SENSEP and SENSEN voltages is converted to detect the current (IPP\_EXT) that is sourced through this path by dividing by the RSENSE resistance.

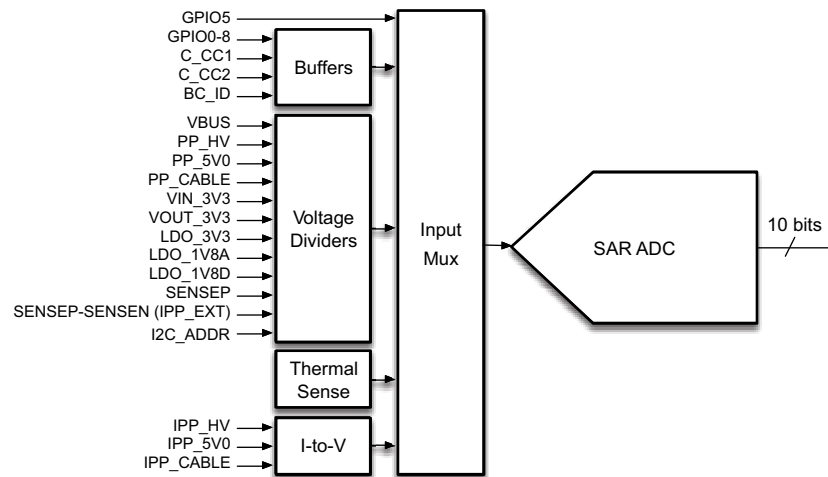


Figure 53. SAR ADC

9.3.17.1 ADC Divider Ratios

The ADC voltage inputs are each divided down to the full-scale input of 1.2 V. The ADC current sensing elements are not divided.

Table 6 shows the divider ratios for each ADC input. The table also shows which inputs are auto-sequenced in the round robin automatic readout mode. The C\_CC1 and C\_CC2 pin voltages each have two conversions values. The divide-by-5 (CCn\_BY5) conversion is intended for use when the C\_CCn pin is configured as VCONN output and the divide-by-2 (CCn\_BY2) conversion is intended for use when C\_CCn pin is configured as the CC data pin.

Table 6. ADC Divider Ratios

CHANNEL #	SIGNAL	TYPE	AUTO-SEQUENCED	DIVIDER RATIO	BUFFERED
0	Thermal Sense	Temperature	Yes	N/A	No
1	VBUS	Voltage	Yes	25	No
2	SENSEP	Voltage	Yes	25	No
3	IPP_EXT	Current	Yes	N/A	No
4	PP_HV	Voltage	Yes	25	No
5	IPP_HV	Current	Yes	N/A	No
6	PP_5V0	Voltage	Yes	5	No
7	IPP_5V0	Current	Yes	N/A	No
8	CC1_BY5	Voltage	Yes	5	Yes
9	IPP_CABLE	Current	Yes	N/A	No
10	CC2_BY5	Voltage	Yes	5	Yes
11	GPIO5	Voltage	No	1	No
12	CC1_BY2	Voltage	No	2	Yes
13	CC2_BY2	Voltage	No	2	Yes
14	PP_CABLE	Voltage	No	5	No
15	VIN_3V3	Voltage	No	3	No
16	VOUT_3V3	Voltage	No	3	No
17	BC_ID	Voltage	No	3	Yes
18	LDO_1V8A	Voltage	No	2	No
19	LDO_1V8D	Voltage	No	2	No
20	LDO_3V3	Voltage	No	3	No
21	I2C_ADDR	Voltage	No	3	Yes

**Table 6. ADC Divider Ratios (continued)**

CHANNEL #	SIGNAL	TYPE	AUTO-SEQUENCED	DIVIDER RATIO	BUFFERED
22	GPIO0	Voltage	No	3	Yes
23	GPIO1	Voltage	No	3	Yes
24	GPIO2	Voltage	No	3	Yes
25	GPIO3	Voltage	No	3	Yes
26	GPIO4	Voltage	No	3	Yes
27	GPIO5	Voltage	No	3	Yes
28	GPIO6	Voltage	No	3	Yes
29	GPIO7	Voltage	No	3	Yes
30	GPIO8	Voltage	No	3	Yes
31	BUSPOWERZ	Voltage	No	3	Yes

### 9.3.17.2 ADC Operating Modes

The ADC is configured into one of three modes: single channel readout, round robin automatic readout and one time automatic readout.

#### 9.3.17.3 Single Channel Readout

In Single Channel Readout mode, the ADC reads a single channel only. Once the channel is selected by firmware, a conversion takes place followed by an interrupt back to the digital core. Figure 5 shows the timing diagram for a conversion starting with an ADC enable. When the ADC is disabled and then enabled, there is an enable time  $T_{ADC\_EN}$  (programmable) before sampling occurs. Sampling of the input signal then occurs for time  $T_{SAMPLE}$  (programmable) and the conversion process takes time  $T_{CONVERT}$  (12 clock cycles). After time  $T_{CONVERT}$ , the output data is available for read and an Interrupt is sent to the digital core for time  $T_{INTA}$  (2 clock cycles).

In Single Channel Readout mode, the ADC can be configured to continuously convert that channel. Figure 6 shows the ADC repeated conversion process. In this case, once the interrupt time has passed after a conversion, a new sample and conversion occurs.

#### 9.3.17.4 Round Robin Automatic Readout

When this mode is enabled, the ADC state machine will read from channel 0 to channel 11 and place the converted data into registers. The host interface can request to read from the registers at any time. During Round Robin Automatic Readout, the channel averaging must be set to 1 sample.

When the TPS65982 is running a Round Robin Readout, it will take approximately 696  $\mu$ s (11 channels  $\times$  63.33  $\mu$ s conversion) to fully convert all channels. Since the conversion is continuous, when a channel is converted, it will overwrite the previous result. Therefore, when all channels are read, any given value may be 649  $\mu$ s out of sync with any other value.

#### 9.3.17.5 One Time Automatic Readout

The One Time Automatic Readout mode is identical to the Round Robin Automatic Readout except the conversion process halts after the final channel is converted. Once all 11 channels are converted, an interrupt occurs to the digital core.

### 9.3.18 I/O Buffers

Table 7 lists the I/O buffer types and descriptions. Table 8 lists the pin to I/O buffer mapping for cross-referencing a pin's particular I/O structure. The following sections show a simplified version of the architecture of each I/O buffer type.

**Table 7. I/O Buffer Type Description**

BUFFER TYPE	DESCRIPTION
IOBUF_GPIOHSSWD	General Purpose High-Speed I/O
IOBUF_GPIOHSSPI	General Purpose High-Speed I/O



**Table 7. I/O Buffer Type Description (continued)**

BUFFER TYPE	DESCRIPTION
IOBUF_GPIOLS	General Purpose Low-Speed I/O
IOBUF_GPIOLSI2C	General Purpose Low-Speed I/O with I <sup>2</sup> C deglitch time
IOBUF_I2C	I <sup>2</sup> C Compliant Clock/Data Buffers
IOBUF_OD	Open-Drain Output
IOBUF_UTX	Push-Pull output buffer for UART
IOBUF_URX	Input buffer for UART
IOBUF_PORT	Input buffer between 1st/2nd stage Port Data Mux

**Table 8. Pin to I/O Buffer Mapping**

I/O GROUP/PIN	BUFFER TYPE	SUPPLY CONNECTION (DEFAULT FIRST)
DEBUG1/2/3/4	IOBUF_GPIOLS	LDO_3V3, VDDIO
DEBUG_CTL1/2	IOBUF_GPIOLSI2C	LDO_3V3, VDDIO
BUSPOWERZ	IOBUF_GPIOLS	LDO_3V3, VDDIO
GPIO0-8	IOBUF_GPIOLS	LDO_3V3, VDDIO
I2C_IRQ1/2Z	IOBUF_OD	LDO_3V3, VDDIO
I2C_SDA1/2/SCL/1/2	IOBUF_I2C	LDO_3V3, VDDIO
LSX_P2R	IOBUF_UTX	LDO_3V3, VDDIO
LSX_R2P	IOBUF_URX	LDO_3V3, VDDIO
MRESET	IOBUF_GPIOLS	LDO_3V3, VDDIO
RESETZ	IOBUF_GPIOLS	LDO_3V3, VDDIO
UART_RX	IOBUF_URX	LDO_3V3, VDDIO
UART_TX	IOBUF_UTX	LDO_3V3, VDDIO
PORT_INT	IOBUF_PORT	LDO_3V3
SPI_MOSI/MISO/CLK/SSZ	IOBUF_GPIOHSSPI	LDO_3V3
SWD_CLK/DATA	IOBUF_GPIOHSSWD	LDO_3V3

### 9.3.18.1 IOBUF\_GPIOLS and IOBUF\_GPIOLSI2C

Figure 54 shows the GPIO I/O buffer for all GPIO pins listed GPIO0-GPIO17 in . GPIO pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a deglitched digital input or an analog input to the ADC. The push-pull output is a simple CMOS output with independent pulldown control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO\_RPU resistance in series with the drain. The supply voltage to this buffer is configurable to be LDO\_3V3 by default or VDDIO. For simplicity, the connection to VDDIO is not shown in Figure 54, but the connection to VDDIO is fail-safe and a diode will not be present from GPIO pin to VDDIO in this configuration. The pullup and pulldown output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

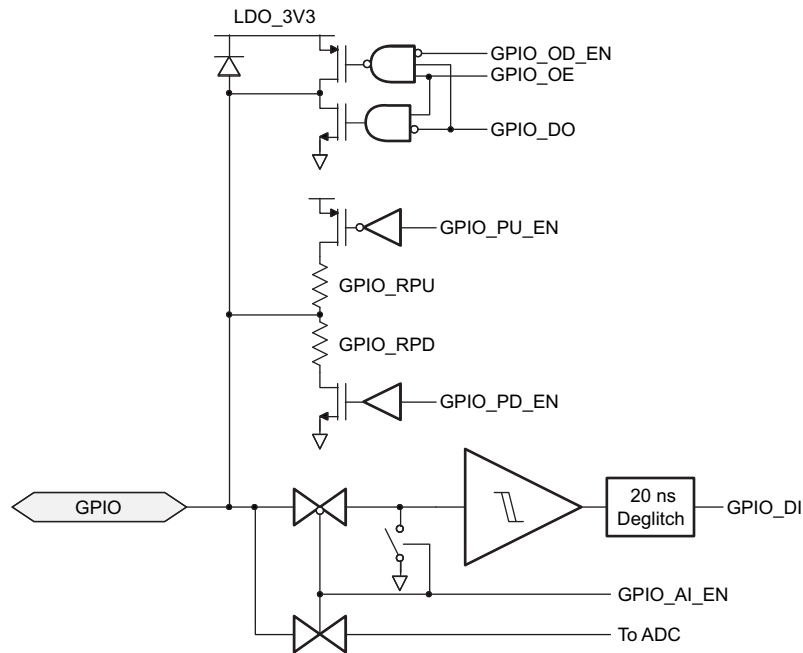


Figure 54. IOBUF\_GPIOLS (General GPIO) I/O

Figure 55 shows the IOBUF\_GPIOLS12C that is identical to IOBUF\_GPIOLS with an extended deglitch time.

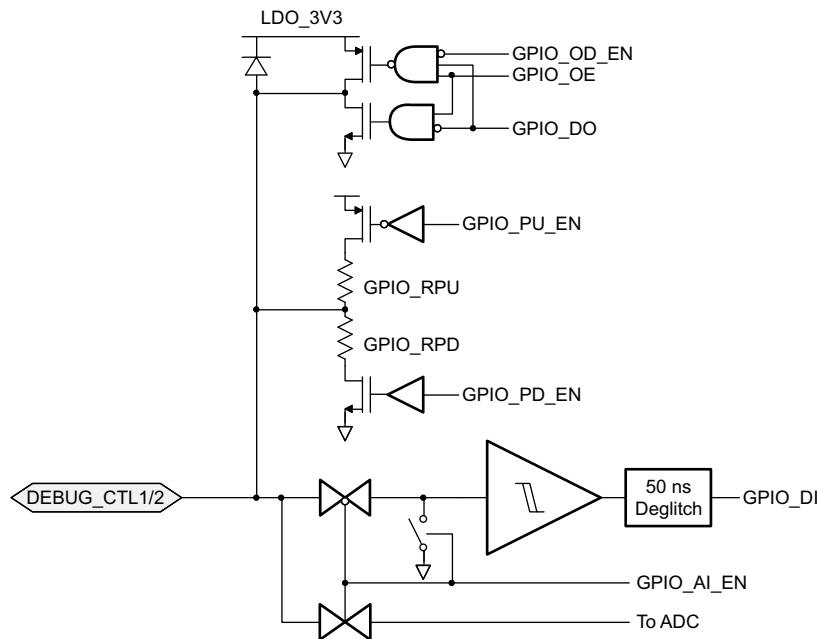


Figure 55. IOBUF\_GPIOLS12C (General GPIO) I/O with I<sup>2</sup>C De-glitch

### 9.3.18.2 IOBUF\_OD

The open-drain output driver is shown in Figure 56 and is the same push-pull CMOS output driver as the GPIO buffer. The output has independent pulldown control allowing open-drain connections.

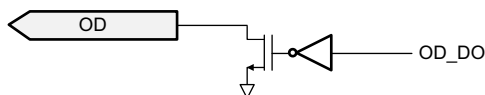


Figure 56. IOBUF\_OD Output Buffer

### 9.3.18.3 IOBUF\_UTX

The push-pull output driver is shown in Figure 57. The output buffer has a UARTTX\_RO source resistance. The supply voltage to the system side buffer is configurable to be LDO\_3V3 by default or VDDIO. This is not shown in Figure 57. The supply voltage to the port side buffers remains LDO\_3V3.

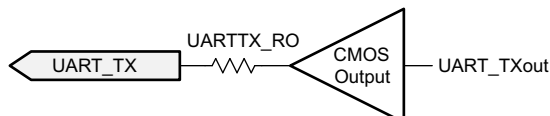


Figure 57. IOBUF\_UTX Output Buffer

### 9.3.18.4 IOBUF\_URX

The input buffer is shown in Figure 58. The supply voltage to the system side buffer is configurable to be LDO\_3V3 by default or VDDIO. This is not shown in Figure 58. The supply voltage to the port side buffers remains LDO\_3V3.

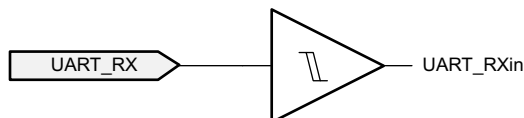


Figure 58. IOBUF\_URX Input

### 9.3.18.5 IOBUF\_PORT

The input buffer is shown in Figure 59. This input buffer is connected to the intermediate nodes between the 1<sup>st</sup> stage switch and the 2<sup>nd</sup> stage switch for each port output (C\_SBU1/2, C\_USB\_TP/N, C\_USB\_BN/P). The input buffer is enabled via firmware when monitoring digital signals and disabled when an analog signal is desired. See the Figure 45 section for more detail on the pullup and pulldown resistors of the intermediate node.

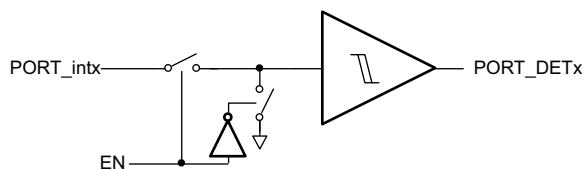


Figure 59. IOBUF\_PORT Input Buffer

### 9.3.18.6 IOBUF\_I2C

The I<sup>2</sup>C I/O driver is shown in Figure 60. This I/O consists of an open-drain output and an input comparator with deglitching. The supply voltage to this buffer is configurable to be LDO\_3V3 by default or VDDIO. This is not shown in Figure 60. Parameters for the I<sup>2</sup>C clock and data I/Os are found in [I<sup>2</sup>C Slave Characteristics](#).

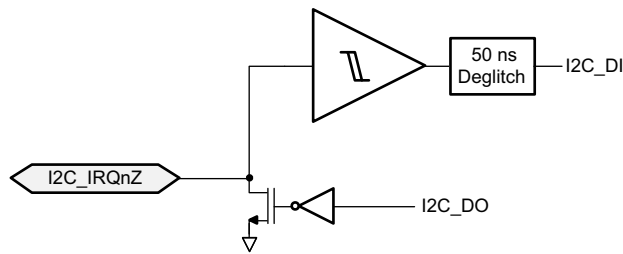


Figure 60. IOBUF\_I2C I/O

### 9.3.18.7 IOBUF\_GPIOHSPI

Figure 61 shows the I/O buffers for the SPI interface.

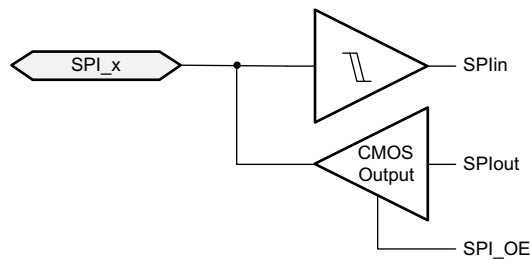


Figure 61. IOBUF\_GPIOHSSPI

### 9.3.18.8 IOBUF\_GPIOHSSWD

Figure 62 shows the I/O buffers for the SWD interface. The CLK input path is a comparator with a pullup SWD\_RPU on the pin. The data I/O consists of an identical input structure as the CLK input but with a tri-state CMOS output driver.

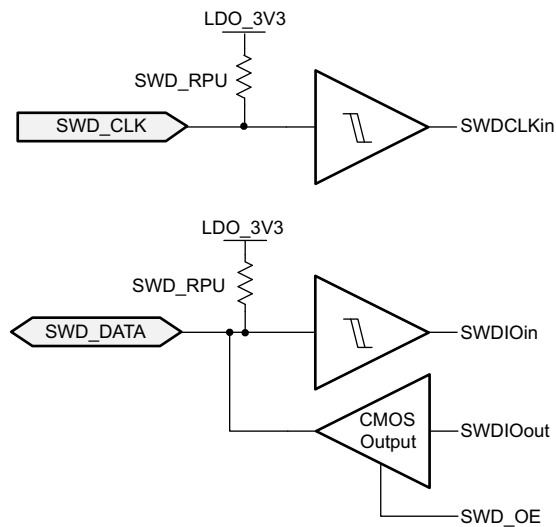


Figure 62. IOBUF\_GPIOHSSWD

### 9.3.19 Thermal Shutdown

The TPS65982 has both a central thermal shutdown to the chip and a local thermal shutdown for the power path block. The central thermal shutdown monitors the temperature of the center of the die and disables all functions except for supervisory circuitry and halts digital core when die temperature goes above a rising temperature of TSD\_MAIN. The temperature shutdown has a hysteresis of TSDH\_MAIN and when the temperature falls back below this value, the device resumes normal operation. The power path block has a local thermal shutdown circuit to detect an overtemperature condition because of overcurrent and quickly turn off the power switches. The power path thermal shutdown values are TSD\_PWR and TSDH\_PWR. The output of the thermal shutdown circuit is deglitched by TSD\_DG before triggering. The thermal shutdown circuits interrupt to the digital core.

### 9.3.20 Oscillators

The TPS65982 has two independent oscillators for generating internal clock domains. A 48-MHz oscillator generates clocks for the core during normal operation and clocks for the USB 2.0 endpoint physical layer. An external resistance is placed on the R\_OSC pin to set the oscillator accuracy. A 100-kHz oscillator generates clocks for various timers and clocking the core during low-power states.

## 9.4 Device Functional Modes

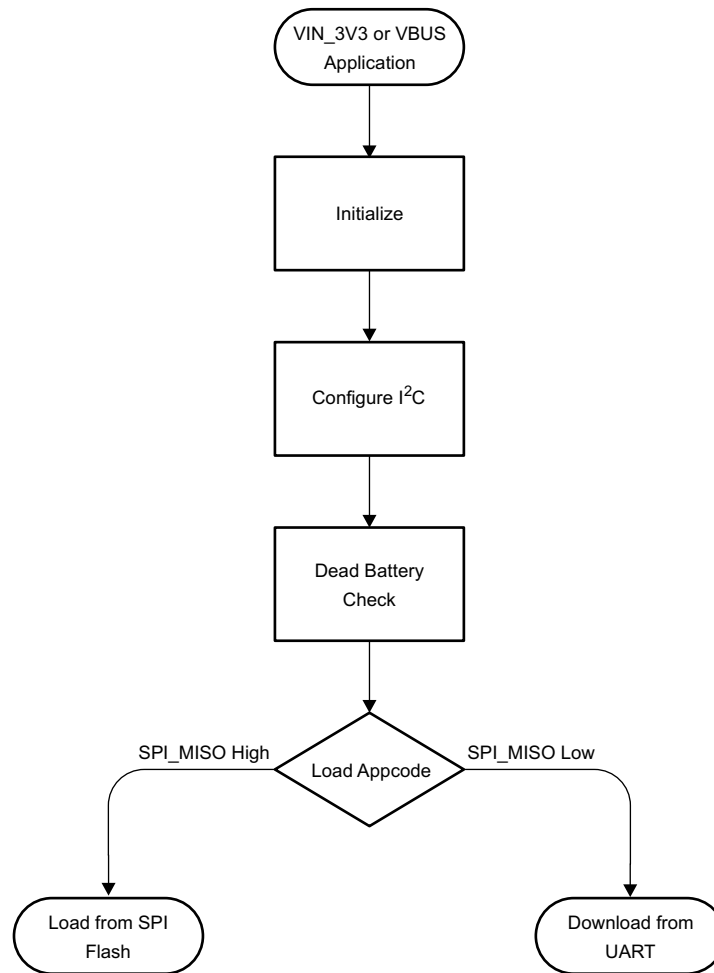
### 9.4.1 Boot Code

The TPS65982 has a Power-on-Reset (POR) circuit that monitors LDO\_3V3 and issues an internal reset signal. The digital core, memory banks, and peripherals receive clock and RESET interrupt is issued to the digital core and the boot code starts executing. [Figure 63](#) provides the TPS65982 boot code sequence.

The TPS65982 boot code is loaded from OTP on POR, and begins initializing TPS65982 settings. This initialization includes enabling and resetting internal registers, loading trim values, waiting for the trim values to settle, and configuring the device I<sup>2</sup>C addresses.

The unique I<sup>2</sup>C address is based on the customer programmable OTP, DEBUG\_CTLX pins, and resistor configuration on the I2C\_ADDR pin.

Once initial device configuration is complete the boot code determines if the TPS65982 is booting under dead battery condition (VIN\_3V3 invalid, VBUS valid). If the boot code determines the TPS65982 is booting under dead battery condition, the BUSPOWERZ pin is sampled to determine the appropriate path for routing VBUS power to the system.

**Device Functional Modes (continued)**


**Figure 63. Flow Diagram for Boot Code Sequence**

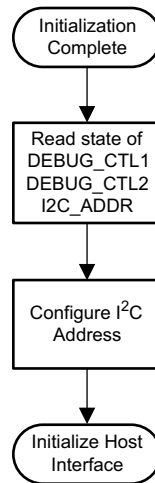
**9.4.2 Initialization**

During initialization the TPS65982 enables device internal hardware and loads default configurations. The 48-MHz clock is enabled and the TPS65982 persistence counters begin monitoring VBUS and VIN\_3V3. These counters ensure the supply powering the TPS65982 is stable before continuing the initialization process. The initialization concludes by enabling the thermal monitoring blocks and thermal shutdown protection, along with the ADC, CRC, GPIO and NVIC blocks.

**9.4.3 I<sup>2</sup>C Configuration**

The TPS65982 features dual I<sup>2</sup>C busses with configurable addresses. The I<sup>2</sup>C addresses are determined according to the flow depicted in [Figure 64](#). The address is configured by reading device GPIO states at boot (refer to the [I<sup>2</sup>C Pin Address Setting](#) section for details). Once the I<sup>2</sup>C addresses are established the TPS65982 enables a limited host interface to allow for communication with the device during the boot process.

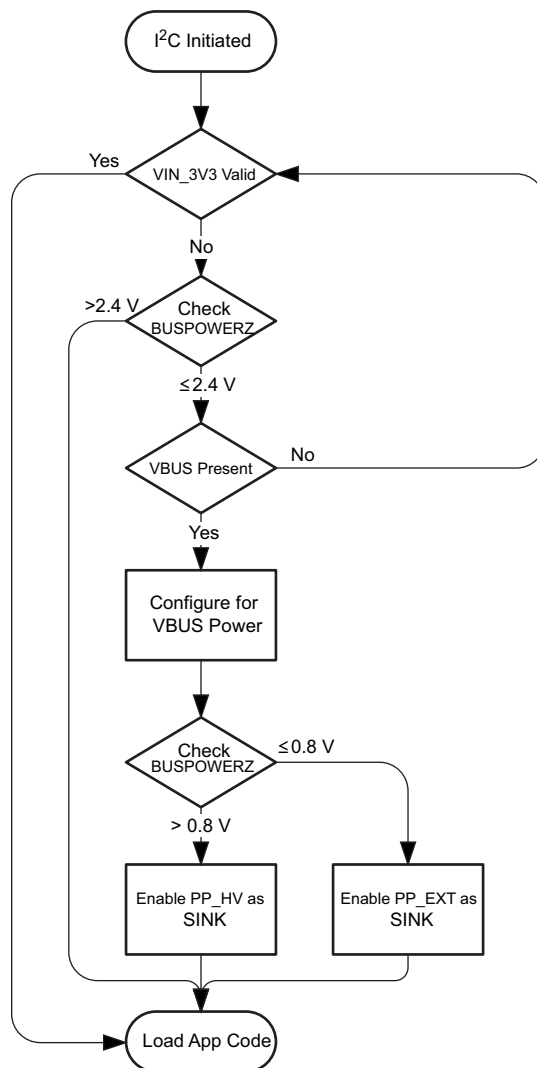
## Device Functional Modes (continued)



**Figure 64. I<sup>2</sup>C Address Configuration**

### 9.4.4 Dead-Battery Condition

After I<sup>2</sup>C configuration concludes the TPS65982 checks VIN\_3V3 to determine the cause of device boot. If the device is booting from a source other than VIN\_3V3, the dead battery flow is followed to allow for the rest of the system to receive power. The state of the BUSPOWERZ pin is read to determine power path configuration for dead battery operation. After the power path is configured, the TPS65982 will continue through the boot process. [Figure 65](#) shows the full dead battery process.

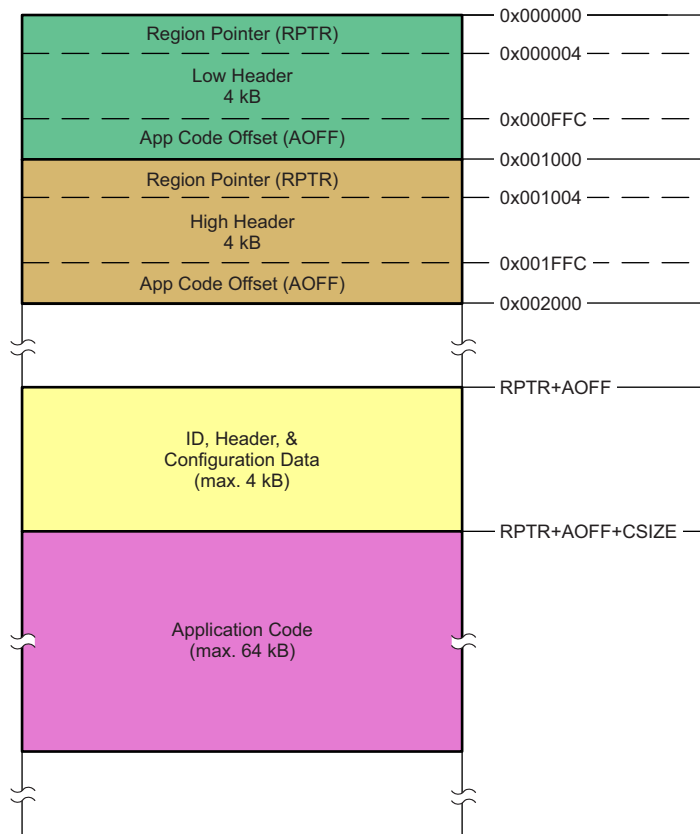
**Device Functional Modes (continued)**

**Figure 65. Dead-Battery Condition Flow Diagram**
**9.4.5 Application Code**

The TPS65982 application code is stored in an external flash memory. The flash memory used for storing the TPS65982 application code may be shared with other devices in the system. The flash memory organization shown in [Figure 66](#) supports the sharing of the flash as well as the TPS65982 using the flash without sharing.

The flash is divided into two separate regions, the Low Region and the High Region. The size of this region is flexible and only depends on the size of the flash memory used. The two regions are used to allow updating the application code in the memory without over-writing the previous code. This ensures that the new updated code is valid before switching to the new code. For example, if a power loss occurred while writing new code, the original code is still in place and used at the next boot.



## Device Functional Modes (continued)



**Figure 66. Flash Memory Organization**

There are two 4 kB header blocks starting at address 0x000000h. The Low Header 4 kB block is at address 0x000000h and the High Header 4 kB block is at 0x001000h. Each header contains a Region Pointer (RPTR) that holds the address of the physical location in memory where the low region application code resides. Each also contains an Application Code Offset (AOFF) that contains the physical offset inside the region where the TPS65982 application code resides. The TPS65982 firmware physical location in memory is  $RPTR + AOFF$ . The first sections of the TPS65982 application code contain device configuration settings where CSIZE is maximum of 4 kB. This configuration determines the devices default behavior after power-up and can be customized using the TPS65982 Configuration Tool. These pointers may be valid or invalid. The Flash Read flow handles reading and determining whether a region is valid and contains good application code.

### 9.4.6 Flash Memory Read

The TPS65982 first attempts to load application code from the low region of the attached flash memory. If any part of the read process yields invalid data, the TPS65982 will abort the low region read and attempt to read from the high region. If both regions contain invalid data the device carries out the Invalid Memory flow. [Figure 67](#) shows the flash memory read flow.

Device Functional Modes (continued)

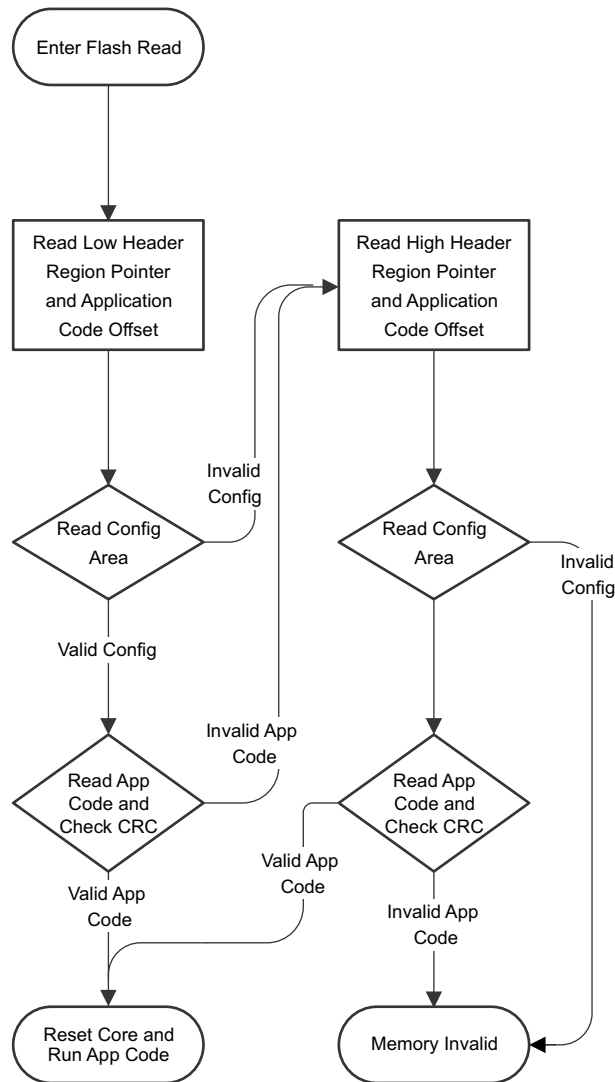


Figure 67. Flash Read Flow

9.4.7 Invalid Flash Memory

If the flash memory read fails because of invalid data, the TPS65982 carries out the memory invalid flow and presents the SWD interface on the USB Type-C SBU pins.

Figure 68 shows the invalid memory process.

Device Functional Modes (continued)

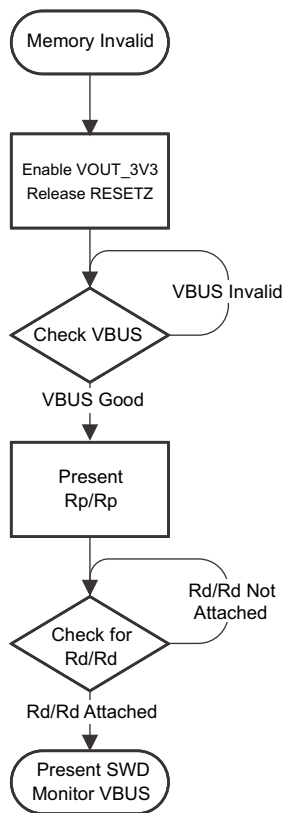
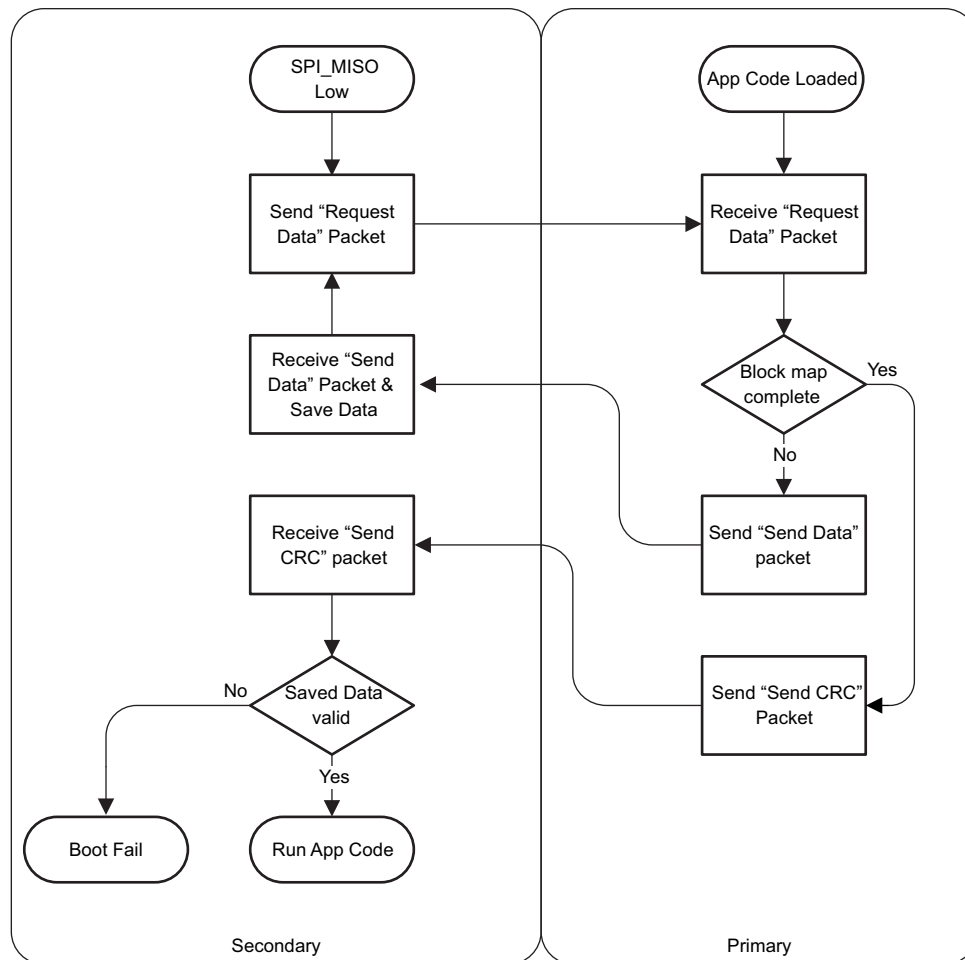


Figure 68. Memory Invalid Flow

9.4.8 UART Download

the secondary TPS65982 downloads the needed application code from the primary TPS65982 via UART. Figure 69 shows the UART download process.

Currently the TPS65982 firmware only supports 2 device (1 primary + 1 secondary) systems.

**Device Functional Modes (continued)**

**Figure 69. UART Download Process**

## 9.5 Programming

### 9.5.1 SPI Master Interface

The TPS65982 loads flash memory during the *Boot Code* sequence. The SPI master electrical characteristics are defined in *SPI Master Characteristics* and timing characteristics are defined in [Figure 8](#). The TPS65982 is designed to power the flash from LDO\_3V3 to support dead-battery or no-battery conditions, and therefore pullup resistors used for the flash memory must be tied to LDO\_3V3. The flash memory IC must support 12 MHz SPI clock frequency. The size of the flash must be at least 1 Mbyte (equivalent to 8 Mbit) to hold the standard application code outlined in *Application Code*. The SPI master of the TPS65982 supports SPI Mode 0. For Mode 0, data delay is defined such that data is output on the same cycle as chip select (SPI\_SSZ pin) becomes active. The chip select polarity is active-low. The clock phase is defined such that data (on the SPI\_MISO and SPI\_MOSI pins) is shifted out on the falling edge of the clock (SPI\_CLK pin) and data is sampled on the rising edge of the clock. The clock polarity for chip select is defined such that when data is not being transferred the SPI\_CLK pin is held (or idling) low. The minimum erasable sector size of the flash must be 4 kB. The W25Q80 flash memory IC is recommended. Refer to TPS65982 I<sup>2</sup>C Host Interface Specification for instructions for interacting with the attached flash memory over SPI using the host interface of the TPS65982.

## Programming (continued)

### 9.5.2 I<sup>2</sup>C Slave Interface

The TPS65982 has three I<sup>2</sup>C interface ports. I<sup>2</sup>C Port 1 is comprised of the I2C\_SDA1, I2C\_SCL1, and I2C\_IRQ1Z pins. I<sup>2</sup>C Port 2 is comprised of the I2C\_SDA2, I2C\_SCL2, and I2C\_IRQ2Z pins. These interfaces provide general status information about the TPS65982, as well as the ability to control the TPS65982 behavior, as well as providing information about connections detected at the USB-C receptacle and supporting communications to and from a connected device, cable supporting BMC USB-PD, or both. The third port is comprised of the DEBUG\_CTL1 and DEBUG\_CTL2 pins. This third port is a firmware emulated I<sup>2</sup>C master. The pins are generic GPIO and do not contain any dedicated hardware for I<sup>2</sup>C such as detecting starts, stops, acks, or other protocol normally associated with I<sup>2</sup>C. This third port is always a master and has no interrupt. This port is intended to master another device that has simple control based on mode and multiplexer orientation. DEBUG\_CTL1 is the serial clock and DEBUG\_CTL2 is serial data.

The first two ports can be a master or a slave, but the default behavior is to be a slave. Port 1 and Port 2 are interchangeable. Each port operates the same way and has the same access in and out of the core. An interrupt mask is set for each that determines what events are interrupted on that given port.

#### 9.5.2.1 I<sup>2</sup>C Interface Description

The TPS65982 support Standard and Fast mode I<sup>2</sup>C interface. The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input/output, while the SCL input is high initiates I<sup>2</sup>C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Figure 70 shows the start and stop conditions of the transfer. Figure 71 shows the SDA and SCL signals for transferring a bit. Figure 72 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

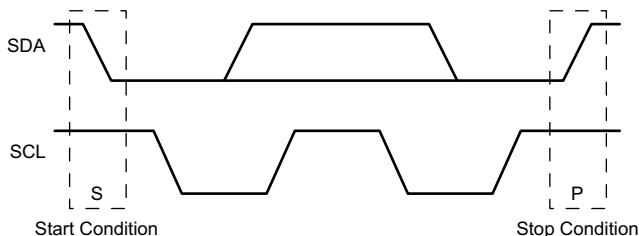
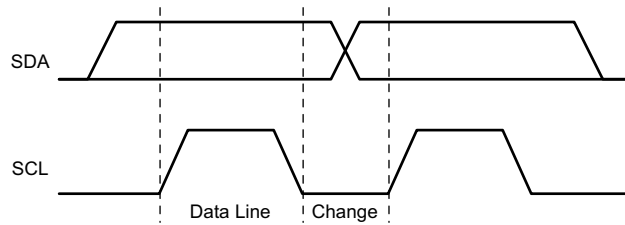
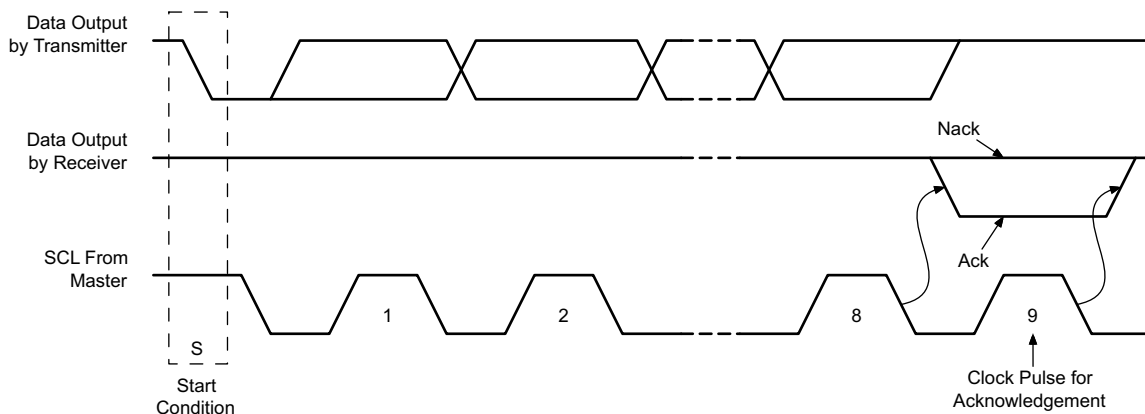


Figure 70. I<sup>2</sup>C Definition of Start and Stop Conditions

**Programming (continued)**

**Figure 71. I<sup>2</sup>C Bit Transfer**

**Figure 72. I<sup>2</sup>C Acknowledgment**
**9.5.2.2 I<sup>2</sup>C Clock Stretching**

The TPS65982 features clock stretching for the I<sup>2</sup>C protocol. The TPS65982 slave I<sup>2</sup>C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line will remain low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 μs for standard 100 kbps I<sup>2</sup>C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

**9.5.2.3 I<sup>2</sup>C Address Setting**

The boot code sets the hardware configurable unique I<sup>2</sup>C address of the TPS65982 before the port is enabled to respond to I<sup>2</sup>C transactions. The unique I<sup>2</sup>C address is determined by a combination of the digital level on the DEBUG\_CTL1/DEBUG\_CTL2 pins (two bits) and the analog level set by the analog I2C\_ADDR strap pin (three bits) as shown in [Table 9](#).

**Table 9. I<sup>2</sup>C Default Unique Address**

Default I <sup>2</sup> C Unique Address for Each Port								
Port Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
I <sup>2</sup> C Port 1 <sup>(1)</sup>	0	1	1	1	I2C_ADDR_DECODE[2:0]			R/W
I <sup>2</sup> C Port 2	0	1	DEBUG_CTL2	DEBUG_CTL1	I2C_ADDR_DECODE[2:0]			R/W

(1) I<sup>2</sup>C Port 1 ignores the hardware setting of the DEBUG\_CTL1 and DEBUG\_CTL2 pins and automatically sets these bits to 1 in Bit 4 and Bit 5 of the address

### 9.5.2.4 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I<sup>2</sup>C master and a single TPS65982. The I<sup>2</sup>C Slave sub-address is used to receive or respond to Host Interface protocol commands. Figure 73 and Figure 74 show the write and read protocol for the I<sup>2</sup>C slave interface, and a key is included in Figure 75 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

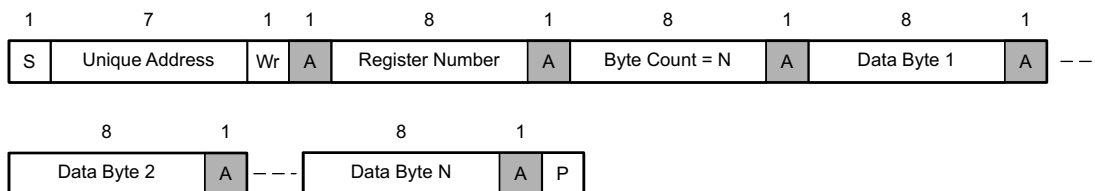


Figure 73. I<sup>2</sup>C Unique Address Write Register Protocol

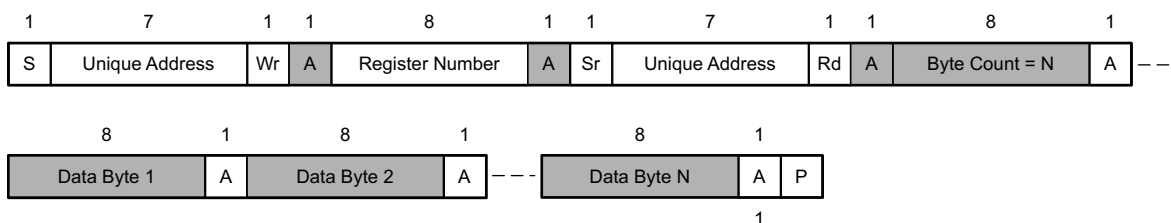


Figure 74. I<sup>2</sup>C Unique Address Read Register Protocol

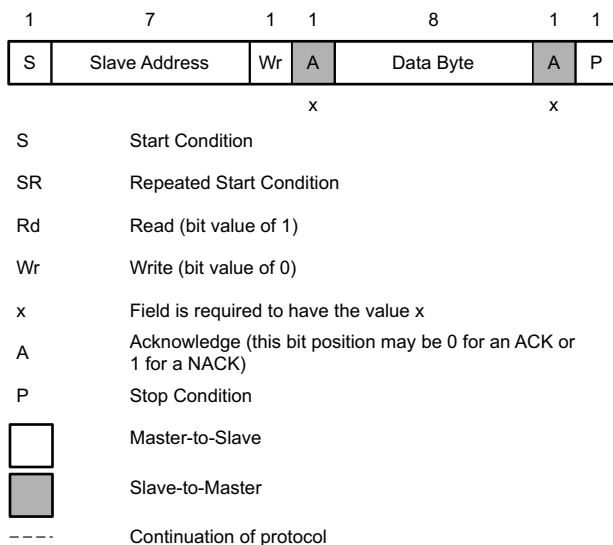


Figure 75. I<sup>2</sup>C Read/Write Protocol Key

### 9.5.2.5 I<sup>2</sup>C Pin Address Setting

To enable the setting of multiple I<sup>2</sup>C addresses using a single TPS65982 pin, a resistance is placed externally on the I2C\_ADDR pin. The internal ADC then decodes the address from this resistance value. Figure 76 shows the decoding. DEBUG\_CTL1/2 are checked at the same time for the DC condition on this pin (high or low) for setting other bits of the address described previously. Note, DEBUG\_CTL1/2 are GPIO and the address decoding is done by firmware in the digital core.

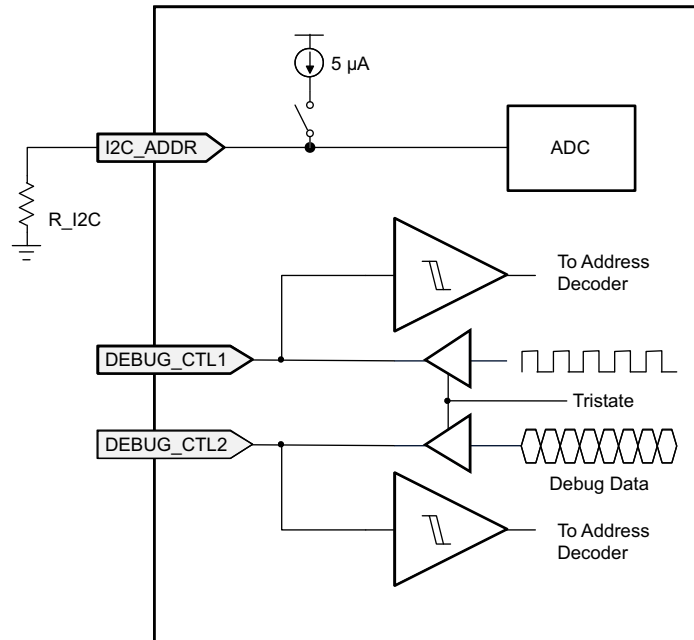

**Figure 76. I<sup>2</sup>C Address Decode**

Table 10 lists the external resistance needed to set bits [3:1] of the I<sup>2</sup>C Unique Address. For the Primary TPS65982 (UART Master), the I2C\_ADDR pin is grounded and this TPS65982 is connected to the SPI Flash. In a two Type-C port system sharing one SPI Flash, I2C\_ADDR is left as an open-circuit (UART Slave 1) and this TPS65982 is referred to as the Secondary.

**Table 10. I<sup>2</sup>C Address Resistance**

TPS65982 DEVICE	EXTERNAL RESISTANCE (1%)	I <sup>2</sup> C UNIQUE ADDRESS [3:1]
SPI Owner, UART Master 0 (Primary)	0 Ω	0x00
UART Slave 7	38.3 kΩ	0x01
UART Slave 6	84.5 kΩ	0x02
UART Slave 5	140 kΩ	0x03
UART Slave 4	205 kΩ	0x04
UART Slave 3	280 kΩ	0x05
UART Slave 2	374 kΩ	0x06
UART Slave 1 (Secondary)	Open	0x07



## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

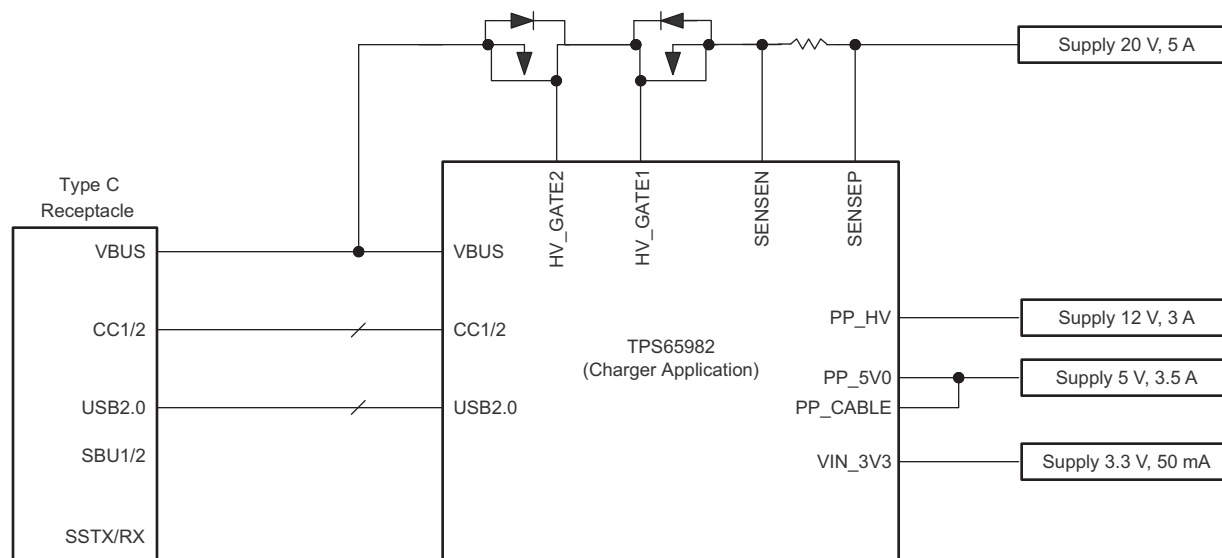
### 10.1 Application Information

The typical applications of the TPS65982 include chargers, notebooks, tablets, ultrabooks, docking systems, dongles, and any other product supporting USB Type-C, USB-PD as a power source, power sink, data DFP, data UFP, or dual-role port (DRP), or supporting both USB Type-C and USB-PD. The typical applications outlined in the following sections detail a [Fully-Featured USB Type-C and PD Charger Application](#) and a [Dual-Port Notebook Application Supporting USB PD Charging and DisplayPort](#).

### 10.2 Typical Applications

#### 10.2.1 Fully-Featured USB Type-C and PD Charger Application

The TPS65982 controls three separate power paths making it a flexible option for Type C PD charger applications. In addition, the TPS65982 supports VCONN power for *e-marked* cables which are required for applications which require greater than 3 A of current on VBUS. [Figure 77](#) below shows the high level block diagram of a Type C PD charger that is capable of supporting 5 V at 3 A, 12 V at 3 A, and 20 V at 5 A. The 5 V and 12 V outputs are supported by the TPS65982 internal FETs and the 20-V output uses the external FET path controlled by the TPS65982 NFET drive. This Type-C PD charger uses a receptacle for flexibility on cable choice.



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Figure 77. Type-C and PD Charger Application

#### 10.2.1.1 Design Requirements

For a USB Type-C and PD Charger application, [Table 11](#) lists the input voltage requirements and expected current capabilities.

## Typical Applications (continued)

**Table 11. Charging Application Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE	DIRECTION OF CURRENT
PP_5V0 Input Voltage and Current Capabilities	5 V, 3 A	Sourcing to VBUS
PP_CABLE Input Voltage and Current Capabilities	5 V, 500 mA	Sourcing to VCONN
PP_HV Input Voltage and Current Capabilities	12 V, 3 A	Sourcing to VBUS
EXT FET Path Input Voltage and Current Capabilities	20 V, 5 A	Sourcing to VBUS
VIN_3V3 Voltage and Current Requirements	2.85 - 3.45 V, 50 mA	Internal TPS65982 Circuitry

### 10.2.1.1.1 External FET Path Components (PP\_EXT and RSENSE)

The external FET path allows for the maximum PD power profile (20 V at 5 A) and design considerations must be taken into account for choosing the appropriate components to optimize performance.

Although a Type C PD charger will be providing power there could be a condition where a non-compliant device can be connected to the charger and force voltage back into the charger. To protect against this the external FET path detects reverse current in both directions of the current path. The TPS65982 uses two *back-to-back* NFETs to protect both sides of the system. Another design consideration is to rate the external NFETs above the Type C and PD specification maximum which is 20 V. In this specific design example, 30-V NFETs are used that have an average  $R_{DS,ON}$  of 5 m $\Omega$  to reduce losses.

The TPS65982 supports either a 10-m $\Omega$  or a 5-m $\Omega$  sense resistor on the external FET path. This RSENSE resistor is used for current limiting and is used for the reverse current protection of the power path. A 5 m $\Omega$  sense resistor is used in the design to minimize losses and I-R voltage drop. Recommended NFET Capabilities summarizes the recommended parameters for the external NFET used. The total voltage drop seen across RSENSE and the external NFET could be determined by Equation 5 below. It is important to consider the drop in the entire system and regulate accordingly to ensure that the output voltage is within its specification. Equation 6 will calculate the power lost through the external FET path.

**Table 12. Recommended NFET Capabilities**

Voltage Rating	Current Rating	$R_{DS,ON}$
30 V (minimum)	10 A (peak current)	< 10 m $\Omega$

$$\text{Voltage Drop} = \text{DC Current} \times (R_{\text{SENSE}} + \text{NFET1 } R_{\text{DS,ON}} + \text{NFET2 } R_{\text{DS,ON}}) \quad (5)$$

$$\text{Power Loss} = \text{Voltage Drop} \times \text{DC Current} \quad (6)$$

### 10.2.1.2 Detailed Design Procedure

#### 10.2.1.2.1 TPS65982 External Flash

The external flash contains the TPS65982 application firmware and must be sized to 256kB minimum when the flash is not shared with another IC, but a recommended minimum of 1 MB is needed when the flash memory of the TPS65982 is shared with another IC. This size will allow for pointers and two copies of the firmware image to reside on the flash along with the needed headers. The flash used is the W25Q80 which is a 3.3-V flash and is powered from the LDO\_3V3 output from the TPS65982.

#### 10.2.1.2.2 I<sup>2</sup>C (I2C), Debug Control (DEBUG\_CTL), and Single-Wire De-bugger (SWD) Resistors

I2C\_ADDR, DEBUG\_CTL1/2 pins must be tied to GND through a 0- $\Omega$  resistor tied to GND directly if needed to reduce solution size. Pullups on the I2C\_CLK, I2C\_SDA, and I2C\_IRQ are used for debugging purposes. In most simple charger designs, I<sup>2</sup>C communication may not be needed. A 3.83-k $\Omega$  pullup resistor from SWD\_DATA to LDO\_3V3 and a 100-k $\Omega$  pulldown resistor from SWD\_CLK to GND must also be used for debugging purposes.

#### 10.2.1.2.3 Oscillator (R\_OSC) Resistor

A 15-k $\Omega$  0.1% resistor is needed for key PD BMC communication timing and the USB2.0 endpoint. A 1% 15-k $\Omega$  resistor is not recommended to be used because the internal oscillators will not be controlled well enough by this loose resistor tolerance.

#### 10.2.1.2.4 VBUS Capacitor and Ferrite Bead

A 1- $\mu$ F ceramic capacitor is placed close to the TPS65982 VBUS pins. A 6 A ferrite bead is used in this design along with four high frequency noise 10-nF capacitors placed close to the Type-C connector to minimize noise.

#### 10.2.1.2.5 Soft Start (SS) Capacitor

The recommended 0.22  $\mu$ F is placed on the TPS65982 SS pin.

#### 10.2.1.2.6 USB Top (C\_USB\_T), USB Bottom (C\_USB\_B), and Sideband-Use (SBU) Connections

Although the charger is configured to be only a power source, SBU1/2, USB Top and Bottom must be routed to the Type C connector. This allows for debugging or for any specific alternate modes for power to be configured if needed. ESD protection is used in the design on all of these nets as good design practice.

#### 10.2.1.2.7 Port Power Switch (PP\_EXT, PP\_HV, PP\_5V0, and PP\_CABLE) Capacitors

The design assumes that a DC-DC converter is connected to the paths where there is significant output capacitance on the DC-DCs to provide the additional capacitance for load steps. TI recommends to for the DC-DC converters for to be capable of supporting current spikes which can occur with certain PD configurations.

The PP\_EXT path is capable of supporting up to 5 A which will require additional capacitance to support system loading by the device connected to the charger. A ceramic 10- $\mu$ F (X7R/X5R) capacitor is used in this design. This capacitor must at least have a 25 V rating and it is recommended to have 30 V or greater rated capacitor.

The PP\_HV path is capable of supporting up to 3 A which will require additional capacitance to support system loading by the device connected to the charger. A ceramic 10- $\mu$ F (X7R/X5R) capacitor coupled with a 0.1  $\mu$ F high frequency capacitor is placed close to the TPS65982.

The PP\_5V0 and PP\_CABLE supplies are connected together therefore a ceramic 22- $\mu$ F (X7R/X5R) capacitor coupled with a 0.1- $\mu$ F high-frequency capacitor is placed close to the TPS65982. The PP\_5V0 path can support 3 A and the PP\_CABLE path supports 600 mA for active Type C PD cables.

The design assumes that a DC-DC converter is connected to the paths where there is significant output capacitance on the DC-DCs to provide the additional capacitance. It is recommended to for the DC-DC converters to be capable of supporting current spikes which can occur with certain PD configurations.

#### 10.2.1.2.8 Cable Connection (CCn) Capacitors and RPD\_Gn Connections

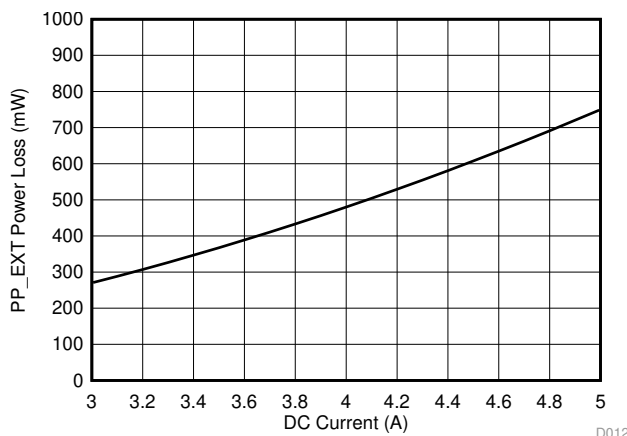
This charger application is designed to only be a source of power and does not support *Dead Battery*. RPD\_G1 and RPD\_G2 must be tied to GND and not connected to the CC1 and CC2 respectively. For CC1 and CC2 lines, they require a 220 pF capacitor to GND.

#### 10.2.1.2.9 LDO\_3V3, LDO\_1V8A, LDO\_1V8D, LDO\_BMC, VOUT\_3V3, VIN\_3V3, and VDDIO

For all capacitances it is important to factor in DC voltage de-rating of ceramic capacitors. Generally the effective capacitance is halved with voltage applied.

VIN\_3V3 is connected to VDDIO which ensures that the I/Os of the TPS65982's will be configured to 3.3 V. A 1  $\mu$ F capacitor is used and is shared between VDDIO and VIN\_3V3. LDO\_1V8D, LDO\_1V8A, and LDO\_BMC each have their own 1  $\mu$ F capacitor. In this design LDO\_3V3 powers the TPS65982's external flash and various pull ups. A 10  $\mu$ F capacitor was chosen to support these additional connections. VOUT\_3V3 is not used in this design and capacitor is not needed.

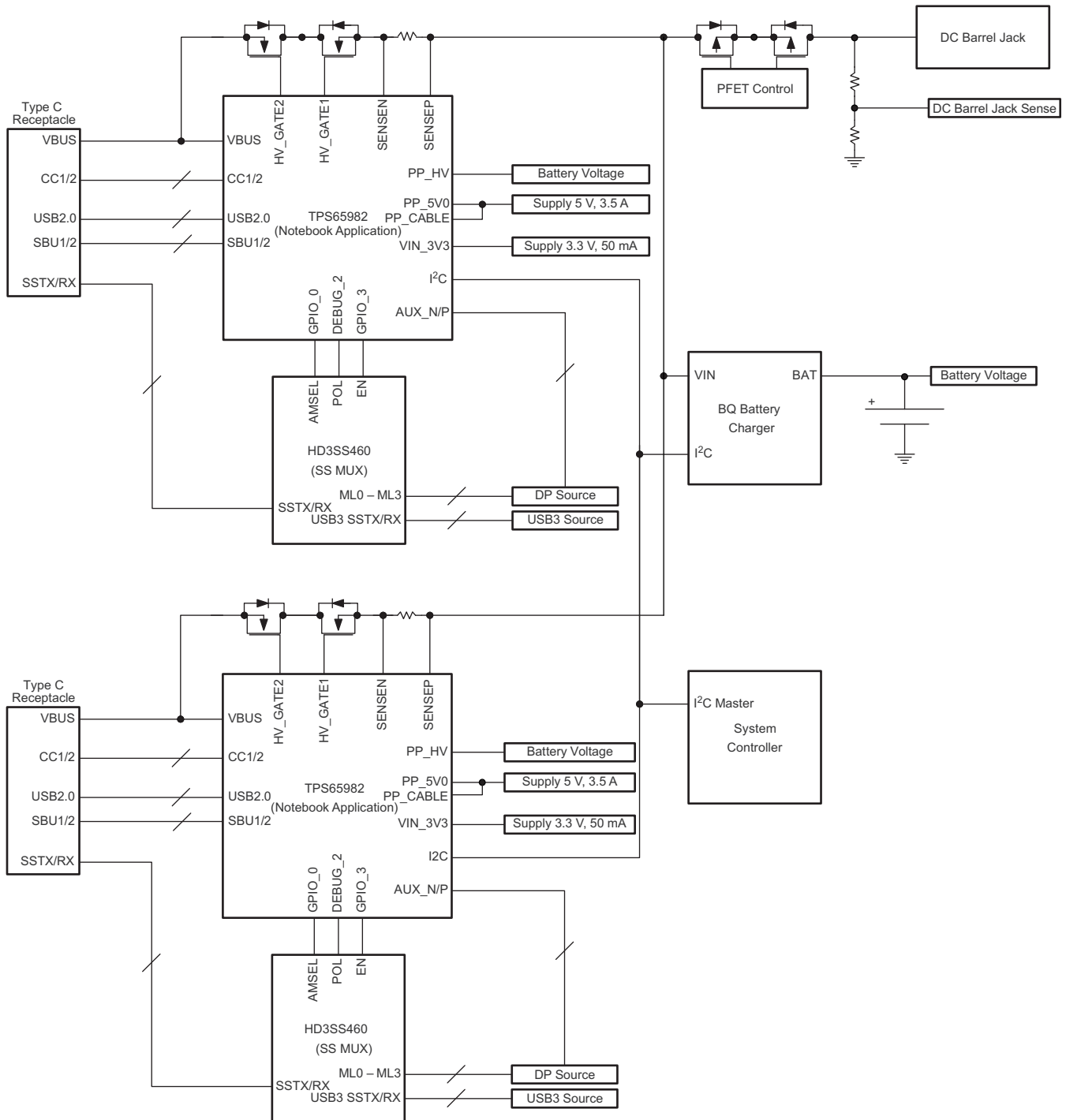
### 10.2.1.3 Application Curve



**Figure 78. PP\_EXT Power Loss ( $R_{NFETS} + R_{SENSE} = 30\text{ m}\Omega$ )**

### 10.2.2 Dual-Port Notebook Application Supporting USB PD Charging and DisplayPort

The TPS65982 features support for DisplayPort over Type-C alternate mode and manages sinking and sourcing of power in Power Delivery. The block diagram, shown in [Figure 79](#), shows a two port system that is capable of charging from either Type C port over PD, DisplayPort Alternate Mode, and delivering Battery Power to a bus-powered device. With the DisplayPort support, the TPS65982 controls an external SuperSpeed multiplexer, HD3SS460, to route the appropriate super-speed signals to the Type-C connector. The HD3SS460 is controlled through GPIOs configured by the TPS65982 application code and the HD3SS460 is designed to meet the timing requirements defined by the DisplayPort over Type-C specification. A system controller is also necessary to handle some of the dynamic aspects of Power Delivery such as reducing power capabilities when system battery power is low. Audio accessory device is supported by the design as well. Although USB\_RP\_P and USB\_RP\_N are not shown in the block diagram, they must be connected to the system-side IC that will receive and send USB2.0 high-speed data through the integrated multiplexer of the TPS65982.



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Figure 79. Dual-Port Notebook Application

10.2.2.1 Design Requirements

For a dual-port notebook application, Table 13 lists the input voltage requirements and expected current capabilities.

**Table 13. Dual-Port Notebook Application Design Parameters**

DESIGN PARAMETERS	EXAMPLE VALUE	DIRECTION OF CURRENT
PP_5V0 Input Voltage and Current Capabilities	5 V, 3 A	Sourcing to VBUS
PP_CABLE Input Voltage and Current Capabilities	5 V, 500 mA	Sourcing to VCONN
PP_HV Input Voltage and Current Capabilities	10-13 V, 3 A	Sourcing to VBUS (directly from Battery)
EXT FET Path Voltage and Current Capabilities	20 V, 3 A	Sourcing to VBUS or Sinking from VBUS
VIN_3V3 Voltage and Current Requirements	2.85-3.45 V, 50 mA	Internal TPS65982 Circuitry

**10.2.2.1.1 Source Power Delivery Profiles for Type-C Ports**

Table 14 lists the summary of the source PD profiles that are supported for this specific design. PDO 1 and 2 will always be present in the system and will be able to be negotiated without any other system interaction. When DC barrel Jack voltage is sensed PDO 3 will become available for power delivery negotiation. The external sense resistor, RSENSE, is configured to only measure the current being sourced by the system. When operating as a sink of power the input current cannot be measured in this configuration.

**Table 14. Source USB PD Profiles**

PDO	POD TYPE	VOLTAGE	CURRENT OR POWER	EXTERNALLY DEPENDENT
PDO1	Fixed Supply	5 V	3 A	No
PDO2	Battery Power	10 V - 13 V	30 W	No
PDO3	Fixed Supply	20 V	3 A	Yes

**10.2.2.1.2 Sink Power Delivery Profile for Type-C Ports**

The two Type-C ports used in this design support Power Delivery and enable charging over a Type-C connection. Table 15 shows the sink profile supported by both of the ports. The reverse current blocking of the device allows both of the Type-C ports to negotiate a power contract, but it is good system practice for the System Controller to change the sink profile when a power contract is established. When the DC barrel jack is connected the TPS65982 is renegotiate the a PD contract to no longer charge of Type C and have the DC Barrel Jack take precedence when connected.

**Table 15. Sink USB PD Profile**

RDO	RDO TYPE	VOLTAGE	EXTERNALLY DEPENDENT
Fixed Supply	20 V	3 A	Yes

**10.2.2.2 Detailed Design Procedure**

The same passive components used in the *Fully-Featured USB Type-C and PD Charger Application* are also applicable in this design to support all of the features of the TPS65982. Additional design information is provided below to explain the connections between the TPS65982 and the system controller and the TPS65982 and the HD3SS460 SuperSpeed multiplexer.

**10.2.2.2.1 TPS65982 and System Controller Interaction**

The TPS65982 features two I<sup>2</sup>C slave ports that can be used simultaneously, where the system controller has the ability to write to either of the I<sup>2</sup>C slave ports. Each I<sup>2</sup>C port has an I<sup>2</sup>C interrupt that will inform the system controller that a change has happened in the system. This allows the system controller to dynamically budget power and reconfigures a port’s capabilities dependent on current state of the system. For example, if a battery power contract is established and the system is running low on battery power the system controller could notify the TPS65982 to re-negotiate a power contract. The system controller is also used for updating the TPS65982 firmware over I<sup>2</sup>C, where the Operating System loads the Firmware update to the system controller and then the system controller updates the firmware stored in the SPI Flash memory via I<sup>2</sup>C writes to the TPS65982.

### 10.2.2.2.2 HD3SS460 Control and DisplayPort Configuration

The two Type-C ports in this design support DisplayPort simultaneously on both ports. When a system is not capable of supporting video on both ports the system controller will disable DisplayPort on the second Type-C port through I<sup>2</sup>C. Table 16 lists the DisplayPort configurations supported in the system. Table 17 lists the summary of the TPS65982 GPIO signals control for the HD3SS460. Although the HD3SS460 is able to multiplex the required AUX\_N/P signals to the SBU\_1/2 pins, they are connected through the TPS65982 for additional support of custom alternate mode configurations.

**Table 16. Supported DisplayPort Configurations**

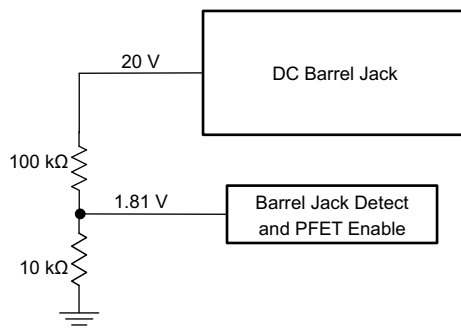
CONFIGURATION	DisplayPort ROLE	DisplayPort PIN ASSIGNMENT	DisplayPort LANES
Configuration 1	DFP_D	Pin Assignment C	4 Lane
Configuration 2	DFP_D	Pin Assignment D	2 Lane and USB 3.1
Configuration 3	DFP_D	Pin Assignment E	4 Lane (Dongle Support)

**Table 17. TPS65982 and HD3SS460 GPIO Control**

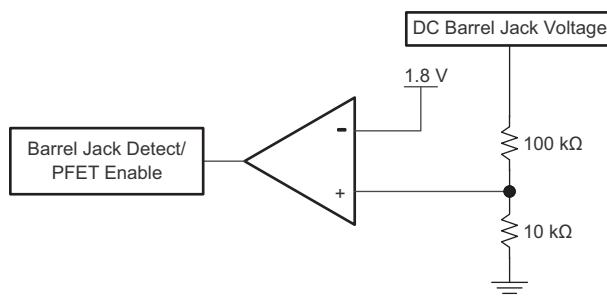
TPS65982 GPIO	HD3SS460 CONTROL PIN	DESCRIPTION
GPIO_0	AMSEL	Alternate Mode Selection (DP/USB3)
GPIO_3	EN	Super Speed Mux Enable
DEBUG2	POL	Type-C Cable

### 10.2.2.2.3 9.3.2.3 DC Barrel Jack and Type-C PD Charging

The system is design to either charge over Type-C or from the DC barrel jack. The TPS65982 detects that the DC barrel jack is connected to GPIO. In the simplest form, a voltage divider could be set to the GPIO I/O level when the DC Barrel jack voltage is present, as shown in Figure 80. A comparator circuit is recommend and used in this design for design robustness, as shown in Figure 81.



**Figure 80. DC Barrel Jack Voltage Divider**



**Figure 81. Barrel Jack Detect Comparator**



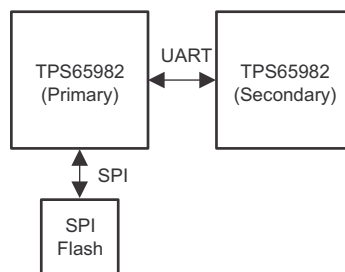
This detect signal is used to determine if the barrel jack is present to support the 20 V PD power contracts and to hand-off charging from barrel jack to Type-C or Type-C to barrel jack. When the DC barrel jack is detected the TPS65982 at each Type-C port will not request 20 V for charging and the system will be able to support a 20 V source power contract to another device. When the DC Barrel Jack is disconnected the TPS65982 will exit any 20 V source power contract and re-negotiate a power contract. When the DC Barrel Jack is connected the TPS65982 will send updated source capabilities and re-negotiate a power contract if needed.

The PFET enable will be controlled by the DC barrel jack detect comparator depicted in [Figure 81](#). This will allow the system to power up from dead battery through the barrel jack as well as the Type-C ports. [Figure 83](#) shows the flow between changing from DC barrel jack charging and USB-PD charging. The example uses back-to-back PFETs for disabling and enabling the power path for the DC Barrel Jack. It is important to use PFETs that are rated above the specified parameters to ensure robustness of the system. The DC Barrel Jack voltage in this design is assumed to be 20 V at 5 A, so the PFETs are recommended to be rated at a minimum of 30 V and 10 A of current.

The TPS65982 in this design also provides the GPIO control for the PFET gate drive that passes the DC Barrel Jack Voltage to the system. [Figure 83](#) shows the flow between changing from DC Barrel Jack charging and Type-C PD charging.

#### 10.2.2.2.4 Primary TPS65982 Flash Master and Secondary Port

A single flash can be used for two TPS65982's in a system where the primary TPS65982 is connected to the flash and the secondary TPS65982 is connected to the primary through UART. UART data is used to pass the firmware from the primary TPS65982 to the secondary TPS65982 in the system. [Figure 82](#) shows a simplified block diagram of how a primary and secondary TPS65982 are connected using a single flash. The primary TPS65982 must have its I2C\_ADDR pin tied to GND with a 0Ω to denote it as the primary TPS65982.



**Figure 82. Primary and Secondary TPS65982 Sharing a Single Flash**

#### 10.2.2.2.5 TPS65982 Dead Battery Support Primary and Secondary Port

The TP65982 supports dead battery functionality to be able to power up from the Type-C port. This design supports dead battery using the PP\_EXT path, where RPD\_G1/2 and CC1/2 are connected respectively, and BUSPOWERZ is connected to GND to path 5 V VBUS into the system through the PP\_EXT path. The TPS65982 will soft-start the PP\_EXT (or PP\_HV) path to comply with USB2.0 inrush current requirements. To enable PD functionality the TPS65982 must boot the application firmware from the flash. For the primary TPS65982, once VBUS is detected at 5 V it will automatically start to load the application firmware from the flash. The TPS65982 will then be able communicate over PD and establish a power contract at the required 20 V. [Figure 84](#) shows the boot up sequence of the primary TPS65982.

When the TPS65982 that is not connected to the flash is connected in dead battery it will pass the 5 V from VBUS in to the battery charger where the battery would be able to generate the needed System 3.3 V rail to both of the TPS65982s. Once the primary TPS65982 has a valid 3.3 V supply (VBUS = 0 V on Primary TPS65982) it will load the application firmware from the flash and pass it to the secondary TPS65982 that is connected. Once the secondary TPS65982 has loaded the application firmware over UART it will be able to negotiate a 20-V power contract. [Figure 85](#) shows the dead battery sequence of the secondary TPS65982.



### 10.2.2.2.6 Debugging Methods

The TPS65982 has methods of debugging a Type-C and PD system. In addition to the resistances recommended in the *I<sup>2</sup>C (I2C), Debug Control (DEBUG\_CTL), and Single-Wire De-bugger (SWD) Resistors* section, additional series resistors are used for debugging. The two I<sup>2</sup>C channels allow a designer to check the system state through the Host Interface Specification. By attaching 0-Ω series resistors between the I<sup>2</sup>C master and the TPS65982 and additionally adding 0-Ω series resistors between the TPS65982 and test points, a multi-master scenario can be avoided. This allows breaking the connection between the I<sup>2</sup>C channels and the system to allow I<sup>2</sup>C access to the TPS65982 from an external tool. A header is used to allow for connections without soldering; however, SMT test pads can be used to provide a place to solder *blue-wires* for testing.

Exposing the SWD\_DATA and SWD\_CLK pins will allow for more advanced debugging if needed. A header or SMT test point is also used for the SWD\_DATA and SWD\_CLK pins.

### 10.2.2.3 Application Curves

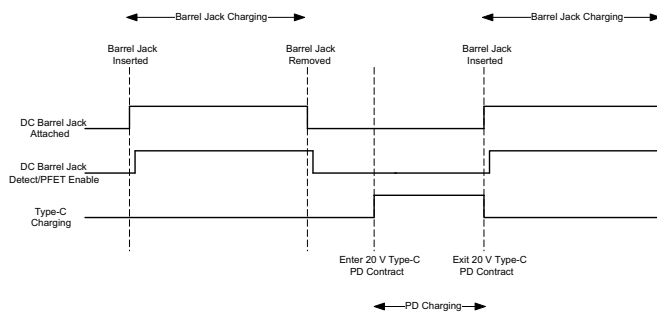


Figure 83. DC Barrel Jack and Type-C PD Charging Hand-Off

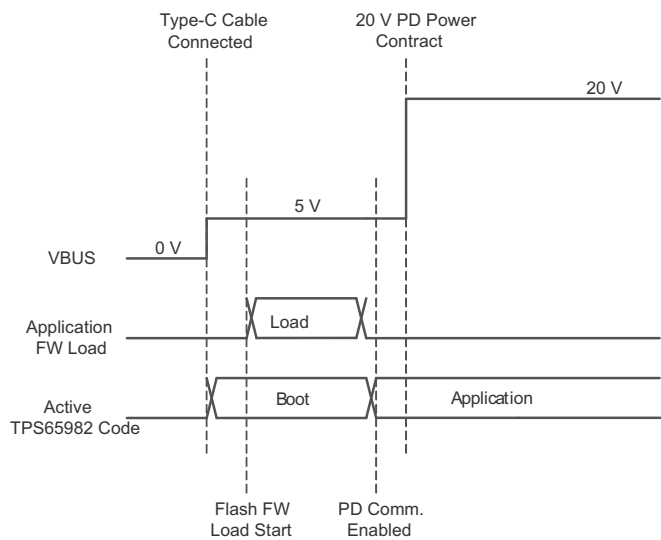


Figure 84. Primary TPS65982 Dead Battery Sequence

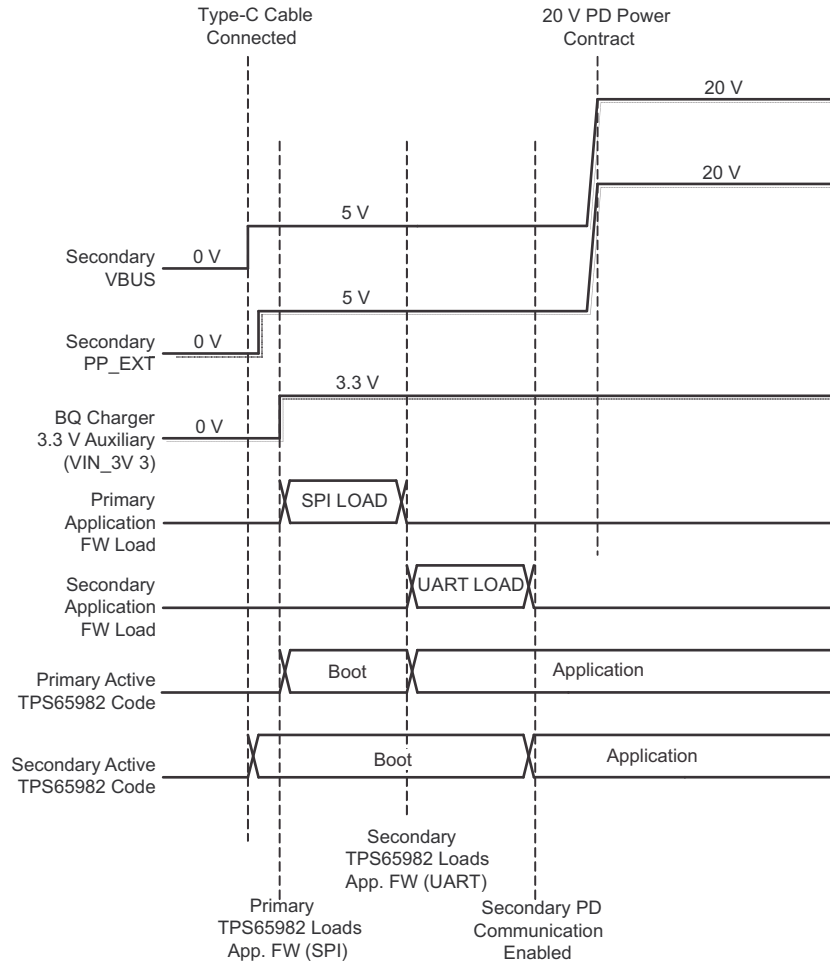


Figure 85. Secondary TPS65982 Dead Battery Sequence

## 11 Power Supply Recommendations

### 11.1 3.3-V Power

#### 11.1.1 VIN\_3V3 Input Switch

The VIN\_3V3 input is the main supply to the TPS65982. The VIN\_3V3 switch (S1 in [Figure 49](#)) is a unidirectional switch from VIN\_3V3 to LDO\_3V3, not allowing current to flow backwards from LDO\_3V3 to VIN\_3V3. This switch is on when 3.3 V is available. See [Table 18](#) for the recommended external capacitance on the VIN\_3V3 pin.

#### 11.1.2 VOUT\_3V3 Output Switch

The VOUT\_3V3 output switch (S2 in [Figure 49](#)) enables a low-current auxiliary supply to an external element. This switch is controlled by and is off by default. The VOUT\_3V3 output has a supervisory circuit that drives the RESETZ output as a POR signal to external elements. RESETZ is also asserted by the MRESET pin or a host controller. See RESETZ and MRESET for more details on RESETZ. See [Table 18](#) for the recommended external capacitance on the VOUT\_3V3 pin.

#### 11.1.3 VBUS 3.3-V LDO

The 3.3-V LDO from VBUS steps down voltage from VBUS to LDO\_3V3. This allows the TPS65982 to be powered from VBUS when VIN\_3V3 is not available. This LDO steps down any recommended voltage on the VBUS pin. When VBUS is 20 V, as is allowable by USB PD, the internal circuitry of the TPS65982 will operate without triggering thermal shutdown; however, a significant external load on the LDO\_3V3 pin may increase temperature enough to trigger thermal shutdown. The VBUS 3.3-V LDO blocks reverse current from LDO\_3V3 back to VBUS allowing VBUS to be unpowered when LDO\_3V3 is driven from another source. See [Table 18](#) for the recommended external capacitance on the VBUS and LDO\_3V3 pins.

### 11.2 1.8 V Core Power

Internal circuitry is powered from 1.8 V. There are two LDOs that step the voltage down from LDO\_3V3 to 1.8 V. One LDO powers the internal digital circuits. The other LDO powers internal low voltage analog circuits.

#### 11.2.1 1.8 V Digital LDO

The 1.8 V Digital LDO provides power to all internal low voltage digital circuits. This includes the digital core, memory, and other digital circuits. See [Table 18](#) for the recommended external capacitance on the LDO\_1V8D pin.

#### 11.2.2 1.8 V Analog LDO

The 1.8 V Analog LDO provides power to all internal low voltage analog circuits. See [Table 18](#) for the recommended external capacitance on the LDO\_1V8A pin.

### 11.3 VDDIO

The VDDIO pin provides a secondary input allowing some I/Os to be powered by a source other than LDO\_3V3. The default state is power from LDO\_3V3. The memory stored in the flash will configure the I/O's to use LDO\_3V3 or VDDIO as a source and application code will automatically scale the input and output voltage thresholds of the I/O buffer accordingly. See [I/O Buffers](#) for more information on the I/O buffer circuitry. See [Table 18](#) for the recommended external capacitance on the VDDIO pin.

#### 11.3.1 Recommended Supply Load Capacitance

[Table 18](#) lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage de-rating ensuring proper operation.

**VDDIO (continued)**
**Table 18. Recommended Supply Load Capacitance**

PARAMETER	DESCRIPTION	VOLTAGE RATING	CAPACITANCE		
			MIN (ABS MIN)	TYP (TYP PLACED)	MAX (ABS MAX)
CVIN_3V3	Capacitance on VIN_3V3	6.3 V	5 $\mu$ F	10 $\mu$ F	
CLDO_3V3	Capacitance on LDO_3V3	6.3 V	5 $\mu$ F	10 $\mu$ F	25 $\mu$ F
CVOUT_3V3	Capacitance on VOUT_3V3	6.3 V	0.1 $\mu$ F	1 $\mu$ F	2.5 $\mu$ F
CLDO_1V8D	Capacitance on LDO_1V8D	4 V	500 nF	2.2 $\mu$ F	12 $\mu$ F
CLDO_1V8A	Capacitance on LDO_1V8A	4 V	500 nF	2.2 $\mu$ F	12 $\mu$ F
CLDO_BMC	Capacitance on LDO_BMC	4 V	1 $\mu$ F	2.2 $\mu$ F	4 $\mu$ F
CVDDIO	Capacitance on VDDIO. When shorted to LDO_3V3, the CLDO_3V3 capacitance may be shared.	6.3 V	0.1 $\mu$ F	1 $\mu$ F	
CVBUS	Capacitance on VBUS 1	25 V	0.5 $\mu$ F	1 $\mu$ F	12 $\mu$ F
CPP_5V0	Capacitance on PP_5V0	10 V	2.5 $\mu$ F	4.7 $\mu$ F	
CPP_HV	Capacitance on PP_HV (Source to VBUS)	25 V	2.5 $\mu$ F	4.7 $\mu$ F	
	Capacitance on PP_HV (Sink from VBUS)	25 V		47 $\mu$ F	120 $\mu$ F
CPP_CABLE	Capacitance on PP_CABLE. When shorted to PP_5V0, the CPP_5V0 capacitance may be shared.	10 V	2.5 $\mu$ F	4.7 $\mu$ F	
CPP_HVEXT	Capacitance on external high voltage source to VBUS	25 V	2.5 $\mu$ F	4.7 $\mu$ F	
	Capacitance on external high voltage sink from VBUS	25 V		47 $\mu$ F	120 $\mu$ F
CSS	Capacitance on soft start pin	6.3 V		220 nF	
CC_CC1	Capacitance on C_CC1 pin	25 V	220 pF	330 pF	470 pF
CC_CC2	Capacitance on C_CC2 pin	25 V	220 pF	330 pF	470 pF

**11.3.2 Schottky for Current Surge Protection**

To prevent the possibility of large ground currents into the TPS65982 during sudden disconnects because of inductive effects in a cable, it is recommended that a Schottky be placed from VBUS to GND as shown in [Figure 86](#). The NSR20F30NXT5G is recommended.

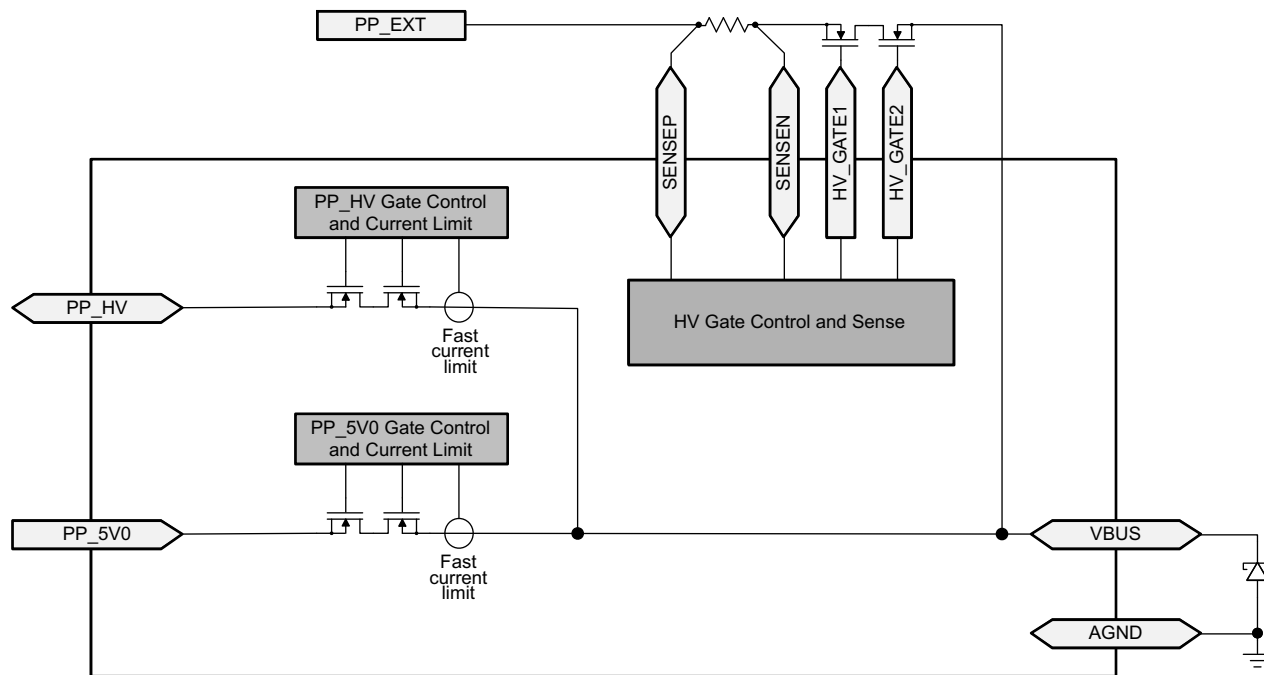


Figure 86. Schottky on VBUS for Current Surge Protection

## 12 Layout

### 12.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high-speed signals and improve the thermal dissipation from the TPS65982 power path. The combination of power and high-speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with a printed circuit board (PCB) manufacturer to verify manufacturing capabilities.

#### 12.1.1 TPS65982 Recommended Footprints

##### 12.1.1.1 Standard TPS65982 Footprint (Circular Pads)

Figure 87 shows the TPS65982 footprint using a 0.25mm pad diameter. This footprint is applicable to boards that will be using an HDI PCB process that uses smaller vias to fan-out into the inner layers of the PCB. This footprint requires via fill and tenting and is recommended for size-constrained applications. The circular footprint allows for easy fan-out into other layers of the PCB and better thermal dissipation into the GND planes. Figure 88 shows the recommended via sizing for use under the balls. The size is 5mil hole and 10mil diameter. This via size will allow for approximately 1.5A current rating at 3 mΩ of DC resistance with 1.6nH of inductance. It is recommended to verify these numbers with board manufacturing processes used in fabrication of the PCB. This footprint is available for download on the TPS65982 product folder on the [TPS65982 product folder](#).

Layout Guidelines (continued)

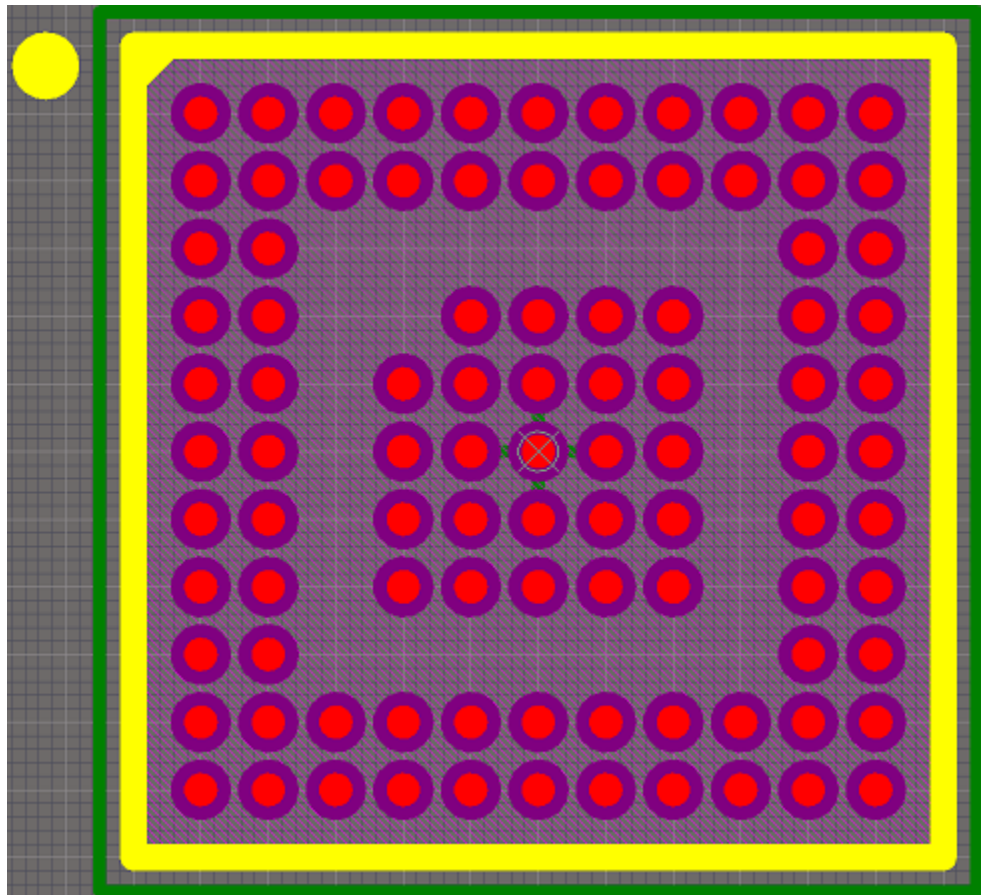


Figure 87. Top View Standard TPS65982 Footprint (Circular Pads)



Figure 88. Under Ball Recommended Via Size

12.1.2 Alternate TPS65982 Footprint (Oval Pads)

Figure 89 shows the TPS65982 footprint using oval-shaped pads in specific locations. This allows the PCB designer to route the inner perimeter balls through the top layer. The balls around the perimeter have their pads in an oval shape with the exception of the corner balls. Figure 90 shows the sizing for the oval pads, 0.25 mm by 0.17 mm. All of the other non-oval shaped pads will have a 0.25 mm diameter. This footprint is recommended for MDI (Medium Density) PCB designs that are generally less expensive to build. The void under the TPS65982 allows for vias to route the inner signals and connect to the GND and power planes. Figure 91 shows the recommended minimum via size (8mil hole and 16 mil diameter). The recommended 8mil vias will be rated for approximately 1.8 A of DC current and 1.5 mΩ of resistance with 1.3 nH of inductance. Some board manufactures may offer 6mil hole and 12 mil diameter vias with a mechanical drill. This footprint is available for download on the [TPS65982 product folder](#).

Layout Guidelines (continued)

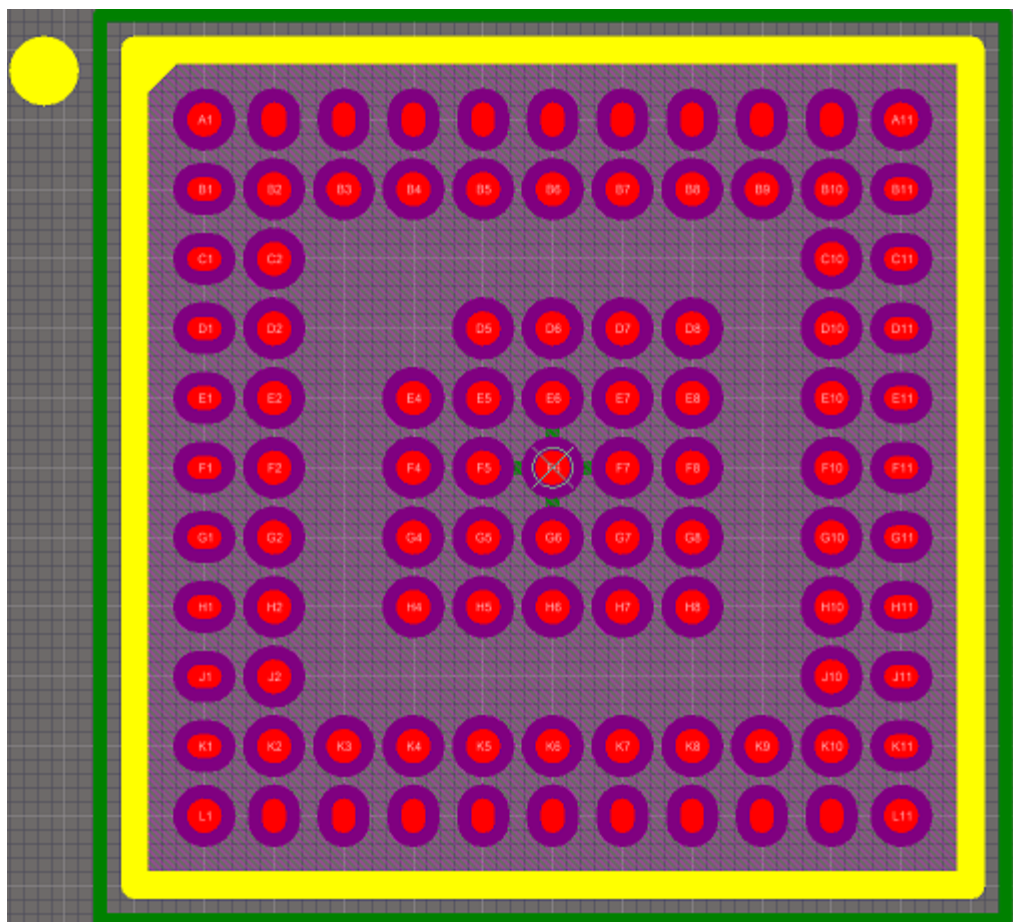


Figure 89. Top View Alternate TPS65982 Footprint (Oval Pads)

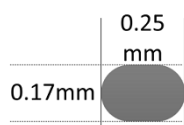


Figure 90. Oval Pad Sizing



Figure 91. Recommended Minimum Via Sizing

12.1.3 Top TPS65982 Placement and Bottom Component Placement and Layout

When the TPS65982 is placed on top and its components on bottom the solution size will be at its smallest. For systems that do not use the optional external FET path the solution size will average less than 64 mm<sup>2</sup> (8 mm × 8 mm). Systems that implement the optional external FET path will average a solution size of less than 100 mm<sup>2</sup> (10 mm × 10 mm). These averages will vary with component selection (NFETs, Passives, etc.). Selection of the oval pad TPS65982 footprint or standard TPS65982 footprint will allow for similar results.



## Layout Guidelines (continued)

### 12.1.4 Oval Pad Footprint Layout and Placement

The oval pad footprint layout is generally more difficult to route than the standard footprint because of the top layer fan-out and void via placement needed; however, when the footprint with oval pads is used, *Via on Pads*, laser-drilled vias, and HDI board processes are not required. Therefore, a footprint with oval pads is ideal for cost-optimized applications and will be used for the following the layout example. This layout example follows the charger application example (see [Typical Applications](#)) and includes all necessary passive components needed for this application. This design uses both the internal and optional external FET paths for sourcing and sinking power respectively. Follow the differential impedances for High Speed signals defined by their specifications (DisplayPort - AUXN/P and USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will use all of the I/O on the TPS65982.

### 12.1.5 Component Placement

Placement of components on the top and bottom layers is used for this example to minimize solution size. The TPS65982 is placed on the top layer of the board and the majority of its components are placed on the bottom layer. When placing the components on the bottom layer, it is recommended that they are placed directly under the TPS65982 in a manner where the pads of the components are not directly under the void on the top layer. [Figure 92](#) and [Figure 93](#) show the placement in 2-D. [Figure 94](#) and [Figure 95](#) show the placement in 3-D.

### 12.1.6 Designs Rules and Guidance

When starting to route nets it is best to start with 4 mil clearance spacing. The designer may have to adjust the 4mil clearance to 3.5 mil when fanning out the top layer routes. With the routing of the top layer having a tight clearance, it is recommended to have the layout grid snapped to 1 mil. For certain routes on the layout done in this guide, the grid snap was set to 0.1 mil. For component spacing this design used 20 mil clearance between components. The silk screen around certain passive components may be deleted to allow for closer placement of components.

### 12.1.7 Routing PP\_HV, PP\_EXT, PP\_5V0, and VBUS

On the top layer, create pours for PP\_HV, PP\_5V0 and VBUS to extend area to place 8 mil hole and 16 mil diameter vias to connect to the bottom layer. A minimum of 4 vias is needed to connect between the top and bottom layer. For the bottom layer, place pours that will connect the PP\_HV, PP\_5V0, and VBUS capacitors to their respective vias. The external FETS must also be connected through pours and place vias for the external FET gates. For 5 A systems, special consideration must be taken for ensuring enough copper is used to handle the higher current. For 0.5 oz copper top or bottom pours with 0.5-oz plating will require approximately a 120-mil pour width for 5-A support. When routing the 5 A through a 0.5 oz internal layer, more than 200 mil will be required to carry the current. [Figure 96](#) and [Figure 97](#) show the pours used in this example.

### 12.1.8 Routing Top and Bottom Passive Components

The next step is to route the connections to the passive components on the top and bottom layers. For the top layer only CC1 and CC2 capacitors will be placed on top. Routing the CC1 and CC2 lines with a 8 mil trace will facilitate the needed current for supporting powered Type C cables through VCONN. For more information on VCONN please refer to the Type C specification. [Figure 98](#) shows how to route to the CC1 and CC2 to their respective capacitors. For capacitor GND pin use a 10 mil trace if possible. This particular system support Dead Battery, which has RPD\_G1/2 connected to CC1/2.

The top layer pads will have to be connected the bottom placed component through Vias (8 mil hole and 16 mil diameter recommended). For the VIN\_3V3, VDDIO, LDO\_3V3, LDO\_1V8A, LDO1V8D, LDO\_BMC, and VOUT\_3V3 use 6mil traces to route. For PP\_CABLE route using an 8 mil trace and for all other routes 4 mil traces may be used. To allow for additional space for routing, stagger the component vias to leave room for routing other signal nets. [Figure 99](#) and [Figure 100](#) show the top and bottom routing. [Table 19](#) provides a summary of the trace widths.

**Table 19. Routing Trace Widths**

ROUTE	WIDTH (mil)
CC1, CC2, PP_CABLE	8



## Layout Guidelines (continued)

**Table 19. Routing Trace Widths (continued)**

ROUTE	WIDTH (mil)
LDO_3V3, LDO_1V8A, LDO_1V8D, LDO_BMC, VIN_3V3, VOUT_3V3, VDDIO, HV_GATE1, HV_GATE2	6
Component GND	10

### 12.1.9 Void Via Placement

The void under the TPS65982 is used to via out I/O and for thermal relief vias. A minimum of 6 vias must be used for thermal dissipation to the GND planes. The thermal relief vias must be placed on the right side of the device by the power path. [Figure 101](#) shows the recommended placement of the vias. Note the areas under the void where vias are not placed. This is done to allow the external FET gate drive and sense pins to route under the TPS65982 through an inner layer. [Figure 102](#) shows the top layer GND pour to connect the vias and GND balls together.

### 12.1.10 Top Layer Routing

Once the components are routed, the rest of the area can be used to route all of the additional I/O. After all nets have been routed place a polygonal pour under to connect the TPS65982 GND pins to the GND vias. Refer to [Figure 103](#) for the final top routing and GND pour.

### 12.1.11 Inner Signal Layer Routing

The inner signal layer is used to route the I/O from the internal balls of the TPS65982 and the external FET control and sensing. [Figure 104](#) shows how to route the internal layer.

### 12.1.12 Bottom Layer Routing

The bottom layer has most of the components placed and routed already. Place a polygon pour to connect all of the GND nets and vias on the bottom layer, refer to [Figure 105](#).

## 12.2 Layout Example

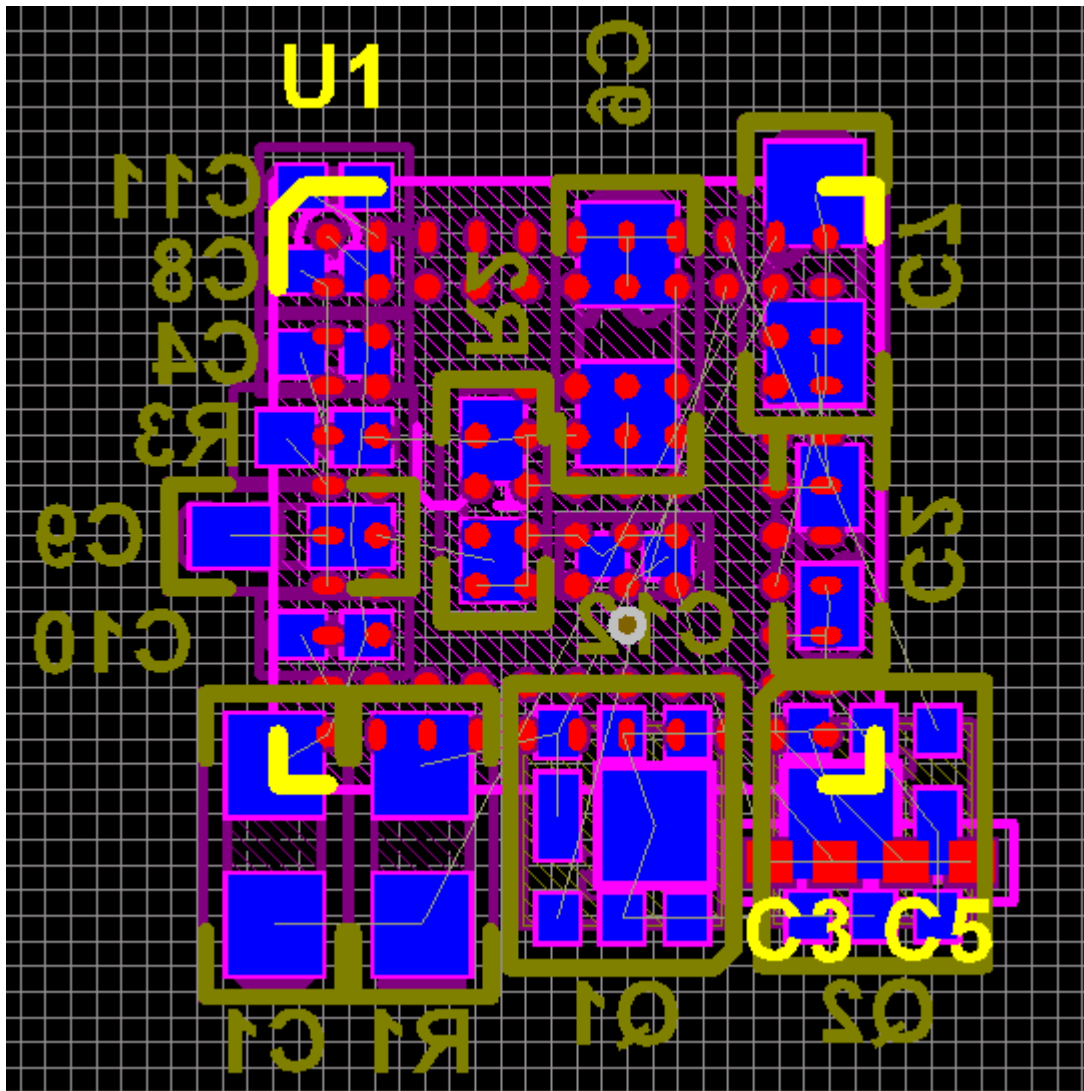


Figure 92. Example Layout (Top View in 2-D)

Layout Example (continued)

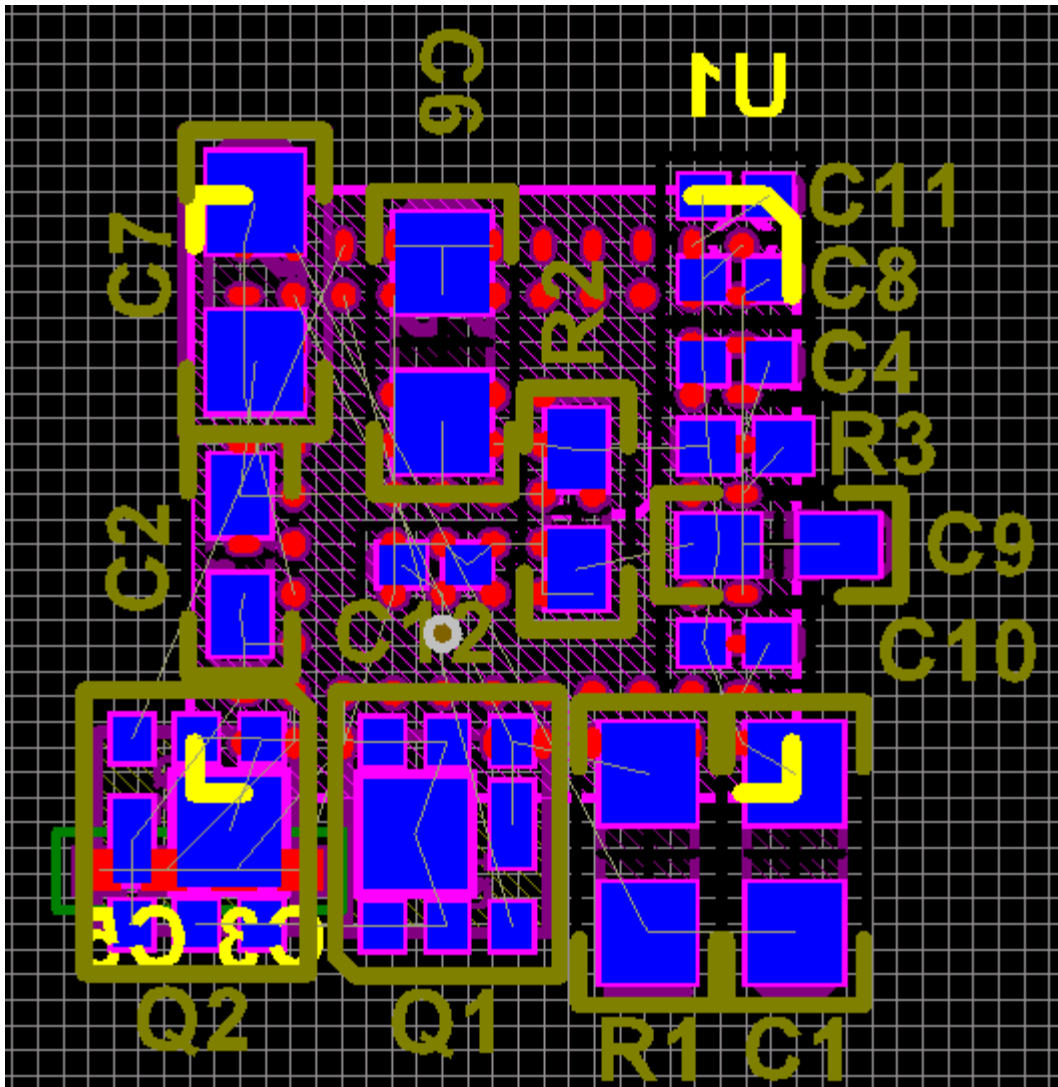
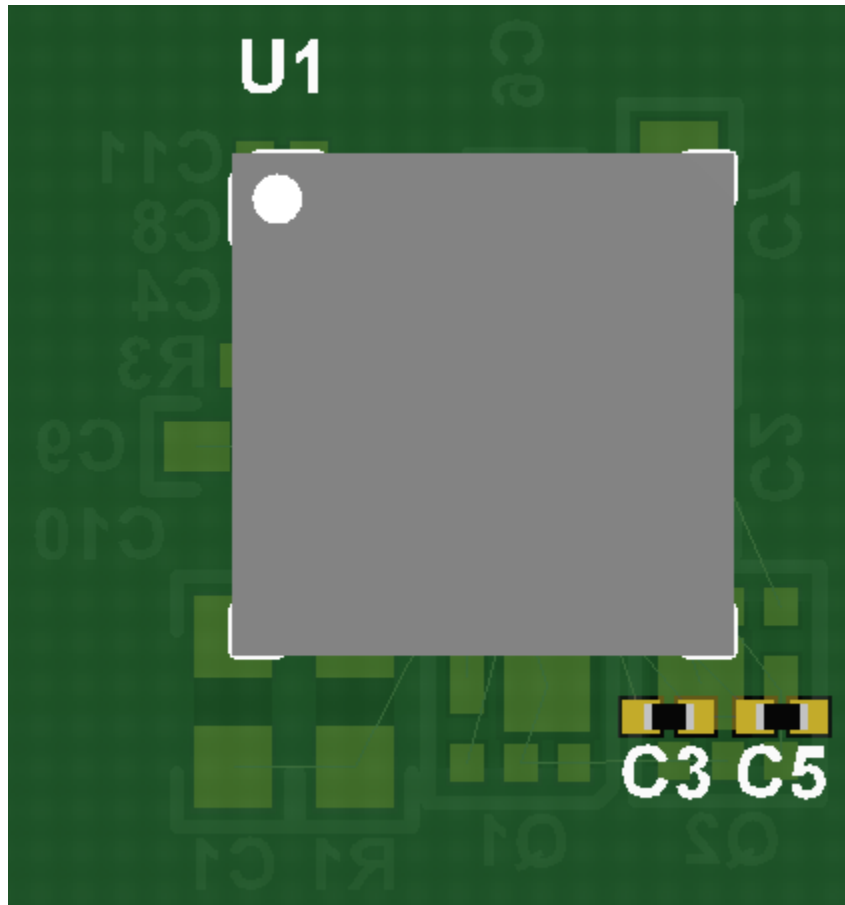


Figure 93. Example Layout (Bottom View in 2-D)

**Layout Example (continued)**



**Figure 94. Example Layout (Top View in 3-D)**

Layout Example (continued)

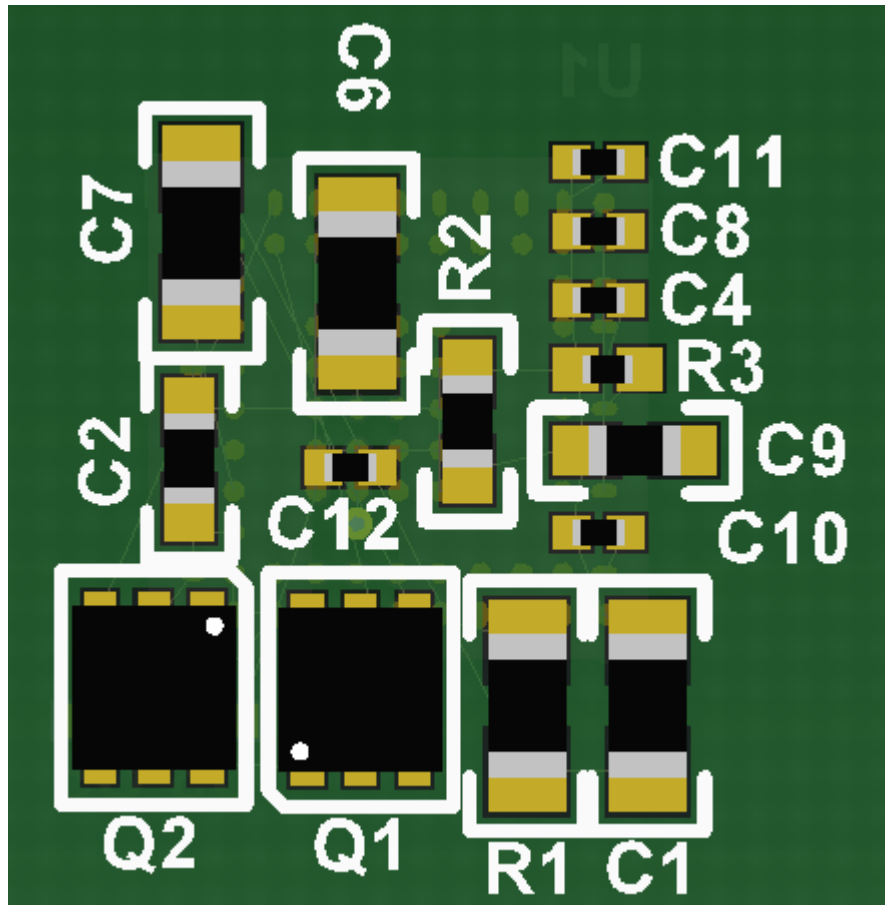


Figure 95. Example Layout (Bottom View in 3-D)

Layout Example (continued)

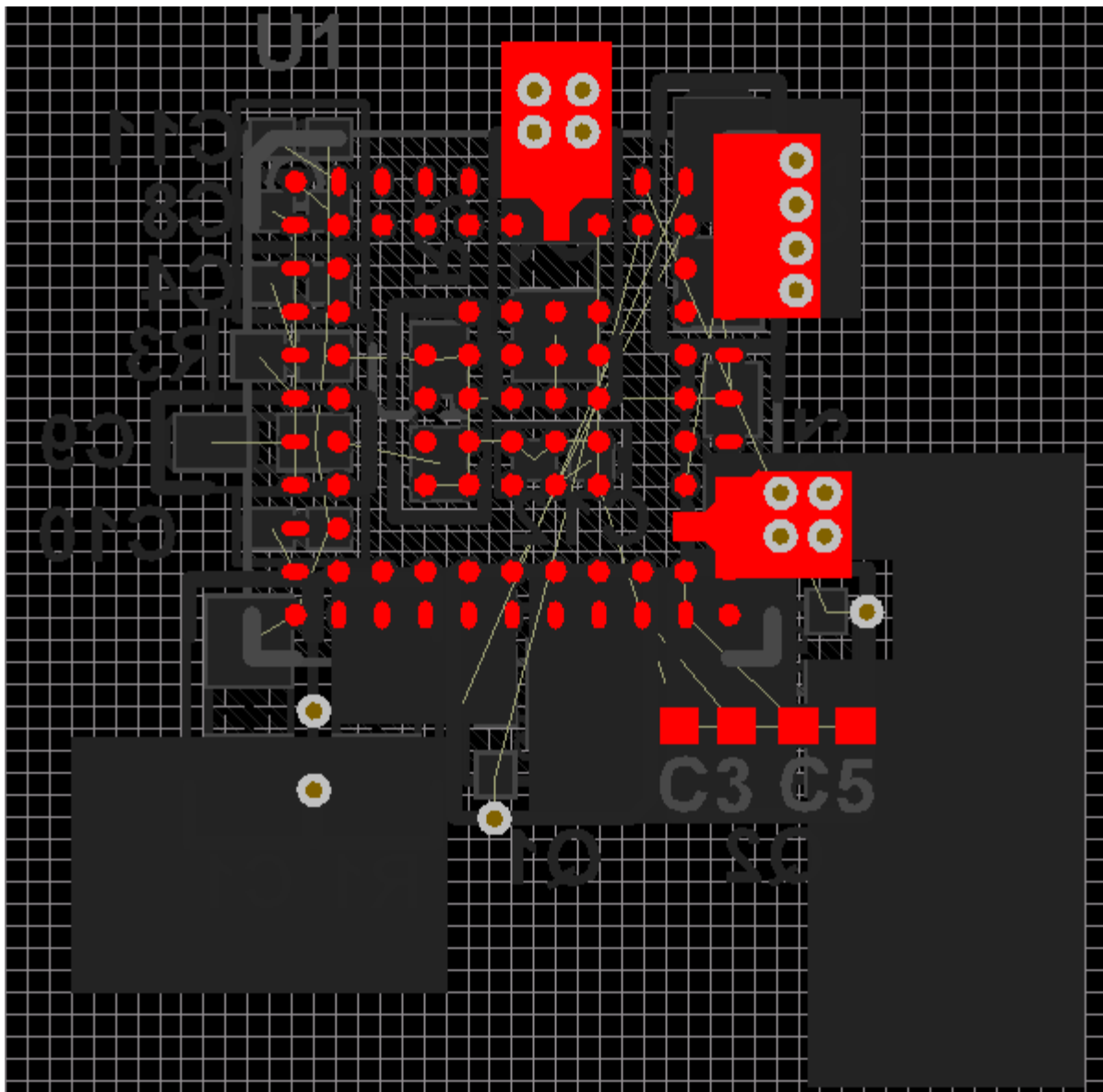


Figure 96. Top Polygonal Pours

Layout Example (continued)

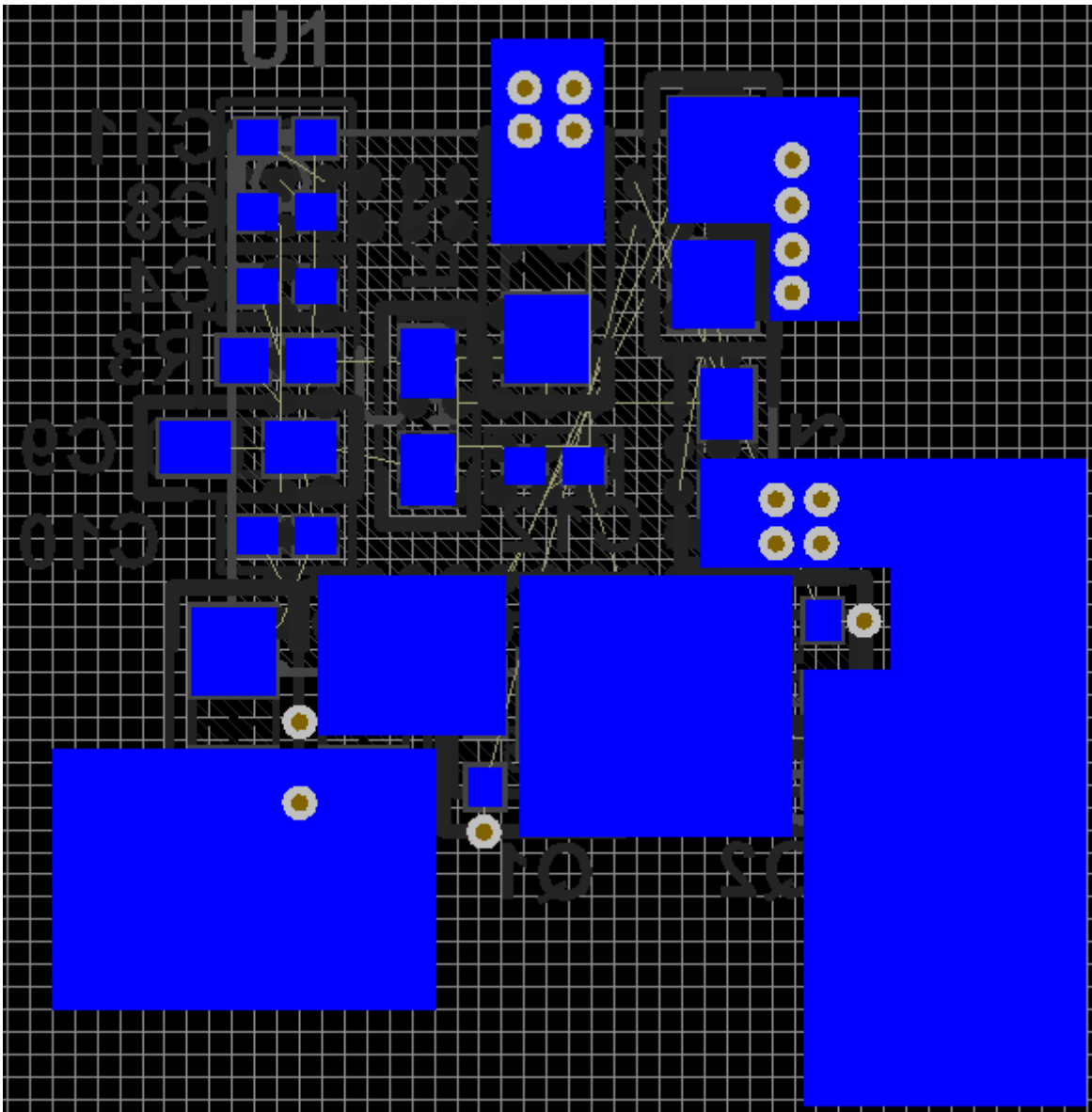


Figure 97. Bottom Polygonal Pours

Layout Example (continued)

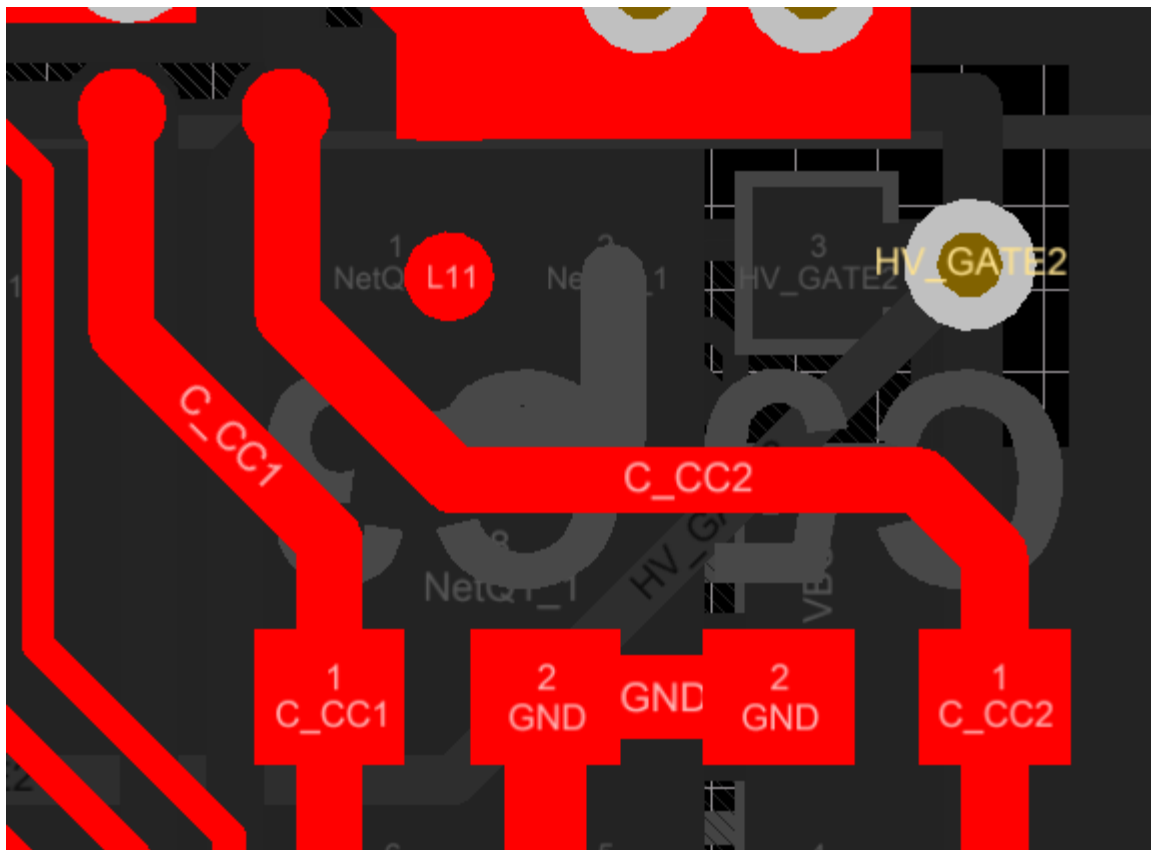


Figure 98. CC1 and CC2 Capacitor Routing



### Layout Example (continued)

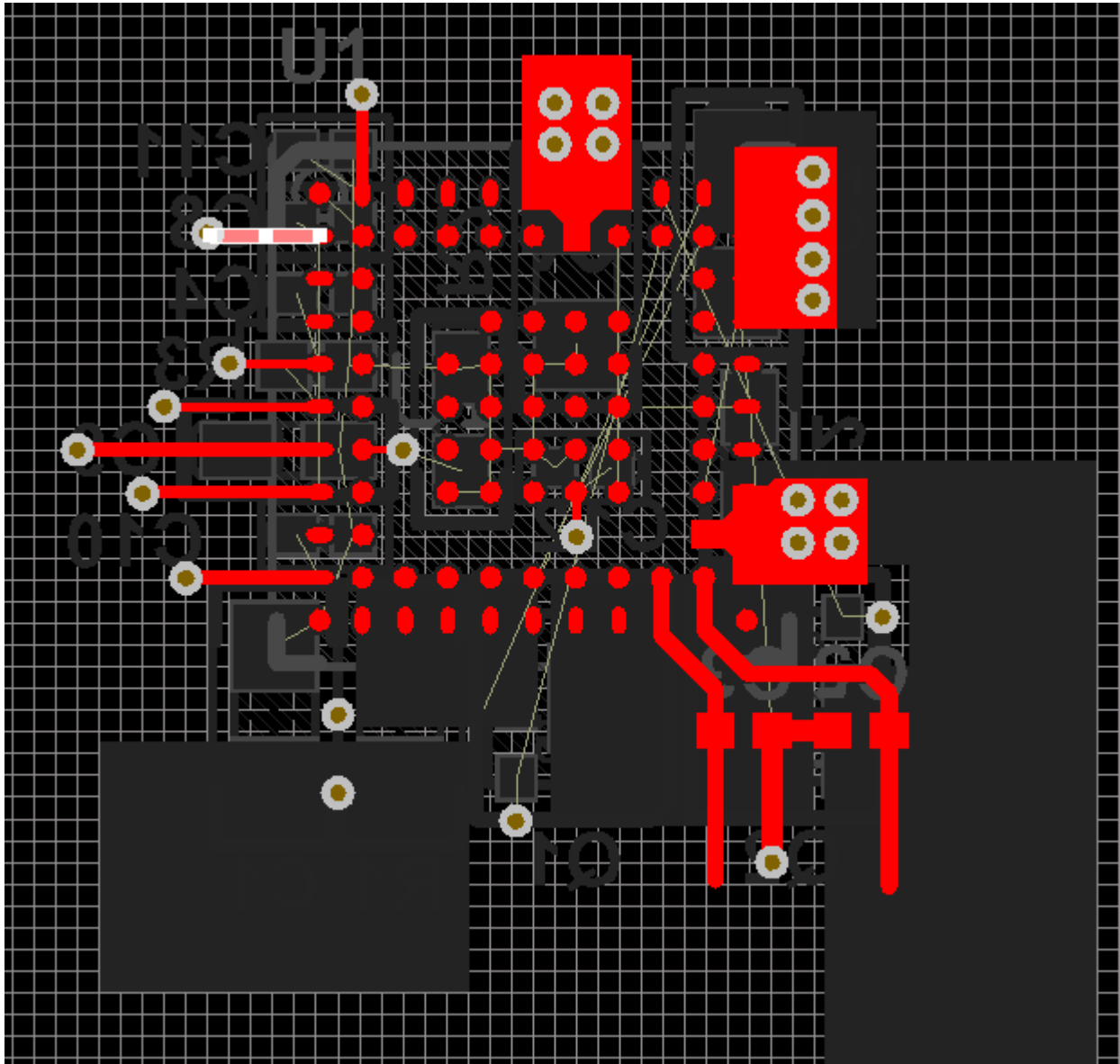
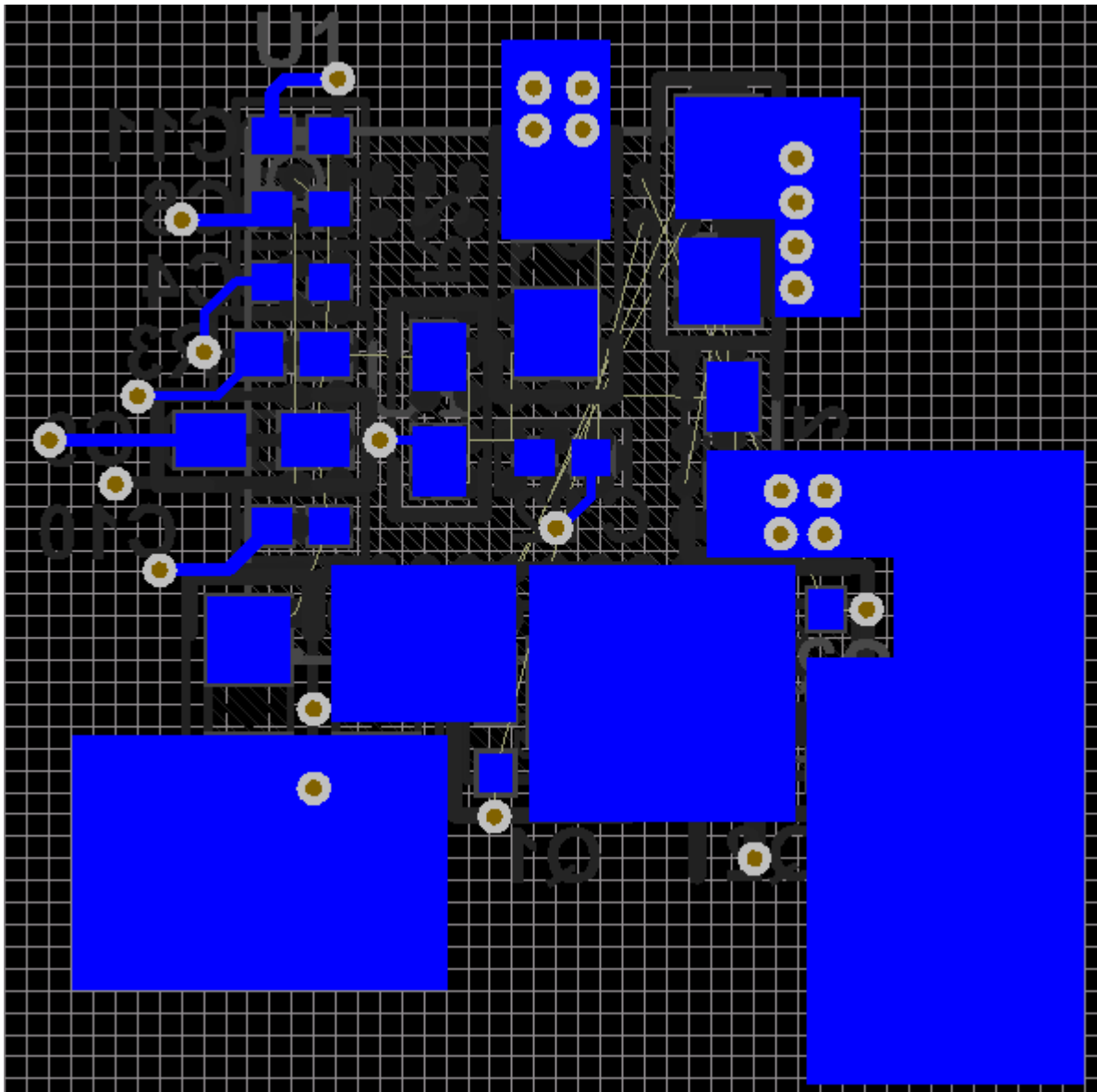


Figure 99. Top Layer Component Routing

**Layout Example (continued)**



**Figure 100. Bottom Layer Component Routing**

Layout Example (continued)

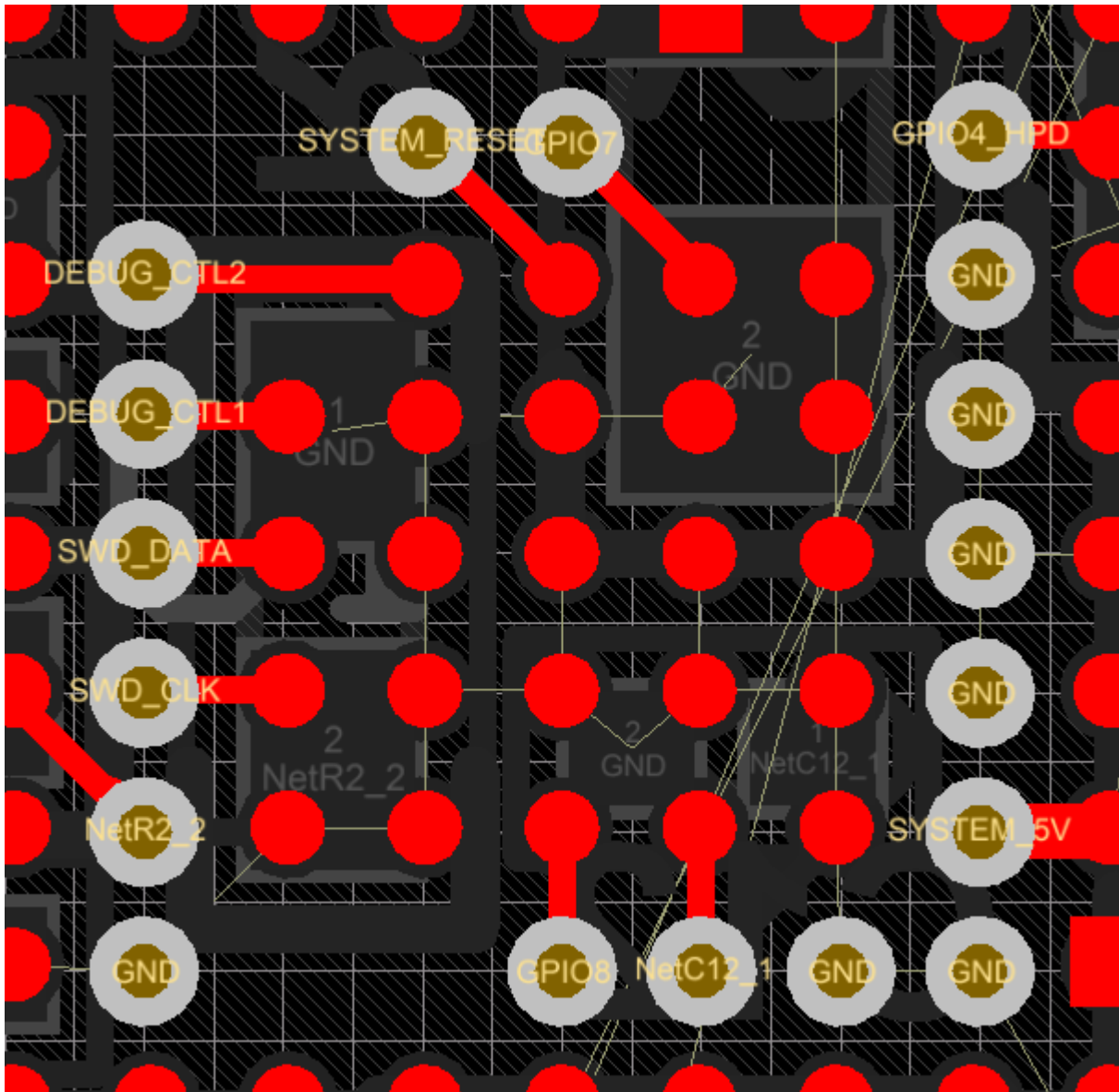
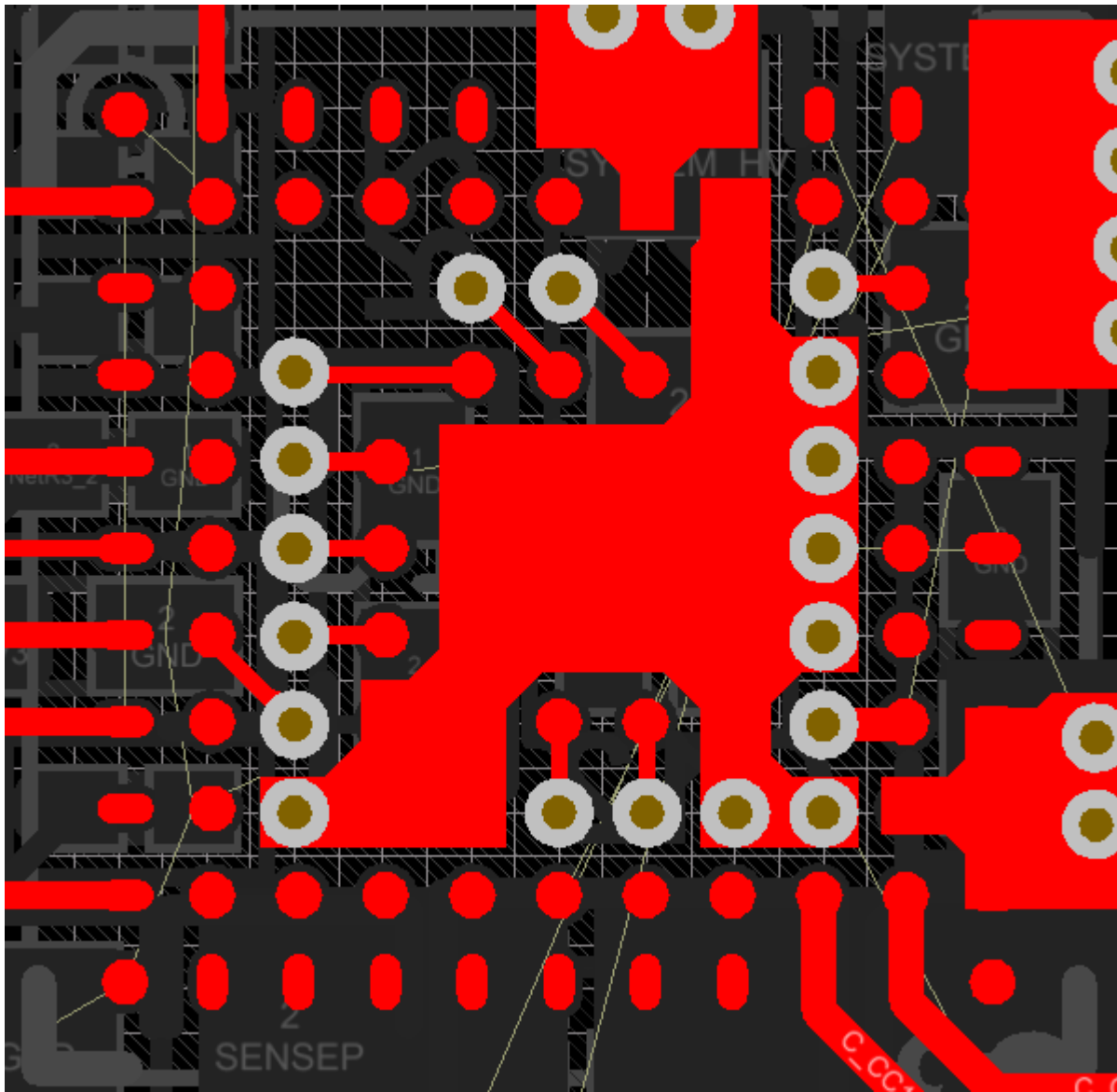


Figure 101. Void Via Placement

**Layout Example (continued)**



**Figure 102. Top Layer GND Pour**

Layout Example (continued)

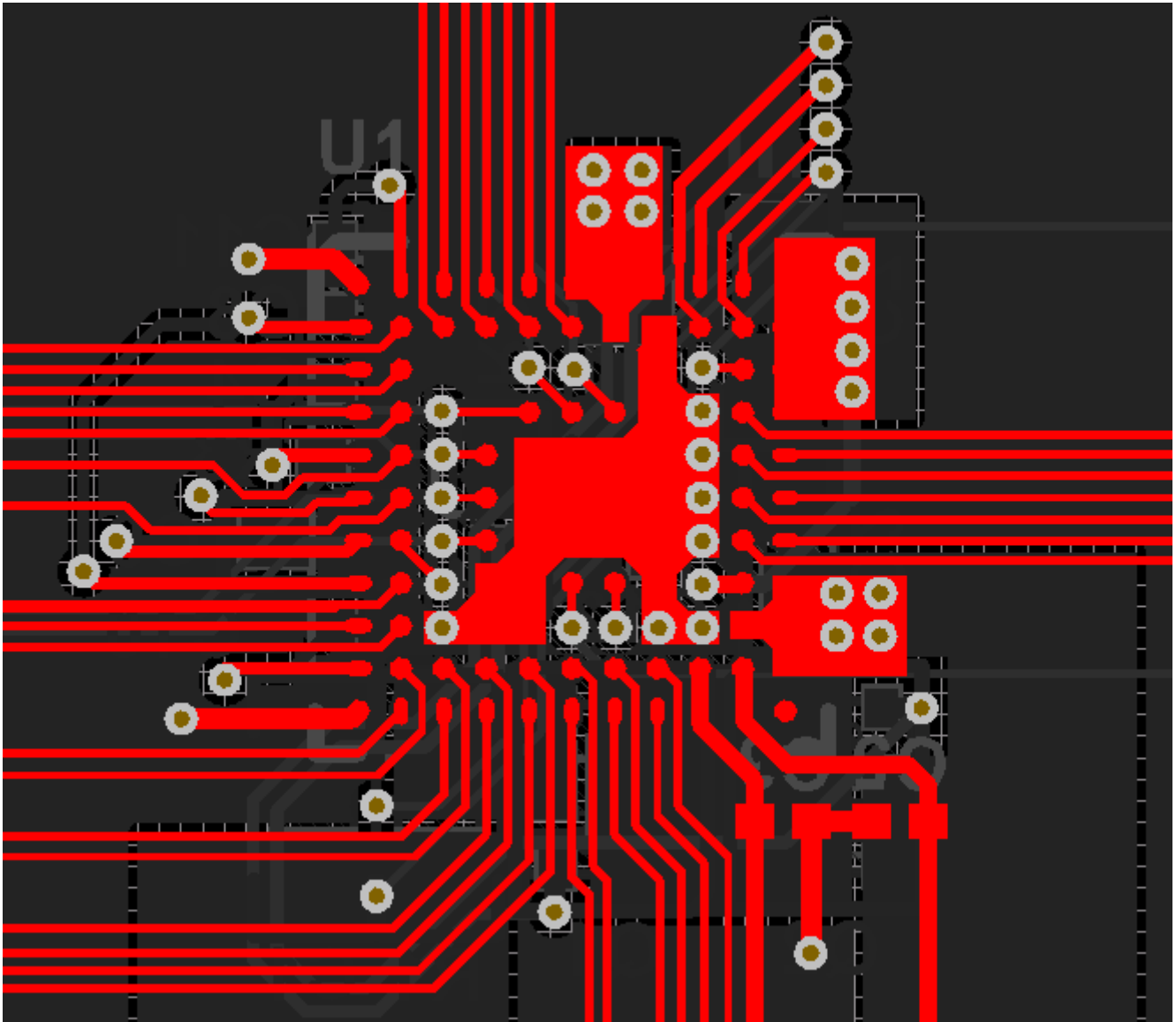
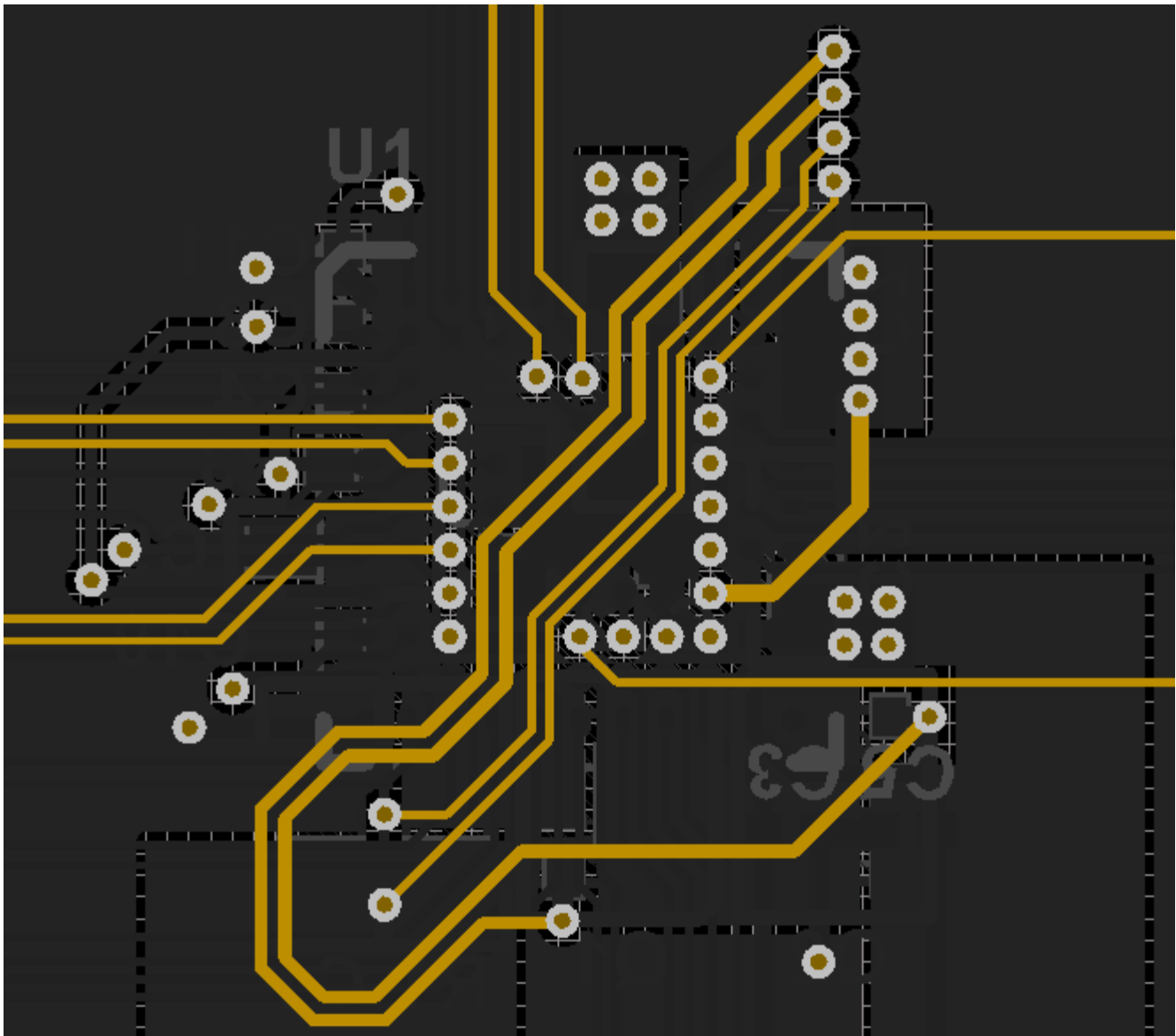


Figure 103. Final Routing and GND Pour (Top Layer)

**Layout Example (continued)**



**Figure 104. Final Routing (Inner Signal Layer)**

Layout Example (continued)

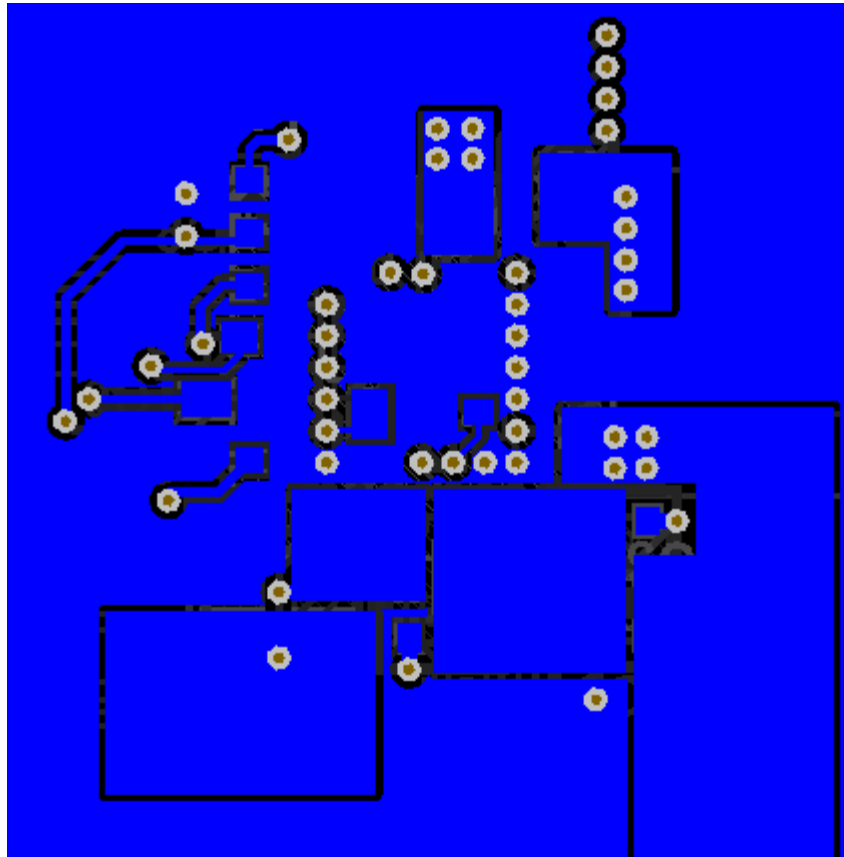


Figure 105. Final Routing (Bottom Layer)

## 13 器件和文档支持

### 13.1 器件支持

#### 13.1.1 开发支持

对于 IBIS 模型，请参阅 [TPS65982ZQZR IBIS 模型 \(SLVMAY7\)](#)

### 13.2 文档支持

#### 13.2.1 相关文档

请参阅如下相关文档：

- 《USB 供电规范，修订版 2.0，版本 1.2》（2016 年 3 月 25 日）
- 《USB Type-C 规范，修订版 1.2》（2016 年 3 月 25 日）
- 《USB 电池充电规范，修订版 1.2》（2010 年 12 月 7 日）
- 《TPS65981、TPS65982 和 TPS65986 固件用户指南》（文献编号：SLVUAH7）
- 《TPS65981、TPS65982 和 TPS65986 主机接口技术参考手册》（文献编号：SLVUAN1）
- W25Q80DV 数据表，《具有双 SPI 和四 SPI 的 8Mb、16Mb 和 32Mb 串行闪存》
- NSR20F30NXT5G 数据表，《肖特基势垒二极管》

### 13.3 接收文档更新通知

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### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.


This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65982ABZBHR	ACTIVE	NFBGA	ZBH	96	2500	RoHS & Green	Call TI	Level-3-260C-168 HR	-10 to 85	TPS65982 AB	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

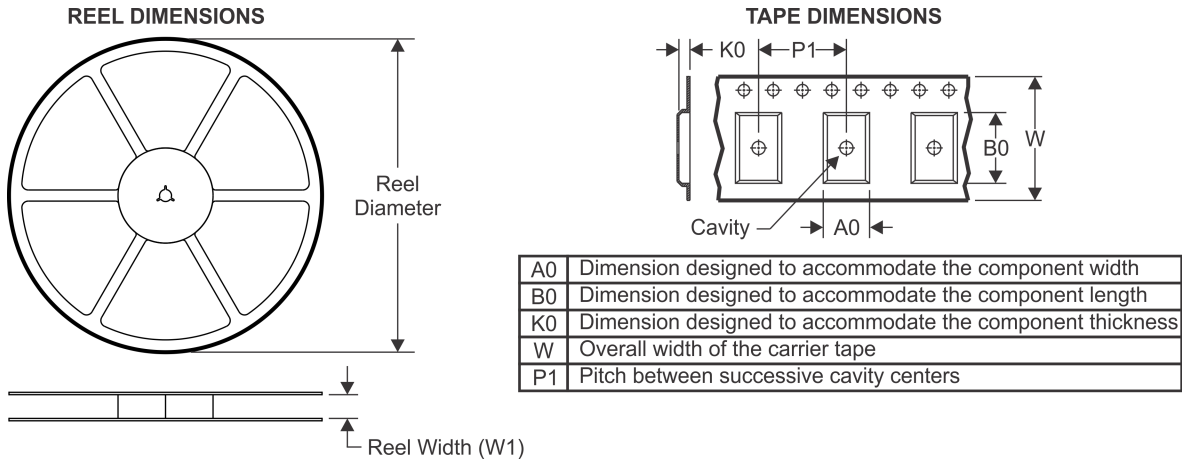
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

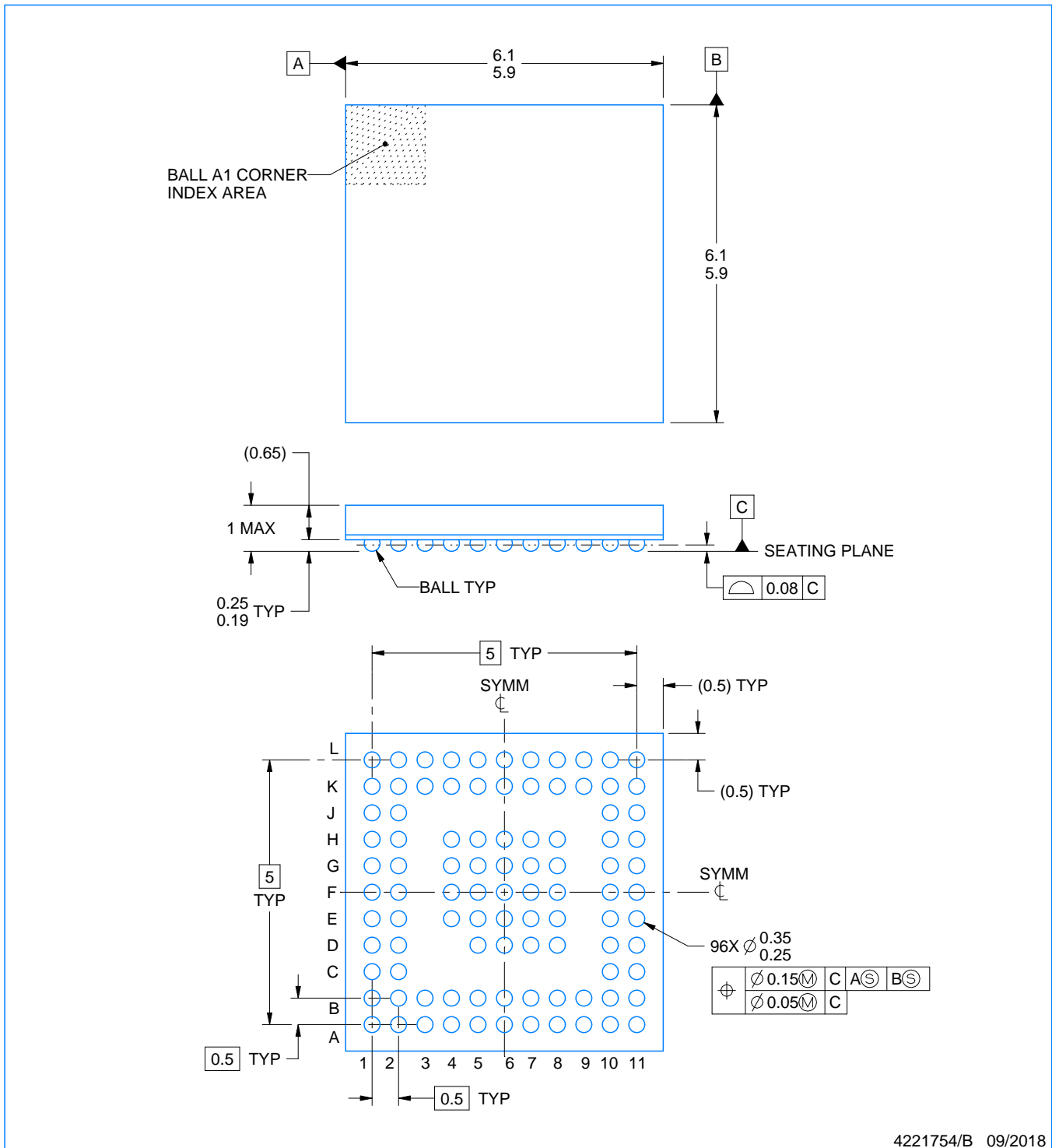
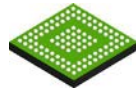
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65982ABZBHR	NFBGA	ZBH	96	2500	330.0	16.4	6.3	6.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65982ABZBHR	NFBGA	ZBH	96	2500	336.6	336.6	31.8



NOTES:

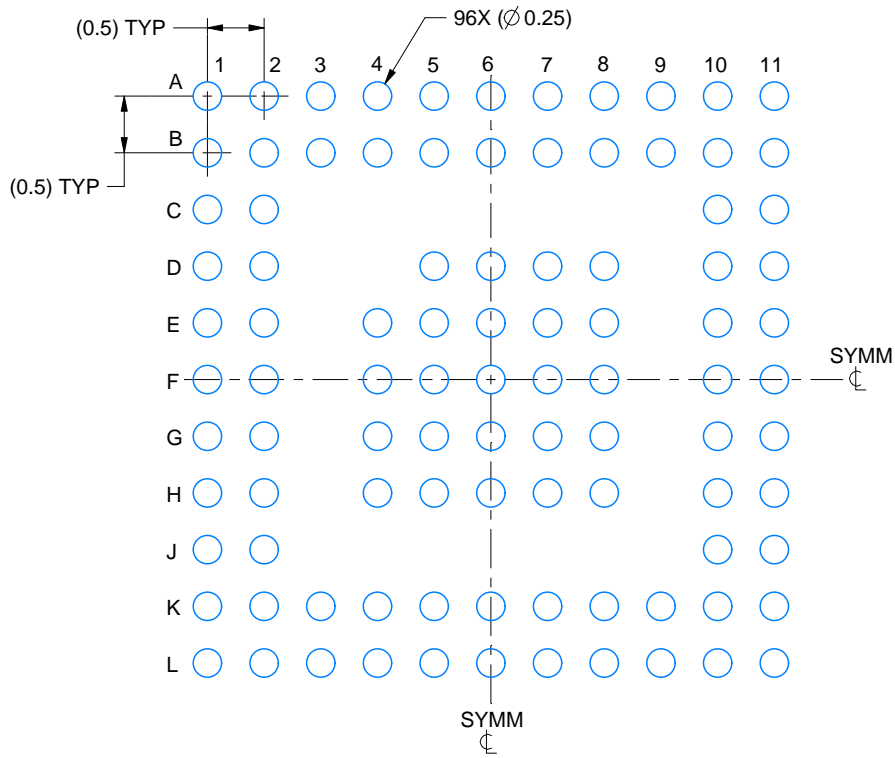
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

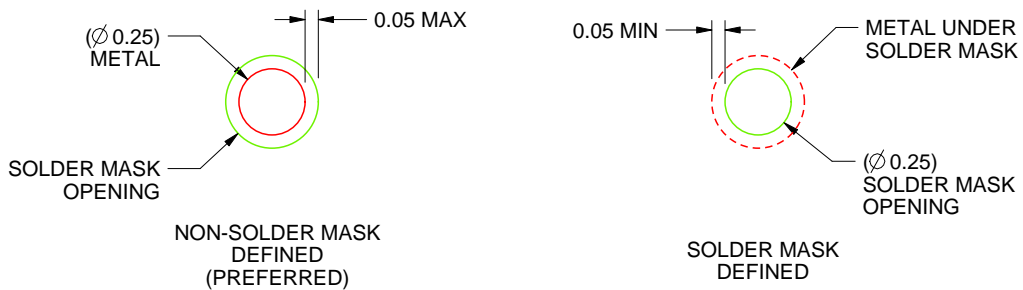
ZBH0096A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS  
NOT TO SCALE

4221754/B 09/2018

NOTES: (continued)

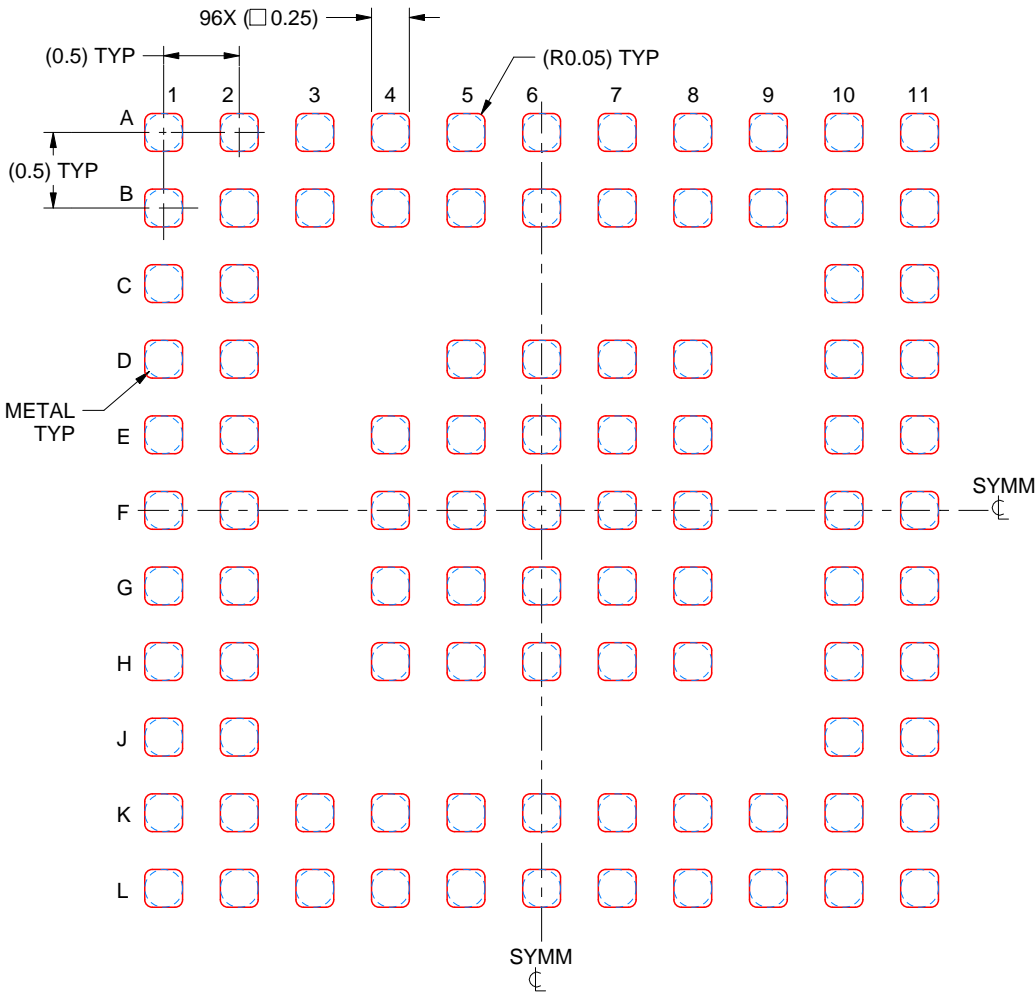
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

EXAMPLE STENCIL DESIGN

ZBH0096A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:20X

4221754/B 09/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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