# Applications Note: SY7701

## High Efficiency 500kHz, 25V PWM Controller For WLED backlight application

## General Description

SY7701 is a current mode boost controller targeted for WLED backlight application. The device has a wide input voltage range of 3V to 25V. The external compensation provides flexible adjustment of control loop for different applications. The internal low side driver is capable of sourcing 1.5A and sinking 3A current.

## Ordering Information

SY7701 □(□□)□

Temperature Code
Package Code
Optional Spec Code

| Ordering Number | Package type | Note |
|---|---|---|
| SY7701DBC | DFN3x3-10 | ---- |
| SY7701FHC | SOP10 | |

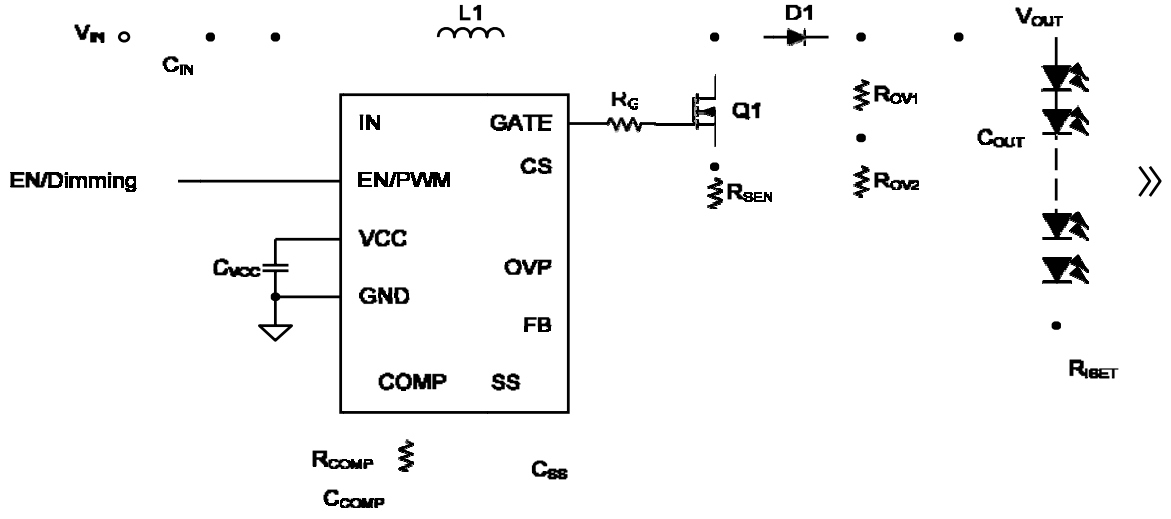
## Features

- Input voltage range 3V to 25V
- 500kHz fixed switching frequency
- 100Hz~1kHz dimming frequency
- 10%~100% dimming duty cycle @200Hz dimming frequency
- External compensation
- Integrated low side driver: 1.5A sourcing and 3A sinking
- OVP, OTP functions
- RoHS Compliant and Halogen Free
- Compact package: DFN3x3-10,SOP10

## Applications

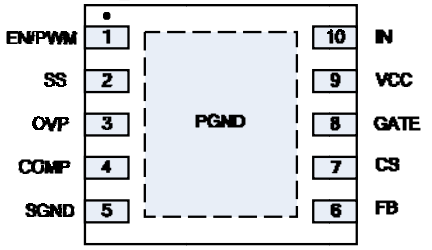
- Monitor LCD Panel Backlight
- TV LCD Panel Backlight
- LED Lighting

## Typical Applications

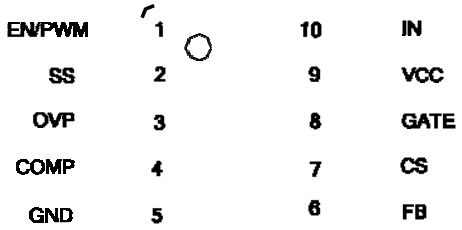



**SY7701**
**Figure 1. Schematic Diagram**

## Pinout (top view)




(DFN3x3-10)




(SOP10)

**Top Mark: GO*xyz* for SY7701DBC** (Device code:GO, ***x=year code, y=week code, z= lot number code***)
**AEY*xyz* for SY7701FHC** (Device code:AEY, ***x=year code, y=week code, z= lot number code***)

| Pin Name | Pin Number | Pin Description |
|---|---|---|
| IN | 10 | Input pin. Decouple this pin to GND pin with at least 1uF ceramic capacitor |
| VCC | 9 | 5V Internal LDO output from VIN. Connect a 4.7 uF capacitor from this pin to GND |
| GATE | 8 | Driver pin. Connect to the gate of power MOSFET |
| CS | 7 | Current sense pin. Connect an external current sensing resistor $R_S$ from this pin to GND. The voltage on this pin is used to provide mosfet current feedback in the control loop and cycle by cycle peak current limit. Peak current limit is triggered when the sensed voltage plus the slope compensation exceed 340mV |
| FB | 6 | Feedback pin. The LED current equals to: $I_{LED}=\frac{100mV}{R_{ISET}}$ |
| GND | 5(Exposed Paddle) | Ground pin |
| COMP | 4 | External compensation pin. Connect RC network from this pin to GND to compensate the control loop |
| OVP | 3 | Over Voltage Protection input pin.The OVP set point equals to : $V_{OVP}=\frac{1}{R_{OV2}}\left(R_{OV1}+R_{OV2}\right)$ |
| SS | 2 | Soft start pin. Connect a capacitor from this pin to GND to program the soft start time |
| EN/PWM | 1 | Enable and PWM dimming input pin. Pull it high to turn on the chip. Do not float this pin |

## Absolute Maximum Ratings (Note 1)

IN,EN----------V
GATE---------- VCC+0.3V
All other pins----------V
Power Dissipation, $P_D$ @ $T_A$ = 25°C, DFN3x3-10,SOP10 ---------- 2.6W/TBD
Package Thermal Resistance (Note 2)
$\theta_{JA}$ ----------38°C/W/TBD
$\theta_{JC}$----------130°C/W/TBD
Junction Temperature Range---------- 125°C
Lead Temperature (Soldering, 10 sec.)----------260°C
Storage Temperature Range---------- 65°C to 150°C

## Recommended Operating Conditions (Note 3)

IN ---------- V to 25V
Junction Temperature Range----------40°C to 125°C
Ambient Temperature Range ---------- 40°C to 85°C

## Electrical Characteristics

($V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise specified)

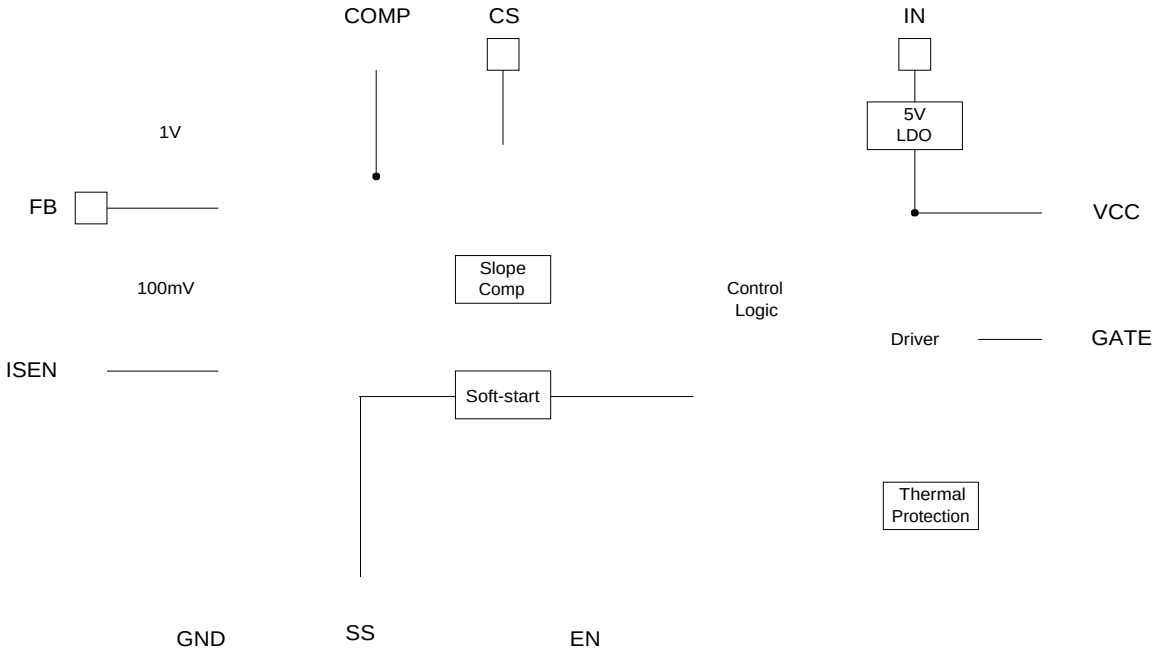
| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 3 | | 25 | V |
| Quiescent Current | $I_Q$ | $V_{OVP}$=1.1V | | 170 | | uA |
| Shutdown Current | $I_{SHDN}$ | EN=0 | | 0.1 | | uA |
| OVP Threshold | $V_{OVP}$ | | 0.98 | 1 | 1.02 | V |
| FB Input Current | $I_{FB}$ | | -50 | | 50 | nA |
| Feedback Reference Voltage | $V_{REF}$ | | 98 | 100 | 102 | mV |
| Internal Slope Compensation | $V_{SLOPE}$ | | | 40 | | mV/uS |
| Gate Driver Output Peak Current | $I_{SOURCE}$ | | | 1.5 | | A |
| | $I_{SINK}$ | | | 3 | | A |
| EN Rising Threshold | $V_{ENH}$ | | 1.5 | | | V |
| EN Falling Threshold | $V_{ENL}$ | | | | 0.4 | V |
| Input UVLO threshold | $V_{UVLO}$ | | | | 2.9 | V |
| UVLO hysteresis | $V_{HYS}$ | | | 0.3 | | V |
| Oscillator Frequency | $F_{OSC}$ | | | 500 | | kHz |
| Min On Time | | | | 200 | | ns |
| Min Off Time | | | | 200 | | ns |
| Internal LDO Output | $V_{VCC}$ | $V_{IN}$=5.5V | 4.9 | 5 | 5.1 | V |
| Thermal Shutdown | $T_{SD}$ | | | 150 | | ℃ |
| Thermal Hysteresis | $T_{HYST}$ | | | 20 | | ℃ |

**Note 1**: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

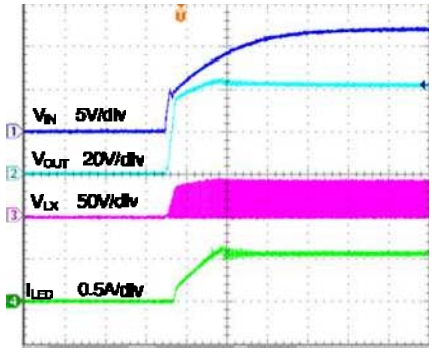
**Note 3:** The device is not guaranteed to function outside its operating conditions.

## Block Diagram



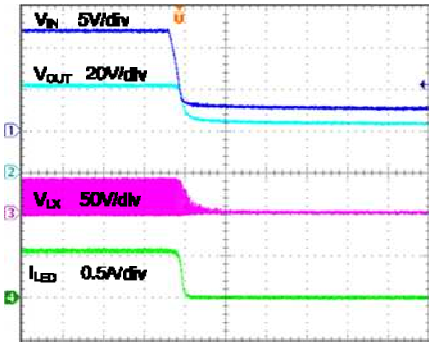
## Typical Performance Characteristics

Startup from $V_{IN}$
($V_{IN}$=12V, 10 LED in series, $I_{LED}$=560mA)



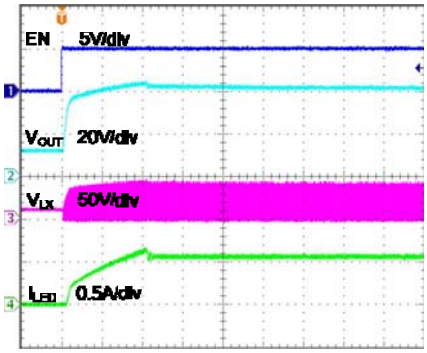

Time (2mS/div)

Shutdown from $V_{IN}$
($V_{IN}$=12V, 10 LED in series, $I_{LED}$=560mA)



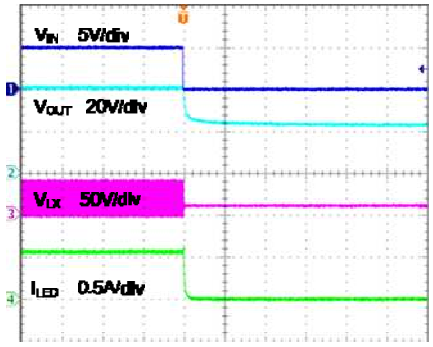

Time (2mS/div)

Startup from Enable
($V_{IN}$=12V, 10 LED in series, $I_{LED}$=560mA)



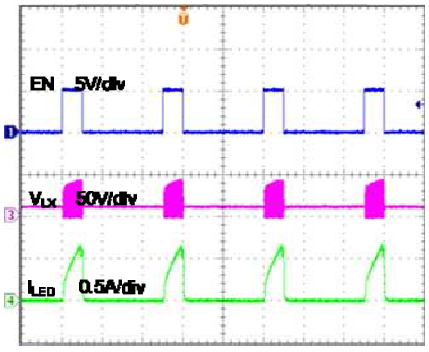

Time (1mS/div)

Shutdown from Enable
($V_{IN}$=12V, 10 LED in series, $I_{LED}$=560mA)



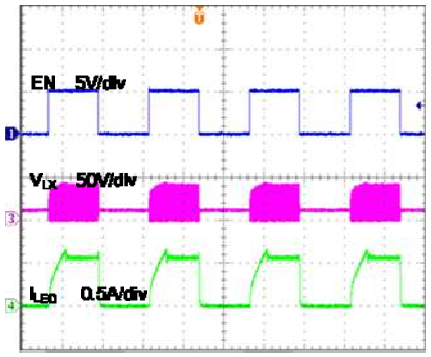

Time (1mS/div)

Dimming
($V_{IN}$=12V, 10 LED in series,
$I_{LED}$=560mA, $f_{PWM}$=100Hz, Duty=20%)




Time (4mS/div)

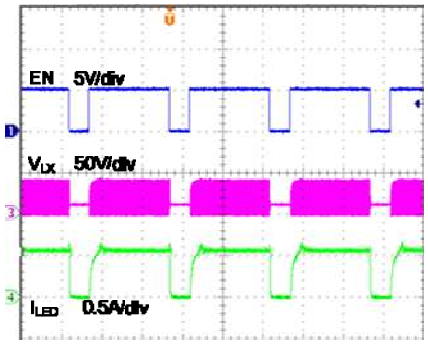
Dimming
($V_{IN}$=12V, 10 LED in series,
$I_{LED}$=560mA, $f_{PWM}$=100Hz, Duty=50%)




Time (4mS/div)

Dimming

($V_{IN}$=12V, 10 LED in series,
$I_{LED}$=560mA, $f_{PWM}$=100Hz, Duty=80%)




Time (4mS/div)

# Operation

SY7701 is a boost controller targetted for white LED lighting. It integrates a low side driver which is capable of sourcing 1.5A and sinking 3A current. External compensation can supply a flexible adjustment of control loop under different applications. OVP function can protect the part from LED open event, OVP point can be programmed using a voltage divider.

# Applications Information

**LED current programming resister $R_{ISET}$**

LED current is programmed by a resistor which is in series with the LED string. LED current is calculated as:
$I_{LED}$=100mV/Riset

LED may be shorted if the current is higher than its rating. SY7701 will fold back the LED current from 100% to 30% when the OVP pin voltage changes from 0.5V to 0.15V. For typical application, it is recommended the OVP point is less than twice of the LED string voltage

**OVP point programming divider $R_{OV1}$ and $R_{OV2}$:**

Choose proper resistor $R_{OV1}$ and $R_{OV2}$ to program the output voltage OVP point. $V_{OVP}$ is calculated as:
$V_{OVP}$=1V*(1+$R_{OV1}$/$R_{OV2}$)

Make sure the resister will not exceed its power rating when output voltage reaches the OVP point.

**Peak Current Sense Resistor**

An external sensing resistor Rsen is used to sense the current flow through the MOSFET. The sensed voltage is for peak current mode control and cycle by cycle peak current limit. Peak current limit will be triggered when the voltage on CS pin plus the internal slop compensation exceed 340mV, which is the typical clamping voltage of the PWM comparator. It is desirable to make the maximum value of sensing voltage plus the slope compensation to be about 70% of the clamping voltage during normal operation. Thus,

$$Rs=\frac{70\% \times 0.34\text{-}Vslope\times D\times Ts}{I_{PEAK}}$$

Vslope is the slew rate of the internal compensation, $I_{PEAK}$ is the peak current through MOSFET.

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**Inductor L:**

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L=\left(\frac{V_{IN}}{V_{OUT}}\right)^2\frac{(V_{OUT}-V_{IN})}{F_{SW}\times I_{OUT,MAX}\times 40\%}$$

where $F_{SW}$ is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY7701 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN}>\left(\frac{V_{OUT}}{V_{IN}}\right)\times I_{OUT\_MAX}+\frac{V_{IN}(V_{OUT}-V_{IN})}{2\times F_{SW}\times L\times V_{OUT}}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

**Input capacitor $C_{IN}$:**

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS}=\frac{V_{IN}\cdot(V_{OUT}-V_{IN})}{2\sqrt{3}\cdot L\cdot F_{SW}\cdot V_{OUT}}$$

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by $C_{IN}$, and IN/GND pins.

**Output capacitor $C_{OUT}$:**

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. Voltage rating of the

capacitor should be carefully selected to at least over the programmed OVP point.

**Layout Design:**

To minimize noise problem, attention should be paid to the PCB layout:.

1) The internal LDO output capacitor $C_{VCC}$ should be put as close as possible to the VCC pin and GND pin.

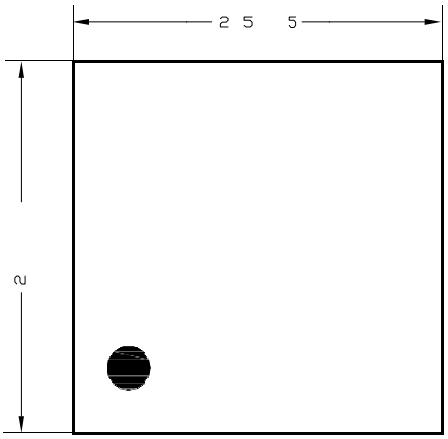
2) The input capacitor $C_{IN}$ should be put as close as possible to the IN pin and GND pin.

3) The loop formed by inductor L1, Power MOS Q1, output capacitor $C_{OUT}$ and power GND should be small enough to suppress voltage spike on Power MOS when it is turned off.

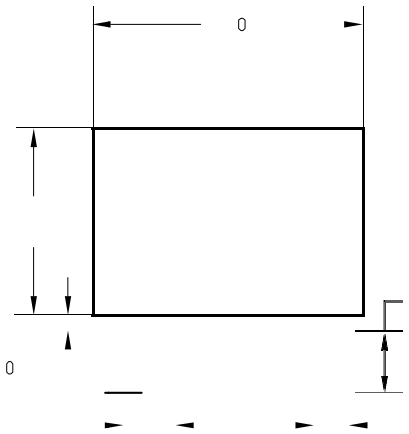
4)Current sense signal generated by $R_{SEN}$ should return to CS PIN as short as possible.

5) Gate drive wire from GATE pin to gate terminal of the Power MOS should be short enough to avoid drive problem.

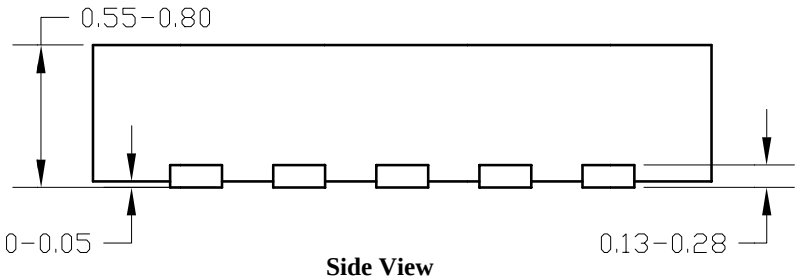
# DFN3x3-10 Package outline



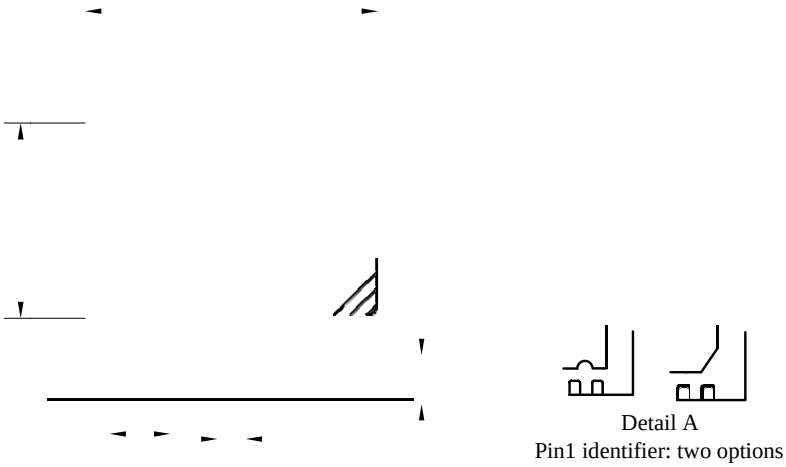

Top View




PCB layout (recommended)




Side View

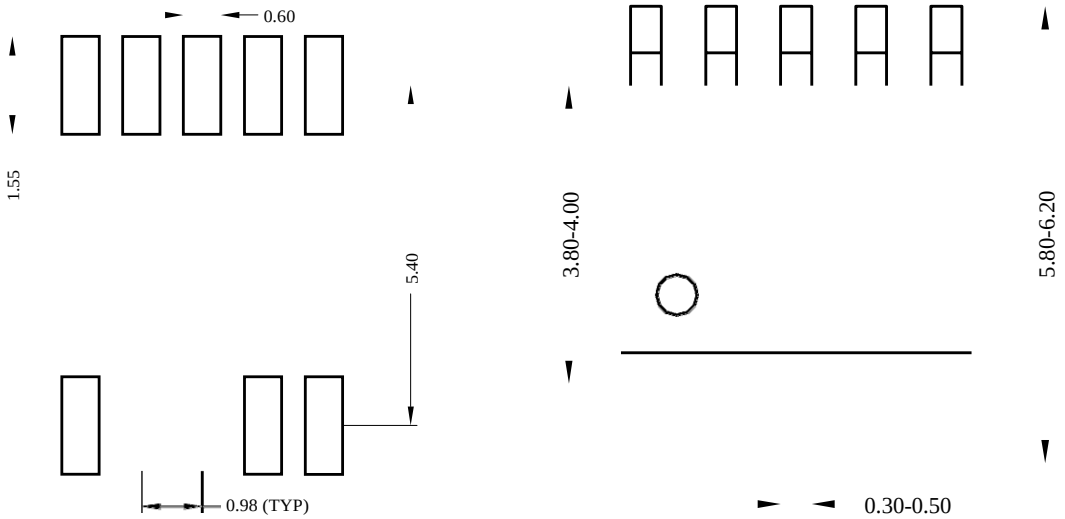


Detail A
Pin1 identifier: two options

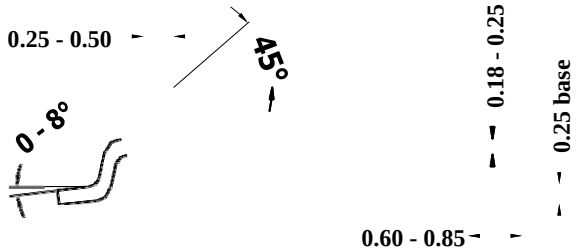
Bottom View

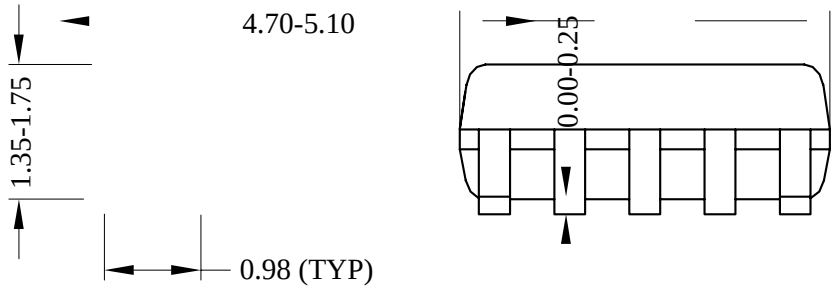
**Notes: All dimensions are in millimeters and exclude mold flash & metal burr.**

# SO10 Package outline & PCB layout design




**Recommended Pad Layout**

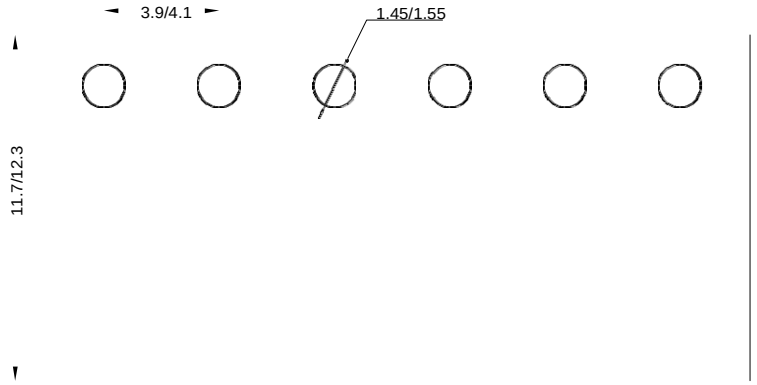



**Notes:** **All dimension in MM**
**All dimension don't not include mold flash & metal burr**

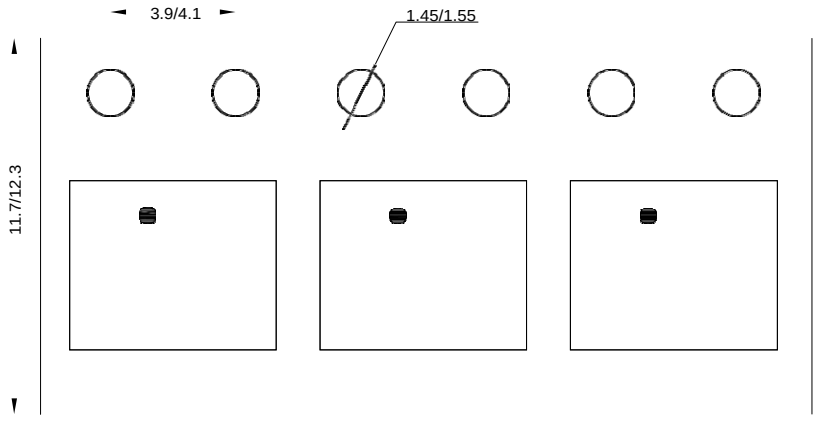
# Taping & Reel Specification

## 1. DFN3x3-10 taping orientation



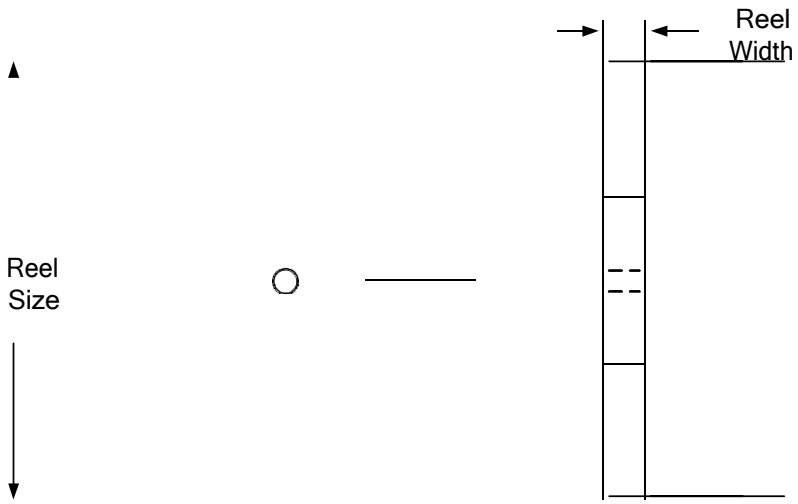

**Feeding direction** ⟶

## SOP10 taping orientation




**Feeding direction** ⟶

## 2. Carrier Tape & Reel specification for packages




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Reel width(mm) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|---|
| DFN3x3 | 12 | 8 | 13" | 12.4 | 400 | 400 | 5000 |
| SO10 | 12 | 8 | 13" | 12.4 | 400 | 400 | 2500 |