DACx0504 Quad, 16-, 14-, 12-bit, SPI voltage output DACs with internal reference

1 Features

- Performance
  - INL: ±1 LSB Maximum at 16-Bit Resolution
  - TUE: ±0.1% of FSR Maximum
- Integrated 2.5 V Precision Internal Reference
  - Initial Accuracy: ±5 mV, Maximum
  - Low Drift: 2 ppm/°C Typical
- High Drive Capability: 20 mA With 0.5 V From Supply Rails
- Flexible Output Configuration
  - User Selectable Gain: 2, 1 or ½
  - Reset to Zero Scale or Midscale
- Wide Operating Range
  - Power Supply: 2.7 V to 5.5 V
  - Temperature: –40˚C to +125˚C
- 50-MHz, SPI-Compatible Serial Interface
  - 4-Wire Mode, 1.7 V to 5.5 V Operation
  - Daisy-Chain Operation
  - CRC Error Check
- Low Power: 0.7 mA/Channel at 5.5 V
- Small Package: 3-mm × 3-mm, 16-Pin WQFN

2 Applications

- Optical Networking
- Wireless Infrastructure
- Industrial Automation
- Data Acquisition Systems

3 Description

The DAC80504, DAC70504, and DAC60504 (DACx0504) are a pin-compatible family of low-power, four-channel, buffered voltage-output, digital-to-analog converters (DACs) with 16-, 14-, and 12-bit resolution. The DACx0504 includes a low drift, 2.5-V internal reference, eliminating the need for an external precision reference in most applications. A user-selectable gain configuration provides full-scale output voltages of 1.25 V (gain = ½), 2.5 V (gain = 1), or 5 V (gain = 2). These devices operate from a single 2.7-V to 5.5-V supply, are specified monotonic, and provide high linearity of ±1 LSB INL.

Communication to the DACx0504 is performed through a 4-wire serial interface that operates at clock rates of up to 50 MHz. The VIO pin enables serial interface operation from 1.7 V to 5.5 V. The DACx0504 flexible interface enables operation with a wide range of industry-standard microprocessors and microcontrollers.

The DACx0504 incorporate a power-on-reset circuit that powers up and maintains the DAC outputs at either zero scale or midscale until a valid code is written to the device. These device consume a low current of 0.7 mA/channel at 5.5 V, making these devices an excellent choice for battery-operated equipment. A per-channel power-down feature reduces the device current consumption to 15 µA.

The DACx0504 is characterized for operation over the temperature range of –40°C to +125°C, and is available in a small, 3-mm × 3-mm QFN package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DACx0504	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Block Diagram

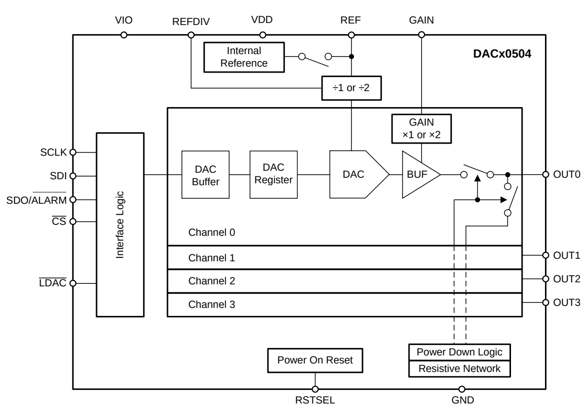


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2018) to Revision C — **Page**

- Added DAC60504 device to data sheet ... 1
- Changed TUE values for DAC70504 in *Electrical Characteristics* ... 7
- Changed Full-scale error values for DAC70504 in *Electrical Characteristics* ... 7
- Changed Gain error values for DAC70504 in *Electrical Characteristics* ... 7
- Changed channel-to-channel dc crosstalk values for DAC70504 in *Electrical Characteristics* ... 8
- Changed reference output drift values for DAC70504 in *Electrical Characteristics* ... 9
- Changed reference thermal hysteresis values for DAC70504 in *Electrical Characteristics* ... 9
- Deleted Figure 58, DAC70504 Solder Heat Reflow Reference Voltage Shift ... 23
- Changed reset value for VERSIONID from 10 to 11 in Table 10, DEVICE ID Field Descriptions ... 31

Changes from Revision A (December 2017) to Revision B — **Page**

- Changed TUE in Features from ±0.14% to ±0.1% ... 1
- Changed Low Drift in Features from 5 ppm/°C to 2 ppm/°C and added DAC80504 ... 1
- Deleted Product Preview for DAC80504 from Device Information ... 1
- Deleted Product Preview for DAC80504 from *Device Comparison Table* ... 4
- Added Added TUE DAC80504. All Gains row in *Electrical Characteristics* ... 7
- Added Added Full-scale error DAC80504. All Gains row in *Electrical Characteristics* ... 7
- Added Added Gain error DAC80504. All Gains row in *Electrical Characteristics* ... 7
- Changed Short circuit current, DAC code = full scale, output shorted to GND in *Electrical Characteristics*TYP from 35 mA to 30 mA ... 8
- Changed Short circuit current, DAC code = zero scale, output shorted to V_{DD} in *Electrical Characteristics* TYP from 30 mA to 35 mA ... 8
- Added Channel-to channel dc crosstalk, Measured channel at midscale. Adjacent channel at full scale. DAC80504 in *Electrical Characteristics* ... 8

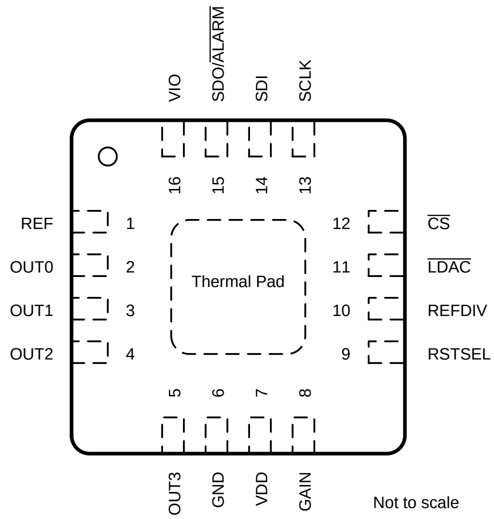
Changes from Original (August 2017) to Revision A **Page**

5 Device Comparison Table

DEVICE	RESOLUTION	REFERENCE
DAC80504	16-Bit	Internal (default) or External
DAC70504	14-Bit	Internal (default) or External
DAC60504	12-Bit	Internal (default) or External

6 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
REF	1	I/O	When using internal reference, this is the reference output voltage pin (default). When using an external reference, this is the reference input pin to the device.
OUT0	2	O	Analog output voltage from DAC 0.
OUT1	3	O	Analog output voltage from DAC 1.
OUT2	4	O	Analog output voltage from DAC 2.
OUT3	5	O	Analog output voltage from DAC 3.
GND	6	GND	Ground reference point for all circuitry on the device.
VDD	7	PWR	Analog supply voltage (2.7 V to 5.5 V).
GAIN	8	I	Sets the gain configuration after a power-up or reset event. When tied to GND, the initial buffer amplifier gain for all four channels is set to 1. When tied to V_{IO} the initial buffer amplifier gain is 2. Changing the state of this pin after power-up does not affect the device operation.
RSTSEL	9	I	Reset select pin. When tied to GND all four DACs reset to zero scale. When connected to V_{IO} all four DACs reset to midscale.
REFDIV	10	I	Sets the reference divider configuration after a power-up or reset event. When tied to GND, the reference voltage is not divided down. When tied to V_{IO} the reference voltage is divided by 2. Changing the state of this pin after power-up does not affect the device operation.
$\overline{\text{LDAC}}$	11	I	A high-to-low transition on the $\overline{\text{LDAC}}$ pin causes the DAC outputs of those channels configured in synchronous mode to update simultaneously. The pin can be tied permanently to GND.
$\overline{\text{CS}}$	12	I	Active low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, it enables the serial interface input shift register.
SCLK	13	I	Serial interface clock.
SDI	14	I	Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.
SDO/$\overline{\text{ALARM}}$	15	O	Serial interface data output (default). The SDO pin is in high impedance when $\overline{\text{CS}}$ pin is high. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit. Alternatively the pin can be configured as an $\overline{\text{ALARM}}$ open-drain output to indicate a CRC or reference alarm event. If configured as $\overline{\text{ALARM}}$ a 10 kΩ, pull-up resistor to V_{IO} is required.
VIO	16	PWR	IO supply voltage (1.7 V to 5.5 V). This pin sets the I/O operating voltage for the serial interface.
Thermal Pad	–	–	The thermal pad is located on the bottom-side of the QFN package. The thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Suppy voltage	V_{DD} to GND	–0.3	6	V
	V_{IO} to GND	–0.3	6	
Pin voltage	DAC outputs to GND	–0.3	V_{DD} + 0.3	V
	REF to GND	–0.3	V_{DD} + 0.3	
	Digital pins to GND	–0.3	V_{IO} + 0.3	
Input current	Input current to any pin except supply pins	–10	10	mA
Temperature	Operating free-air, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 [1]	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 [2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V_{DD}	Analog supply voltage		2.7		5.5	V
V_{IO}	IO supply voltage		1.7		5.5	
DIGITAL INPUTS						
	Digital input voltage		0		V_{IO}	V
REFERENCE INPUT						
V_{REFIN}	V_{DD} = 2.7 V to 3.3 V	Reference divider disabled	1.2		$(V_{DD} – 0.2)/2$	V
		Reference divider enabled	2.4		$V_{DD} – 0.2$	
	V_{DD} = 3.3 V to 5.5 V	Reference divider disabled	1.2		$V_{DD}/2$	
		Reference divider enabled	2.4		V_{DD}	
TEMPERATURE						
T_A	Operating free-air temperature		–40		125	°C

7.4 Thermal Information

THERMAL METRIC[(1)]		DACx0504 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

all minimum and maximum specifications at V_{DD}= 2.7 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, V_{REFIN} = 1.25 V to 5.5 V, R_{LOAD} = 2 kΩ to GND, C_{LOAD} = 200 pF to GND, digital inputs at V_{IO} or GND, and T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE[(1)]						
	Resolution	DAC80504	16			Bits
		DAC70504	14			
		DAC60504	12			
INL	Integral nonlinearity	DAC80504		±0.5	±1	LSB
		DAC70504		±0.5	±1	
		DAC60504		±0.5	±1	
DNL	Differential nonlinearity	DAC80504, specified 16-bit monotonic		±0.5	±1	LSB
		DAC70504, specified 14-bit monotonic		±0.5	±1	
		DAC60504, specified 12-bit monotonic		±0.5	±1	
TUE	Total unadjusted error			±0.05	±0.1	%FSR
	Offset error			±0.75	±1.5	mV
	Zero-code error	DAC code = zero scale		0.5	1.5	mV
	Full-scale error			±0.05	±0.1	%FSR
	Gain error			±0.05	±0.1	%FSR
	Offset error drift			±1		µV/°C
	Zero-code error drift			±2		µV/°C
	Full-scale error drift			±2		ppm of FSR/°C
	Gain error drift			±1		ppm of FSR/°C
	Output voltage drift over time	T_A = 25°C, DAC code = midscale, 1600 hours		20		ppm of FSR

(1) Static performance specified with DAC outputs unloaded for all gain options, unless otherwise noted. End point fit between codes. 16-bit: Code 256 to 65280, 14-bit: Code 128 to 16127, 12-bit: Code 16 to 4031.

Electrical Characteristics (continued)

all minimum and maximum specifications at V_{DD}= 2.7 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, V_{REFIN} = 1.25 V to 5.5 V, R_{LOAD} = 2 kΩ to GND, C_{LOAD} = 200 pF to GND, digital inputs at V_{IO} or GND, and T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS					
Voltage range	Gain = 2 (BUFF-GAIN = 1, REF-DIV = 0)	0		2 × V_{REF}	V
	Gain = 1 (BUFF-GAIN = 1, REF-DIV = 1)	0		V_{REF}	
	Gain = ½ (BUFF-GAIN = 0, REF-DIV = 1)	0		½ × V_{REF}	
Output voltage headroom	to GND or V_{DD} (unloaded)		0.004		V
	to GND or V_{DD} (–5 mA ≤ I_{OUT} ≤ 5 mA)	0.15			
	to GND or V_{DD} (–10 mA ≤ I_{OUT} ≤ 10 mA)	0.3			
	to GND or V_{DD} (–20 mA ≤ I_{OUT} ≤ 20 mA)	0.5			
Short circuit current(2)	DAC code = full scale, output shorted to GND		30		mA
	DAC code = zero scale, output shorted to V_{DD}		35		
Load regulation	DAC code = midscale, -10 mA ≤ I_{OUT} ≤ 10 mA		85		µV/mA
Maximum capacitive load(3)	R_{LOAD} = ∞	0		2	nF
	R_{LOAD} = 2 kΩ	0		10	
DC output impedance	DAC code = midscale		0.085		Ω
	DAC code at GND or V_{DD}		15		
DYNAMIC PERFORMANCE					
Output voltage settling time	¼ to ¾ scale and ¾ to ¼ scale settling time to ±2 LSB, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 2		5		µs
Slew rate	V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 2		1.8		V/µs
Power-up time	DAC*x*-PWDWN 1 to 0 transition, DAC code = full scale, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 2(4)		12		µs
Power-up glitch magnitude	DAC code = zero scale, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 2. C_{LOAD} = 50 pF		25		mV
Output noise	0.1 Hz to 10 Hz, DAC code = midscale, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 2		14		$µV_{PP}$
Output noise density	1 kHz, DAC code = midscale, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 2		78		nV/√Hz
	10 kHz, DAC code = midscale, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 2		74		
	1 kHz, DAC code = full scale, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 1		55		
	10 kHz, DAC code = full scale, V_{DD} = 5.5 V, V_{REFIN} = 2.5 V, gain = 1		50		
AC PSRR	DAC code = midscale, frequency = 60 Hz, amplitude = 200 mV_{PP} superimposed on V_{DD}		85		dB
DC PSRR	DAC code = midscale, V_{DD} = 5 V ± 10%		10		µV/V
Code change glitch impulse	1 LSB change around major carrier		4		nV-s
Channel-to-channel ac crosstalk	DAC code = midscale. Code 32 to full-scale swing on adjacent channel		0.2		nV-s
Channel-to-channel dc crosstalk	Measured channel at midscale, adjacent channel at full scale		5		µV
	Measured channel at midscale, all other channels at full scale		10		
Digital feedthrough	DAC code = midscale. f_{SCLK} = 1 MHz, SDO disabled		0.1		nV-s
EXTERNAL REFERENCE INPUT					
Reference input current	V_{REFIN} = 2.5 V		25		µA
Reference input impedance			100		kΩ
Reference input capacitance			5		pF

(2) Temporary overload condition protection. Junction temperature can be exceeded during current limit. Operation above the specified maximum junction temperature may impair device reliability.
(3) Specified by design and characterization. Not tested during production.
(4) Time to exit DAC power-down mode. Measured from $\overline{CS}$ rising edge to 90% of DAC final value.

Electrical Characteristics (continued)

all minimum and maximum specifications at V_{DD}= 2.7 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, V_{REFIN} = 1.25 V to 5.5 V, R_{LOAD} = 2 kΩ to GND, C_{LOAD} = 200 pF to GND, digital inputs at V_{IO} or GND, and T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE						
V_{REFOUT}	Reference output voltage	T_A = 25°C	2.495	2.5	2.505	V
	Reference output drift			2	5	ppm/°C
	Reference output impedance			0.1		Ω
	Reference output noise	0.1 Hz to 10 Hz		15		μV_{PP}
	Reference output noise density	10 kHz, REF_{LOAD} = 10 nF		130		$nV/\sqrt{Hz}$
	Reference load current			±5		mA
	Reference load regulation	Source and sink		100		µV/mA
	Reference line regulation			20		µV/V
	Reference output drift over time	T_A = 25°C, 1600 hours		4.8		ppm
	Reference thermal hysteresis	First cycle		50		ppm
		Additional cycle		18		
DIGITAL INPUTS						
V_{IH}	High-level input voltage		0.7 × V_{IO}			V
V_{IL}	Low-level input voltage				0.3 × V_{IO}	V
	Input current			±2		µA
	Input pin capacitance			2		pF
DIGITAL OUTPUTS						
V_{OH}	High-level output voltage	I_{LOAD} = 0.2 mA	V_{IO} – 0.4			V
V_{OL}	Low-level output voltage	I_{LOAD} = –0.2 mA			0.4	V
	Output pin capacitance			4		pF
POWER SUPPLY REQUIREMENTS						
I_{DD}	V_{DD} supply current	Active mode, internal reference enabled, gain = 1, DAC code = full scale, outputs unloaded, SPI static		2.8	3.6	mA
		Active mode, internal reference disabled, gain = 1, DAC code = full scale, outputs unloaded, SPI static		2.3	3	
		Power-down		15		µA
I_{IO}	V_{IO} supply current			2	3	µA

7.6 Typical Characteristics

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)

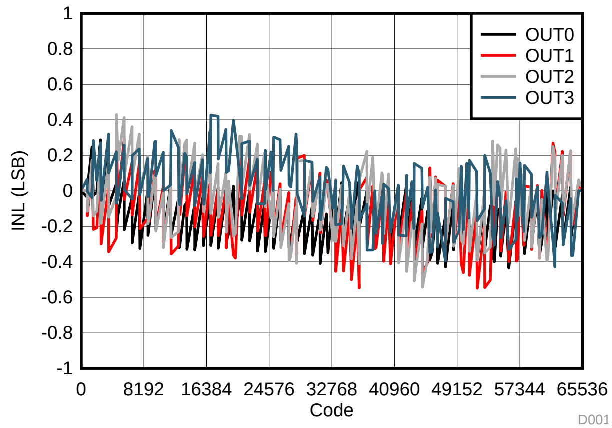


Figure 1. Integral Linearity Error vs Digital Input Code

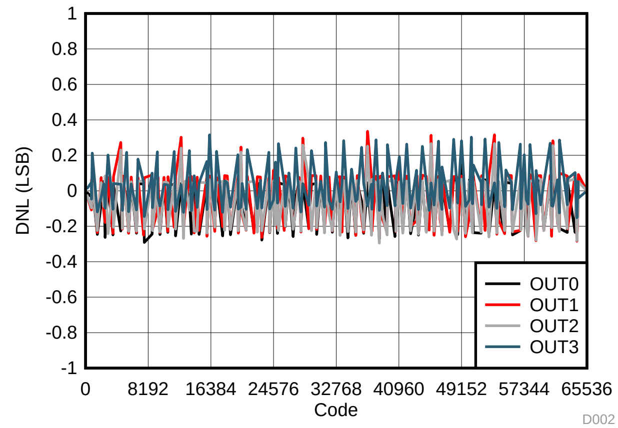


Figure 2. Differential Linearity Error vs Digital Input Code

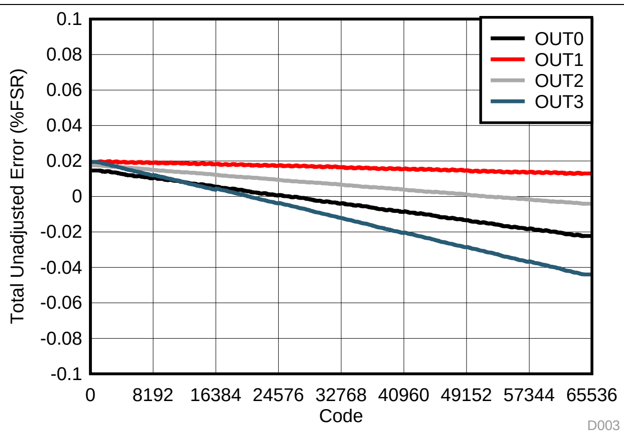


Figure 3. Total Unadjusted Error vs Digital Input Code

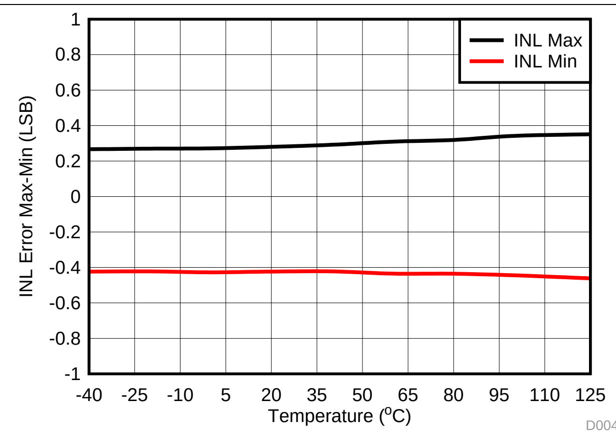


Figure 4. Integral Linearity Error vs Temperature

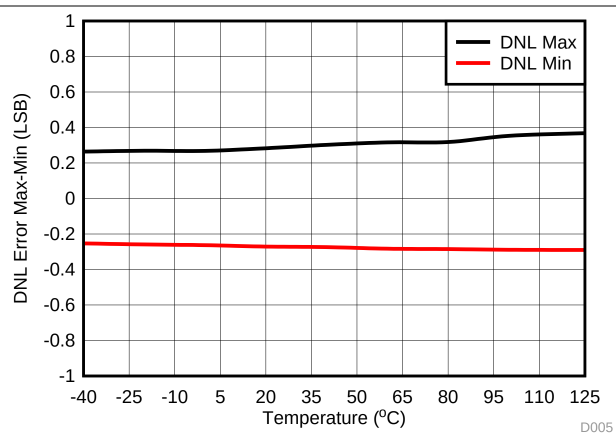


Figure 5. Differential Linearity Error vs Temperature

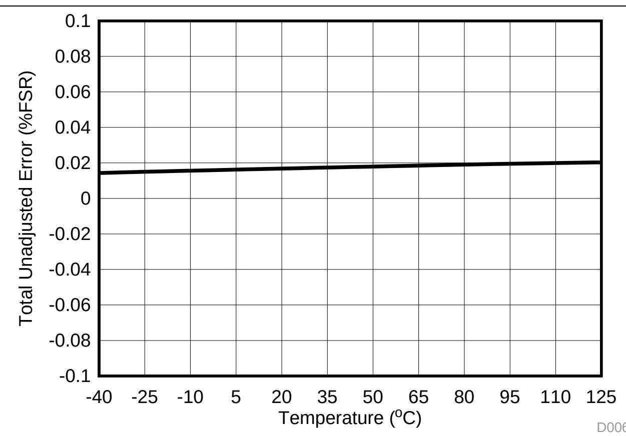


Figure 6. Total Unadjusted Error vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)

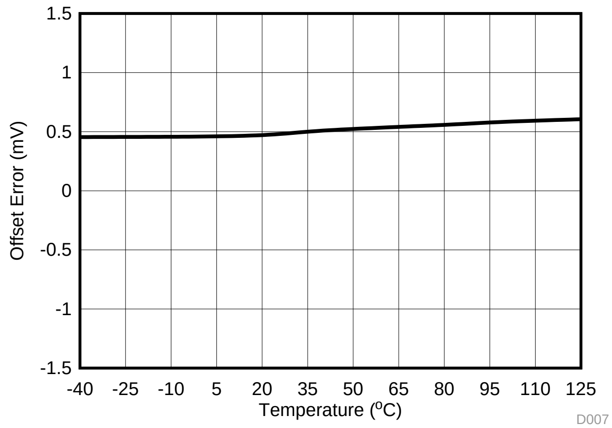


Figure 7. Offset Error vs Temperature

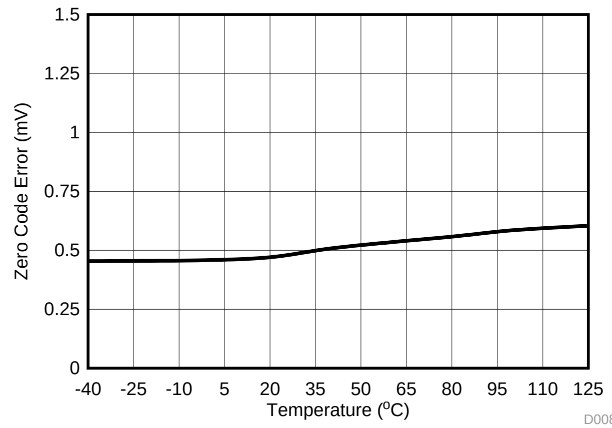


Figure 8. Zero Code Error vs Temperature

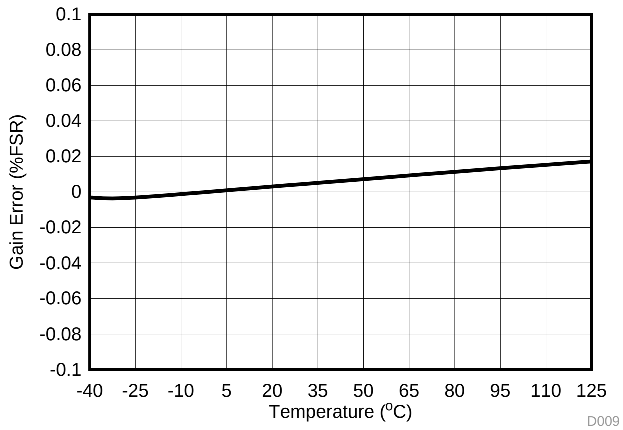


Figure 9. Gain Error vs Temperature

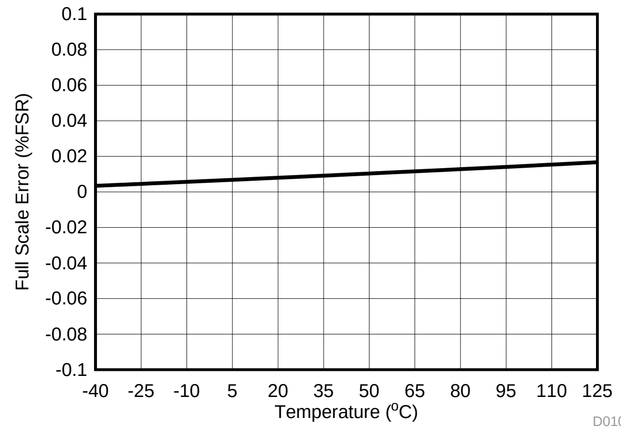
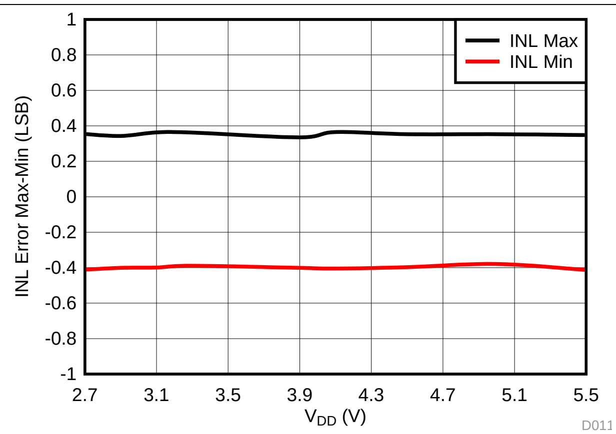
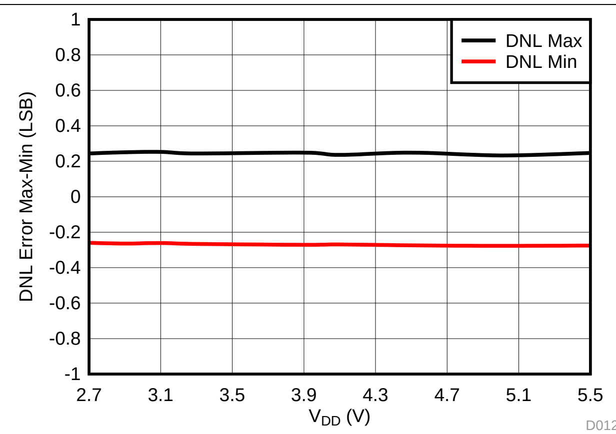


Figure 10. Full Scale Error vs Temperature



Gain = 1

Figure 11. Integral Linearity Error vs Supply Voltage



Gain = 1

Figure 12. Differential Linearity Error vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)

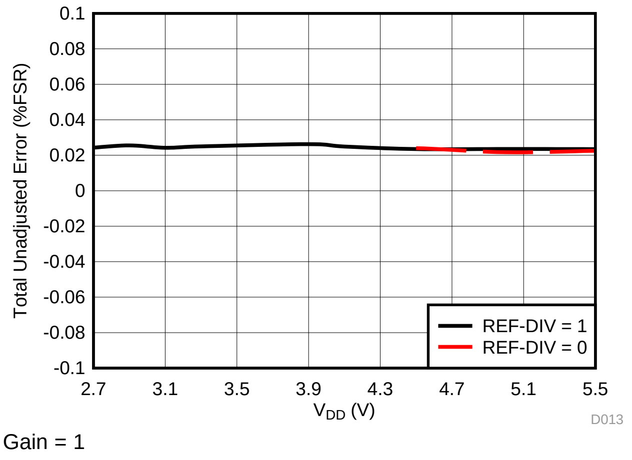


Figure 13. Total Unadjusted Error vs Supply Voltage

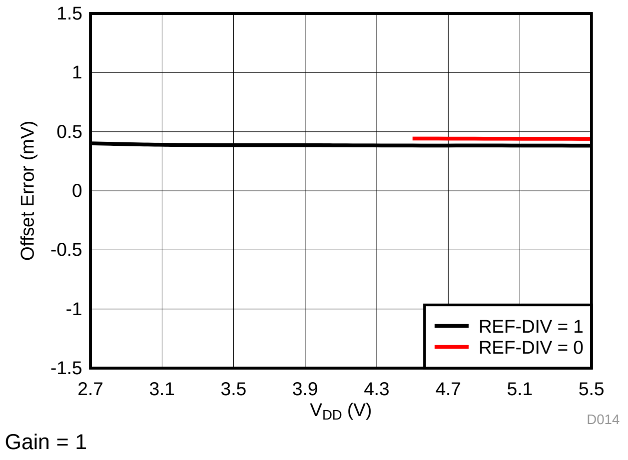


Figure 14. Offset Error vs Supply Voltage

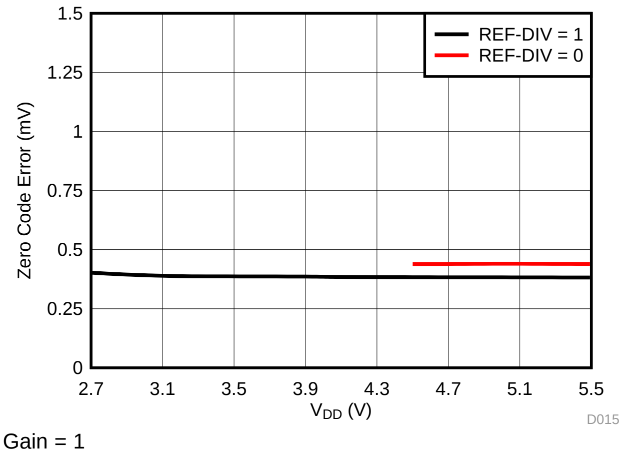


Figure 15. Zero Code Error vs Supply Voltage

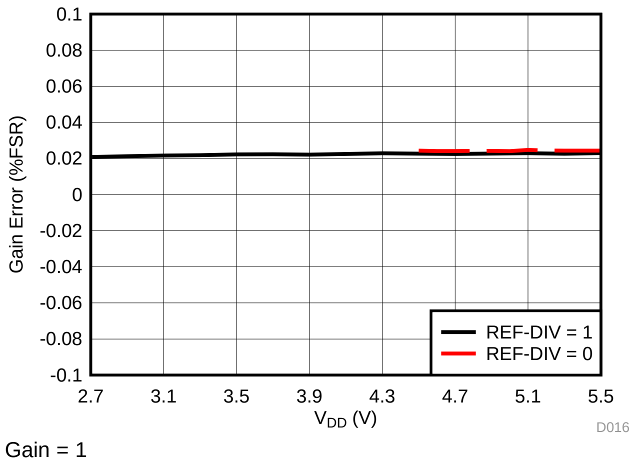


Figure 16. Gain Error vs Supply Voltage

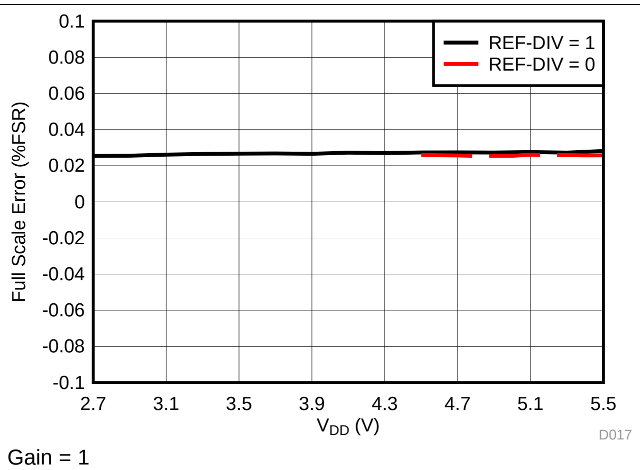


Figure 17. Full Scale Error vs Supply Voltage

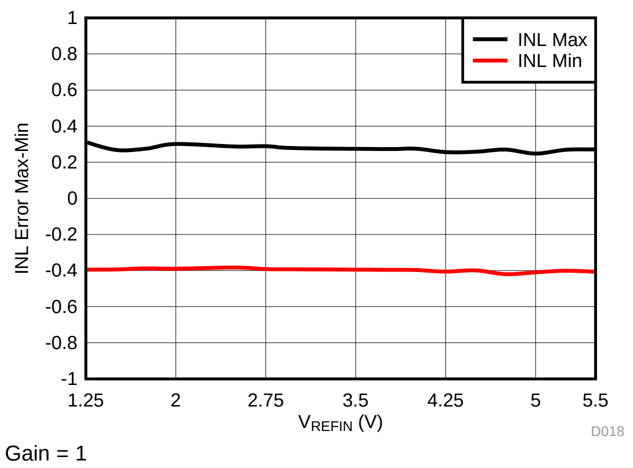
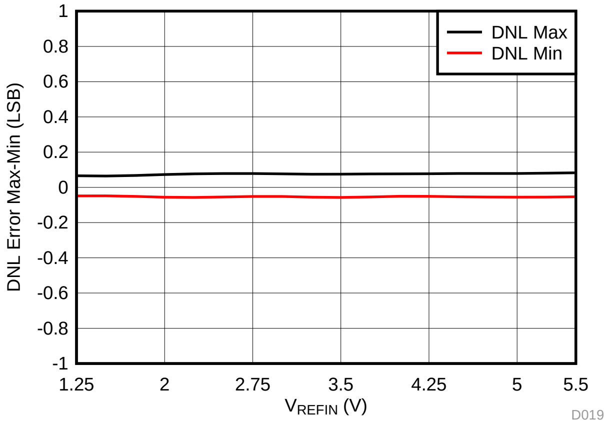


Figure 18. Integral Linearity Error vs Reference Voltage

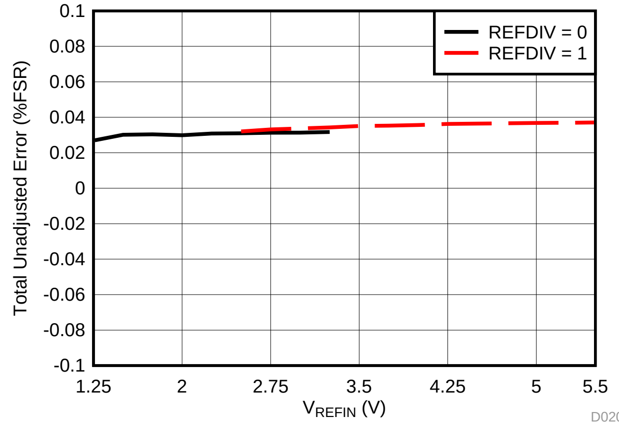
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)



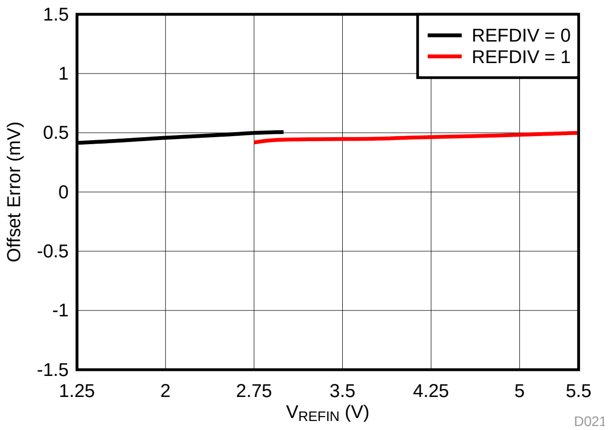
Gain = 1

Figure 19. Differential Linearity Error vs Reference Voltage



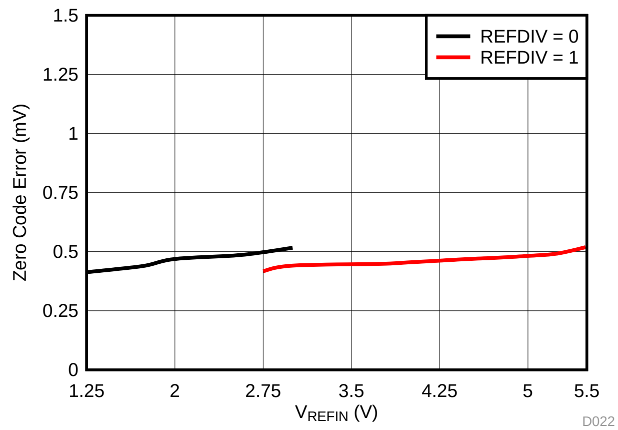
Gain = 1

Figure 20. Total Unadjusted Error vs Reference Voltage



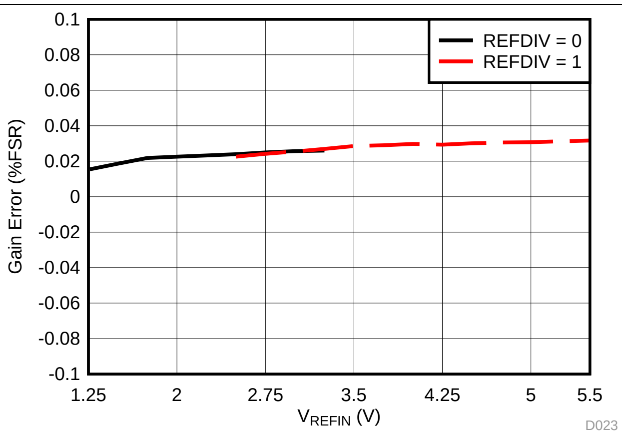
Gain = 1

Figure 21. Offset Error vs Reference Voltage



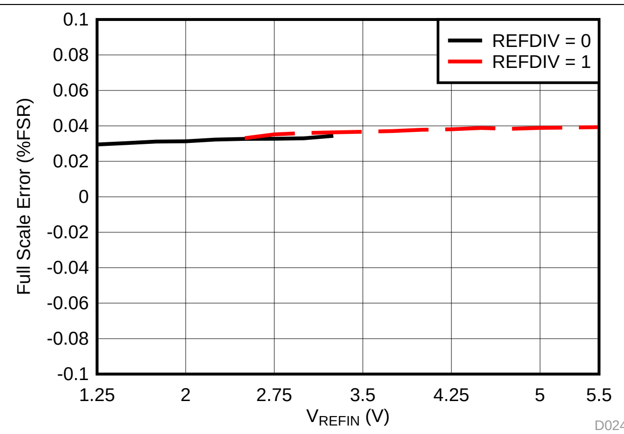
Gain = 1

Figure 22. Zero Code Error vs Reference Voltage



Gain = 1

Figure 23. Gain Error vs Reference Voltage

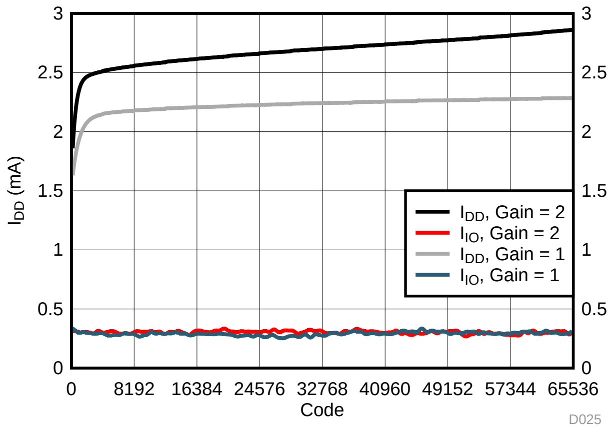


Gain = 1

Figure 24. Full Scale Error vs Reference Voltage

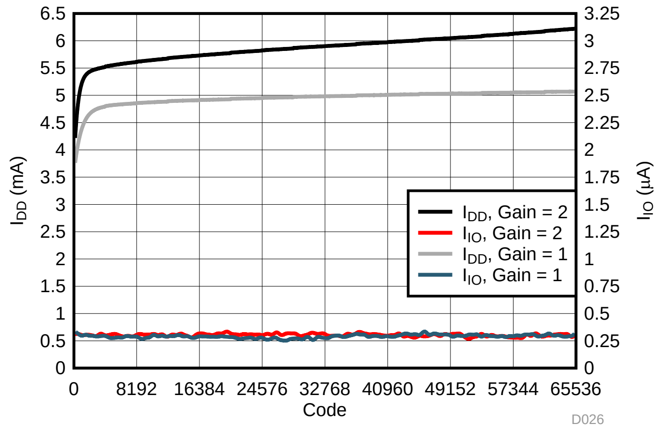
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)



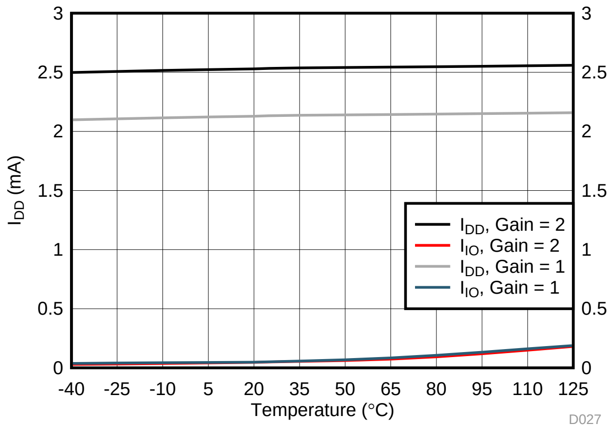
Gain = 1, external reference = 2.5 V

Figure 25. Supply Current With External Reference vs Digital Input Code



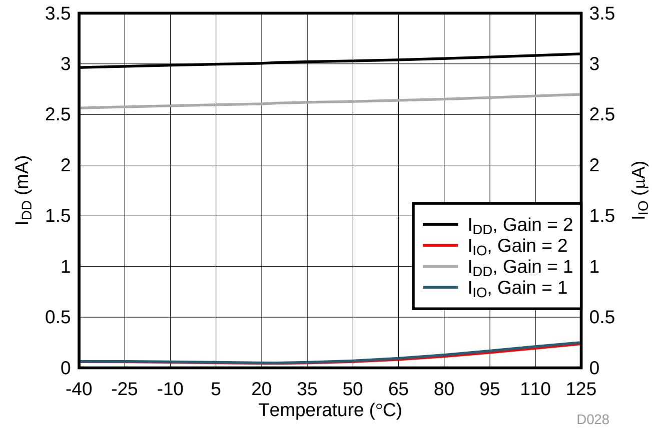
Gain = 1

Figure 26. Supply Current With Internal Reference vs Digital Input Code



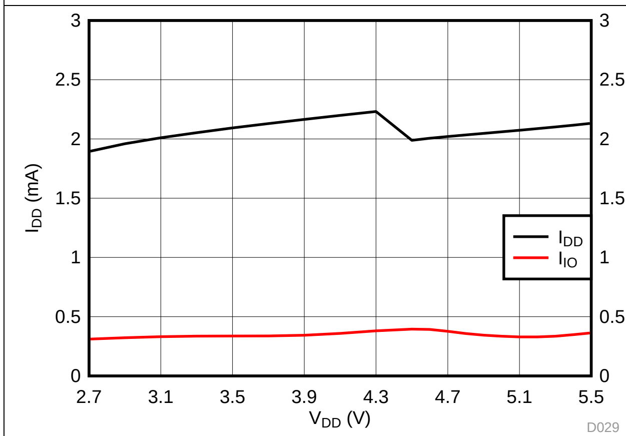
Gain = 1, external reference = 2.5 V

Figure 27. Supply Current With External Reference vs Temperature



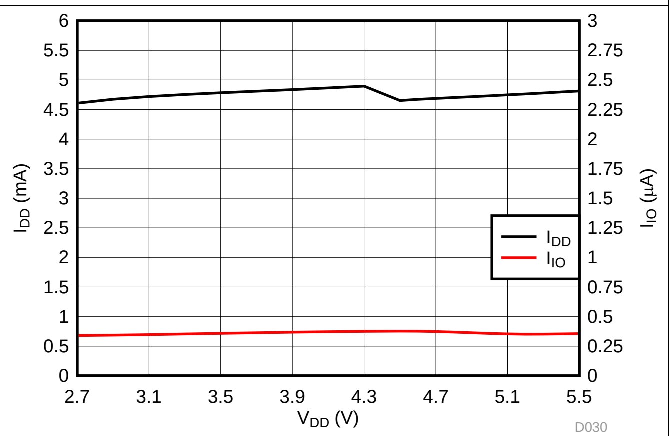
Gain = 1

Figure 28. Supply Current With Internal Reference vs Temperature



Gain = 1, external reference = 2.5 V

Figure 29. Supply Current With External Reference vs Supply Voltage



Gain = 1

Figure 30. Supply Current With Internal Reference vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)

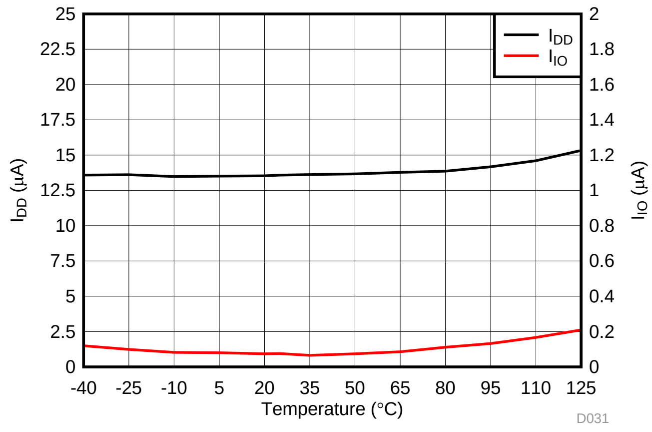


Figure 31. Supply Current and Input Current vs Temperature

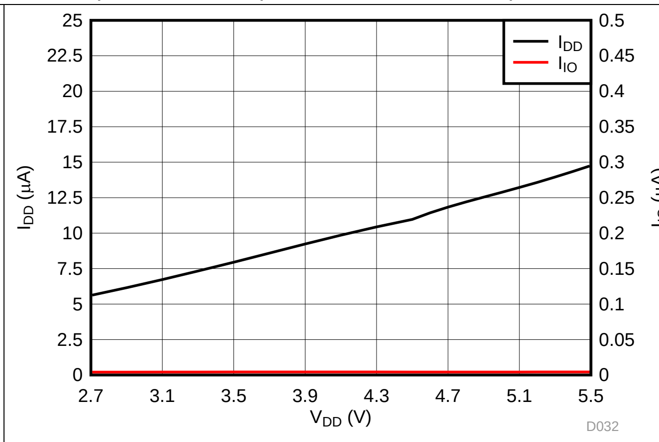


Figure 32. Supply Current and Input Current vs Supply Voltage

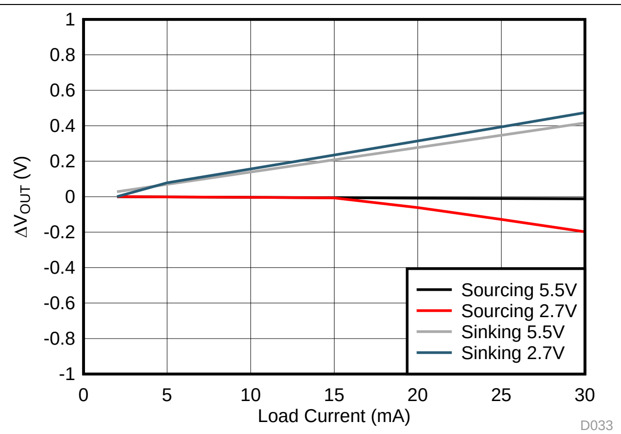


Figure 33. Headroom/Footroom vs Load Current

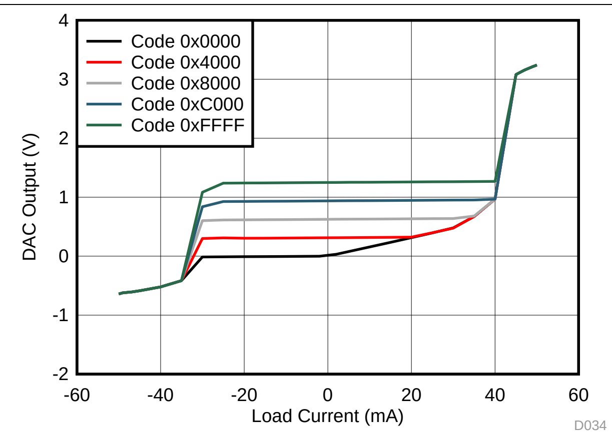


Figure 34. Source and Sink Capability With Gain = ½

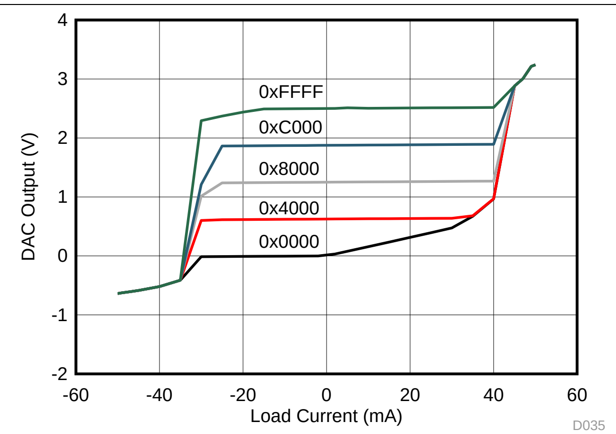


Figure 35. Source and Sink Capability With Gain = 1

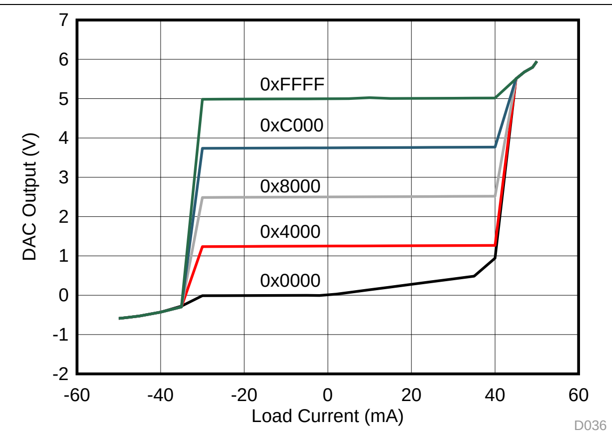
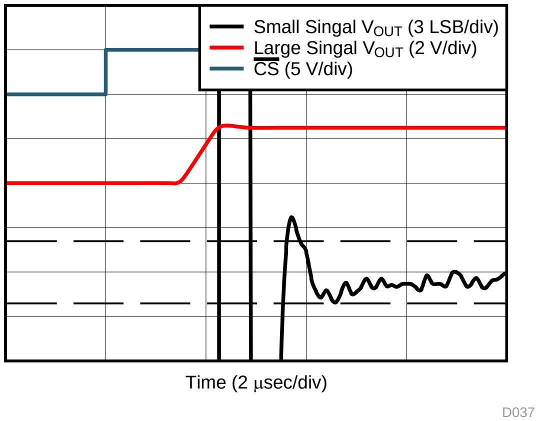


Figure 36. Source and Sink Capability With Gain = 2

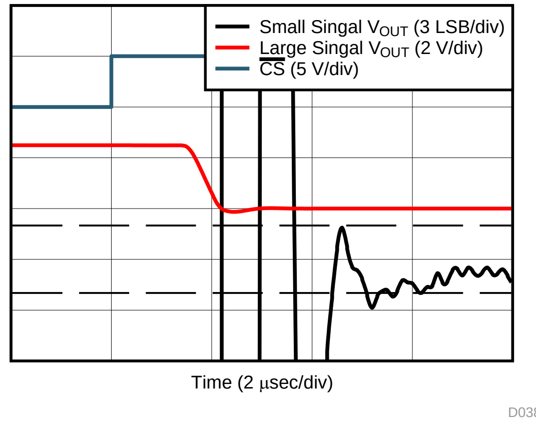
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)



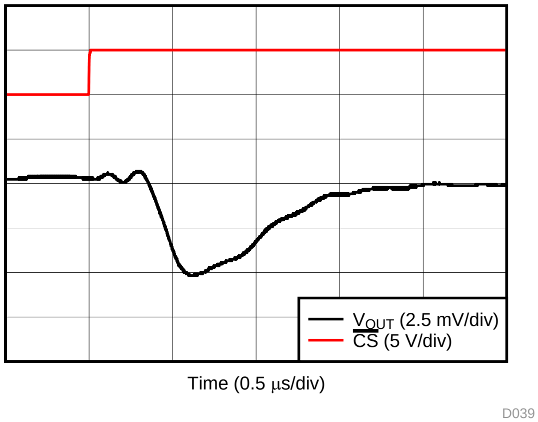
Gain = 1

Figure 37. Full-Scale Settling Time, Rising Edge



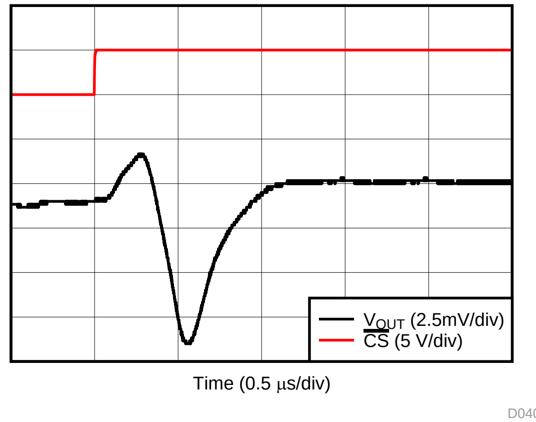
Gain = 1

Figure 38. Full-Scale Settling Time, Falling Edge



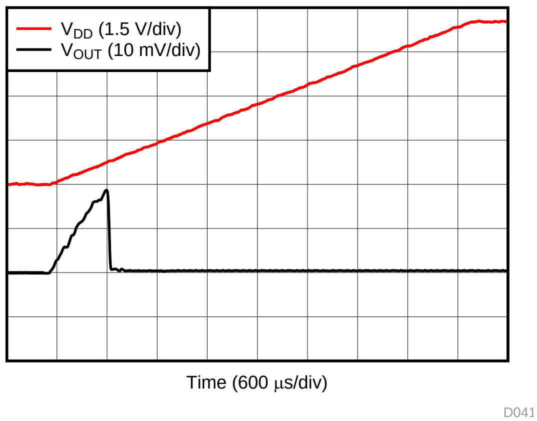
Gain = 1

Figure 39. Glitch Impulse, Falling Edge, 1 LSB Step



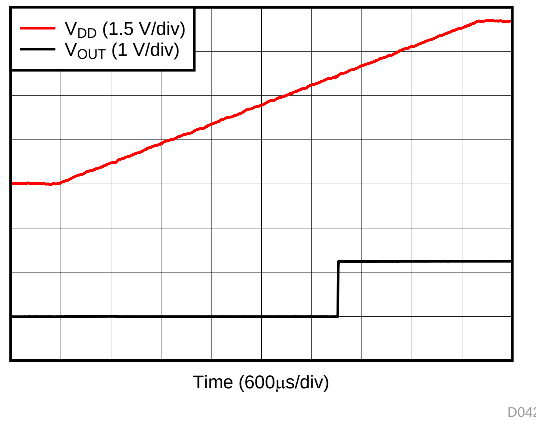
Gain = 1

Figure 40. Glitch Impulse, Rising Edge, 1 LSB Step



Gain = 1

Figure 41. Power-On, Reset to Zero Scale

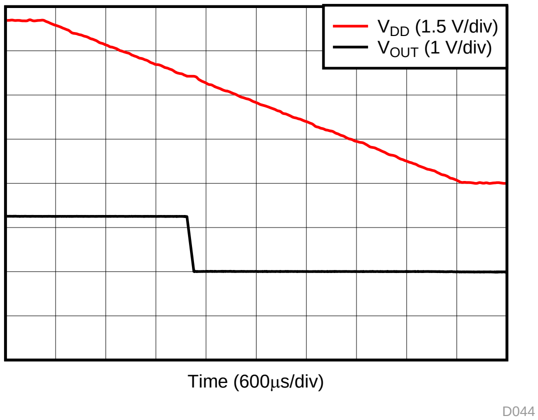


Gain = 1

Figure 42. Power-On, Reset to Midscale

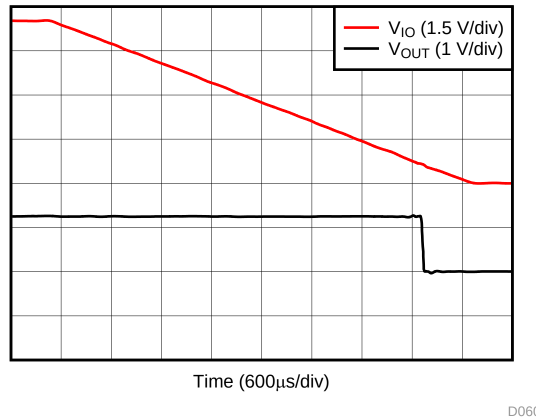
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)



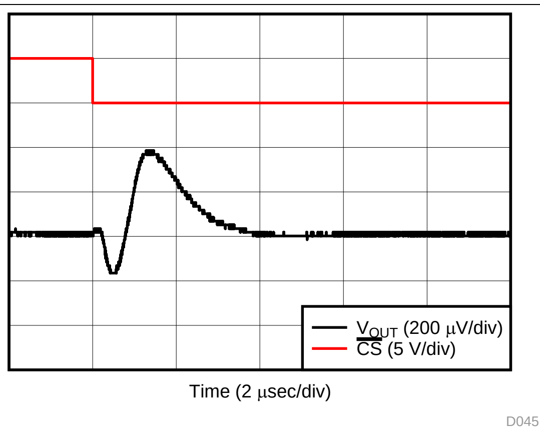
Gain = 1, DAC code at midscale

Figure 43. V_{DD} Power-Down



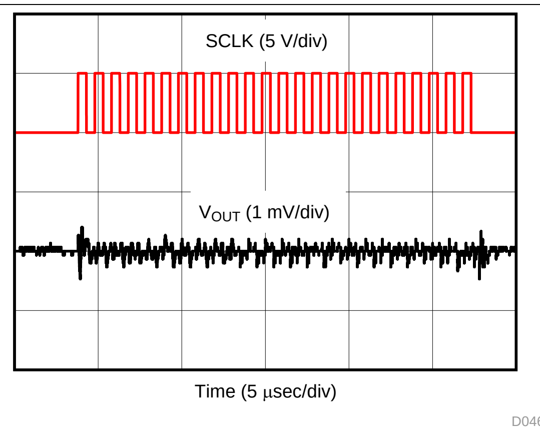
Gain = 1, DAC code at midscale

Figure 44. V_{IO} Power-Down



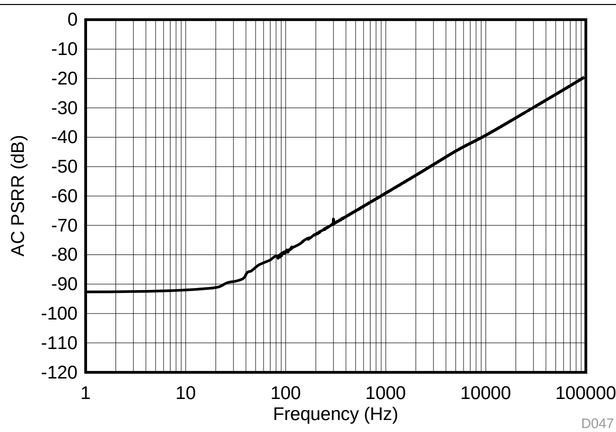
Gain = 1, measured DAC at midscale,
all other DACs switch from code 32 to full scale

Figure 45. Channel to Channel Crosstalk



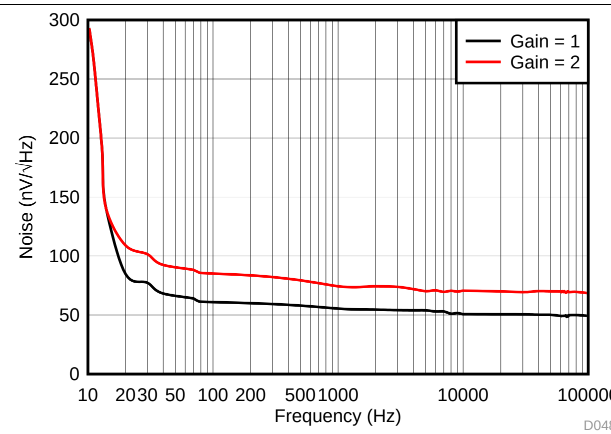
Gain = 1, DAC code at midscale

Figure 46. Clock Feedthrough With SCLK = 1 MHz



Gain = 1, V_{DD} = 5 V + 200 mV_{PP} (Sinusoid), DAC code at fullscale

Figure 47. DAC Output AC PSRR vs Frequency

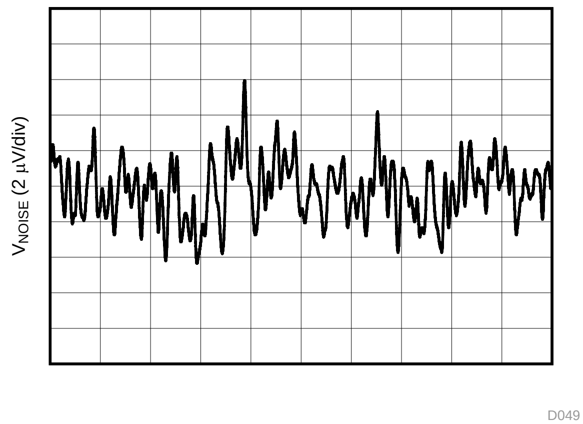


External reference = 2.5 V, DAC code at midscale

Figure 48. DAC Output Noise Density vs Frequency

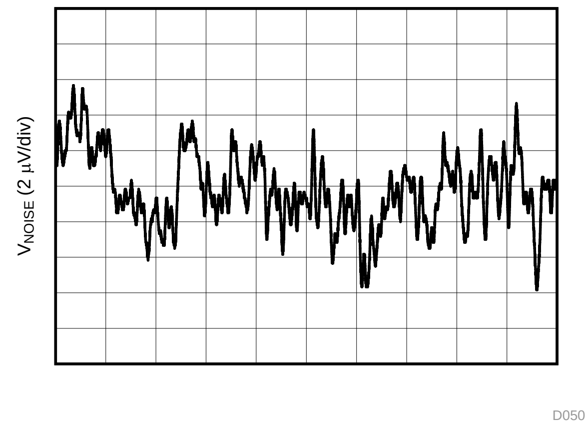
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)



Gain = 1, external reference = 2.5 V, DAC code at midscale

Figure 49. DAC Output Noise With External Reference 0.1 Hz to 10 Hz



Gain = 1, DAC code at midscale

Figure 50. DAC Output Noise With Internal Reference 0.1 Hz to 10 Hz

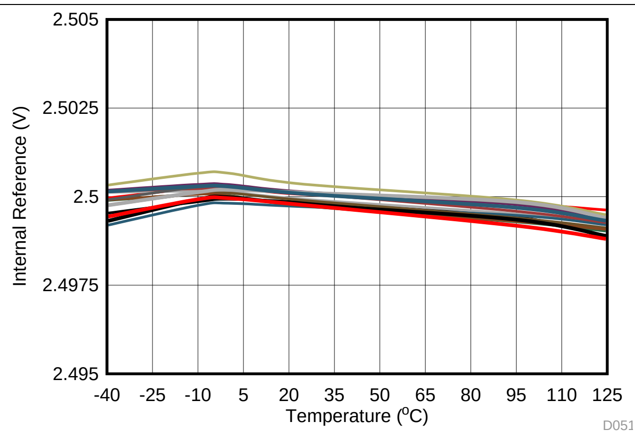


Figure 51. Internal Reference Voltage vs Temperature

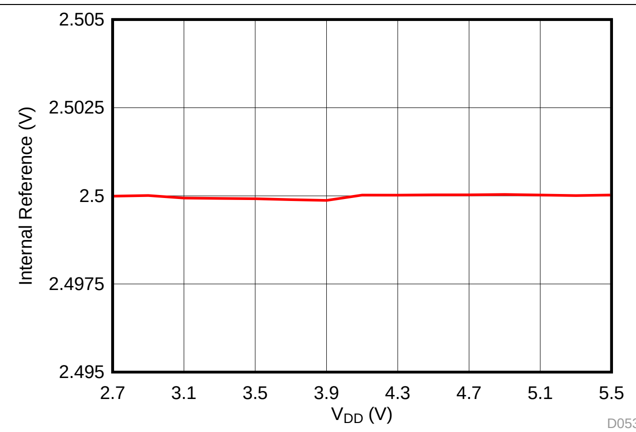


Figure 52. Internal Reference Voltage vs Supply Voltage

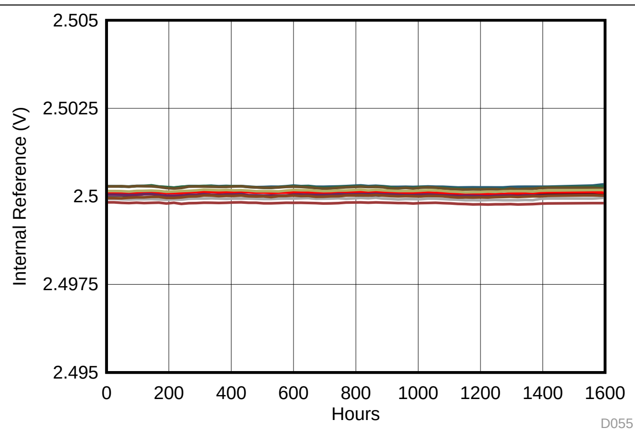


Figure 53. Internal Reference Voltage vs Time

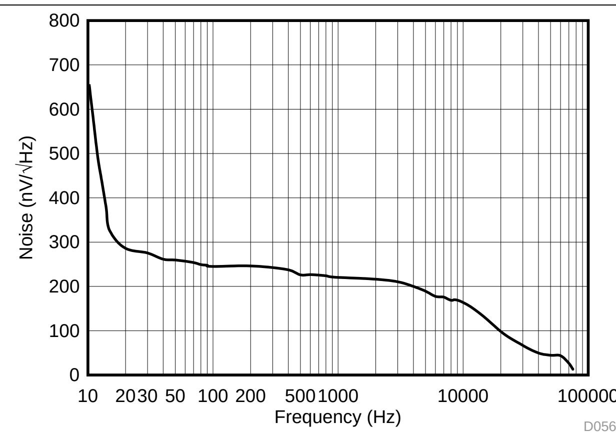
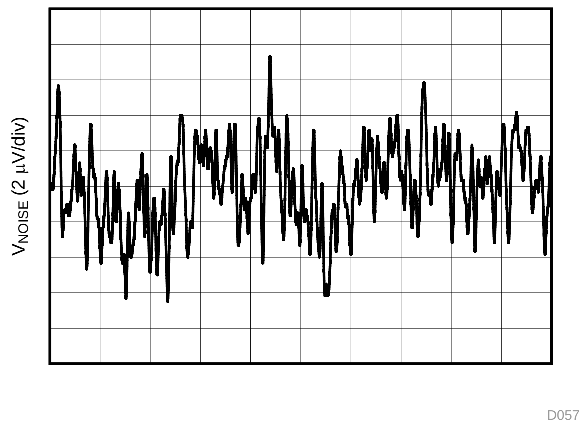


Figure 54. Internal Reference Noise Density vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5.5 V, internal reference = 2.5 V, gain = 2, DAC outputs unloaded (unless otherwise noted)



0.1 Hz to 10 Hz

Figure 55. Internal Reference Noise

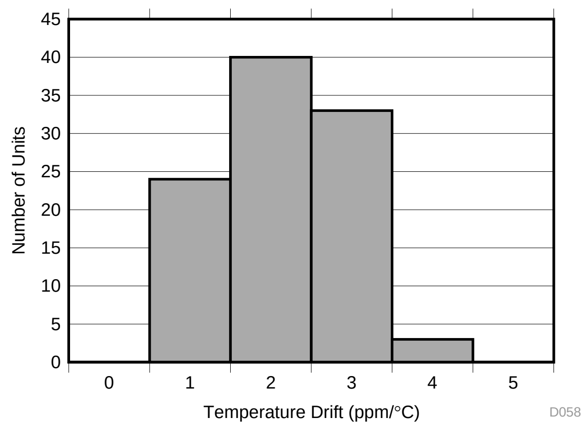


Figure 56. Internal Reference Temperature Drift Histogram

8 Detailed Description

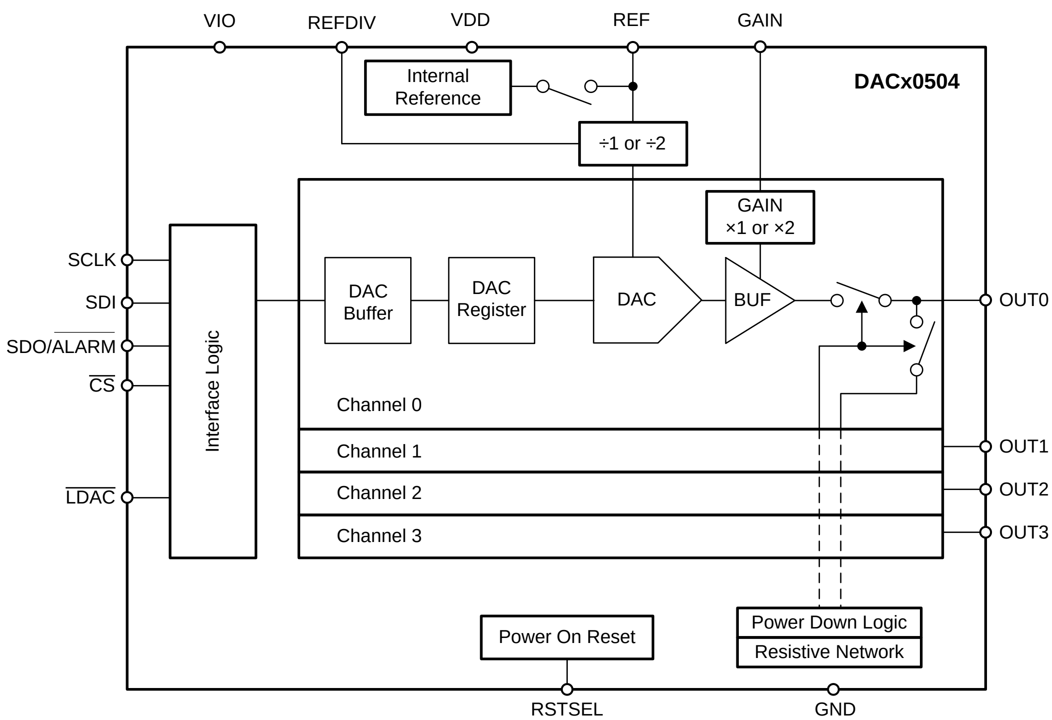
8.1 Overview

The DACx0504 is a pin-compatible family of low-power, four-channel, buffered voltage-output digital-to-analog converters (DACs) with 16-, 14-, and 12-bit resolution. The DACx0504 include a 2.5-V internal reference and user-selectable gain configuration. providing full-scale output voltages of 1.25 V (gain = ½), 2.5 V (gain = 1), or 5 V (gain = 2). The device operates from a single 2.7 V to 5.5 V supply, is specified monotonic, and provides high linearity of ±1 LSB INL.

Communication to the DACx0504 is performed through a 4-wire serial interface that supports stand-alone and daisy-chain operation. The optional frame-error checking provides added robustness to the DACx0504 serial interface.

The DACx0504 incorporates a power-on-reset circuit and RSTSEL pin that powers up and maintains the DAC outputs at either zero scale or midscale until a valid code is written to the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital-to-Analog Converter (DAC)

Each output channel in the DACx0504 consists of an R-2R ladder architecture followed by an output buffer amplifier. Figure 57 shows a block diagram of the DAC architecture.

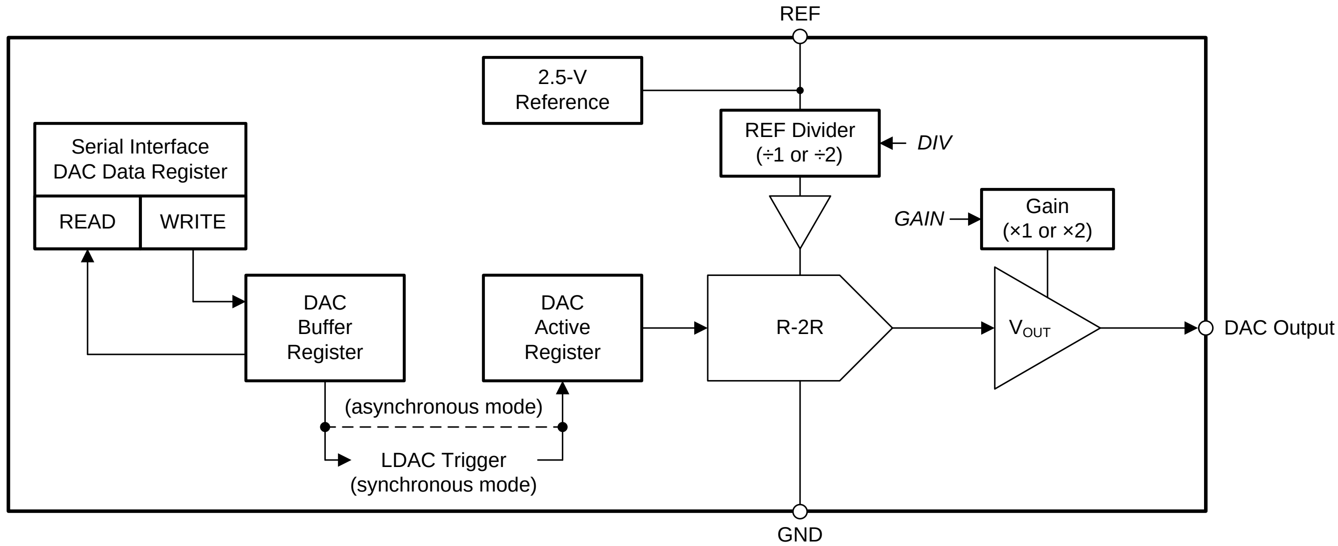


Figure 57. DACx0504 DAC Block Diagram

8.3.1.1 DAC Transfer Function

The input data are written to the individual DAC data registers in straight binary format. After a power-on or a reset event, all DAC registers are set to either zero code or midscale code, as determined by the RSTSEL pin. The DAC transfer function is given by Equation 1.

$$V_{OUT} = \frac{CODE}{2^n} \times \frac{V_{REF}}{DIV} \times GAIN$$

where

- CODE = decimal equivalent of the binary code that is loaded to the DAC register. CODE ranges from 0 to 2^n – 1.
- V_{REF} = DAC reference voltage. Either V_{REFOUT} from the internal 2.5 V reference or V_{REFIN} if using an external one.
- n = resolution in bits. Either 16 (DAC80504), 14 (DAC70504), or 12 (DAC60504).
- DIV = 1 or 2 as set by the REFDIV pin after a reset event or by the REF-DIV bit in the GAIN register.
- GAIN = 1 or 2 as set by the GAIN pin after a reset event or by the BUFF-GAIN bit for that DAC channel in the GAIN register. (1)

Feature Description (continued)

8.3.1.2 Output Amplifiers

The DACx0504 output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0 V to V_{DD}. Each buffer amplifier is capable of driving a load of 2 kΩ in parallel with 10 nF to GND.

The full-scale output voltage for each channel is determined by the reference voltage (V_{REF}), the reference divider setting (DIV), and the output buffer gain for that channel (GAIN), as shown in Table 1. After a power-up or reset event the DIV and GAIN settings are set by the REFDIV and GAIN pins, respectively. During normal operation the DIV and GAIN settings can be reconfigured through the REF-DIV and BUFF-GAIN bit (see Equation 1). The GAIN setting for each output channel can be individually configured thus enabling independent output voltage ranges for each DAC output.

Table 1. DAC Output Range Configuration

DIV SETTING	GAIN SETTING	DAC OUTPUT RANGE
÷2	×1	0 V to ½ × V_{REF}
÷1	×1	Not recommended
÷2	×2	0 V to V_{REF}
÷1	×2	0 V to 2 × V_{REF}

8.3.1.3 DAC Register Structure

Data written to the DAC data registers is initially stored in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be configured to happen immediately (asynchronous mode) or initiated by an LDAC trigger (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to their new values. When the host reads from a DAC Data register, the value held in the DAC buffer register is returned (not the value held in the DAC active register).

8.3.1.3.1 DAC Register Synchronous and Asynchronous Updates

The update mode for each DAC channel is determined by the status of its corresponding SYNC-EN bit. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on $\overline{CS}$ rising edge. In synchronous mode, writing to the DAC data register does not automatically update the DAC output. Instead the update occurs only after an LDAC trigger event. An LDAC trigger is generated either through the LDAC bit in the TRIGGER register or by the $\overline{LDAC}$ pin. The synchronous update mode enables simultaneous update of multiple DAC outputs. In both update modes a minimum wait time of 1 µs is required between DAC output updates.

8.3.1.3.2 Broadcast DAC Register

The DAC broadcast register enables a simultaneous update of multiple DAC outputs with the same value with a single register write. Each DAC channel can be configured to update or remain unaffected by a broadcast command by setting the corresponding DAC-BRDCAST-EN bit in the SYNC register. A register write to the BRDCAST-DATA register forces those DAC channels that have been configured for broadcast operation to update their outputs. The DAC ouputs update to the broadcast value on $\overline{CS}$ rising edge independently of their synchronous mode configuration.

8.3.2 Internal Reference

The DACx0504 includes a 2.5 V precision bandgap reference enabled by default. Operation from an external reference is supported by disabling the internal reference in the CONFIG register. The internal reference is externally available at the REF pin.

A minimum 150 nF capacitor is recommended between the reference output and GND for noise filtering.

8.3.2.1 Reference Divider

The reference voltage to the device, either from the internal reference or an external one can be divided by a factor of two by tying the REFDIV pin high at power-up or by setting the REF-DIV bit in the GAIN register to 1 during normal operation. The reference voltage divider provides additional flexibility in setting the full-scale output voltage for each DAC output and must be configured to make certain that there is sufficient headroom from V_{DD} to the DAC operating reference voltage (V_{REF}/DIV). See the *Recommended Operating Conditions* table for more information.

Improper configuration of the reference divider issues a reference alarm condition. In this case, the reference buffer is shut down, and all the DAC outputs go to 0 V. The DAC data registers are unaffected by the alarm condition thus enabling the DAC output to return to normal operation once the reference divider is configured correctly. The reference alarm status can be read from the REF-ALM bit in the STATUS register. Additionally by setting ALM-EN = 1 and ALM-SEL = 1 in the CONFIG register, the SDO/$\overline{ALARM}$ pin is configured as a reference alarm pin.

8.3.2.2 Solder Heat Reflow

A known behavior of IC reference voltage circuits is the shift induced by the soldering process. Figure 58 shows the effect of solder heat reflow for the DACx0504 internal reference.

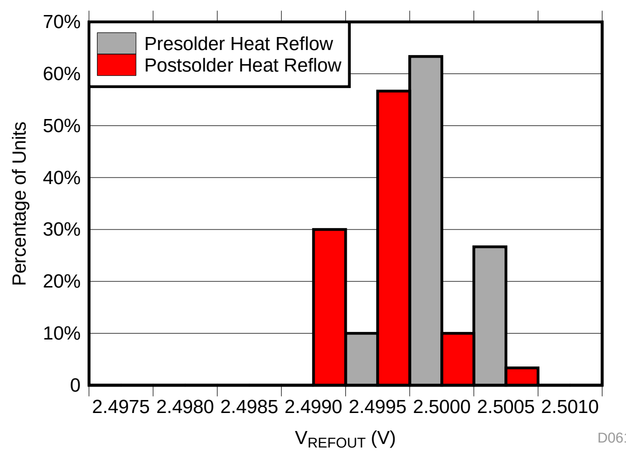


Figure 58. Solder Heat Reflow Reference Voltage Shift

8.3.3 Device Reset Options

8.3.3.1 Power-on-Reset (POR)

The DACx0504 includes a power-on reset function that controls the output voltage at power up. After the V_{DD} and V_{IO} supplies have been established a POR event is issued. The POR causes all registers to initialize to their default values and communication with the device is valid only after a 250 µs power-on-reset delay. The default value for all DACs is either zero-code or midscale-code as determined by the RSTSEL pin. Each DAC channel remains at the power-up voltage until a valid command is written to it.

The POR circuit requires specific supply levels to discharge the internal capacitors and to reset the device on power up, as indicated in Figure 59 and Figure 60. In order to initiate a POR event, V_{DD} or V_{IO} must be below their corresponding low thresholds for at least 100 µs. If V_{DD} and V_{IO} remain above their specified high threshold a POR event will not occur. When the supplies drop below their high threshold but remain over the lower one (shown as the undefined region), the device may or may not reset under all specified temperature and power-supply conditions.

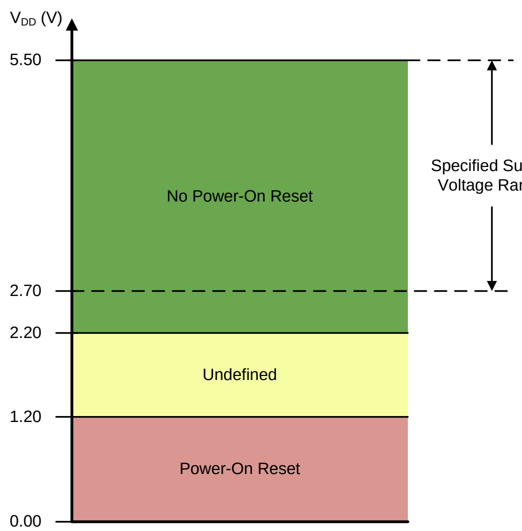


Figure 59. Threshold Levels for V_{DD} POR Circuit

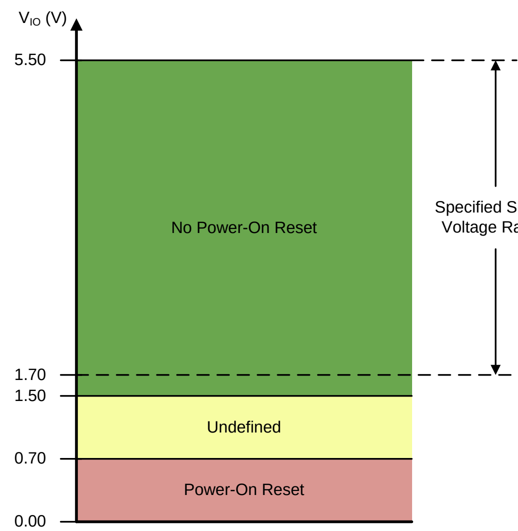


Figure 60. Threshold Levels for V_{IO} POR Circuit

8.3.3.2 Software Reset

A device software reset event is initiated by writing the reserved code 0x1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the $\overline{CS}$ rising edge of the instruction. A software reset initiates a POR event.

8.4 Device Functional Modes

8.4.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled, thus the $\overline{CS}$ pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is de-asserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges are present, only the last 24 or 32 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

In an error checking disabled access cycle (24-bits long) the first byte input to SDI is the instruction cycle which identifies the request as a read or write command and the 4-bit address to be accessed. The following bits in the cycle form the data cycle, as shown in Table 2.

Table 2. Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
22:20	Reserved	Reserved bits. Must be filled with zeros.
19:16	A[3:0]	Register address. Specifies the register to be accessed during the read or write operation.
15:0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[3:0]. If a read command, the data cycle bits are don't care values.

A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data, as shown in Table 3. Data are clocked out on SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit in the CONFIG register.

Table 3. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Echo RW from previous access cycle.
22:20	Reserved	Echo bits 22:20 from previous access cycle (all zeros).
19:16	A[3:0]	Echo address from previous access cycle.
15:0	DO[15:0]	Readback data requested on previous access cycle.

8.4.2 Daisy-Chain Operation

For systems that contain more than one DACx0504 devices, the SDO pin can be used to daisy-chain them together. Daisy-chain operation is useful in reducing the number of serial interface lines.

The first falling edge on the $\overline{CS}$ pin starts the operation cycle. If more than 24 SCLK pulses are applied while the $\overline{CS}$ pin is kept low, the data ripples out of the shift register and is clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. As a result the total number of clock cycles must be equal to 24 × N, where N is the total number of DACx0504 devices in the daisy chain. When the serial transfer to all devices is complete the $\overline{CS}$ signal is taken high. This action transfers the data from the serial peripheral interface (SPI) shift registers to the internal registers of each device in the daisy chain and prevents any further data from being clocked into the input shift register.

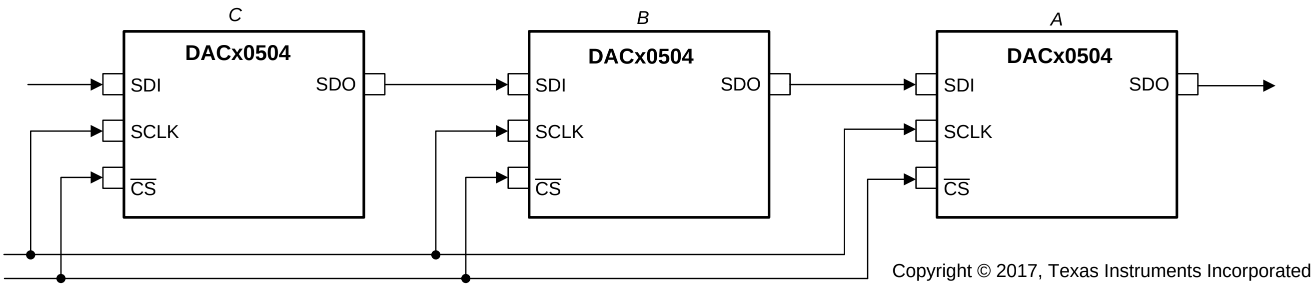


Figure 61. Daisy-Chain Layout

8.4.3 Frame Error Checking

If the DACx0504 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature can be enabled by setting the CRC-EN bit in the CONFIG register.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding it to the device, as shown in Table 4. In all serial interface readback operations the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

Table 4. Error Checking Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
31	RW	Identifies the communication as a read or write command to the addressed register. R/W = 0 sets a write operation. R/W = 1 sets a read operation.
30	CRC-ERROR	Reserved bit. Set to zero.
29:28	Reserved	Reserved bits. Must be filled with zeros.
27:24	A[3:0]	Register address. Specifies the register to be accessed during the read or write operation.
23:8	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[3:0]. If a read command, the data cycle bits are don’t care values.
7:0	CRC	8-bit CRC polynomial.

The DACx0504 decodes the 32-bit access cycle to compute the CRC remainder on $\overline{CS}$ rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking result (CRC-ERROR bit) on the SDO pin, as shown in Table 5. Additionally, by setting ALM-EN = 1 and ALM-SEL = 0 in the CONFIG register, the SDO/$\overline{ALARM}$ pin is configured as a CRC alarm pin.

Table 5. Write Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 0).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29:28	Reserved	Echo bits 29:28 from previous access cycle (all zeros).
27:24	A[3:0]	Echo address from previous access cycle.
23:8	DO[15:0]	Echo data from previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin, as shown in Table 6. As in the case of a write operation failing the CRC check, the SDO/$\overline{ALARM}$ pin if configured as a CRC alarm pin can be used to indicate a read command CRC failure.

Table 6. Read Operation Error Checking Cycle

BIT	FIELD	DESCRIPTION
31	RW	Echo RW from previous access cycle (RW = 1).
30	CRC-ERROR	Returns a 1 when a CRC error is detected, 0 otherwise.
29:28	Reserved	Echo bits 29:28 from previous access cycle (all zeros).
27:24	A[3:0]	Echo address from previous access cycle.
23:8	DO[15:0]	Readback data requested on previous access cycle.
7:0	CRC	Calculated CRC value of bits 31:8.

8.4.4 Power-Down Mode

The DACx0504 DAC output amplifiers and internal reference can be independently powered down through the CONFIG register. At power-up all output channels and the device internal reference are active by default. A DAC output channel in power-down mode is connected internally to GND through a 1-kΩ resistor.

8.5 Programming

The DACx0504 is controlled through a flexible four-wire serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. The interface provides read and write access to all DACx0504 registers and can also be configured to daisy-chain multiple devices for write operations. The DACx0504 incorporates an optional error checking mode to validate SPI data communication integrity in noisy environments. Table 7 shows the SPI timing requirements. Figure 62 and Figure 63 show the SPI write and read timing diagrams, respectively. Figure 64 shows the digital logic timing diagram.

Table 7. Programming Timing Requirements(1)

		V_{IO} = 1.7 V to 2.7 V			V_{IO} = 2.7 V to 5.5 V			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
SERIAL INTERFACE – WRITE OPERATION								
f_{SCLK}	SCLK frequency			50			50	MHz
$t_{SCLKHIGH}$	SCLK high time	9			9			ns
$t_{SCLKLOW}$	SCLK low time	9			9			ns
t_{SDIS}	SDI setup	5			5			ns
t_{SDIH}	SDI hold	10			10			ns
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup	13			13			ns
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	10			10			ns
t_{CSHIGH}	$\overline{CS}$ high time	15			15			ns
$t_{CSIGNORE}$	SCLK falling edge to $\overline{CS}$ ignore	7			7			ns
SERIAL INTERFACE – READ AND DAISY CHAIN OPERATION, FSDO = 0								
f_{SCLK}	SCLK frequency			12			18	MHz
$t_{SCLKHIGH}$	SCLK high time	35			25			ns
$t_{SCLKLOW}$	SCLK low time	35			25			ns
t_{SDIS}	SDI setup	5			5			ns
t_{SDIH}	SDI hold	10			10			ns
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup	32			20			ns
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	10			10			ns
t_{CSHIGH}	$\overline{CS}$ high time	15			15			ns
t_{SDODLY}	SDO output delay from SCLK rising edge	3.5		33.5	3.5		23	ns
t_{SDODZ}	SDO driven to tri-state	0		30	0		25	ns
$t_{CSIGNORE}$	SCLK falling edge to $\overline{CS}$ ignore	7			7			ns
SERIAL INTERFACE – READ AND DAISY CHAIN OPERATION, FSDO = 1								
f_{SCLK}	SCLK frequency			20			25	MHz
$t_{SCLKHIGH}$	SCLK high time	22			18			ns
$t_{SCLKLOW}$	SCLK low time	22			18			ns
t_{SDIS}	SDI setup	5			5			ns
t_{SDIH}	SDI hold	10			10			ns
t_{CSS}	$\overline{CS}$ to SCLK falling edge setup	32			20			ns
t_{CSH}	SCLK falling edge to $\overline{CS}$ rising edge	10			10			ns
t_{CSHIGH}	$\overline{CS}$ high time	15			15			ns
t_{SDODLY}	SDO output delay from SCLK falling edge	3.5		45	3.5		32	ns
t_{SDODZ}	SDO driven to tri-state	0		30	0		25	ns
$t_{CSIGNORE}$	SCLK falling edge to $\overline{CS}$ ignore	7			7			ns
DIGITAL LOGIC								
$t_{RSTDLYPOR}$	POR reset delay		170	250		170	250	µs
$t_{DACWAIT}$	Sequential DAC output updates	1			1			µs
t_{LDACS}	$\overline{LDAC}$ setup	0			0			ns
t_{LDACH}	$\overline{LDAC}$ hold	5			5			ns

(1) All input signals are specified at t_R = t_F = 1 ns/V (10% to 90% of V_{IO}), timed from a voltage level of (V_{IL} + V_{IH}) / 2, V_{DD} = 2.7 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, V_{REFIN} = 1.25 V to 5.5 V, SDO loaded with 20 pF, and T_A = –40°C to +125°C (unless otherwise noted)

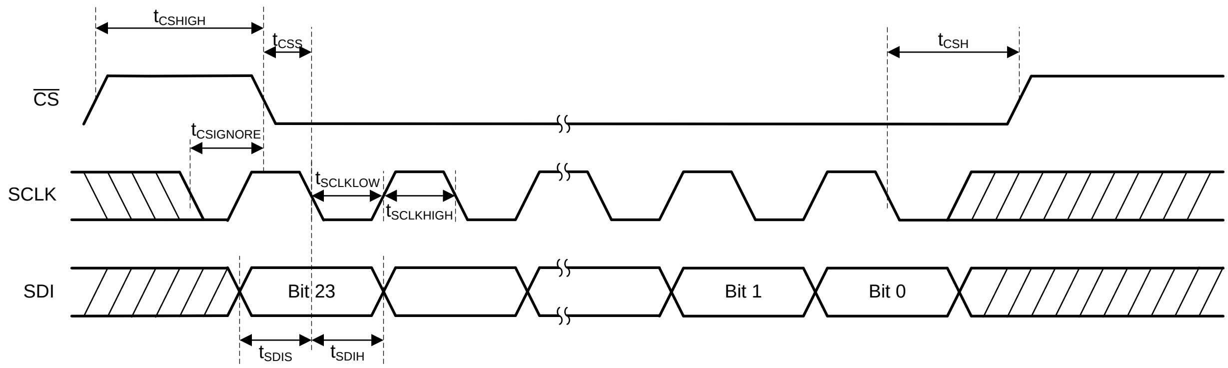


Figure 62. Serial Interface Write Timing Diagram

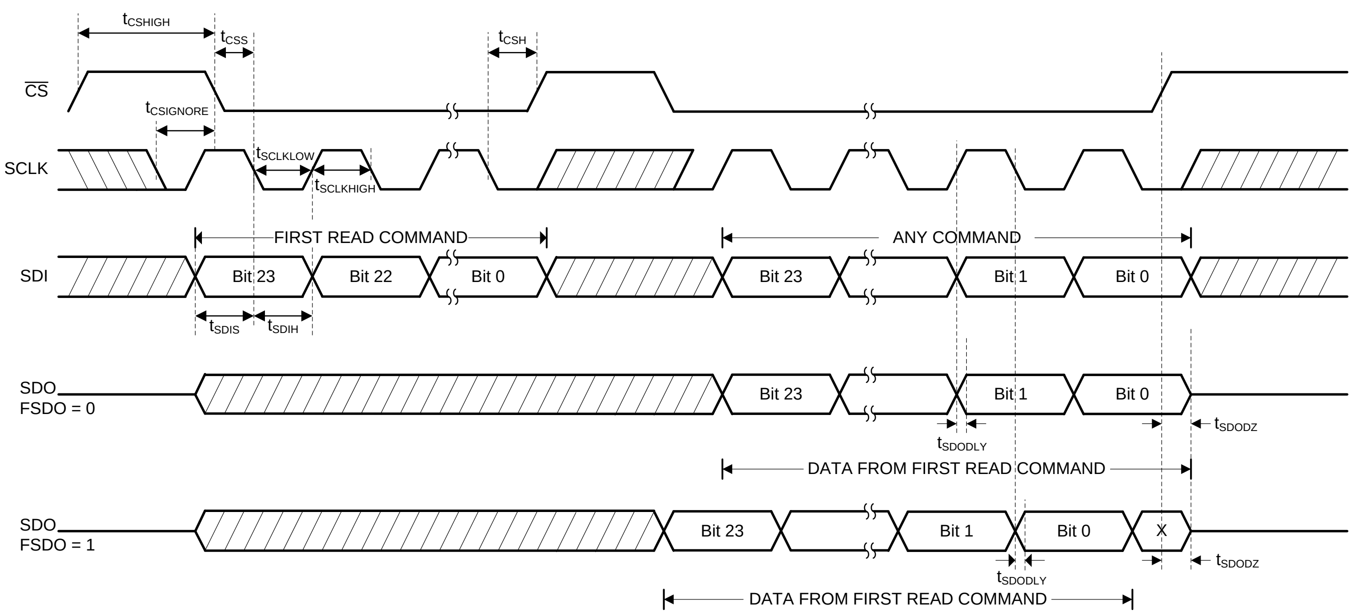


Figure 63. Serial Interface Read Timing Diagram

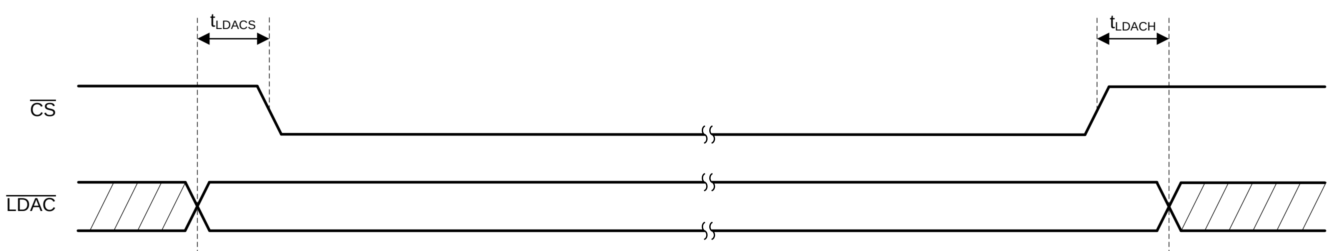


Figure 64. Digital Logic Timing Diagram

8.6 Register Map

Table 8. Register Map

<table>
<tr><th rowspan="2">REGISTER</th><th rowspan="2">TYPE</th><th rowspan="2">RESET</th><th colspan="4">ADDRESS BITS</th><th colspan="16">DATA BITS</th></tr>
<tr><th>A3</th><th>A2</th><th>A1</th><th>A0</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>NOP</td><td>W</td><td>0000</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="16">NOP</td></tr>
<tr><td>DEVICE ID</td><td>R</td><td>—</td><td>0</td><td>0</td><td>0</td><td>1</td><td colspan="14">DEVICEID</td><td colspan="2">VERSIONID</td></tr>
<tr><td>SYNC</td><td>R/W</td><td>FF00</td><td>0</td><td>0</td><td>1</td><td>0</td><td colspan="4">RESERVED</td><td colspan="4">DACx-BRDCAST-EN</td><td colspan="4">RESERVED</td><td colspan="4">DACx-SYNC-EN</td></tr>
<tr><td>CONFIG</td><td>R/W</td><td>0000</td><td>0</td><td>0</td><td>1</td><td>1</td><td colspan="2">RESERVED</td><td>ALM SEL</td><td>ALM EN</td><td>CRC EN</td><td>F SDO</td><td>D SDO</td><td>REF PWDWN</td><td colspan="4">RESERVED</td><td colspan="4">DACx-PWDWN</td></tr>
<tr><td>GAIN</td><td>R/W</td><td>0000</td><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="7">RESERVED</td><td>REF DIV-EN</td><td colspan="4">RESERVED</td><td colspan="4">BUFFx-GAIN</td></tr>
<tr><td>TRIGGER</td><td>W</td><td>0000</td><td>0</td><td>1</td><td>0</td><td>1</td><td colspan="11">RESERVED</td><td>L DAC</td><td colspan="4">SOFT-RESET[3:0]</td></tr>
<tr><td>BRDCAST</td><td>R/W</td><td>0000</td><td>0</td><td>1</td><td>1</td><td>0</td><td colspan="16">BRDCAST-DATA[15:0]</td></tr>
<tr><td>STATUS</td><td>R/W</td><td>0000</td><td>0</td><td>1</td><td>1</td><td>1</td><td colspan="15">RESERVED</td><td>REF ALM</td></tr>
<tr><td>DAC0</td><td>R/W</td><td>0000</td><td>1</td><td>0</td><td>0</td><td>0</td><td colspan="16">DAC0-DATA[15:0]</td></tr>
<tr><td>DAC1</td><td>R/W</td><td>0000</td><td>1</td><td>0</td><td>0</td><td>1</td><td colspan="16">DAC1-DATA[15:0]</td></tr>
<tr><td>DAC2</td><td>R/W</td><td>0000</td><td>1</td><td>0</td><td>1</td><td>0</td><td colspan="16">DAC2-DATA[15:0]</td></tr>
<tr><td>DAC3</td><td>R/W</td><td>0000</td><td>1</td><td>0</td><td>1</td><td>1</td><td colspan="16">DAC3-DATA[15:0]</td></tr>
<tr><td>All Others</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td>—</td><td colspan="16">RESERVED</td></tr>
</table>

8.6.1 NOP Register (address = 0x00) [reset = 0x0000]

Figure 65. NOP Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP															
W															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. NOP Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	NOP	W	0x0000	No operation. Write 0000h for proper no-operation command

8.6.2 DEVICE ID Register (address = 0x01) [reset = 0x---]

Figure 66. DEVICE ID Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICEID														VERSIONID	
R														R	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. DEVICE ID Field Descriptions

Bit	Field	Type	Reset	Description
15:2	DEVICEID	R	----	Device ID: D15 Reserved - 0 D14:12 Resolution - 000 (16-bit); 001 (14-bit); 010 (12-bit) D11:4 Channels - 0100 (4 channels) D7 Reset - Determined by RSTSEL pin. 0 (reset to zero); 1 (reset to midscale) D6:2 Reserved - 00101
1:0	VERSIONID	R	11	Version ID. Subject to change

8.6.3 SYNC Register (address = 0x2) [reset = 0xFF00]

Figure 67. SYNC Register

15	14	13	12	11	10	9	8
Reserved				DAC3-BRDCAST-EN	DAC2-BRDCAST-EN	DAC1-BRDCAST-EN	DAC0-BRDCAST-EN
—				R/W	R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				DAC3-SYNC-EN	DAC2-SYNC-EN	DAC1-SYNC-EN	DAC0-SYNC-EN
—				R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. SYNC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Reserved	—	1111	Reserved for factory use
11	DAC3-BRDCAST-EN	R/W	1	When set to 1 the corresponding DAC is set to update its output after a serial interface write to the BRDCAST register. When cleared to 0 the corresponding DAC output remains unaffected after a serial interface write to the BRDCAST register.
10	DAC2-BRDCAST-EN	R/W	1	
9	DAC1-BRDCAST-EN	R/W	1	
8	DAC0-BRDCAST-EN	R/W	1	
7:4	Reserved	—	0000	Reserved for factory use
3	DAC3-SYNC-EN	R/W	0	When set to 1 the corresponding DAC output is set to update in response to an LDAC trigger (synchronous mode). When cleared to 0 the corresponding DAC output is set to update immediately on a $\overline{CS}$ rising edge (asynchronous mode).
2	DAC2-SYNC-EN	R/W	0	
1	DAC1-SYNC-EN	R/W	0	
0	DAC0-SYNC-EN	R/W	0	

8.6.4 CONFIG Register (address = 0x3) [reset = 0x0000]

Figure 68. CONFIG Register

15	14	13	12	11	10	9	8
Reserved		ALM-SEL	ALM-EN	CRC-EN	FSDO	DSDO	REF-PWDWN
—		R/W	R/W	R/W	R/W	R/W	R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				DAC3-PWDWN	DAC2-PWDWN	DAC1-PWDWN	DAC0-PWDWN
—				R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	Reserved	—	00	Reserved for factory use
13	ALM-SEL	R/W	0	ALARM select. 0: ALARM pin is CRC-ERROR 1: ALARM pin is REF-ALARM
12	ALM-EN	R/W	0	Configure SDO/ALARM pin. When 1: SDO/ALARM pin is an active-low, open-drain, alarm pin. An external 10 kΩ pullup resistor to V_{IO} is required. FSDO and DSDO bits are ignored. When 0: SDO/ALARM pin is a serial interface, push-pull, SDO pin
11	CRC-EN	R/W	0	CRC enable bit. Set to 1 to enable CRC. Set to 0 to disable
10	FSDO	R/W	0	Fast SDO bit (half-cycle speedup). When 0, SDO updates on an SCLK rising edge. When 1, SDO updates a half-cycle earlier, during an SCLK falling edge.
9	DSDO	R/W	0	Disable SDO bit. When 1, SDO is always tri-stated. When 0, SDO is driven while CS is low, and tri-stated while CS is high
8	REF-PWDWN	R/W	0	When set to 1 disables the device internal reference
7:4	Reserved	—	0000	Reserved for factory use
3	DAC3-PWDWN	R/W	0	When set to 1 the corresponding DAC is set in power-down mode and its output is connected to GND through a 1 kΩ internal resistor.
2	DAC2-PWDWN	R/W	0	
1	DAC1-PWDWN	R/W	0	
0	DAC0-PWDWN	R/W	0	

8.6.5 GAIN Register (address = 0x04) [reset = 0x---]

Figure 69. GAIN Register

15	14	13	12	11	10	9	8
Reserved							REFDIV-EN
—							R/W
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved				BUFF3-GAIN	BUFF2-GAIN	BUFF1-GAIN	BUFF0-GAIN
—				R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	Reserved	—	0	Reserved for factory use.
8	REFDIV-EN	R/W	0/1	When set to 1 the reference voltage is internally divided by a factor of 2. When cleared to 0 the reference voltage is unaffected. Default value is determined by the REFDIV pin.
7:4	Reserved	—	0000	Reserved for factory use
3	BUFF3-GAIN	R/W	0/1	When set to 1 the buffer amplifier for corresponding DAC has a gain of 2. When cleared to 0 the buffer amplifier for corresponding DAC has a gain of 1. Default value is determined by the GAIN pin.
2	BUFF2-GAIN	R/W	0/1	
1	BUFF1-GAIN	R/W	0/1	
0	BUFF0-GAIN	R/W	0/1	

8.6.6 TRIGGER Register (address = 0x05) [reset = 0x0000]

Figure 70. TRIGGER Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved											LDAC	SOFT-RESET[3:0]			
—											W	W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
15:5	Reserved	—	0	Reserved for factory use.
4	LDAC	W	0	Set this bit to 1 to synchronously load those DACs that have been set in synchronous mode in the SYNC register.
3:0	SOFT-RESET[3:0]	W	0x0	When set to the reserved code 1010 resets the device to its default state.

8.6.7 BRDCAST Register (address = 0x6) [reset = 0x0000]

Figure 71. BRDCAST Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRDCAST-DATA[15:0]															
R/W															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. BRDCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BRDCAST-DATA[15:0]	R/W	0x0000	Writing to the BRDCAST register forces those DAC channels that have been set to broadcast in the SYNC register to update their active data register with the BRDCAST-DATA value. Data are MSB aligned in straight binary format and follows the format below: DAC80504: { DATA[15:0] } DAC70504: { DATA[13:0], x, x } DAC60504: { DATA[11:0], x, x, x, x } x – Don't care bits

8.6.8 STATUS Register (address = 0x7) [reset = 0x0000]

Figure 72. STATUS Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															REF-ALM
—															R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	—	0	Reserved for factory use.
0	REF-ALM	R	0	Reference alarm bit. Reads 1 when the difference between V_{REF}/DIV and V_{DD} is below the required minimum analog threshold. Reads 0 otherwise.

8.6.9 DACx Register (address = 0x8 to 0xF) [reset = 0x0000 or 0x8000]

Figure 73. DACx Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DACx-DATA[15:0]															
R/W															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. DACx Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DACx-DATA[15:0]	R/W	0x0000 or 0x8000	Stores the 16- or 14-bit data to be loaded to DACx in MSB aligned straight binary format. The default value is determined by the RSTSEL pin. Data follows the format below: DAC80504: { DATA[15:0] } DAC70504: { DATA[13:0], x, x } DAC60504: { DATA[11:0], x, x, x, x } x – Don't care bits

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The high linearity, small package size and wide temperature range make the DACx0504 suitable in applications such as optical networking, wireless infrastructure, industrial automation and data acquisition systems. The device incorporates a 2.5 V internal reference with an internal reference divider circuit that enables full-scale DAC output voltages of 1.25 V, 2.5 V, or 5 V.

9.1.1 Interfacing to a Microcontroller

Figure 74 displays a typical serial interface that may be observed when connecting the DACx0504 SPI serial interface to a (master) microcontroller type platform. The setup for the interface is as follows: the microcontroller output SPI CLK drives the SCLK pin of the DACx0504, while the DACx0504 SDI pin is driven by the MOSI pin of the microcontroller. The $\overline{CS}$ pin of the DACx0504 can be asserted from a general program input/output pin of the microcontroller. When data are to be transmitted to the DACx0504, the $\overline{CS}$ pin is taken low. The data from the microcontroller is then transmitted to the DACx0504, totaling 24 bits latched into the DACx0504 device through the falling edge of SCLK. $\overline{CS}$ is then brought high after the completed write. The DACx0504 requires data with the MSB as the first bit received.

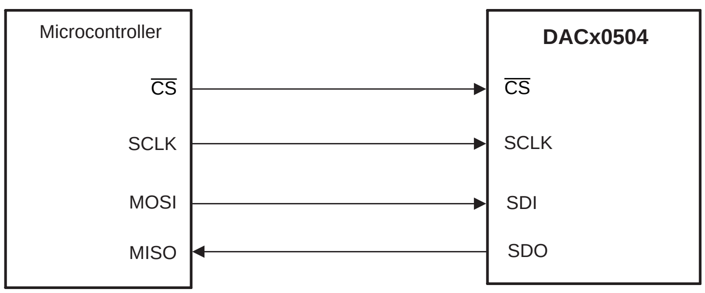


Figure 74. Typical Serial Interface

Application Information (continued)

9.1.2 Programmable Current Source Circuit

The DACx0504 can be integrated into the circuit in Figure 75 to implement an improved Howland current pump for precise voltage to current conversions. Bidirectional current flow and high voltage compliance are two features of the circuit. With a matched resistor network, the load current of the circuit is shown by Equation 2.

$$I_L = \frac{(R2 + R3)/R1}{R3} \times V_{REF} \times \frac{CODE}{2^n} \quad (2)$$

The value of R3 in Equation 2 can be reduced to increase the output current drive of U3. U3 can drive ±20 mV in both directions with voltage compliance limited up to 15 V by the U3 voltage supply. Elimination of the circuit compensation capacitor C1 in the circuit is not suggested as a result of the change in the output impedance Z_O, according to Equation 3.

$$Z_O = \frac{(R1')(R3)(R1 + R2)}{R1(R2' + R3') - R1'(R2 + R3)} \quad (3)$$

As shown in Equation 3, with matched resistors, Z_O is infinite and the circuit is optimum for use as a current source. However, if unmatched resistors are used, Z_O is positive or negative with negative output impedance being a potential cause of oscillation. Therefore, by incorporating C1 into the circuit, possible oscillation problems are eliminated. The value of C1 can be determined for critical applications; for most applications, however, a value of several pF is suggested.

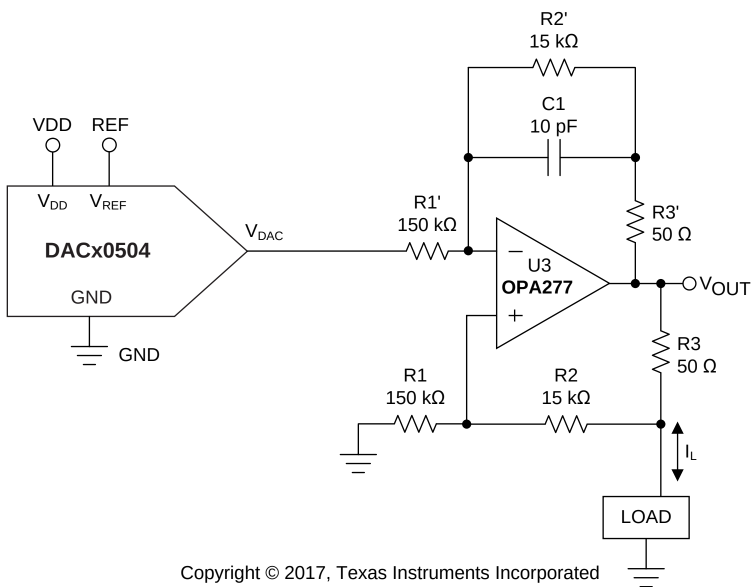


Figure 75. Programmable Bidirectional Current Source Circuit

9.2 Typical Application

The DACx0504 is designed for single-supply operation; however, a bipolar output is also possible using the circuit shown in Figure 76.

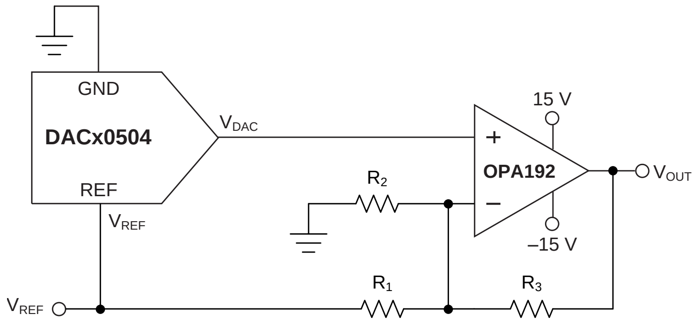


Figure 76. Bipolar Operation Using the DACx0504

9.2.1 Design Requirements

The circuit shown in Figure 76 gives a bipolar output voltage at V_{OUT}. When GAIN = 1, V_{OUT} can be calculated using Equation 4:

$$V_{OUT}(CODE) = \left[\left(V_{REF} \times \frac{CODE}{2^n}\right)\left(1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right) - \left(V_{REF} \times \frac{R_3}{R_1}\right)\right]$$

where

- V_{OUT}(CODE) = output voltage versus code
- CODE = 0 to 2^n – 1. This is the digital code loaded to the DAC
- V_{REF} = reference voltage applied to the DACx0504
- n = resolution in bits (4)

Table 18. Design Parameters

PARAMETER	VALUE
V_{OUT}	±10 V
V_{REF}	2.5 V
n	12

9.2.2 Detailed Design Procedure

The bipolar output span can be calculated through Equation 4 by defining a few parameters, the first being the value for the reference voltage. Once a reference voltage is chosen, the gain resistors can be set accordingly by determining the desired V_{OUT} at code 0 and code 2^n. For a V_{REF} of 2.5 V and a desired output voltage range of ±10 V the calculation is as follows.

CODE = 0:

$$V_{OUT}(0) = -\left(V_{REF} \times \frac{R_3}{R_1}\right) = -\left(2.5V \times \frac{R_3}{R_1}\right) \quad (5)$$

Setting the equation to minimum output span, $V_{OUT}(0)$ = –10 V, will reduce the equation to: R_3/R_1 = 4:

CODE = 4096:

Setting the equation to maximum output scan, $V_{OUT}(4096)$ = 10 V, and R_3/R_1 = 4 will reduce the equation to: R_3/R_2 = 3

It is important to note that the maximum code of a 12-bit DAC is 4095; code 4096 was used to simplify the equation above. For practical use, the true output span will encompass a range of –10 V to (10 V – 1 LSB), which in this case is –10 V to 9.995 V.

9.2.3 Application Curve

The ±10 V output span with a reference voltage of 2.5 V can be achieved by using values of 30 kΩ, 10 kΩ, and 7.5 kΩ for R3, R2, and R1, respectively. A curve to illustrate this output span is shown in Figure 77. For this example, 1% tolerance resistors were used in evaluating bipolar operation.

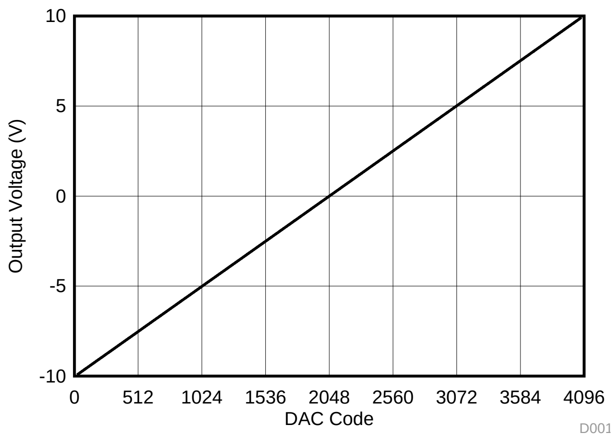


Figure 77. Bipolar Operation

10 Power Supply Recommendations

The DACx0504 operates within the specified V_{DD} supply range of 2.7 V to 5.5 V, and V_{IO} supply range of 1.7 V to 5.5 V. The DACx0504 does not require specific supply sequencing.

The V_{DD} supply must be well-regulated and low-noise. Switching power supplies and dc-dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output. In order to further minimize noise from the power supply, include a 1-µF to 10-µF capacitor and 0.1-µF bypass capacitor. The current consumption on the V_{DD} pin, the short-circuit current limit, and the load current for the device is listed in the *Electrical Characteristics*. The power supply must meet the aforementioned current requirements.

11 Layout

11.1 Layout Guidelines

A precision analog component requires careful layout, the list below provides some insight into good layout practices.

- Bypass all power supply pins to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 0.1-µF to 0.22-µF ceramic with a X7R or NP0 dielectric.
- Place power supplies and REF bypass capacitors close to the pins to minimize inductance and optimize performance.
- Use a high-quality ceramic type NP0 or X7R for its optimal performance across temperature, and very low dissipation factor.
- The digital and analog sections must have proper placement with respect to the digital pins and analog pins of the DACx0504 device. The separation of analog and digital blocks minimizes coupling into neighboring blocks, as well as interaction between analog and digital return currents.

11.2 Layout Example

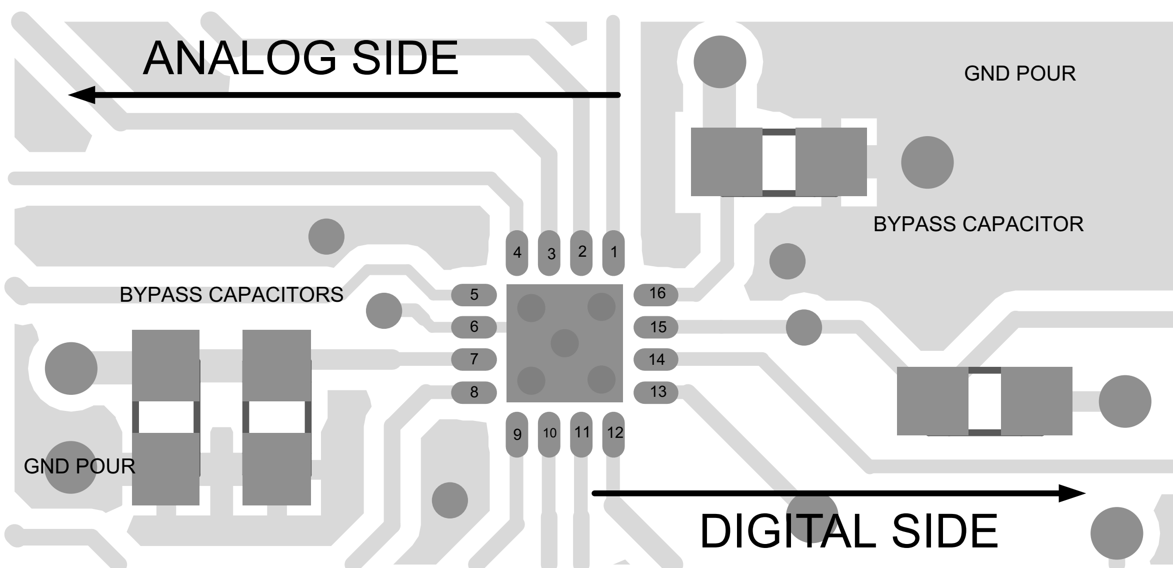


Figure 78. DACx0504 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following: *DACx0504 Evaluation Module User's Guide*

12.2 Related Links

Table 19 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 19. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DAC80504	Click here	Click here	Click here	Click here	Click here
DAC70504	Click here	Click here	Click here	Click here	Click here
DAC60504	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC60504BRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	654B	Samples
DAC60504BRTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	654B	Samples
DAC70504RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	70504	Samples
DAC70504RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	70504	Samples
DAC80504RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(80504, 854)	Samples
DAC80504RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(80504, 854)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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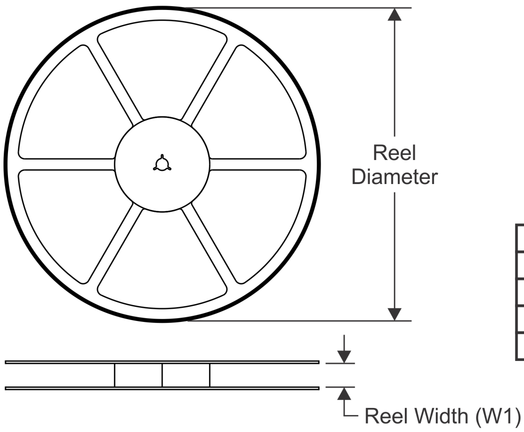
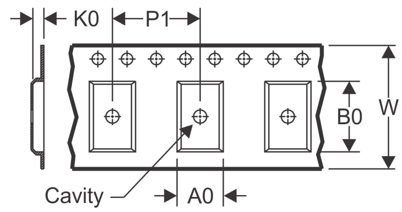
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

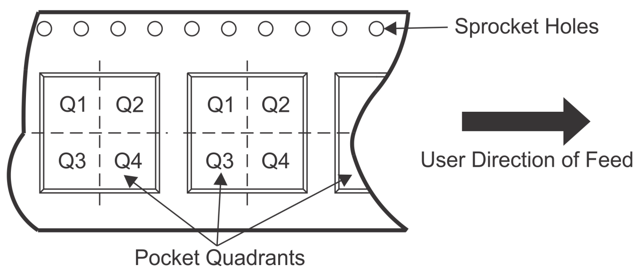


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

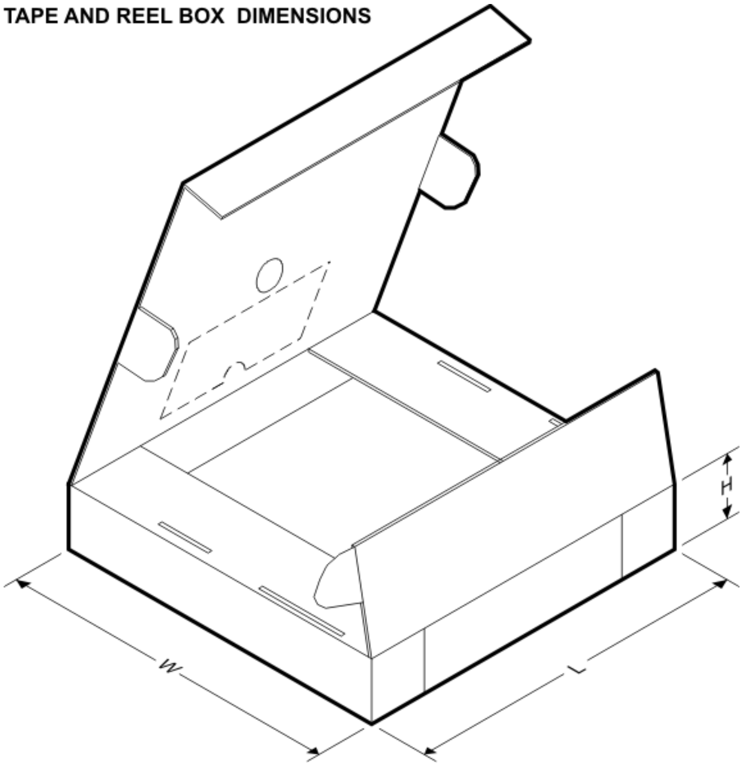
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC60504BRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
DAC60504BRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
DAC70504RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
DAC70504RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
DAC80504RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
DAC80504RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

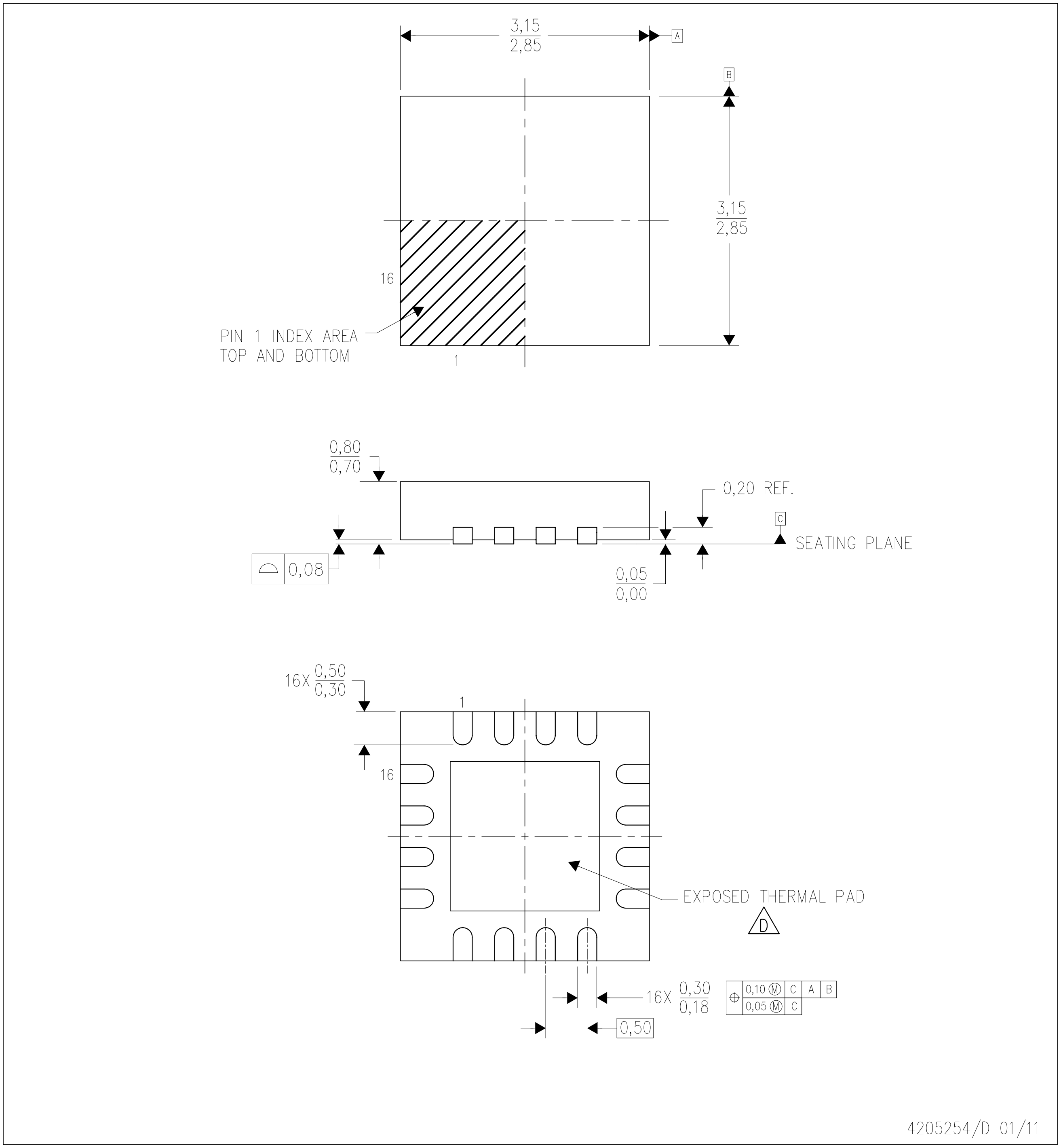
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC60504BRTER	WQFN	RTE	16	3000	367.0	367.0	38.0
DAC60504BRTET	WQFN	RTE	16	250	213.0	191.0	35.0
DAC70504RTER	WQFN	RTE	16	3000	367.0	367.0	38.0
DAC70504RTET	WQFN	RTE	16	250	213.0	191.0	35.0
DAC80504RTER	WQFN	RTE	16	3000	367.0	367.0	38.0
DAC80504RTET	WQFN	RTE	16	250	213.0	191.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

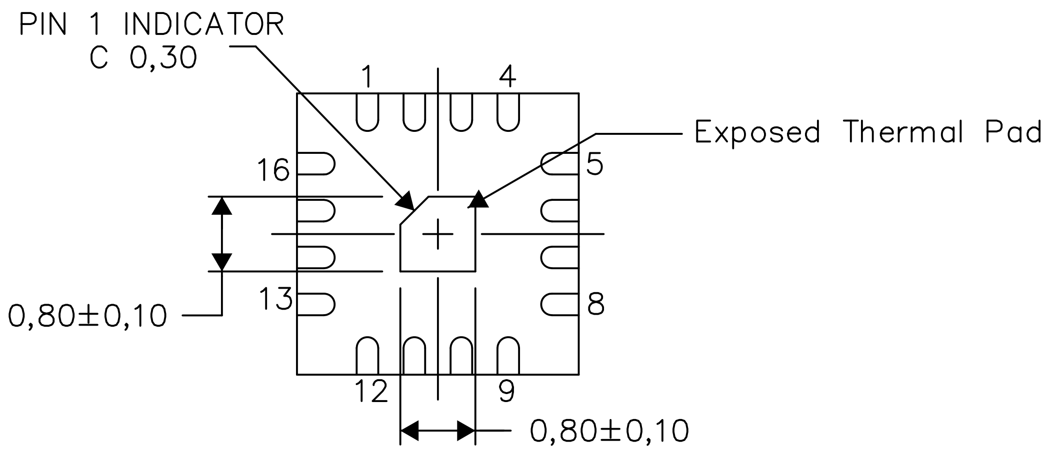
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



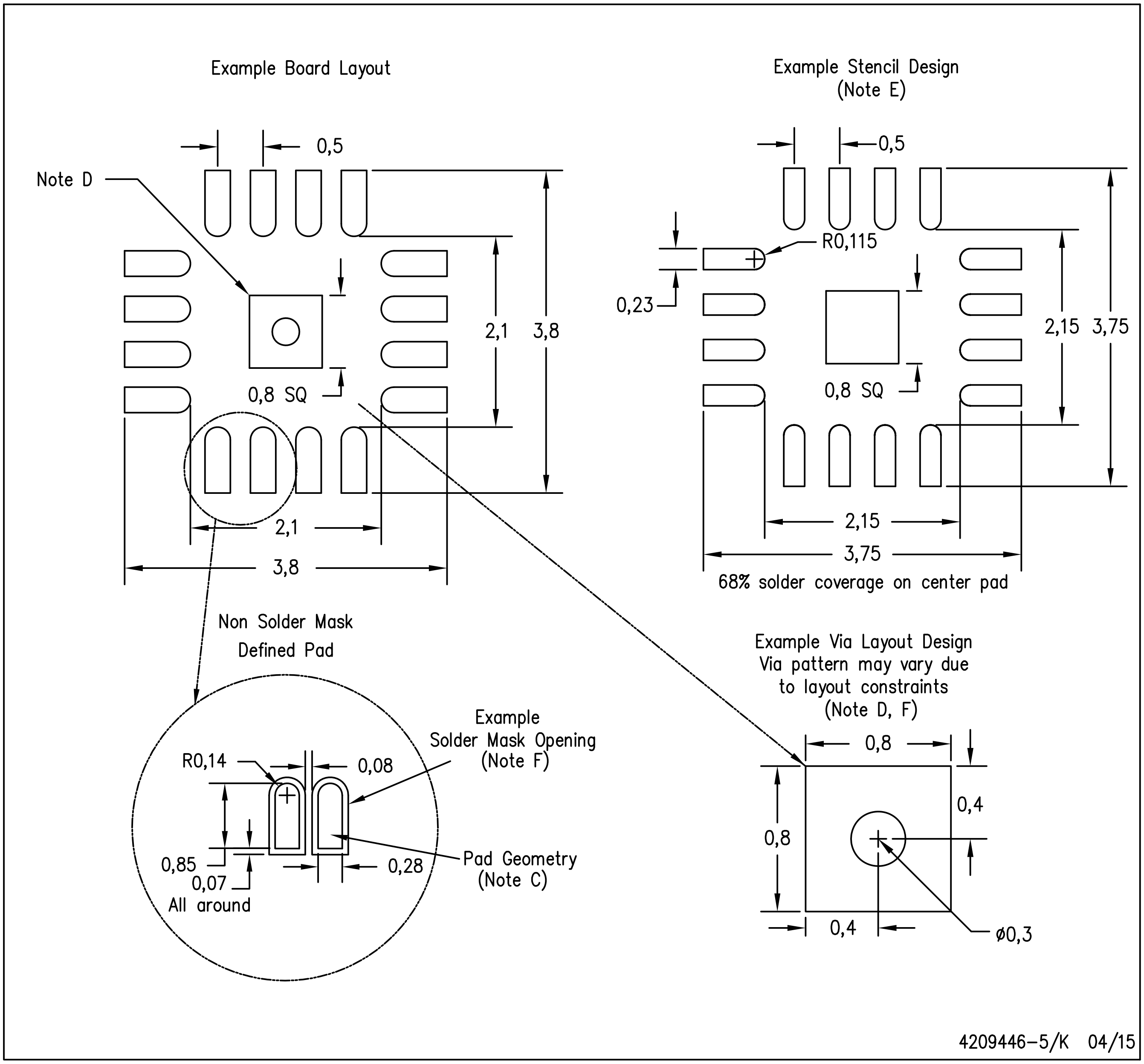
Bottom View

Exposed Thermal Pad Dimensions

4206446–5/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.