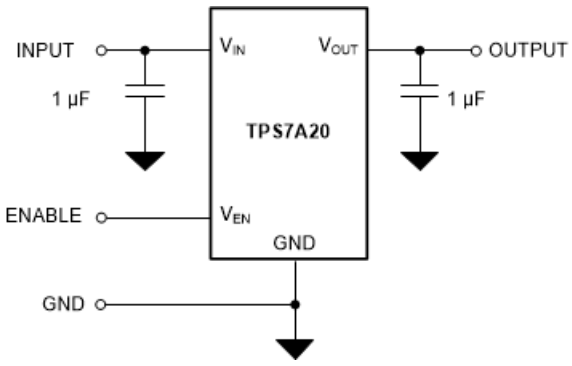
# TPS7A20 300-mA, Ultra-Low-Noise, Low-$I_Q$, High PSRR LDO

## 1 Features

- Low output voltage noise: 7 $\mu V_{RMS}$
  - No noise-bypass capacitor required
- High PSRR: 95 dB at 1 kHz
- Very low $I_Q$: 6.5 µA
- Input voltage range: 1.6 V to 6.0 V
- Output voltage range: 0.8 V to 5.5 V
- Output voltage tolerance: ±1.5% (max)
- Very low dropout:
  - 140 mV (max) at 300 mA ($V_{OUT}$ = 3.3 V)
  - 145 mV (max) at 300 mA ($V_{OUT}$ = 3.3 V, DBV)
- Low inrush current
- Smart enable pulldown
- Stable with 1-µF minimum ceramic output capacitor
- Packages:
  - 1-mm × 1-mm X2SON
  - 0.603-mm × 0.603-mm DSBGA
  - 2.90-mm × 1.60-mm SOT23-5

## 2 Applications

- Smartphones and tablets
- IP network cameras
- Portable medical equipment
- Smart meters and field transmitters
- Motor drives
- Wearables




**Simplified Schematic**

## 3 Description

The TPS7A20 is an ultra-small, low-dropout (LDO) linear regulator that can source 300 mA of output current. The TPS7A20 is designed to provide low noise, high PSRR, and excellent load and line transient performance that can meet the requirements of RF and other sensitive analog circuits. Using innovative design techniques, the TPS7A20 offers an ultra-low noise performance without the addition of a noise bypass capacitor. The TPS7A20 also provides the advantage of low quiescent current, which can be ideal for battery-powered applications. With an input voltage range of 1.6 V to 6.0 V and an output range of 0.8 V to 5.5 V, the TPS7A20 can be used for a wide variety of applications. The device uses a precision reference circuit to provide a maximum accuracy of 1.5% over load, line, and temperature variations.

The TPS7A20 features an internal soft-start to lower the inrush current, thus minimizing the input voltage drop during start up. The device is stable with small ceramic capacitors, allowing for a small overall solution size.

The TPS7A20 has a smart enable input circuit with an internally controlled pulldown resistor that keeps the LDO disabled even when the EN pin is left floating and helps eliminate the external components used to pulldown the EN pin.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPS7A20 | X2SON (4) | 1.00 mm × 1.00 mm |
| | DSBGA (4) | 0.603 mm × 0.603 mm |
| | SOT-23 (5) | 2.90 mm × 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision D (July 2021) to Revision E (December 2021) | Page |
|---|---|
| • Changed YCJ and YCK packages from *Preview* to *Production Data* | 1 |
| • Changed maximum current limit for YCJ and YCK packages | 6 |
| • Changed minimum UVLO thresholds for YCJ and YCK packages | 6 |

| Changes from Revision C (November 2020) to Revision D (July 2021) | Page |
|---|---|
| • Added YCJ package to document | 1 |
| • Changed maximum operating junction temperature $T_J$ to 150°C | 5 |
| • Added thermal information for DSBGA packages | 6 |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# 5 Pin Configuration and Functions

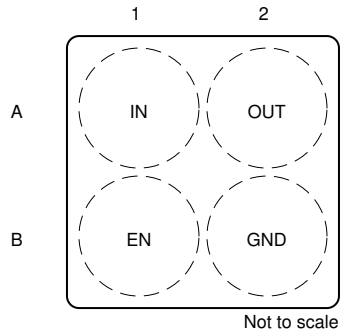


**Figure 5-1. YCJ and YCK Packages, 4-Pin DSBGA (Top View)**

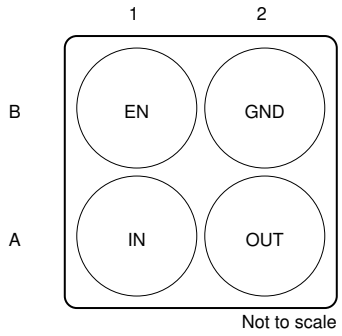


**Figure 5-2. YCJ and YCK Packages, 4-Pin DSBGA (Bottom View)**

**Pin Functions: DSBGA**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| A1 | IN | I | Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible. |
| A2 | OUT | O | Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on $V_{OUT}$ when the regulator is in shutdown mode ($V_{EN} < V_{EN(LOW)}$). |
| B1 | EN | I | Enable input. A low voltage ($< V_{EN(LOW)}$) on this input turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default. When $V_{EN} > V_{EN(HI)}$, the 500-kΩ pulldown is disconnected to reduce input current. |
| B2 | GND | — | Common ground. |

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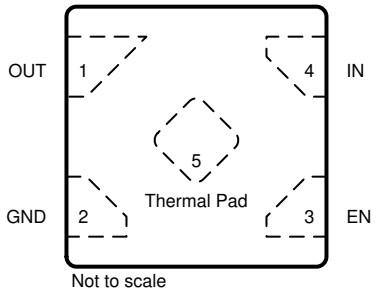


**Figure 5-3. DQN Package, 4-Pin X2SON (Top View)**

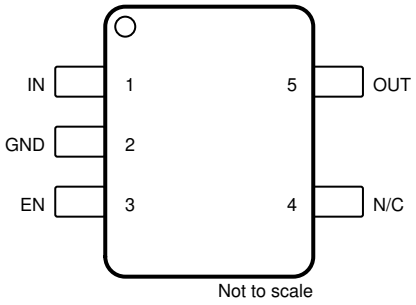


**Figure 5-4. DBV Package, 5-Pin SOT-23 (Top View)**

**Pin Functions: X2SON, SOT-23**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | X2SON | SOT-23 | | |
| IN | 4 | 1 | I | Input voltage supply. For best transient response and to minimize input impedance, use the nominal value or larger capacitor from IN to ground as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible. |
| OUT | 1 | 5 | O | Regulated output voltage. A low equivalent series resistance (ESR) capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger capacitor listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible. An internal 150-Ω (typical) pulldown resistor prevents a charge from remaining on $V_{OUT}$ when the regulator is in shutdown mode ($V_{EN} < V_{EN(LOW)}$). |
| EN | 3 | 3 | I | Enable input. A low voltage ($< V_{EN(LOW)}$) on this pin turns the regulator off and discharges the output pin to GND. A high voltage ($> V_{EN(HI)}$) on this pin enables the regulator output. This pin has an internal 500-kΩ pulldown resistor to hold the regulator off by default. When $V_{EN} > V_{EN(HI)}$, the 500-kΩ pulldown is disconnected to reduce input current. |
| GND | 2 | 2 | — | Common ground. |
| N/C | — | 4 | — | No internal electrical connection. |
| Thermal Pad | 5 | — | — | Thermal pad for the X2SON package. Connect this pad to GND or leave floating. Do not connect to any potential other than GND. Connect the thermal pad to a large-area ground plane for best thermal performance. |


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (3)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 6.5 | V |
| | $V_{OUT}$ | –0.3 | 6.5 or $V_{IN}$ + 0.3 (2) | |
| | $V_{EN}$ | –0.3 | 6.5 | |
| Current | Maximum output(4) | Internally limited | | A |
| Temperature | Operating junction, $T_J$ | –40 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum value of $V_{OUT}$ is the lesser of 6.5 V or ($V_{IN}$ + 0.3 V).
(3) All voltages are with respect to the GND pin.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input supply voltage | 1.6 | | 6.0 | V |
| $V_{EN}$ | Enable input voltage | 0 | | 6.0 | V |
| $V_{OUT}$ | Nominal output voltage range | 0.8 | | 5.5 | V |
| $I_{OUT}$ | Output current | 0 | | 300 | mA |
| $C_{IN}$ | Input capacitor(2) | | 1 | | µF |
| $C_{OUT}$ | Output capacitor(3) | 1 | | 200 | µF |
| ESR | Output capacitor effective series resistance | | | 100 | mΩ |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.47 µF minimum is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system-level instability such as ringing or oscillation, especially in the presence of load transients.
(3) Effective output capacitance of 0.47 µF minimum and 200 µF maximum is required for stability.

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## 6.4 Thermal Information

| THERMAL METRIC[1] | | TPS7A20 | | | | UNIT |
|---|---|---|---|---|---|---|
| | | DBV (SOT-23) | DQN (X2SON) | YCJ (DSBGA) | YCK (DSBGA) | |
| | | 5 PINS | 4 PINS | 4 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 187.1 | 166.1 | 199.6 | 201.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 85.5 | 103.6 | 2.8 | 2.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 54.4 | 110.6 | 67.5 | 69.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 27.1 | 3.0 | 1.4 | 1.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 54.1 | 103.3 | 67.4 | 69.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 98.8 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, $V_{EN}$ = 1.0 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF (unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta V_{OUT}$ | Output voltage tolerance | $V_{IN}$ = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, $I_{OUT}$ = 1 mA to 300 mA, $V_{OUT}$ ≥ 1.85 V (DQN, YCJ, YCK packages) | | –1.5 | | 1.5 | % |
| | | $V_{IN}$ = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, $I_{OUT}$ = 1 mA to 300 mA, $V_{OUT}$ ≥ 2.8 V (DBV package) | | -1.5 | | 1.5 | |
| | | $V_{IN}$ = ($V_{OUT(NOM)}$ + 0.5 V) to 6.0 V, $I_{OUT}$ = 1 mA to 300 mA $V_{OUT}$ < 1.85 V (DQN, YCJ, YCK packages) | | –30 | | 30 | mV |
| | | $V_{IN}$ = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, $I_{OUT}$ = 1 mA to 300 mA, $V_{OUT}$ < 2.8 V (DBV package) | | -40 | | 40 | |
| $\Delta V_{OUT}$ | Line regulation | $V_{IN}$ = ($V_{OUT(NOM)}$ + 0.3 V) to 6.0 V, $I_{OUT}$ = 1 mA | | | 0.03 | | %/V |
| $\Delta V_{OUT}$ | Load regulation | $I_{OUT}$ = 1 mA to 300 mA (DQN, YCJ, YCK packages) | | | 13 | | mV |
| | | $I_{OUT}$ = 1 mA to 300 mA (DBV package) | | | 19 | | |
| $I_{GND}$ | Quiescent ground current | $V_{EN}$ = $V_{IN}$ = 6 V, $I_{OUT}$ = 0 mA | $T_J$ = 25°C | | 6.5 | 8.5 | µA |
| | | | $T_J$ = –40°C to 85°C | | | 10 | |
| | | | $T_J$ = –40°C to 125°C | | | 15 | |
| | | $V_{EN}$ = $V_{IN}$ = 6 V, $I_{OUT}$ = 300 mA | | | 2000 | | |
| $I_{SHDN}$ | Shutdown ground current | $V_{EN}$ = 0 V (disabled), $V_{IN}$ = 6.0 V, $T_J$ = 25°C | | | 0.07 | 0.2 | µA |
| $I_{GND(DO)}$ | $I_{GND}$ in dropout | $V_{IN}$ ≤ $V_{OUT(NOM)}$ , $I_{OUT}$ = 0 mA, $V_{EN}$ = $V_{IN}$ | | | 6.5 | 15 | µA |
| $V_{DO}$ | Dropout voltage | $I_{OUT}$ = 300 mA, $V_{OUT}$ = 95% x $V_{OUT(NOM)}$, (DQN, YCJ, YCK packages unless otherwise noted) | 0.8 V ≤ $V_{OUT}$ < 1.0 V[1] | | | 690 | mV |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V[1] | | | 490 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V[1] | | | 355 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 2.5 V | | | 200 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 2.5 V (DBV) | | | 205 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 5.5 V | | | 140 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 5.5 V (DBV) | | | 145 | |


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## 6.5 Electrical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, $V_{EN}$ = 1.0 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF (unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 0.9 x $V_{OUT(NOM)}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V | $V_{OUT}$ < 1.5 V (YCJ, YCK packages) | 360 | 520 | 770 | mA |
| | | $V_{OUT}$ = 0.9 x $V_{OUT(NOM)}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V | $V_{OUT}$ < 1.5 V (DQN package) | 360 | 520 | 730 | |
| | | $V_{OUT}$ = $V_{OUT(NOM)}$ - 150 mV, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V | $V_{OUT}$ < 1.5 V (DBV package) | 360 | 520 | 730 | |
| | | $V_{OUT}$ = 0.9 x $V_{OUT(NOM)}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V | $V_{OUT}$ ≥ 1.5 V (YCJ, YCK packages) | 360 | 520 | 770 | |
| | | $V_{OUT}$ = 0.9 x $V_{OUT(NOM)}$, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V | $V_{OUT}$ ≥ 1.5 V (DQN package) | 360 | 520 | 730 | |
| $I_{SC}$ | Short-circuit current limit | $V_{OUT}$ = 0 V | | | 160 | | mA |
| PSRR | Power-supply rejection ratio | $I_{OUT}$ = 20 mA, $V_{IN}$ = $V_{OUT}$ + 1.0 V | f = 100 Hz | | 95 | | dB |
| | | | f = 1 kHz | | 95 | | |
| | | | f = 10 kHz | | 75 | | |
| | | | f = 100 kHz | | 75 | | |
| | | | f = 1 MHz | | 45 | | |
| | | $I_{OUT}$ = 300 mA, $V_{IN}$ = $V_{OUT}$ + 1.0 V | f = 100 Hz | | 65 | | |
| | | | f = 1 kHz | | 92 | | |
| | | | f = 10 kHz | | 75 | | |
| | | | f = 100 kHz | | 60 | | |
| | | | f = 1 MHz | | 40 | | |
| $V_N$ | Output noise voltage | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 2.8 V | $I_{OUT}$ = 300 mA | | 7 | | $µV_{RMS}$ |
| | | | $I_{OUT}$ = 1 mA | | 10 | | |
| $R_{PULLDOWN}$ | Output automatic discharge pulldown resistance | $V_{EN}$ < $V_{EN(LOW)}$ (output disabled), $V_{IN}$ = 3.1 V | | | 150 | | Ω |
| $T_{SD}$ | Thermal shutdown | $T_J$ rising | | | 165 | | °C |
| | | $T_J$ falling | | | 140 | | |
| $V_{EN(LOW)}$ | Low input threshold | $V_{IN}$ = 1.6 V to 6.0 V, $V_{EN}$ falling until the output is disabled | | | | 0.3 | V |
| $V_{EN(HI)}$ | High input threshold | $V_{IN}$ = 1.6 V to 6.0 V $V_{EN}$ rising until the output is enabled | | 0.9 | | | V |
| $V_{UVLO}$ | UVLO threshold | $V_{IN}$ rising (YCJ and YCK packages) | | 1.11 | 1.35 | 1.59 | V |
| | | $V_{IN}$ rising (DBV and DQN packages) | | 1.17 | 1.35 | 1.59 | |
| | | $V_{IN}$ rising (YCJ and YCK packages) | | 1.05 | 1.3 | 1.55 | |
| | | $V_{IN}$ falling (DBV and DQN packages) | | 1.11 | 1.3 | 1.55 | |
| $V_{UVLO(HYST)}$ | UVLO hysteresis | | | | 50 | | mV |
| $I_{EN}$ | EN input leakage current | $V_{EN}$ = 6.0 V and $V_{IN}$ = 6.0 V | | | 90 | 250 | nA |
| $R_{EN(PULL-DOWN)}$ | Smart enable pulldown resistor | $V_{EN}$ = 0.25 V | | | 500 | | KΩ |

(1) Design simulation data only

## 6.6 Switching Characteristics

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6V, whichever is greater, $V_{EN}$ = 1.0 V, $I_{OUT}$ = 1 mA, $C_{IN}$= 1 µF, $C_{OUT}$ = 1 µF (unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STR}$ | Start-up time | From $V_{EN}$ > $V_{EN(HI)}$ to $V_{OUT}$ = 95% of $V_{OUT(NOM)}$, | | 750 | 1150 | µs |

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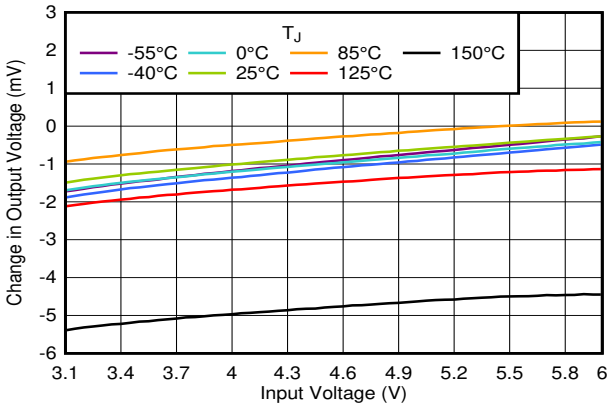
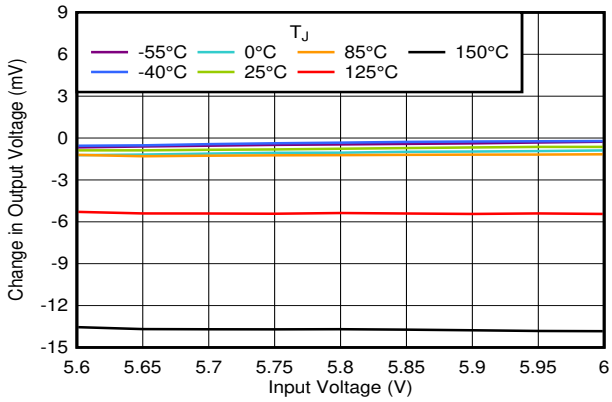
## 6.7 Typical Characteristics

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



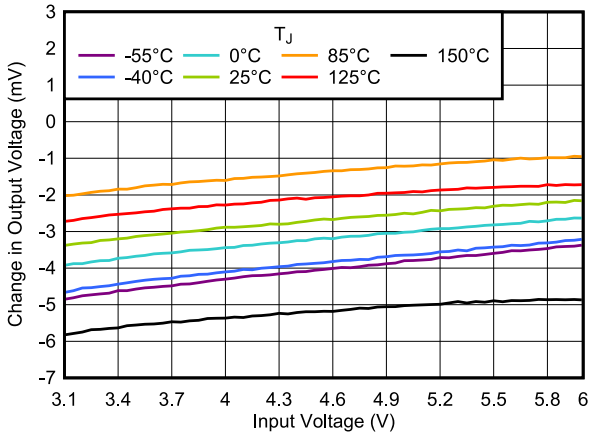

$V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-1. Line Regulation vs $V_{IN}$**



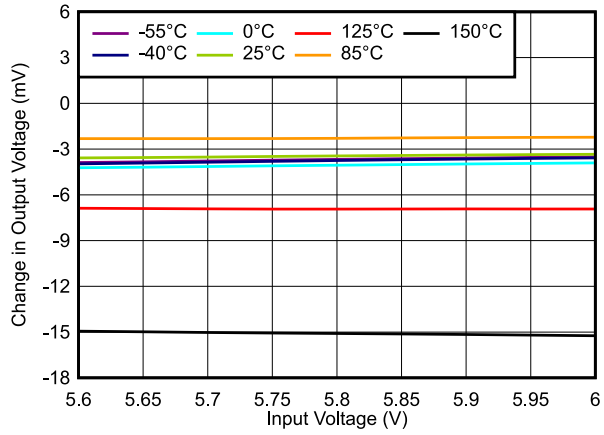

$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-2. Line Regulation vs $V_{IN}$**



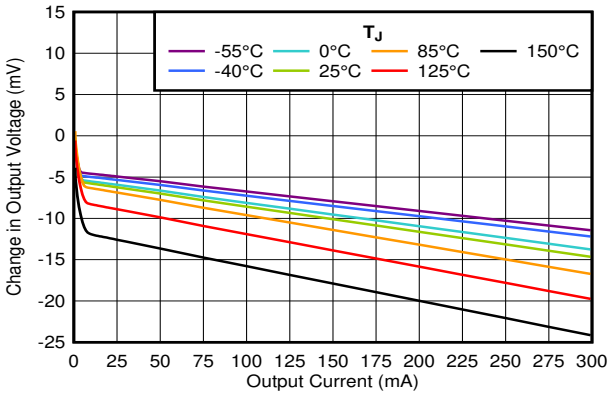

$V_{EN}$ = 1 V, DBV package

**Figure 6-3. Line Regulation vs $V_{IN}$**



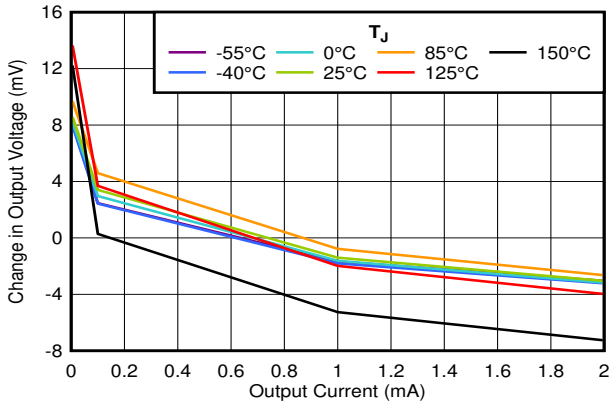

$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-4. Line Regulation vs $V_{IN}$**




$V_{IN}$ = 3.1 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-5. Load Regulation vs $I_{OUT}$**




$V_{IN}$ = 3.1 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-6. Load Regulation vs $I_{OUT}$**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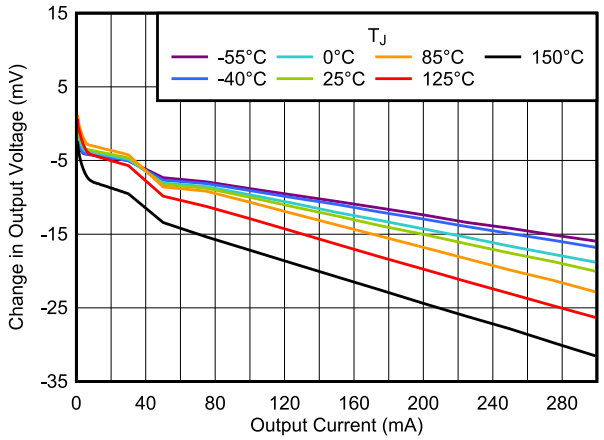
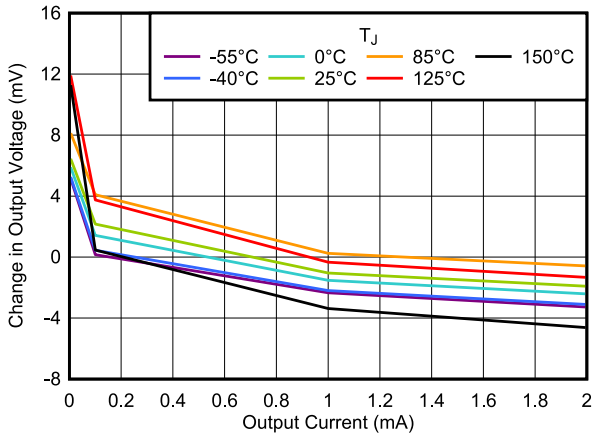
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



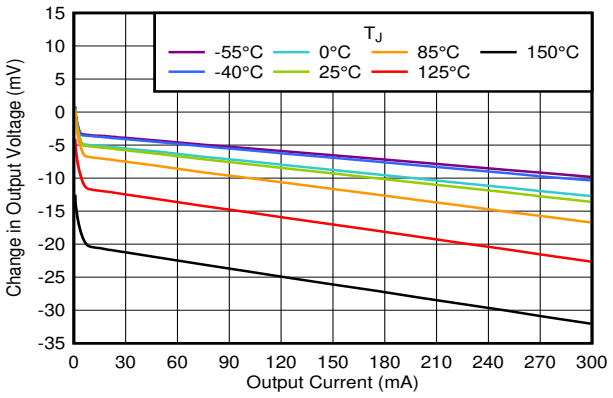

$V_{IN}$ = 2.8 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-7. Load Regulation vs $I_{OUT}$**



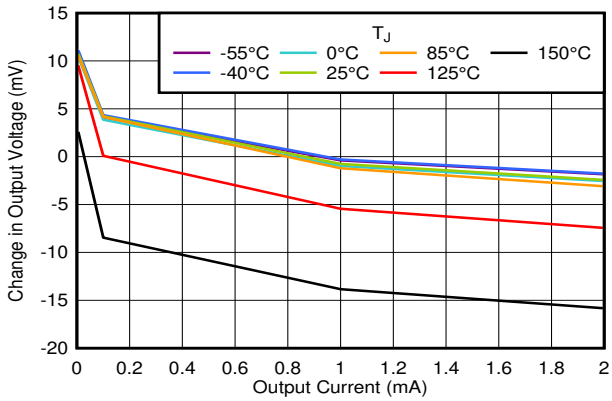

$V_{IN}$ = 2.8 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-8. Load Regulation vs $I_{OUT}$**



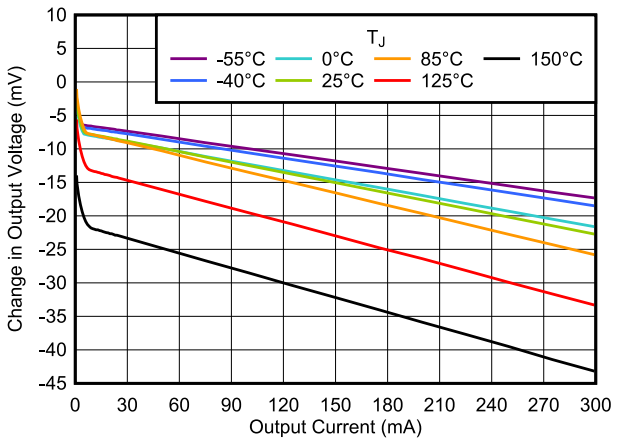

$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-9. Load Regulation vs $I_{OUT}$**



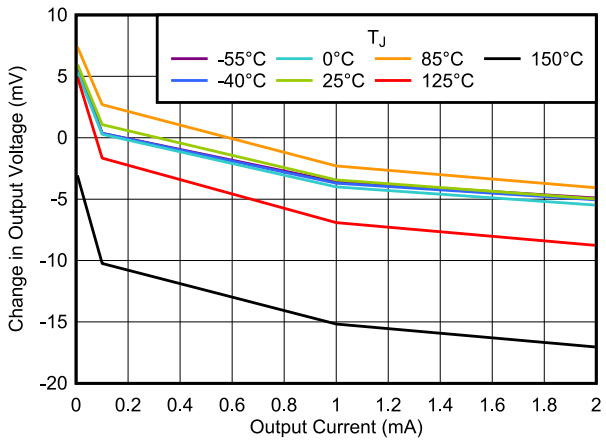

$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-10. Load Regulation vs $I_{OUT}$**




$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-11. Load Regulation vs $I_{OUT}$**




$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-12. Load Regulation vs $I_{OUT}$**

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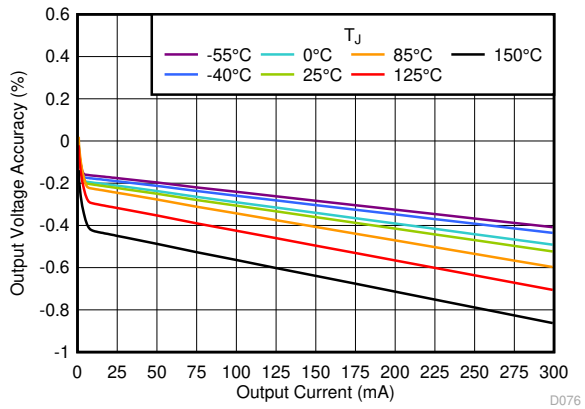
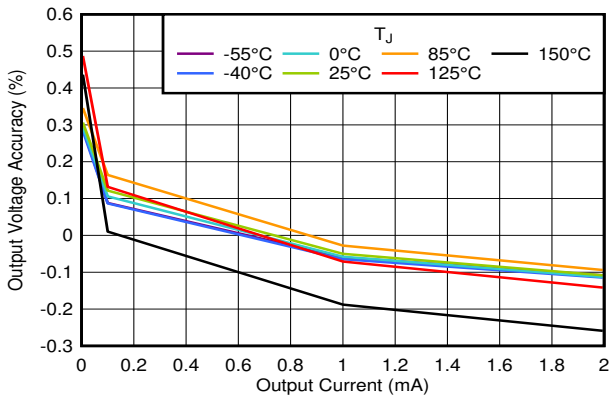
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



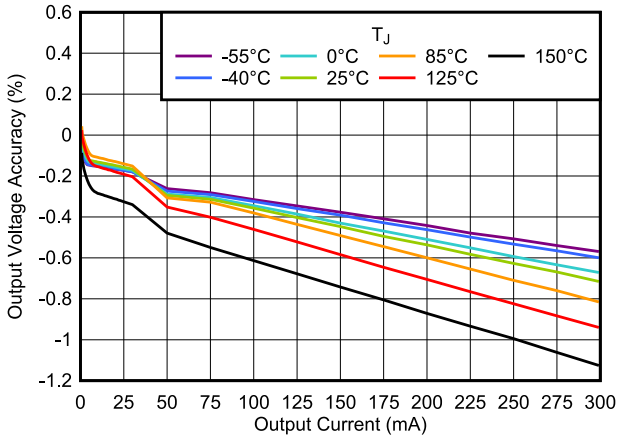

$V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-13. Output Voltage Accuracy vs $I_{OUT}$**



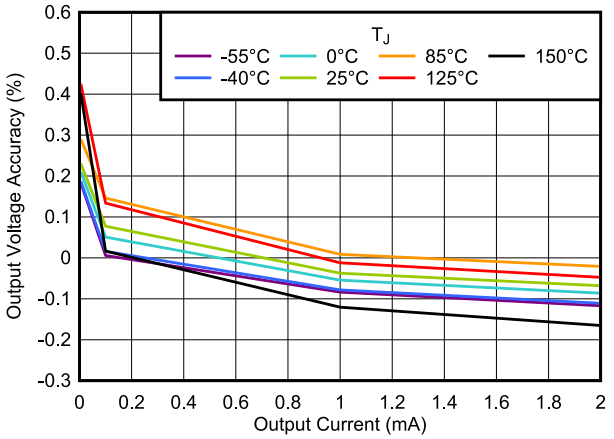

$V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-14. Output Voltage Accuracy vs $I_{OUT}$**



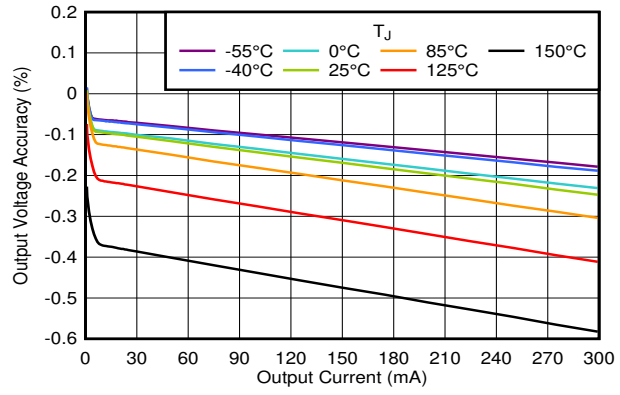

$V_{EN}$ = 1 V, DBV package

**Figure 6-15. Output Voltage Accuracy vs $I_{OUT}$**



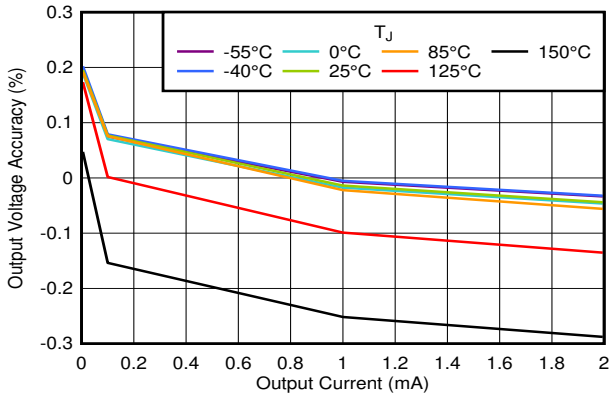

$V_{EN}$ = 1 V, DBV package

**Figure 6-16. Output Voltage Accuracy vs $I_{OUT}$**




$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-17. Output Voltage Accuracy vs $I_{OUT}$**




$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-18. Output Voltage Accuracy vs $I_{OUT}$**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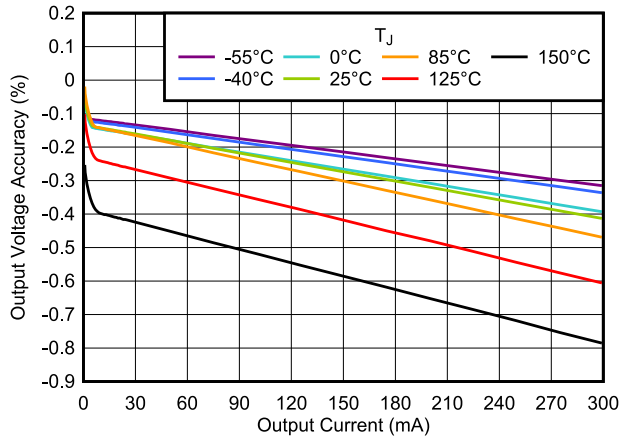
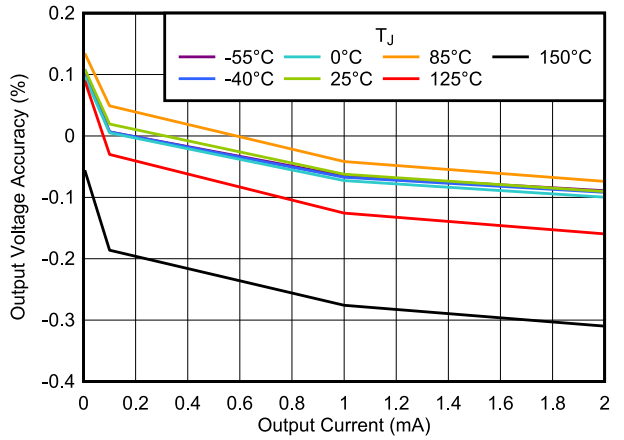
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



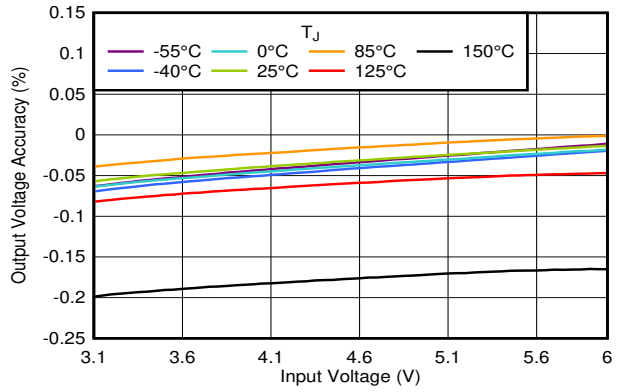

$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-19. Output Voltage Accuracy vs $I_{OUT}$**



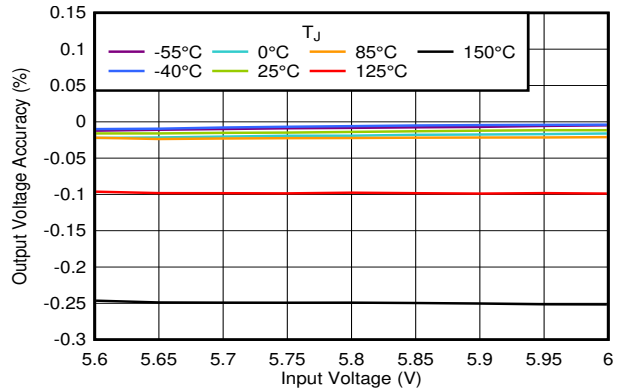

$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-20. Output Voltage Accuracy vs $I_{OUT}$**



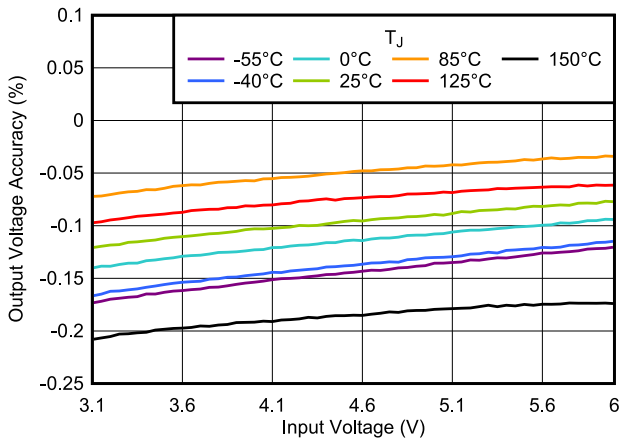

$V_{EN}$ = 1 V, $I_{OUT}$ = 1 mA, DQN, YCJ, and YCK packages

**Figure 6-21. Output Voltage Accuracy vs $V_{IN}$**



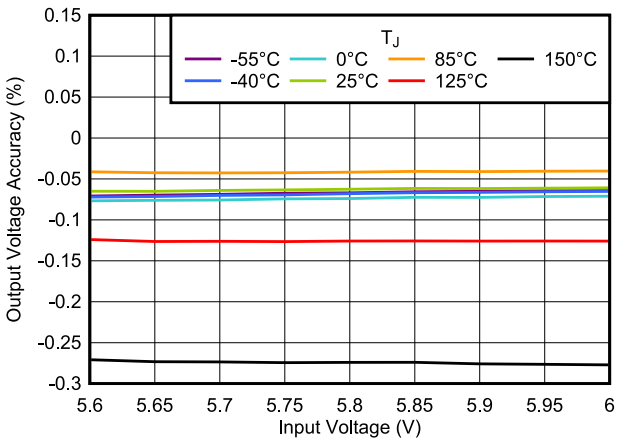

$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-22. Output Voltage Accuracy vs $V_{IN}$**




$V_{EN}$ = 1 V, $I_{OUT}$ = 1 mA, DBV package

**Figure 6-23. Output Voltage Accuracy vs $V_{IN}$**




$V_{OUT}$ = 5.5 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-24. Output Voltage Accuracy vs $V_{IN}$**

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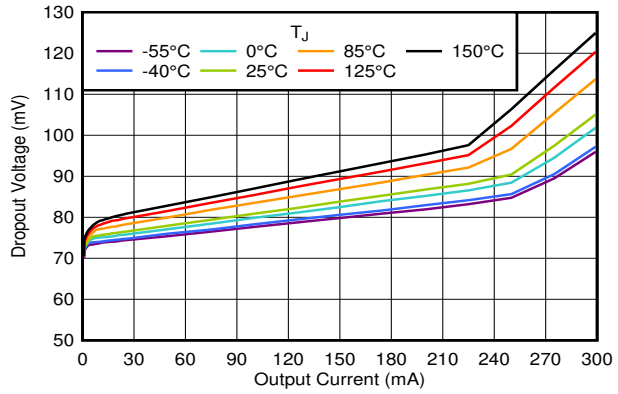
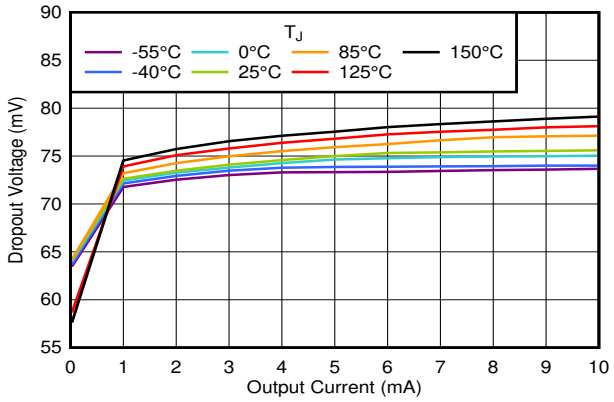
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



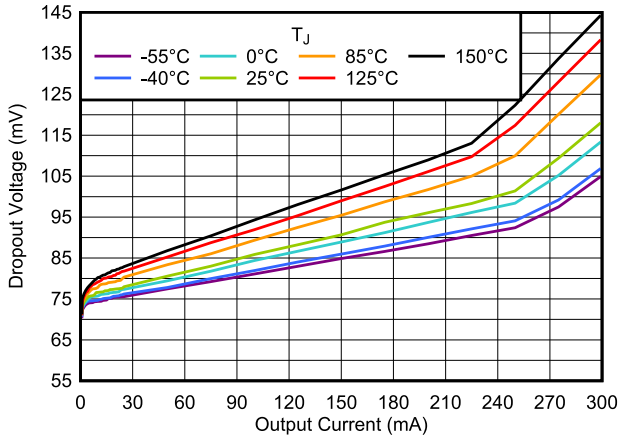

$V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-25. Dropout Voltage vs $I_{OUT}$**



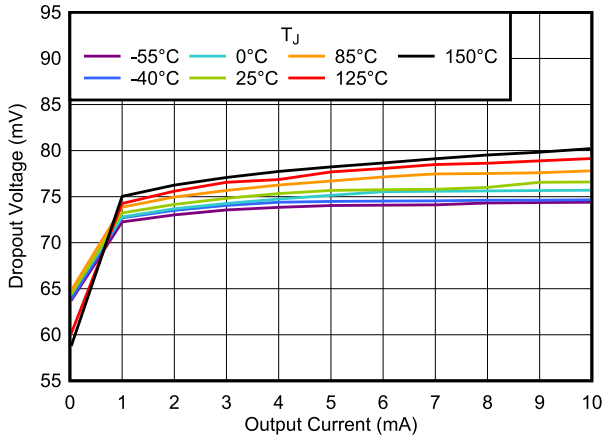

$V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-26. Dropout Voltage vs $I_{OUT}$**



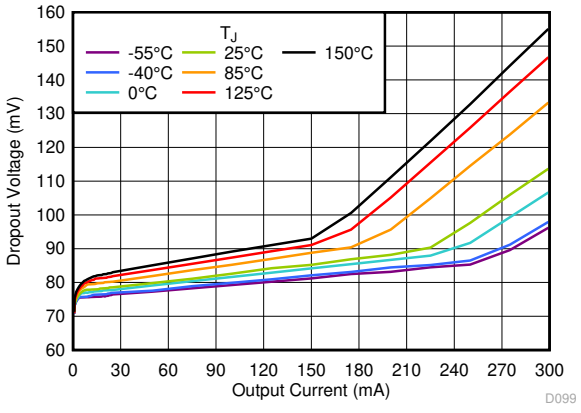

$V_{EN}$ = 1 V, DBV package

**Figure 6-27. Dropout Voltage vs $I_{OUT}$**



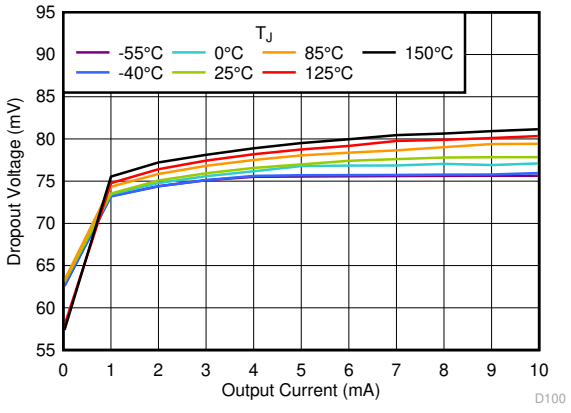

$V_{EN}$ = 1 V, DBV package

**Figure 6-28. Dropout Voltage vs $I_{OUT}$**




$V_{OUT}$ = 1.8 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-29. Dropout Voltage vs $I_{OUT}$**




$V_{OUT}$ = 1.8 V, $V_{EN}$ = 1 V, DQN, YCJ, and YCK packages

**Figure 6-30. Dropout Voltage vs $I_{OUT}$**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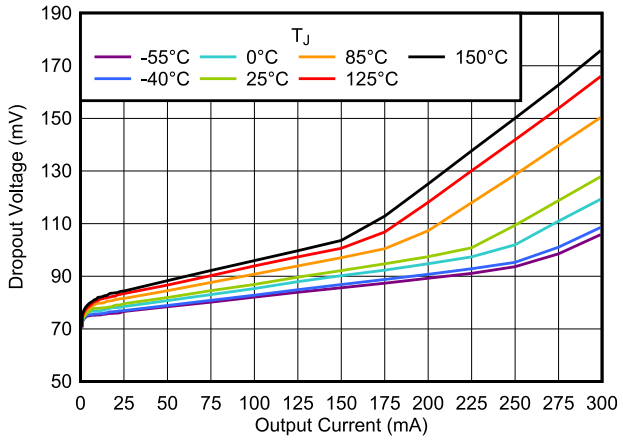
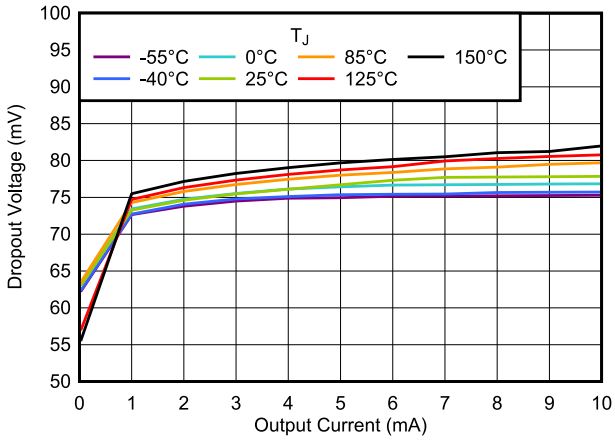
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



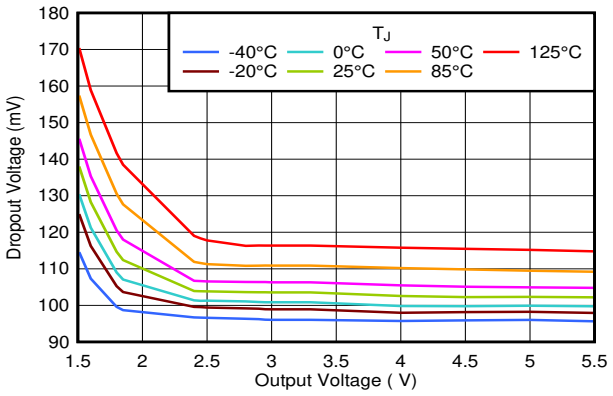

$V_{OUT}$ = 1.8 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-31. Dropout Voltage vs $I_{OUT}$**



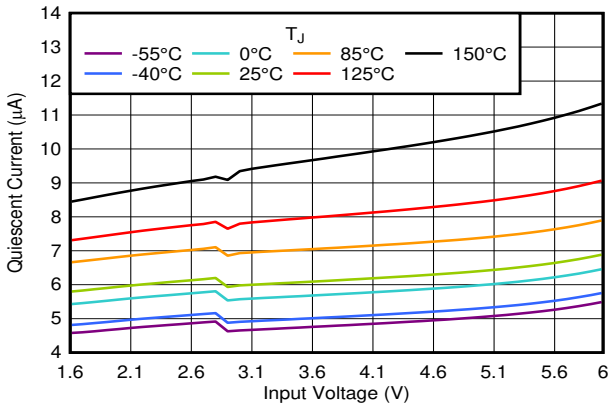

$V_{OUT}$ = 1.8 V, $V_{EN}$ = 1 V, DBV package

**Figure 6-32. Dropout Voltage vs $I_{OUT}$**



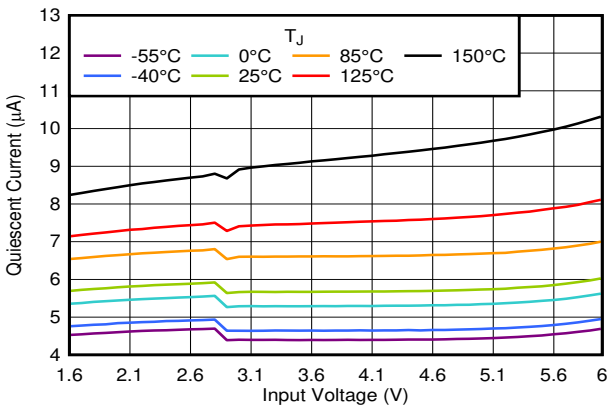

$I_{OUT}$ = 300 mA

**Figure 6-33. Dropout Voltage vs $V_{OUT}$**



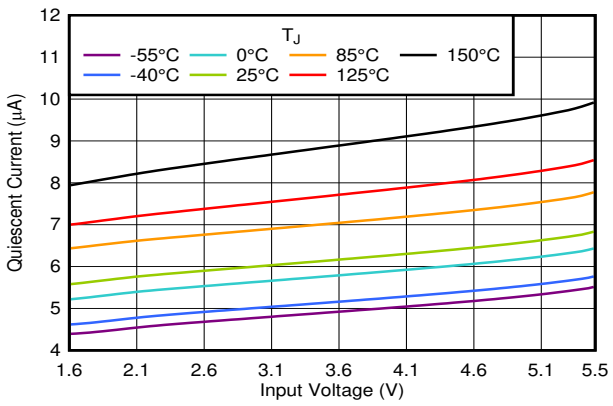

$V_{EN}$ = 1 V, $I_{OUT}$ = 0 mA

**Figure 6-34. $I_{GND}$ vs $V_{IN}$**




$V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 0 mA

**Figure 6-35. $I_{GND}$ vs $V_{IN}$**




$V_{OUT(NOM)}$ = 5.5 V, $V_{EN}$ = 1 V, $I_{OUT}$ = 0 mA

**Figure 6-36. $I_{GND}$ vs $V_{IN}$ in the Dropout Region**

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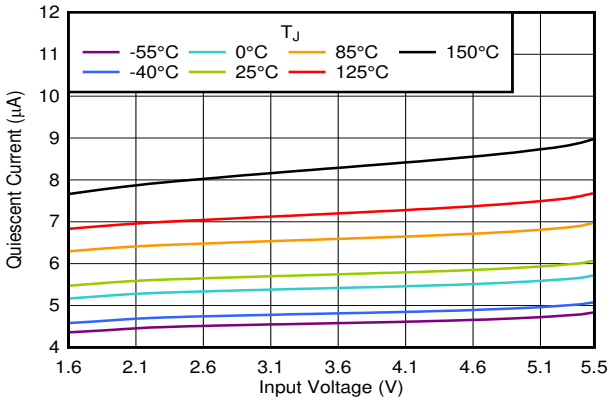
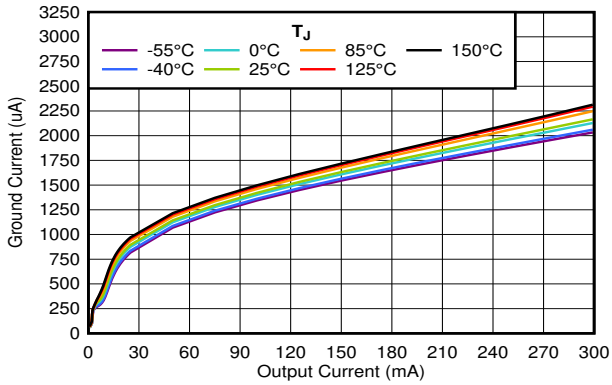
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



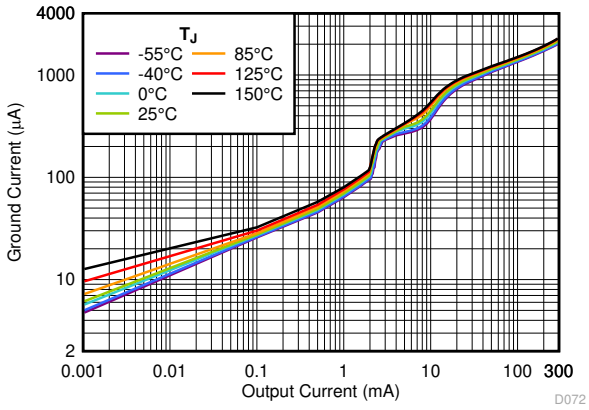

$V_{OUT(NOM)}$ = 5.5 V, $V_{EN}$ = $V_{IN}$, $I_{OUT}$ = 0 mA

**Figure 6-37. $I_{GND}$ vs $V_{IN}$ in the Dropout Region**



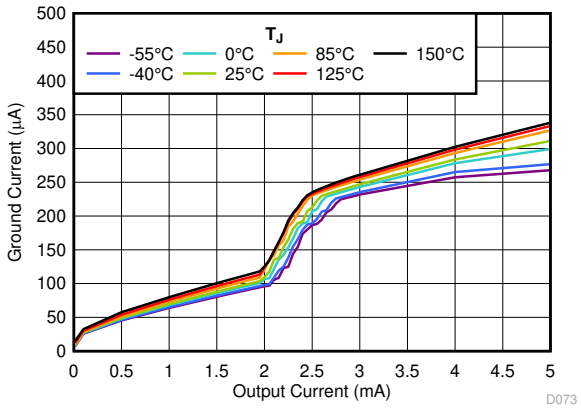

$V_{EN}$ = 1 V

**Figure 6-38. $I_{GND}$ vs $I_{OUT}$**



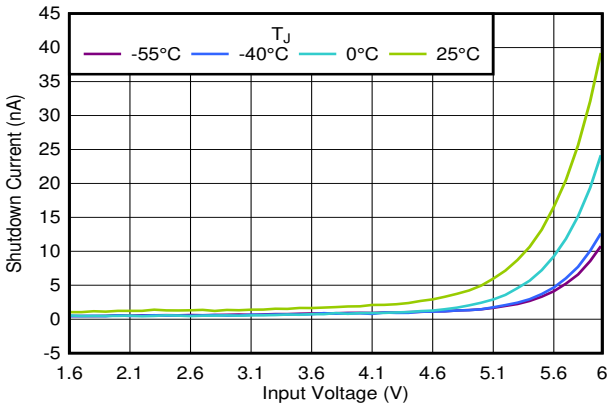

$V_{EN}$ = 1 V

**Figure 6-39. $I_{GND}$ vs $I_{OUT}$**



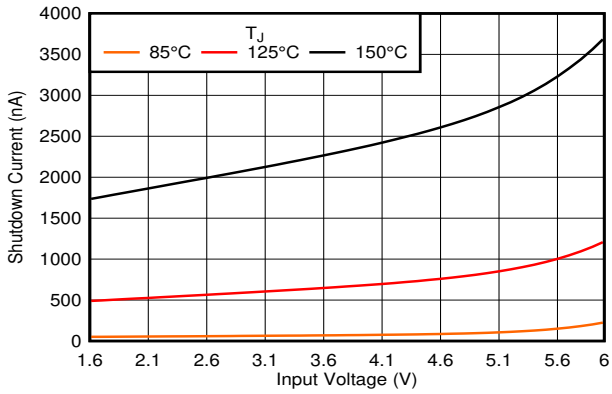

$V_{EN}$ = 1 V

**Figure 6-40. $I_{GND}$ vs $I_{OUT}$**




$V_{EN}$ = 0 V

**Figure 6-41. Shutdown Current vs $V_{IN}$**




$V_{EN}$ = 0 V

**Figure 6-42. Shutdown Current vs $V_{IN}$**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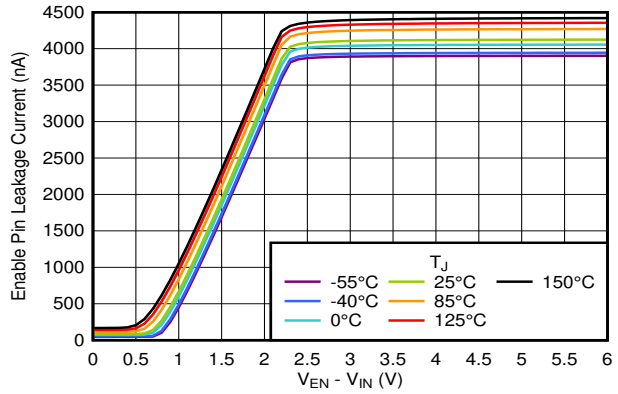
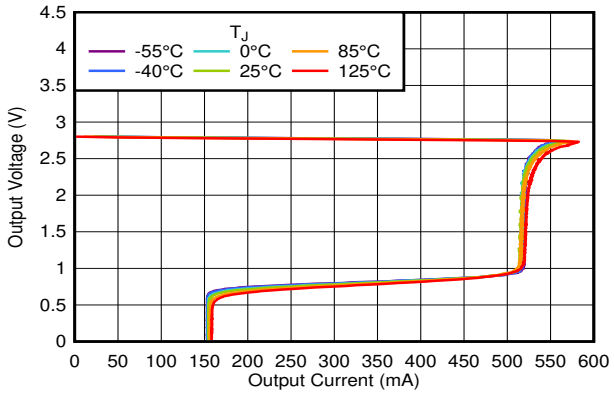
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



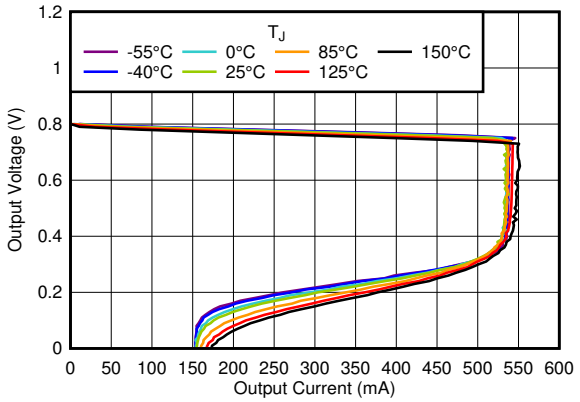

$V_{EN}$ = 6 V, $I_{OUT}$ = 0 mA

**Figure 6-43. Enable Pin Leakage Current vs $V_{EN}$ - $V_{IN}$**



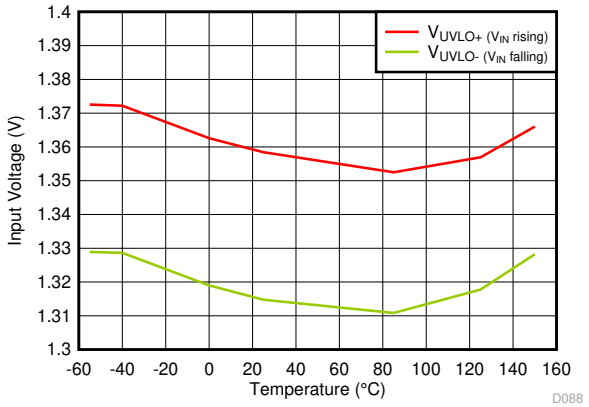

$V_{EN}$ = 1 V

**Figure 6-44. Current Limit**




$V_{OUT}$ = 0.8 V, $V_{EN}$ = 1 V

**Figure 6-45. Current Limit**




$V_{EN}$ = 1 V

**Figure 6-46. UVLO Threshold vs Temperature**

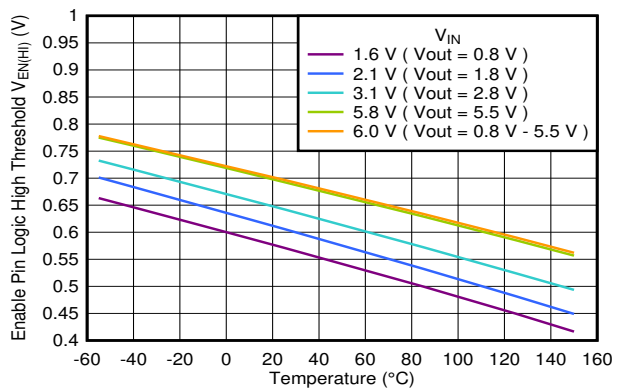



**Figure 6-47. Enable Logic High Threshold vs Temperature**

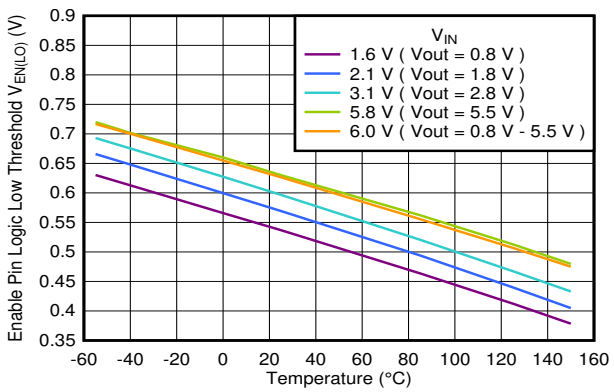



**Figure 6-48. Enable Logic Low Threshold Low vs Temperature**

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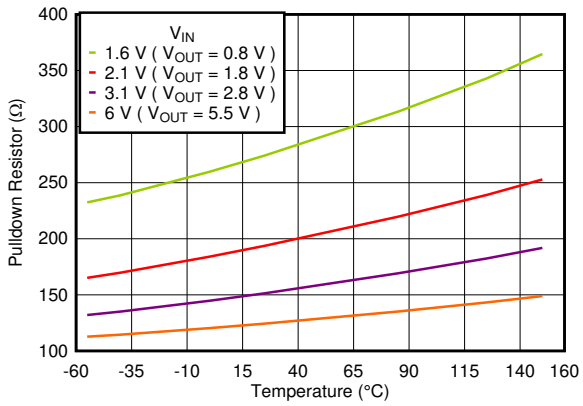
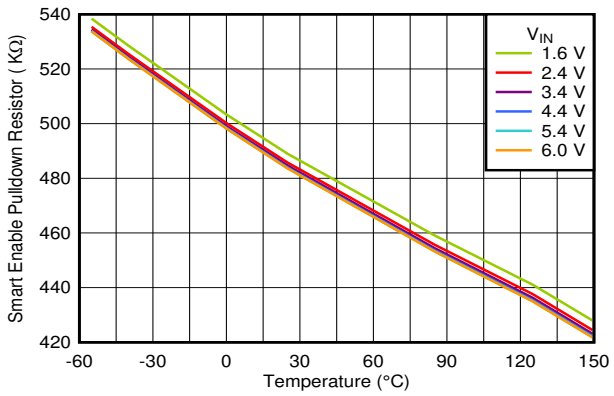
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



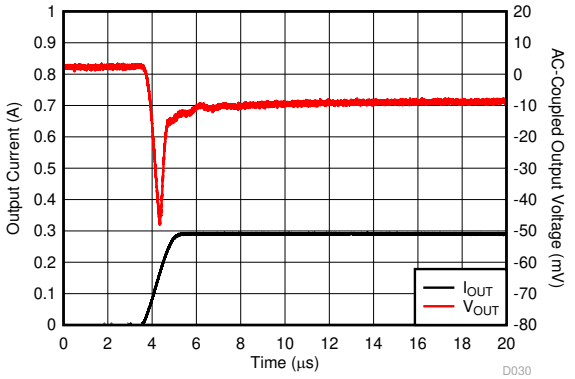

$V_{EN}$ = 0.25 V

**Figure 6-49. Output Pulldown Resistor vs Temperature**



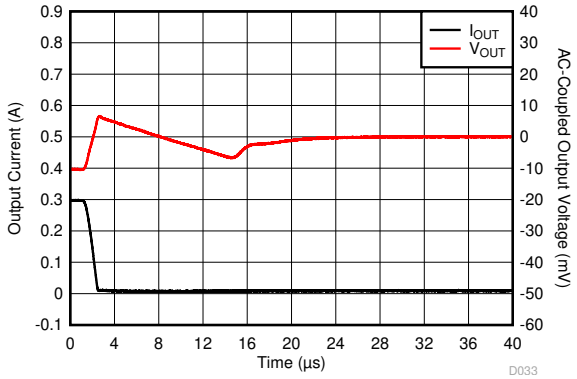

$V_{EN}$ = 0.25 V

**Figure 6-50. Smart Enable Pulldown Resistor vs Temperature and $V_{IN}$**



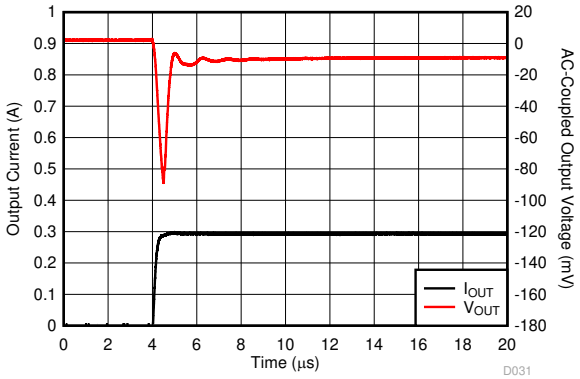

$I_{OUT}$ = 1 mA to 300 mA, $t_{RISING}$ = 1 µs

**Figure 6-51. Load Transient**



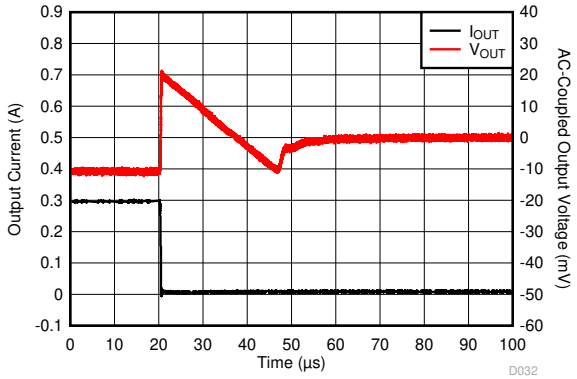

$I_{OUT}$ = 300 mA to 1 mA, $t_{FALLING}$ = 1 µs

**Figure 6-52. Load Transient**




$I_{OUT}$ = 1 mA to 300 mA, $t_{RISING}$ = 200 ns

**Figure 6-53. Load Transient**




$I_{OUT}$ = 300 mA to 1 mA, $t_{FALLING}$ = 200 ns

**Figure 6-54. Load Transient**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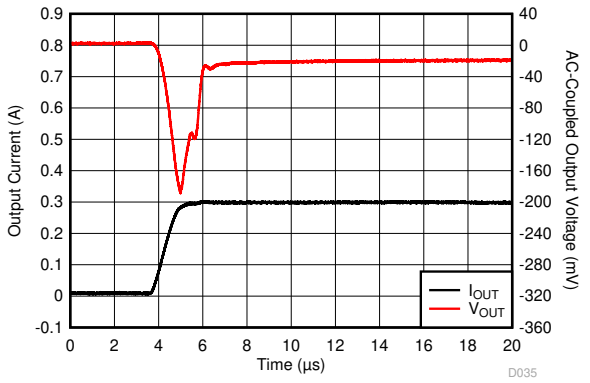
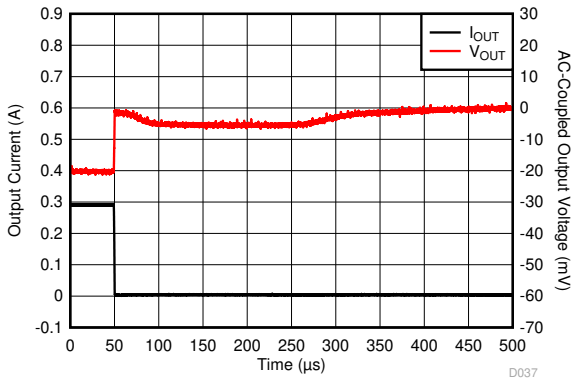
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



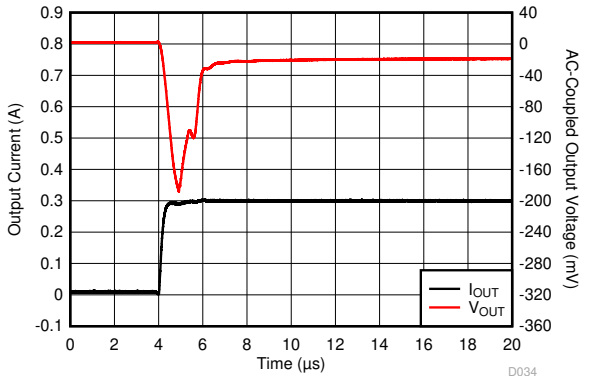

$I_{OUT}$ = 0 mA to 300 mA, $t_{RISING}$ = 1 µs

**Figure 6-55. Load Transient**



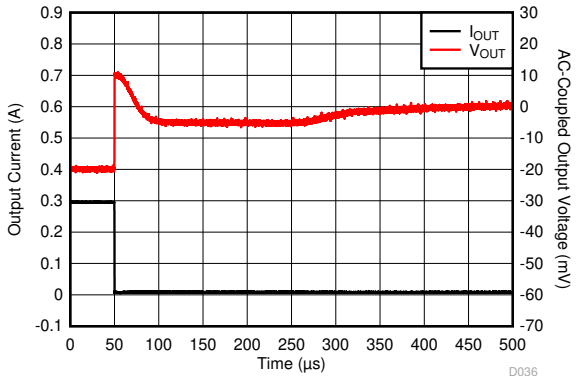

$I_{OUT}$ = 300 mA to 0 mA, $t_{FALLING}$ = 1 µs

**Figure 6-56. Load Transient**



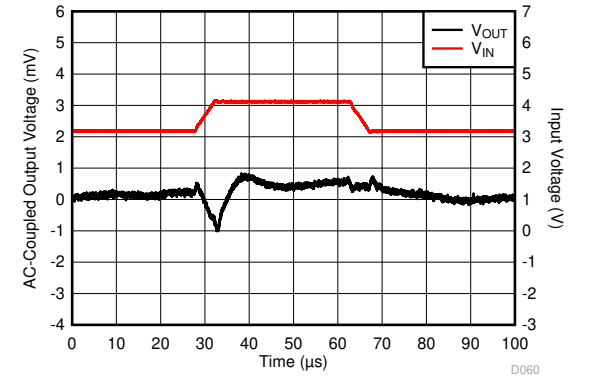

$I_{OUT}$ = 0 mA to 300 mA, $t_{RISING}$ = 200 ns

**Figure 6-57. Load Transient**



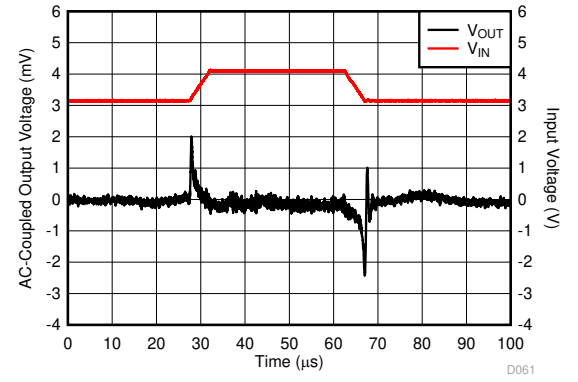

$I_{OUT}$ = 300 mA to 0 mA, $t_{FALLING}$ = 200 ns

**Figure 6-58. Load Transient**




$V_{IN}$ = 3.1 V → 4.1 V → 3.1 V, $V_{IN}$ $t_{RISING}$ = 5 µs, $I_{OUT}$ = 1 mA

**Figure 6-59. Line Transient**




$V_{IN}$ = 3.1 V → 4.1 V → 3.1 V, $V_{IN}$ $t_{RISING}$ = 5 µs, $I_{OUT}$ = 300 mA

**Figure 6-60. Line Transient**

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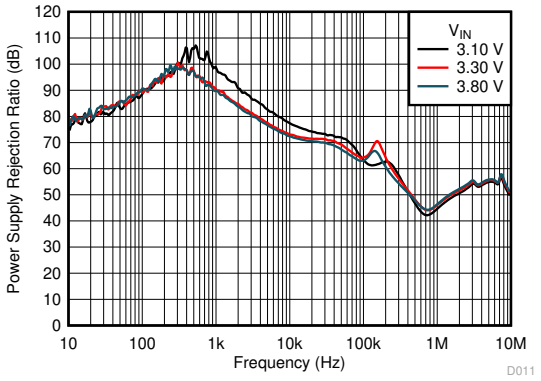
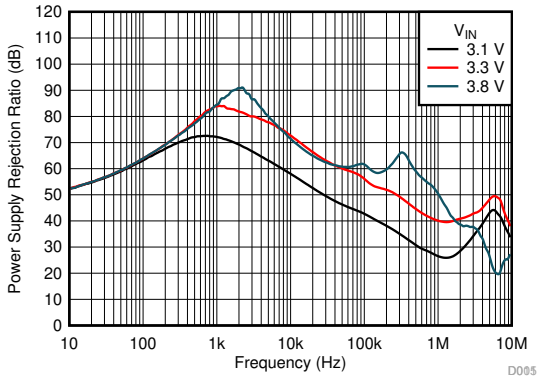
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)




$I_{OUT}$ = 20 mA

**Figure 6-61. PSRR vs $V_{IN}$ vs Frequency and $V_{IN}$**




$I_{OUT}$ = 300 mA

**Figure 6-62. PSRR vs Frequency and $V_{IN}$**

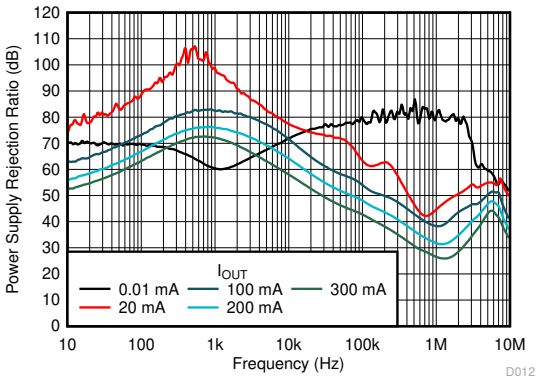
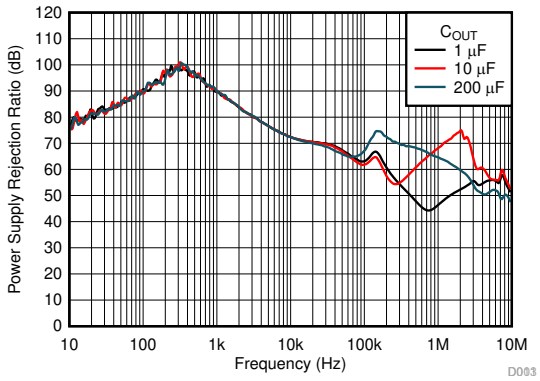
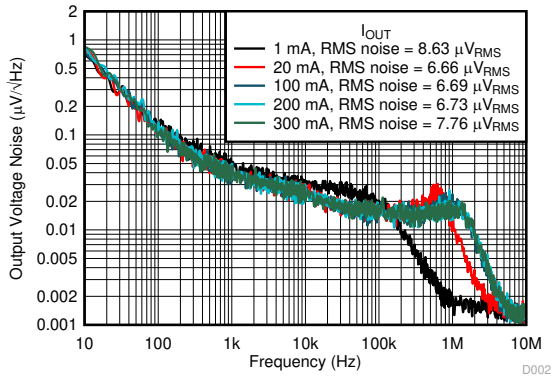



**Figure 6-63. PSRR vs Frequency and $I_{OUT}$**



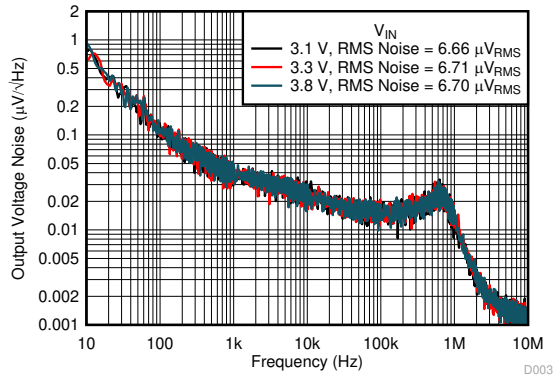

$I_{OUT}$ = 20 mA

**Figure 6-64. PSRR vs Frequency and $C_{OUT}$**




$V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-65. Noise vs Frequency and $I_{OUT}$**




$I_{OUT}$ = 20 mA, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-66. Noise vs Frequency and $V_{IN}$**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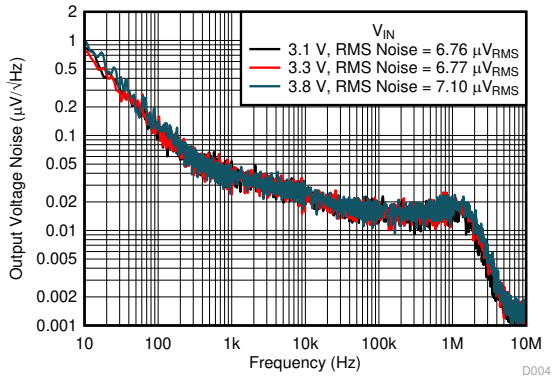
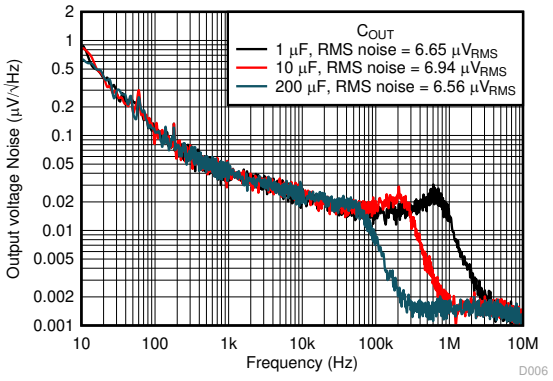
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



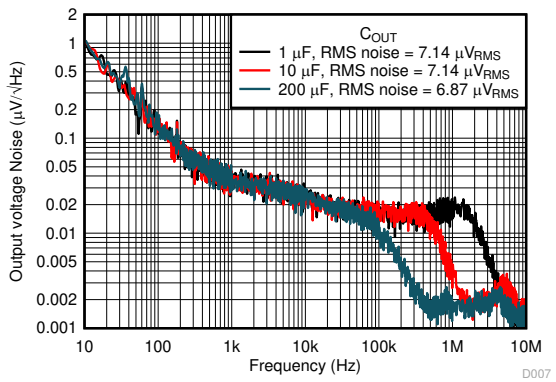

$I_{OUT}$ = 300 mA, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-67. Noise vs Frequency and $V_{IN}$**



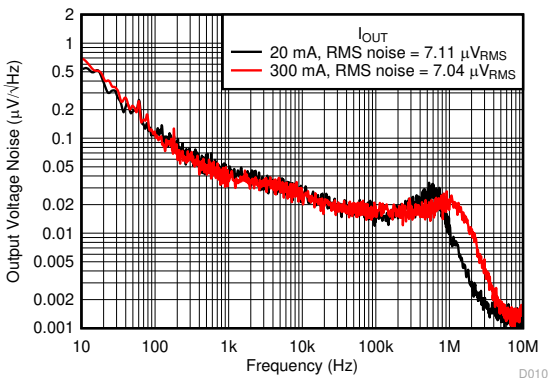

$V_{IN}$ = 3.8 V, $I_{OUT}$ = 20 mA, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-68. Noise vs Frequency and $C_{OUT}$**



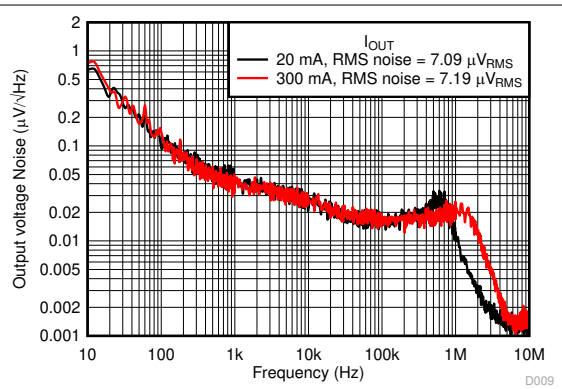

$V_{IN}$ = 3.8 V, $I_{OUT}$ = 300 mA, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-69. Noise vs Frequency and $C_{OUT}$**



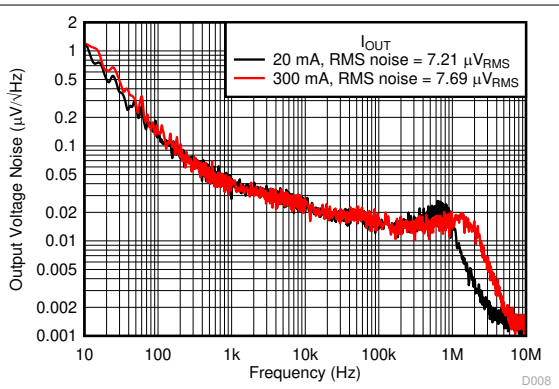

$V_{OUT}$ = 0.8 V, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-70. Noise vs Frequency and $I_{OUT}$**




$V_{OUT}$ = 0.8 V, $V_{IN}$ = 1.8 V, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-71. Noise vs Frequency and $I_{OUT}$**




$V_{OUT}$ = 5.5 V, $V_{IN}$ = 6 V, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 6-72. Noise vs Frequency and $I_{OUT}$**

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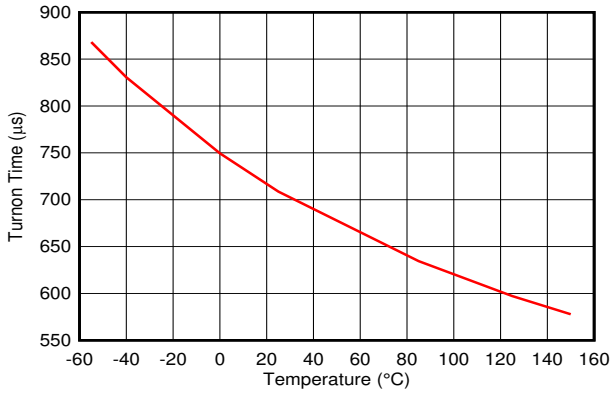
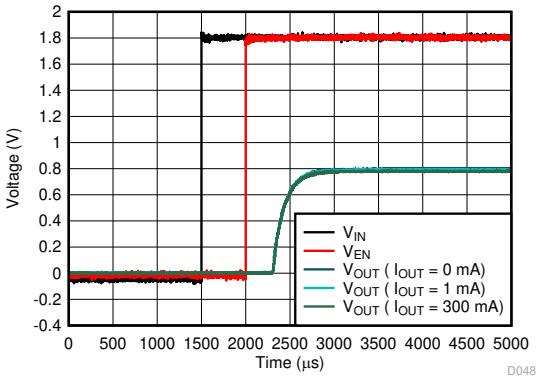
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



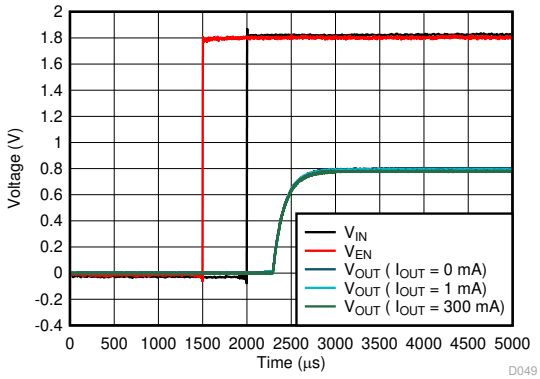

From $V_{EN}$ = $V_{EN(HI)}$ to $V_{OUT}$ = 95% of $V_{OUT(NOM)}$, $I_{OUT}$ = 0 mA

**Figure 6-73. Start-Up Turn-On Time**



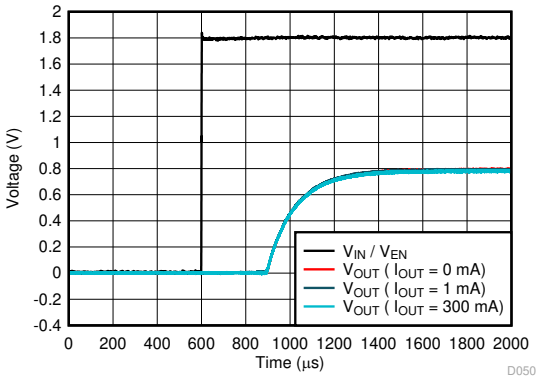

$V_{OUT}$ = 0.8 V, $V_{IN}$ = 0 V to 1.8 V, $V_{EN}$ = 0 V to 1.8 V, $V_{EN}$ rises 500 µs behind $V_{IN}$, $V_{IN}$ and $V_{EN}$ slew rate = 1 V/µs

**Figure 6-74. Start-Up**



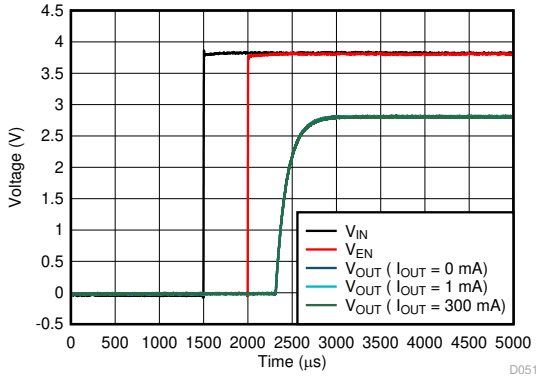

$V_{OUT}$ = 0.8 V, $V_{IN}$ = 0 V to 1.8 V, $V_{EN}$ = 0 V to 1.8 V, $V_{EN}$ rises 500 µs ahead of $V_{IN}$, $V_{IN}$ and $V_{EN}$ slew rate = 1 V/µs

**Figure 6-75. Start-Up**



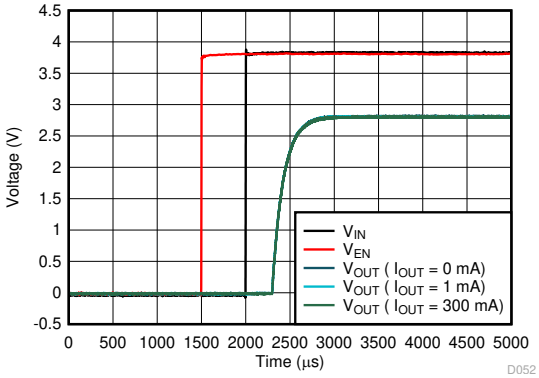

$V_{OUT}$ = 0.8 V, $V_{IN}$ = 0 V to 1.8 V, $V_{EN}$ = $V_{IN}$, $V_{IN}$ slew rate = 1 V/µs

**Figure 6-76. Start-Up**




$V_{IN}$ = 0 V to 3.8 V, $V_{EN}$ = 0 V to 3.8 V, $V_{EN}$ rises 500 µs behind $V_{IN}$, $V_{IN}$ and $V_{EN}$ slew rate = 1 V/µs

**Figure 6-77. Start-Up**




$V_{IN}$ = 0 V to 3.8 V, $V_{EN}$ = 0 V to 3.8 V, $V_{EN}$ rises 500 µs ahead of $V_{IN}$, $V_{IN}$ and $V_{EN}$ slew rate = 1 V/µs

**Figure 6-78. Start-Up**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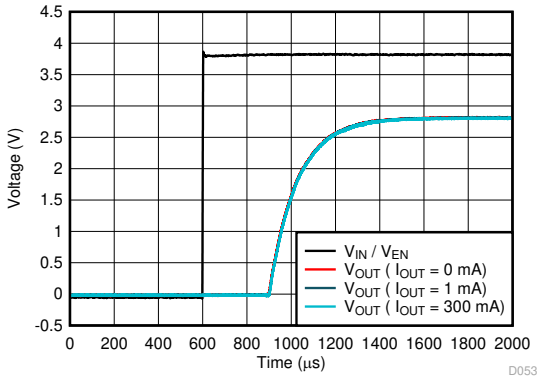
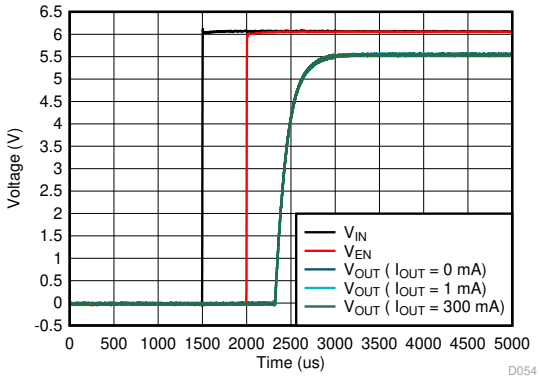
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)



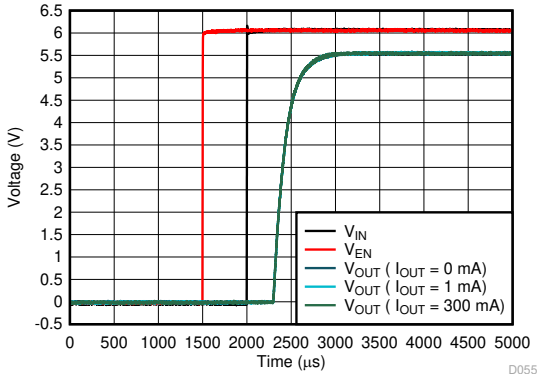

$V_{IN}$ = 0 V to 3.8 V, $V_{EN}$ = 0 V to 3.8 V, $V_{EN}$ = $V_{IN}$, $V_{IN}$ and slew rate = 1 V/µs

**Figure 6-79. Start-Up**



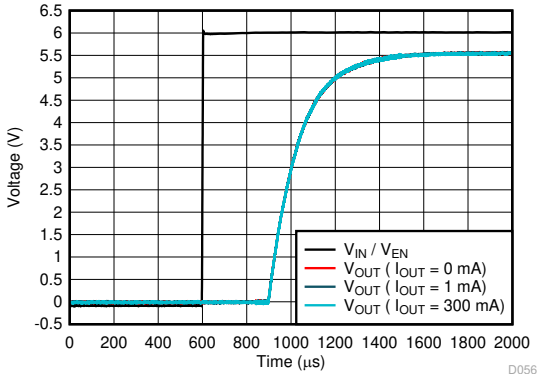

$V_{OUT}$ = 5.5 V, $V_{IN}$ = 0 V to 6.0 V, $V_{EN}$ = 0 V to 6.0 V, $V_{EN}$ rises 500 µs behind $V_{IN}$, $V_{IN}$ and $V_{EN}$ slew rate = 1 V/µs

**Figure 6-80. Start-Up**



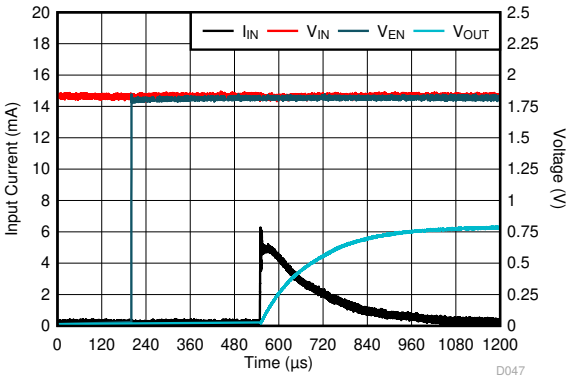

$V_{OUT}$ = 5.5 V, $V_{IN}$ = 0 V to 6.0 V, $V_{EN}$ = 0 V to 6.0 V, $V_{EN}$ rises 500 µs ahead of $V_{IN}$, $V_{IN}$ and $V_{EN}$ slew rate = 1 V/µs

**Figure 6-81. Start-Up**



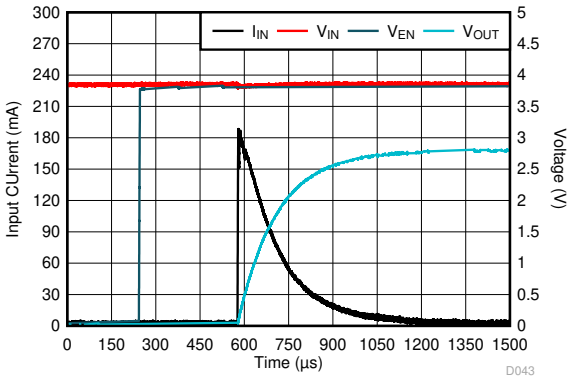

$V_{OUT}$ = 5.5 V, $V_{IN}$ = 0 V to 6 V, $V_{EN}$ = $V_{IN}$, $V_{IN}$ slew rate = 1 V/µs

**Figure 6-82. Start-Up**




$V_{OUT}$ = 0.8 V, $V_{IN}$ = 1.8 V, $V_{EN}$ = 0 V to 1.8 V, $V_{EN}$ slew rate = 1 V/µs, $C_{OUT}$ = 10 µF

**Figure 6-83. Inrush Current**




$V_{IN}$ = 3.8 V, $V_{EN}$ = 0 V to 3.8 V, $V_{EN}$ slew rate = 1 V/µs, $C_{OUT}$ = 10 µF

**Figure 6-84. Inrush Current**

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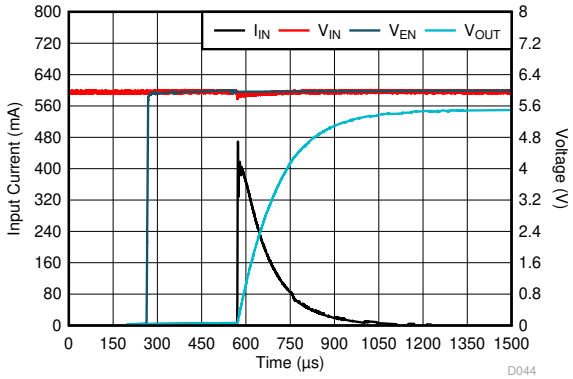
## 6.7 Typical Characteristics (continued)

$V_{IN}$ = $V_{OUT(NOM)}$ + 0.3 V or 1.6 V (whichever is greater), $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN}$ = 1 µF, $C_{OUT}$ = 1 µF, and $T_A$ = 25°C (unless otherwise noted)




$V_{OUT}$ = 5.5 V, $V_{IN}$ = 6.0 V, $V_{EN}$ = 0 V to 6.0 V,
$V_{EN}$ slew rate = 1 V/µs, $C_{OUT}$ = 10 µF

**Figure 6-85. Inrush Current**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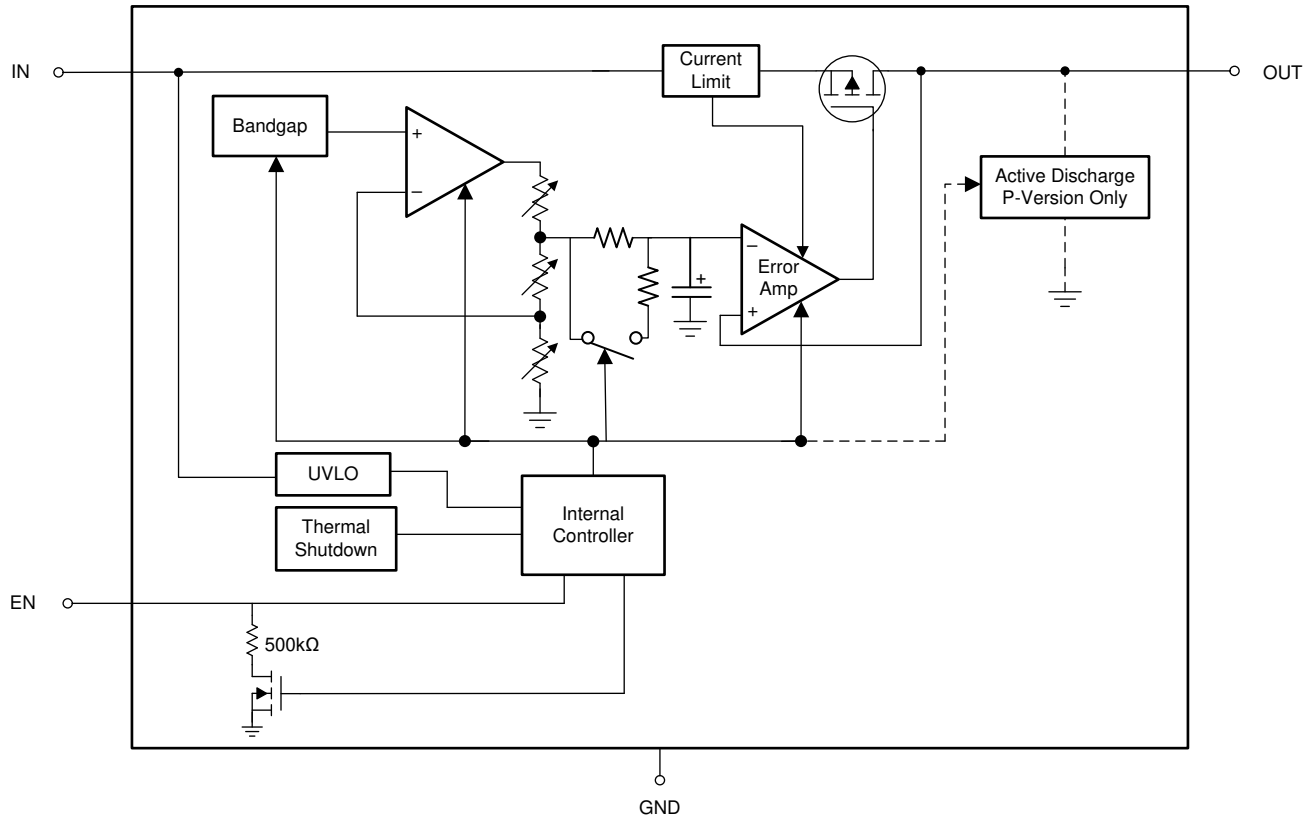
# 7 Detailed Description

## 7.1 Overview

Designed to meet the needs of sensitive RF and analog circuits, the TPS7A20 provides low noise, high PSRR, low quiescent current, as well as low line and load transient response figures. Using innovative design techniques, the TPS7A20 offers class-leading noise performance without the need for a separate noise filter capacitor.

The TPS7A20 is designed to operate with a single 1-µF input capacitor and a single 1-µF ceramic output capacitor.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Low Output Noise

Any internal noise at the TPS7A20 reference voltage is reduced by a first-order, low-pass RC filter before being passed to the output buffer stage. The low-pass RC filter has a –3-dB cut-off frequency of approximately 0.1 Hz.

During start-up, the filter resistor is bypassed to reduce output rise time; the filter begins normal operation after the output voltage reaches the correct value.

### 7.3.2 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the voltage of the enable input is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

### 7.3.3 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

### 7.3.4 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.


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Figure 7-1 shows a diagram of the foldback current limit.

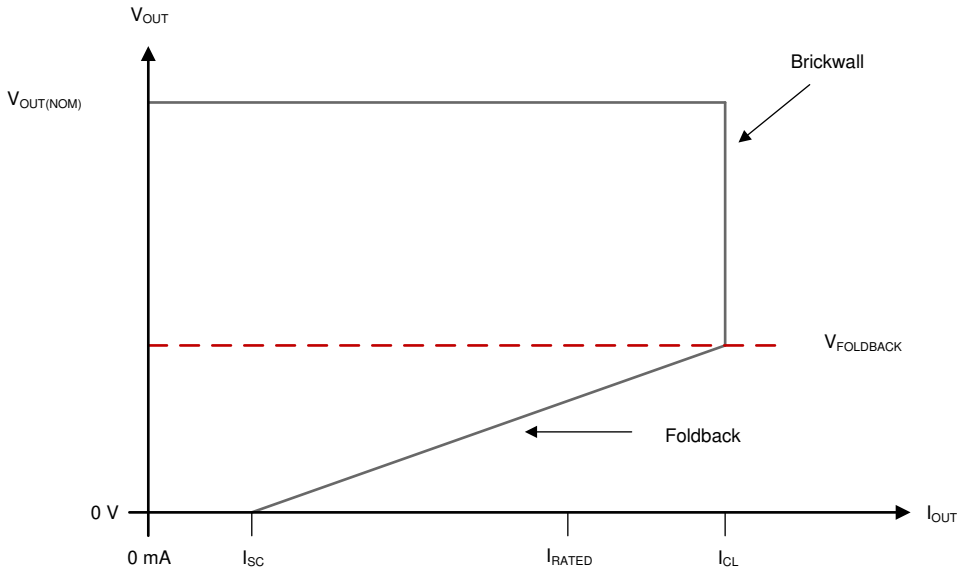


**Figure 7-1. Foldback Current Limit**

### 7.3.5 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

### 7.3.6 Thermal Shutdown

A thermal shutdown protection circuit disables the LDO when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN}$ – $V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

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### 7.3.7 Active Discharge

An internal pulldown MOSFET connects a resistor from OUT to ground when the device is disabled to actively discharge the output capacitance. The active discharge circuit is activated by driving EN low or by the voltage on IN falling below the undervoltage lockout (UVLO) threshold.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input. This reverse current flow can cause damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

## 7.4 Device Functional Modes

### 7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 7-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 7.4.4 Disabled

The output of the LDO can be shut down by driving EN to less than $V_{EN(LOW)}$ (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shut down, and the output voltage is actively discharged to ground by an internal discharge circuit between OUT and ground.


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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

### 8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

### 8.1.2 Input and Output Capacitor Requirements

Although the LDO itself is stable without an input capacitor, good analog design practice is to connect a capacitor from IN to GND, with a value at least equal to the nominal value specified in the *Recommended Operating Conditions* table. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR, and is recommended if the source impedance is greater than 0.5 Ω. When the source resistance and inductance are sufficiently high, especially in the presence of load transients, the overall system may be susceptible to instability (including ringing and sustained oscillation) and other performance degradation if there is insufficient capacitance between IN and GND. A capacitor with a value greater than the minimum may be necessary if large, fast-rise-time load or line transients are anticipated or if the device is located more than a few centimeters from the input power source.

An output capacitor of an appropriate value helps ensure stability and improve dynamic performance. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table.

### 8.1.3 Load Transient Response

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load and the transition from a heavy to a light load. The regions shown in Figure 8-1 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

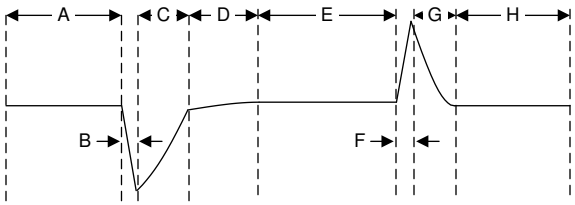


**Figure 8-1. Load Transient Waveform**

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)

- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger DC load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

### 8.1.4 Undervoltage Lockout (UVLO) Operation

The UVLO circuit ensures that the device stays disabled before its input supply reaches the minimum operational voltage range, and ensures that the device shuts down when the input supply collapses. Figure 8-2 shows the UVLO circuit response to various input voltage events. The diagram can be separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

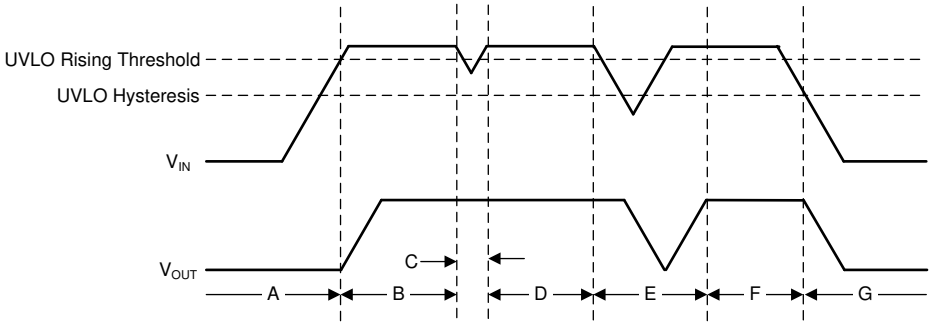


**Figure 8-2. Typical UVLO Operation**

### 8.1.5 Power Dissipation ($P_D$)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate $P_D$:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A20 allows for maximum efficiency across a wide range of output voltages.


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The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ($T_J$) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$). Equation 4 rearranges Equation 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{4}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper.

#### 8.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ($\Psi$) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are used in accordance with Equation 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \tag{5}$$

where:

- $P_D$ is the power dissipated as explained in Equation 2
- $T_T$ is the temperature at the center-top of the device package
- $T_B$ is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

#### 8.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 8-3 and can be separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by Equation 4. The slope is nonlinear because the maximum-rated junction temperature of the LDO is controlled by the power dissipation across the LDO; thus when $V_{IN} - V_{OUT}$ increases the output current must decrease.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

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Figure 8-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

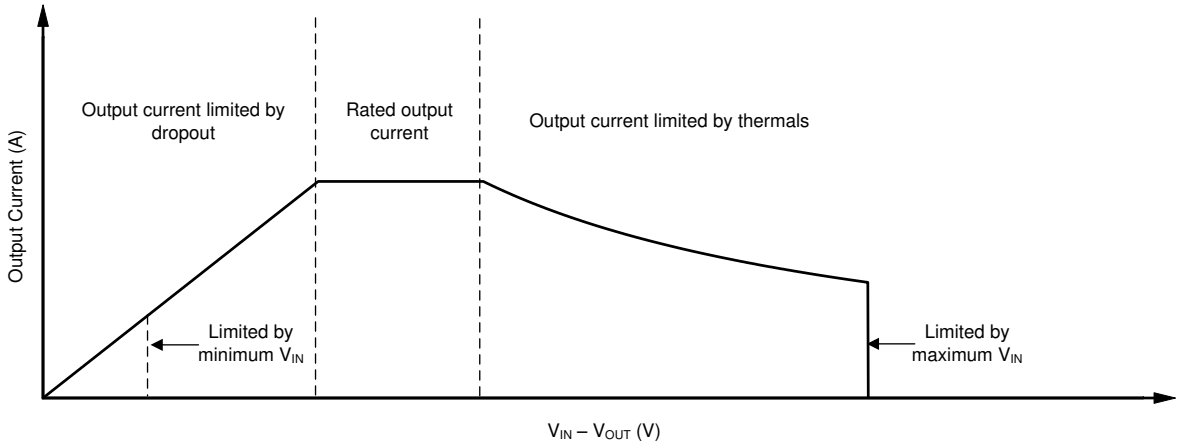


**Figure 8-3. Region Description of Continuous Operation Regime**


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## 8.2 Typical Application

Figure 8-4 shows the typical application circuit for the TPS7A20. Input and output capacitances may need to be increased above the 1 µF minimum for some applications.

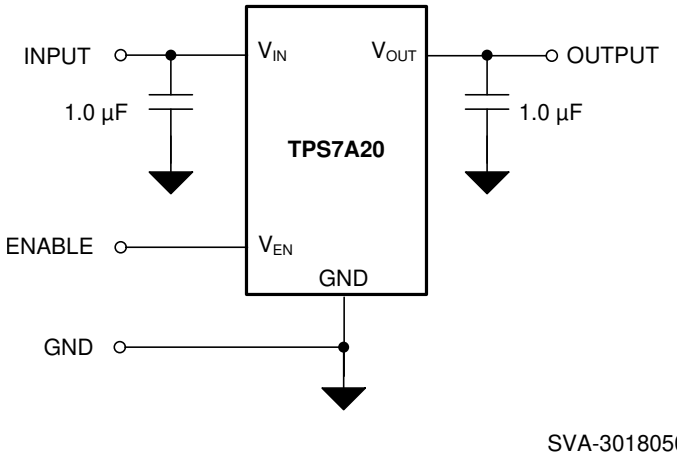


**Figure 8-4. TPS7A20 Typical Application**

### 8.2.1 Design Requirements

Table 8-1 summarizes the design requirements for Figure 8-4.

**Table 8-1. Design Parameters**

| DESIGN PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 3.1 V to 3.6 V |
| Output voltage | 2.8 V |
| Output current | 200 mA |
| Maximum ambient temperature | 85°C |

### 8.2.2 Detailed Design Procedure

For this design example, the 2.8-V output version (TPS7A2028) is selected. A nominal 3.3-V input supply is assumed. A minimum 1.0-µF input capacitor is recommended to minimize the effect of resistance and inductance between the 3.3-V source and the LDO input. A minimum 1.0-µF output capacitor is also recommended for stability and good load transient response. The dropout voltage ($V_{DO}$) is less than 140 mV maximum at a 2.8-V output voltage and 300-mA output current, so there are no dropout issues with a minimum input voltage of 3.0 V and a maximum output current of 200 mA.

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### 8.2.3 Application Curves

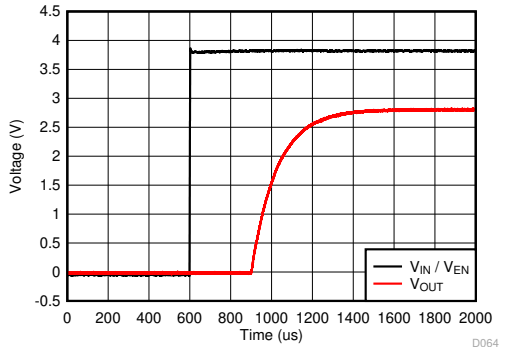


**Figure 8-5. Start-Up**

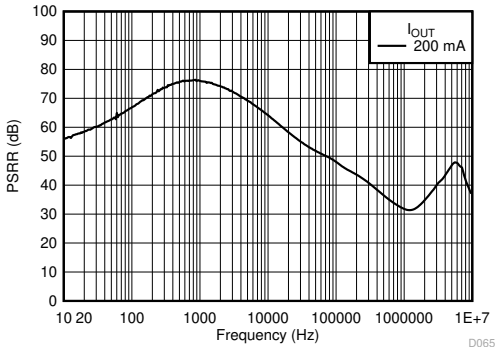


**Figure 8-6. PSRR**

## 9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.6 V to 6.0 V. The input supply must be well regulated and free of spurious noise. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 0.3 V or 1.6 V, whichever is greater. TI highly recommends using a 1-µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.


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# 10 Layout

## 10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

## 10.2 Layout Examples

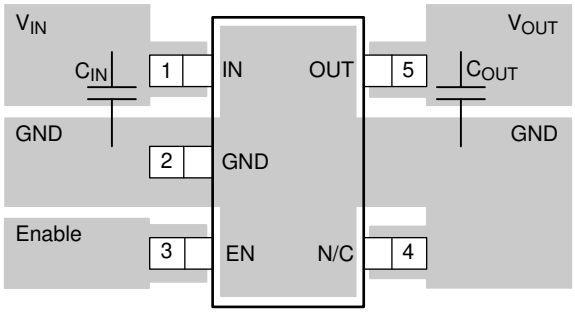


**Figure 10-1. DBV Package (SOT-23) Typical Layout**

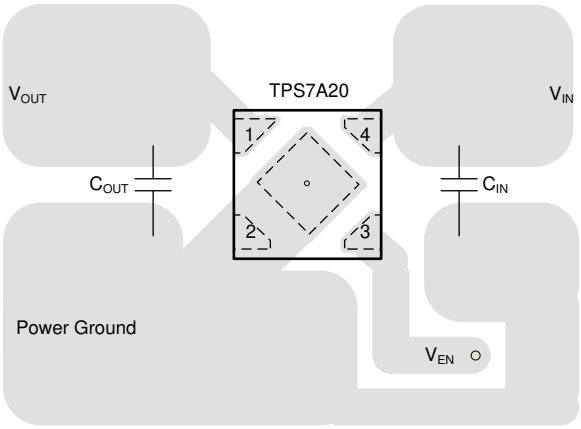


**Figure 10-2. DQN Package (X2SON) Typical Layout**

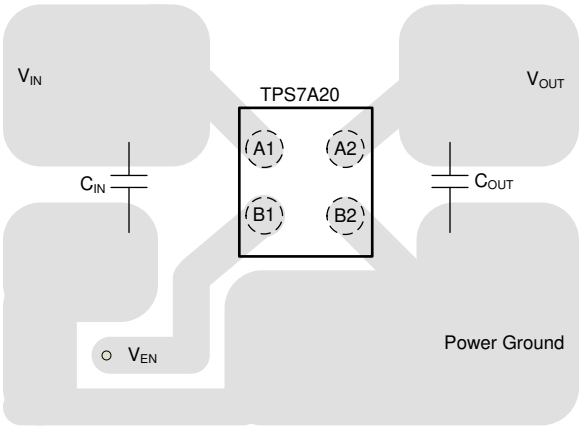


**Figure 10-3. YCJ and YCK Package (DSBGA) Typical Layout**

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# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 Device Nomenclature

**Table 11-1. Device Nomenclature**

| PRODUCT (1) (2) | $V_{OUT}$ |
|---|---|
| TPS7A20**xx(x)Pyyyz** | **xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V).<br>**P** indicates an active output discharge feature. All members of the TPS7A20 family actively discharge the output when the device is disabled.<br>**yyy** is the package designator.<br>**z** is the package quantity. R is for reel (3000 pieces for DQN and DBV; 12000 pieces for YCJ and YCK). |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.8 V to 5.5 V in 25-mV increments are available. Contact the factory for details and availability.

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 11.4 Trademarks

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## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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