Errata Sheet for Cyclone IV Devices

This errata sheet provides updated information on known device issues affecting Cyclone® IV devices.

Table 1 lists specific Cyclone IV issues, and which Cyclone IV devices are affected by each issue.

Table 1. Known Issues for Cyclone IV Devices (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"PLL phasedone Signal Stuck at Low" In some cases, the Cyclone IV phase-locked loop (PLL) blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift.	All Cyclone IV Devices	Quartus II software version 12.0 and later.
"Human Body Model Electrostatic Discharge" The row I/Os on certain Cyclone IV GX devices do not meet the human body model (HBM) electrostatic discharge (ESD) specification stated in the device datasheet.	EP4CGX15 and EP4CGX30 (except for the F484 package) Devices	No plan to fix silicon.
"DisplayPort Receiver Specification" The Cyclone IV GX transceiver is compliant with the DisplayPort transmitter specifications only for 1.62 Gbps and 2.7 Gbps data rates. The transceiver is not compliant with the DisplayPort receiver jitter tolerance specification.	All Cyclone IV GX Devices	No plan to fix silicon.
"Asynchronous Spread Spectrum Clock Modulation Tracking" The transceiver channels do not support tracking of the incoming data with asynchronous spread spectrum clock (SSC) modulation.	EP4CGX30 (F484 package), EP4CGX50, and EP4CGX75 Devices only. Support of asynchronous SSC tracking capability was never planned for other Devices.	No plan to fix silicon.
"SATA CDR PPM Tolerance" To support the serial ATA (SATA) protocol in Cyclone IV GX devices, you must constrain the clock data recovery (CDR) parts-per-million (PPM) tolerance to a specified range.	EP4CGX30 (F484 package), EP4CGX50, and EP4CGX75 Devices	No plan to fix silicon.
"Remote System Upgrade" The remote system upgrade (RSU) feature fails when loading an invalid configuration image.	All Cyclone IV GX Devices	Quartus II software version 11.1

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Table 1. Known Issues for Cyclone IV Devices (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"Pin Connection Guidelines Update for Transceiver Applications that Run at ≥ 2.97 Gbps Data Rate" The affected Cyclone IV GX devices may not able to meet the protocol jitter specification or may have a higher bit error rate (BER) if you do not follow these guidelines.	EP4CGX30 (F484 package), EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 Devices	No plan to fix silicon.
"Quartus II Mapping Issue with a PCIe ×1 Interface Using the Hard IP Block" The Quartus II software incorrectly maps the PCIe interfaces when using the hard IP block.	All Cyclone IV GX Devices	Quartus II software version 10.1
"PLL Cascading for Transceiver Applications is not Supported" Only the direct `REFCLK` or `DIFFCLK` pins driving the phase-locked loop (PLL) input of a transceiver are allowed.	All Cyclone IV GX Devices	Fix is not applicable. Software restriction is added in Quartus II software version 10.1 and later.
"Removal of the ±500 PPM and ±1000 PPM Options for the Programmable PPM Detector in the ALTGX MegaWizard Plug-In Manager" The ±**500 PPM** and ±**1000 PPM** options in the ALTGX MegaWizard Plug-In Manager are not supported.	All Cyclone IV GX Devices	No plan to fix silicon.
"External Memory Specification for DDR2 SDRAM" Final full-rate DDR2 SDRAM maximum clock rate specification on column and row I/Os.	All Cyclone IV E Core Voltage 1.0-V I8L Devices	For the solution, refer to "External Memory Specification for DDR2 SDRAM" on page 10.

PLL phasedone Signal Stuck at Low

In some cases, the Cyclone IV PLL blocks exhibit the `phasedone` signal stuck at low during the PLL dynamic phase shift. When the PLL `phasedone` signal is stuck at low, the intended phase shift does not happen. You can recover from the PLL `phasedone` signal being stuck at low by resetting the PLL or by restarting the phase shift operation by asserting the `phasestep` signal.

Solution

To resolve the PLL `phasedone` signal stuck at low issue, the Altera® PLL megafunction is enhanced to automatically restart the phase shift operation internally in the Altera PLL megafunction whenever the PLL `phasedone` signal is stuck at low. Restarting the phase shift operation compensates for the missing phase shift operation and also recovers the `phasedone` signal.

This Altera PLL megafunction solution will be implemented in the Quartus II software version 12.0 and later. Altera recommends upgrading to the latest Quartus II software, regenerating the PLL megafunction, and recompiling your design.

Additionally, software patches are available for the Quartus II software versions 9.1 SP2 and 10.1 SP1 to upgrade the PLL megafunction with the solution. To download and install the Quartus II software patch, refer to the PLL Phasedone Stuck at Low Solution.

If you need additional support, file a service request using mySupport.

Human Body Model Electrostatic Discharge

The row I/Os on certain Cyclone IV GX devices do not meet the human body model (HBM) electrostatic discharge (ESD) specification stated in the device datasheet. All other I/Os, including the high-speed serial interface (HSSI) I/Os, meet the HBM ESD specification.

This issue only affects the EP4CGX15 and EP4CGX30 (except for the F484 package) devices and there will not be a silicon fix.

The EP4CGX15 and EP4CGX30 (except for the F484 package) devices are considered HBM Class 0 per JEDEC standard 22-A114. Altera recommends handling the ESD-sensitive devices using the ESD control methods as stated in ANSI/ESD S20.20 or IEC61340-5-1.

If you have additional questions, contact your local Altera sales representative.

DisplayPort Receiver Specification

The Cyclone IV GX transceiver meets the transmitter compliance specifications as a 1.62 Gbps and 2.7 Gbps transmitter for a digital display interface unit.

However, the Cyclone IV GX transceiver does not meet the receiver jitter tolerance specification that requires tracking of at least one unit interval (UI) at 2 MHz jitter tolerance test without asynchronous spread spectrum clocking (SSC) modulation enabled. If you want to use the transceiver as a DisplayPort receiver, you must verify the system margin and its jitter components in the application design.

Asynchronous Spread Spectrum Clock Modulation Tracking

The receiver clock data recover (CDR) is not able to track the incoming data with asynchronous SSC modulation for the serial ATA (SATA), DisplayPort, and V-by-one HS protocols.

The receiver CDR is able to track the incoming data with synchronous SSC modulation for the PCI Express® (PCIe®) Gen1 protocol.

If you are considering a custom protocol design that requires SSC modulation in a Basic mode configuration, Altera recommends designing with synchronous SSC modulation.

SATA CDR PPM Tolerance

You must constrain the CDR PPM tolerances for both SATA Gen1 and Gen2 data rates based on Table 2 without asynchronous SSC modulation for incoming data.

Table 2. CDR PPM Device Tolerances (Asynchronous SSC Not Enabled)

	Device								Unit
	EP4CGX15	EP4CGX22	EP4CGX30 (F169/F324 packages)	EP4CGX30 (F484 package)	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150	
CDR PPM tolerance (Async SSC not enabled)	±350 (1)	±350 (1)	±350 (1)	±200	±200	±200	±350 (1)	±350 (1)	PPM

Note to Table 2:

(1) To support CDR PPM tolerances greater than ±300 PPM, implement a PPM detector in your user logic and configure your device in CDR to Manual Lock mode.

Remote System Upgrade

The remote system upgrade (RSU) feature does not operate correctly when you initiate a reconfiguration cycle that goes from a factory configuration image to an invalid application configuration image. In this scenario, the Cyclone IV GX device fails to revert back to the factory configuration image after a configuration error is detected while loading the invalid application configuration image. The failure is indicated by a continuous toggling of the nSTATUS pin, or the CONF_DONE pin stays low after configuration.

In a correct operation, the Cyclone IV GX device would revert back to the factory configuration image after a configuration error is detected with the invalid configuration image.

An invalid application configuration image is classified as one of the following:

- A partially programmed application image
- An application image assigned with a wrong start address

The RSU feature works correctly with all other reconfiguration trigger conditions.

Workaround

A workaround is implemented in the ALTREMOTE_UPDATE megafunction and is available in Quartus® II software version 11.1 by enabling the **POF checking** feature.

For more information about the **POF checking** feature, refer to *AN 603: Active Serial Remote System Upgrade Reference Design*.

Pin Connection Guidelines Update for Transceiver Applications that Run at ≥ 2.97 Gbps Data Rate

You may not meet the protocol jitter specification or may have a higher bit error rate (BER) if you do not use the following guidelines.

If your transceiver applications run at ≥ 2.97 Gbps data rate, you must ground specific pins (refer to Table 3) next to the reference clock directly through the via under the device to the PCB ground plane on your board. You also must assign the specific pins to ground in the Quartus II software. To minimize the impact listed in Table 3, Altera recommends using REFCLK[1..0] and REFCLK[5..4] reference clocks before using REFCLK2 and REFCLK3 reference clocks.

There is no action required and no performance degradation for input reference clocks that are used to drive transceiver channels at < 2.97 Gbps data rates.

Table 3 lists the reference clock pins and the associated I/O pins to be grounded for transceiver applications that run at ≥ 2.97 Gbps data rate.

Table 3. Reference Clock Pins and the Associated I/O Pins to be Grounded for ≥ 2.97 Gbps Transceiver Applications (Part 1 of 3)

Package	Reference Clock	Bank	Reference Clock Pins	I/O Pins to Ground	Impact
F23	REFCLK[1..0]	3B (1)	M7 M8 N7 N8	AA4 (CRC_ERROR) (5) W8 (INIT_DONE) (5) AB3 (nCEO) (5) T7 T8 V6	MPLL_5 and/or GPLL_1 ZDB mode is not supported. (7)
	REFCLK2	3A (2)	M11 N11	AB10 AB11 R13 T13 W12 W13	If you use a DDR system, the following DQ groups will not be supported (8): ■ DQ4B in ×8 groups ■ DQ5B in ×8/×9 groups ■ DQ3B and DQ5B in ×16/×18 groups ■ DQ5B in ×32/×36 groups

Table 3. Reference Clock Pins and the Associated I/O Pins to be Grounded for ≥ 2.97 Gbps Transceiver Applications (Part 2 of 3)

Package	Reference Clock	Bank	Reference Clock Pins	I/O Pins to Ground	Impact
F27	REFCLK[1..0]	3B (1)	T9 T10 U9 U10	AC6 (CRC_ERROR) (5) AB7 (INIT_DONE) (5) AC7 (nCEO) (5) AC5 AD4 AB5	MPLL_5 and/or GPLL_1 ZDB mode is not supported. (7)
	REFCLK[5..4]	8B (1)	K9 K10 L9 L10	E6 (DATA1/ASDO) (5) D5 (nCSO) (5) E2 D4 (CLKUSR) (5), (6) E1 D6 (DATA0) (5)	MPLL_8 ZDB mode is not supported. (7)
	REFCLK2	3A (2), (4)	T14 T15	AC14 AD14 AE14 AF10 AF11 AF12	If you use a DDR system, the following DQ groups will not be supported (7): ■ DQ4B in ×8 groups ■ DQ5B in ×8/×9 groups ■ DQ3B and DQ5B in ×16/×18 groups ■ DQ5B in ×32/×36 groups
	REFCLK3	8A (3), (4)	L14 L15	A12 A13 B13 C13 C14 C15	If you use a DDR system, the following DQ groups will not be supported (7): ■ DQ5T in ×8 groups ■ DQ3T and DQ5T in ×16/×18 groups ■ DQ5T in ×32/×36 groups

Table 3. Reference Clock Pins and the Associated I/O Pins to be Grounded for ≥ 2.97 Gbps Transceiver Applications (Part 3 of 3)

Package	Reference Clock	Bank	Reference Clock Pins	I/O Pins to Ground	Impact
F31	REFCLK[1..0]	3B (1)	V11 V12 W11 W12	AD6 (CRC_ERROR) (5) AE8 (INIT_DONE) (5) AE7 (nCEO) (5) AE6 AF6 AG6	MPLL_5 and/or GPLL_1 ZDB mode is not supported. (7)
	REFCLK[5..4]	8B (1)	K11 L10 L11 M10	G9 (DATA1/ASDO) (5) B4 (nCSO) (5) A4 (CLKUSR) (5), (6) A3 (DATA0) (5) F8 G8	MPLL_8 ZDB mode is not supported. (7)
	REFCLK2	3A (2), (4)	V15 W15	AA17 AF16 AG16 AH16 AJ13 AK14	If you use a DDR system, the following DQ groups will not be supported (8): ■ DQ4B in ×8 groups ■ DQ5B in ×8/×9 groups ■ DQ4B in ×16/×18 groups ■ DQ2B in ×32/×36 groups
	REFCLK3	8A (3), (4)	K15 L15	A16 B16 C16 F16 G15 K17	If you use a DDR system, DQ5T in ×8/×9, ×16/×18, and ×32/×36 groups will not be supported. (8)

Notes to Table 3:

(1) The unused adjacent reference clock pins in the same bank can only be used as differential input clock.

(2) The unused adjacent reference clock pins in Bank 4 (Package F23: AA12 and AB12 pins, package F27: AF13 and AF14 pins, and package F31: AJ16 and AK16 pins) can only be used as differential input clock.

(3) The unused adjacent reference clock pins in Bank 7 (Package F27: A14 and B14 pins and package F31: A15 and B15 pins) can only be used as differential input clock.

(4) You can only use REFCLK2 in Bank 3A for transceiver block GXBL0 and REFCLK3 in Bank 8A for transceiver block GXBL1.

(5) Do not tie this pin to ground if it is used for configuration or a dedicated function in User mode. Dedicated functions include using the DATA1/ASDO, nCSO, and DATA0 pins for EPCS access and the crc_error pin for a cyclic redundancy check (CRC) error function. Do not use this pin as a user I/O in User mode.

(6) Do not toggle the CLKUSR pin in User mode. Reassign the CLKUSR pin to another I/O pin if it is being used in User mode.

(7) You can alternatively use zero delay buffer (ZDB) mode with other phase-locked loops (PLLs).

(8) You can alternatively use other DQ/DQS groups or wraparound DQ/DQS groups. For more information about wraparound DQ/DQS performance, refer to the External Memory Interface Spec Estimator page on Altera website.

Table 4 lists the Quartus II software support planning.

Table 4. Quartus II Software Planned Support

Quartus II Software Version	Software Enforcement Plan
Releases prior to version 11.0	Follow the guidelines documented in this errata sheet as the Quartus II software does not enforce these guidelines.
Version 11.0 release and later	The Quartus II software enforces the guidelines documented in this errata sheet.

The *Cyclone IV Device Family Pin Connection Guidelines* has been updated with the guidelines for transceiver applications that run at ≥ 2.97 Gbps data rate.

Quartus II Mapping Issue with a PCIe ×1 Interface Using the Hard IP Block

The Quartus II software version 10.0 SP1 and prior releases incorrectly allowed logical channel 0 to be placed in any physical channel for the PCIe Gen1 ×1 interface with the hard IP block. For correct operation with the hard IP block, logical channel 0 must be placed in physical channel 0.

This issue is fixed in the Quartus II software version 10.1. If you have already designed or fabricated your boards using the incorrect mapping, file a service request using mysupport for assistance to remedy this issue.

PLL Cascading for Transceiver Applications is not Supported

Using the clock output of another PLL to drive the PLL input of a transceiver is not allowed. Only the direct `REFCLK` or `DIFFCLK` pins driving the PLL input of a transceiver is allowed.

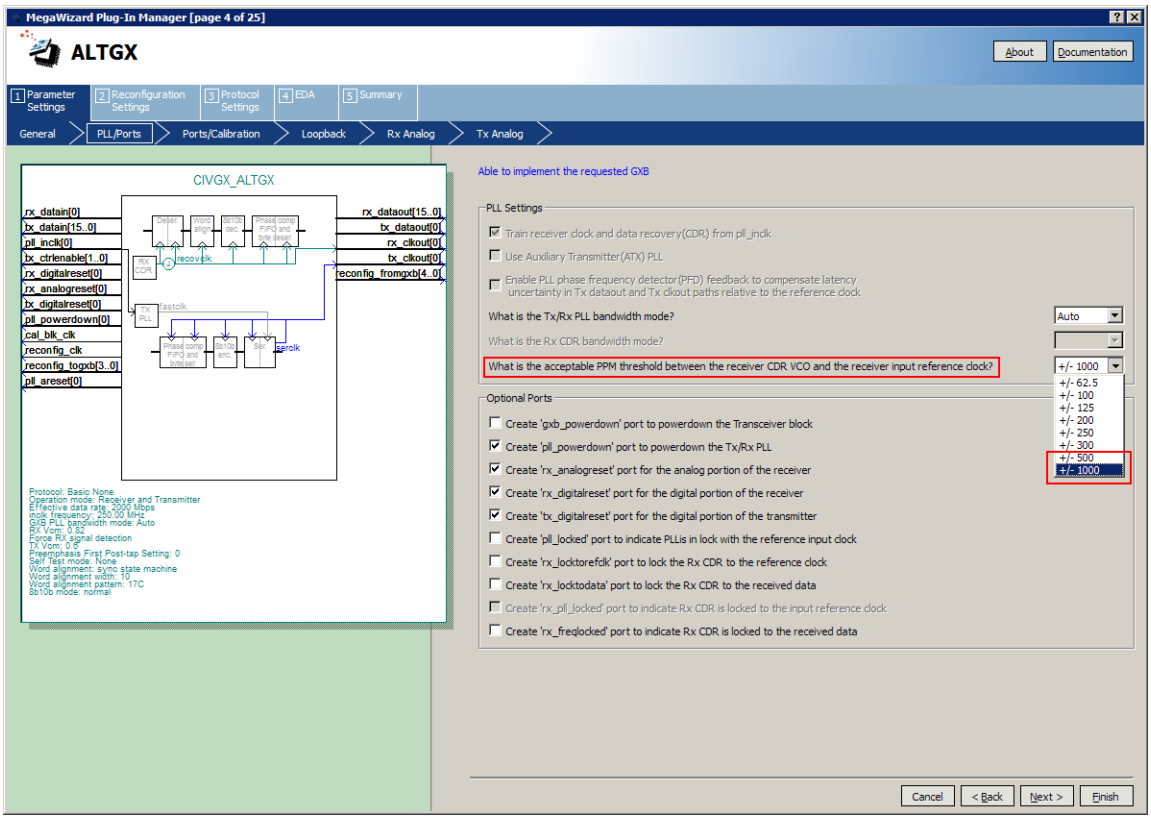
Hence, PLL cascading for transceiver applications is restricted by the Quartus II software version 10.1 and later. If you use PLL cascading for transceiver applications, the Quartus II Analysis and Synthesis reports an error during compilation.

Removal of the ±500 PPM and ±1000 PPM Options for the Programmable PPM Detector in the ALTGX MegaWizard Plug-In Manager

The **±500 PPM** and **±1000 PPM** options for the Programmable PPM Detector feature in the ALTGX MegaWizard™ Plug-In Manager, as shown in Figure 1, are no longer supported in the Quartus II software version 10.0 SP1 and later. These options are removed because the programmed PPM threshold values exceed the receiver CDR PPM tolerance between the upstream transmitter reference clock and the local receiver reference clock.

Figure 1 shows the Programmable PPM Detector options in ALTGX MegaWizard Plug-In Manager in the Quartus II software, version 10.0.

Figure 1. Programmable PPM Detector Options in the ALTGX MegaWizard Plug-In Manager



Designs compiled with the Quartus II software version 10.0 and earlier may have a link failure risk when the receiver is operating in a system that has ±500 PPM or ±1000 PPM differences for the reference clock frequencies between the upstream transmitter and the local receiver. Using CDR Manual Lock mode does not overcome the link failure risk.

For a receiver design that has the **±500 PPM** or **±1000 PPM** options selected in the Programmable PPM Detector feature, Altera recommends evaluating the system operation with different options, ranging between ±62.5 PPM and ±300 PPM. To change the **Programmable PPM Detector** option, regenerate and recompile the ALTGX MegaWizard Plug-In Manager design file with the supported options.

If you compiled your designs using a Quartus II software version prior to 10.0 SP1, and you have selected the **±500 PPM** or the **±1000 PPM** option for the Programmable PPM Detector feature, the Quartus II Analysis and Synthesis error will be reported in the Quartus II software version 10.0 SP1 and later.

External Memory Specification for DDR2 SDRAM

In the Quartus II software version 10.0, the Cyclone IV E I8L speed grade supported full-rate DDR2 SDRAM with a maximum clock rate of up to 150 MHz on column and row I/Os. This maximum clock rate is a preliminary specification pending the finalization of the timing model.

In the Quartus II software version 10.0 SP1 and later, the Cyclone IV E I8L speed grade full-rate DDR2 SDRAM maximum clock rate specification on column and row I/Os has been revised due to the finalization of the timing model for the Cyclone IV E device family. Table 5 lists the current specification.

Table 5. Full-Rate DDR2 SDRAM Support for Cyclone IV E Core Voltage 1.0-V Devices

Memory Standard	Device	Speed Grade	Maximum Clock Rate (MHz)
			Column and Row I/O
			Single Chip Select
DDR2 SDRAM	Cyclone IV E Core Voltage 1.0 V	I8L	133 (1)

Note to Table 5:

(1) You must use the 267-MHz memory device speed grade to achieve the maximum clock rate.

Designs that already use the affected devices running full-rate DDR2 SDRAM at the old maximum clock rate and pass timing in the Quartus II software version 10.0 SP1 and later run acceptably at the old frequencies—provided that the board settings panel in the IP MegaWizard Plug-In Manager is populated accurately and the board trace models representative of the relevant system are correctly entered in the Pin Planner.

Document Revision History

Table 6 lists the revision history for this Errata Sheet.

Table 6. Document Revision History (Part 1 of 2)

Date	Version	Changes
June 2012	2.3	Added the "PLL phasedone Signal Stuck at Low" section.
February 2012	2.2	Updated the "Remote System Upgrade" section and Table 1.
February 2012	2.1	Updated Table 1.
March 2011	2.0	Added the following sections: ■ "Human Body Model Electrostatic Discharge" ■ "DisplayPort Receiver Specification" ■ "Asynchronous Spread Spectrum Clock Modulation Tracking" ■ "SATA CDR PPM Tolerance" ■ "Remote System Upgrade" Removed the old "Human Body Model Electrostatic Discharge" section.

Table 6. Document Revision History (Part 2 of 2)

Date	Version	Changes
November 2010	1.1	Added the following sections: ■ "Cyclone IV GX Pin Connection Guidelines Update for Transceiver Applications that Run at ³ 2.97 Gbps Data Rate" ■ "Quartus II Mapping Issue with PCIe ×1 Interface Using the Hard IP Block" ■ "PLL Cascading for Transceiver Applications is not Supported" ■ "Removal of ±500 PPM and ±1000 PPM Options for Programmable PPM Detector in ALTGX MegaWizard Plug-In Manager" ■ "External Memory Specification for DDR2 SDRAM"
April 2010	1.0	Initial release.