LC²MOS
Complete, 12-Bit, 100 kHz, Sampling ADCs
AD7870/AD7870A/AD7875/AD7876

2

FEATURES

Complete Monolithic 12-Bit ADC with:
- **2 μs Track/Hold Amplifier**
- **8 μs A/D Converter**
- **On-Chip Reference**
- **Laser-Trimmed Clock**
- **Parallel, Byte and Serial Digital Interface**

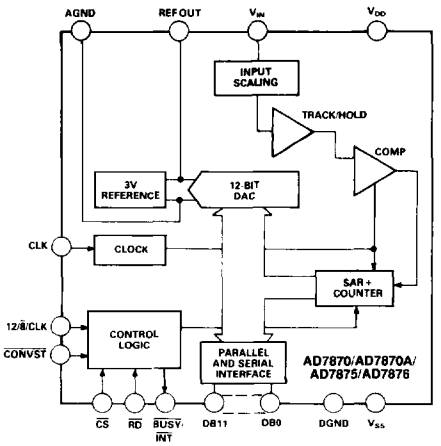
72 dB SNR at 10 kHz Input Frequency (AD7870, AD7870A, AD7875)

57 ns Data Access Time

Low Power −60 mW typ

Variety of Input Ranges:
- **±3 V for AD7870/AD7870A**
- **0 to +5 V for AD7875**
- **±10 V for AD7876**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7870/AD7870A/AD7875/AD7876 is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8 μs successive-approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock which is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required.

The parts offer a choice of three data output formats: a single, parallel, 12-bit word; two 8-bit bytes, or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

All parts operate from ±5 V power supplies. The AD7870 and AD7876 accept input signal ranges of ±3 V and ±10 V, respectively, while the AD7875 accepts a unipolar 0 to +5 V input range. The parts can convert full power signals up to 50 kHz.

The AD7870/AD7870A/AD7875/AD7876 feature dc accuracy specifications such as linearity, full-scale and offset error. In addition, the AD7870/AD7870A and AD7875 are fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

The parts are fabricated in Analog Devices' Linear Compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low-power CMOS logic. The parts are available in a 24-pin, 0.3 inch-wide, plastic or hermetic dual-in-line package (DIP). The AD7870/AD7870A and AD7875 are available in a 28-pin plastic leaded chip carrier (PLCC), while the AD7876 is available and in a 24-pin small outline (SOIC) package.

PRODUCT HIGHLIGHTS

1. Complete 12-Bit ADC on a Chip.
   The AD7870/AD7870A/AD7875/AD7876 provides all the functions necessary for analog-to-digital conversion and combines a 12-bit ADC with internal clock, track/hold amplifier and reference on a single chip.
2. Dynamic Specifications for DSP Users.
   The AD7870/AD7870A and AD7875 are fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion.
3. Fast Microprocessor Interface.
   Data access times of 57 ns make the parts compatible with modern 8- and 16-bit microprocessors and digital signal processors. Key digital timing parameters are tested and guaranteed over the full operating temperature range.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD7870/AD7870A/AD7875/AD7876—SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V, f_{CLK} = 2.5 MHz external, unless otherwise stated. All Specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7870/AD7870A J, A[1]	K, B[1]	L, C[1]	S[1]	T[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]							
Signal to Noise Ratio[3] (SNR)							
@ +25°C	70	70	72	69	69	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	70	71	69	69	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	−80	−80	−80	−78	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−80	−78	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)							
Second Order Terms	−80	−80	−80	−78	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−80	−78	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	2	2	2	2	μs max	
DC ACCURACY							
Resolution	12	12	12	12	12	Bits	
Minimum Resolution for which							
No Missing Codes are Guaranteed	12	12	12	12	12	Bits	
Integral Nonlinearity	±1/2	±1/2	±1/4	±1/2	±1/2	LSB typ	
Integral Nonlinearity		±1	±1/2		±1	LSB max	
Differential Nonlinearity		±1	±1		±1	LSB max	
Bipolar Zero Error	±5	±5	±5	±5	±5	LSB max	
Positive Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
Negative Full-Scale Error[4]	±5	±5	±5	±5	±5	LSB max	
ANALOG INPUT							
Input Voltage Range	±3	±3	±3	±3	±3	Volts	
Input Current	±500	±500	±500	±500	±500	μA max	
REFERENCE OUTPUT							
REF OUT @ +25°C	2.99	2.99	2.99	2.99	2.99	V min	
	3.01	3.01	3.01	3.01	3.01	V max	
REF OUT Tempco	±60	±60	±35	±60	±35	ppm/°C max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	±1	±1	±1	±1	mV max	Reference Load Current Change (0–500 μA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS							
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$/CLK Input Only)	±10	±10	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	10	10	pF max	
LOGIC OUTPUTS							
Output High Voltage, V_{OH}	4.0	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0							
Floating-State Leakage Current	±10	±10	±10	±10	±10	μA max	
Floating-State Output Capacitance[5]	15	15	15	15	15	pF max	
CONVERSION TIME							
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	8	8	μs max	
Internal Clock	7/9	7/9	7/9	7/9	7/9	μs min/μs max	
POWER REQUIREMENTS							
V_{DD}	+5	+5	+5	+5	+5	V nom	±5% for Specified Performance
V_{SS}	−5	−5	−5	−5	−5	V nom	±5% for Specified Performance
I_{DD}	13	13	13	13	13	mA max	Typically 8 mA
I_{SS}	6	6	6	6	6	mA max	Typically 4 mA
Power Dissipation	95	95	95	95	95	mW max	Typically 60 mW

NOTES

[1]Temperature ranges are as follows: J, K, L Versions; 0 to +70°C: A, B, C Versions; −25°C to +85°C: S, T Versions; −55°C to +125°C. AD7870A has only J Version.

[2]V_{IN} (pk–pk) = ±3 V.

[3]SNR calculation includes distortion and noise components.

[4]Measured with respect to internal reference and includes bipolar offset error.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

Parameter	AD7875/AD7876 K, B[1]	L, C[1]	T[1]	Units	Test Conditions/Comments
DC ACCURACY					
Resolution	12	12	12	Bits	
Minimum Resolution for Which					
No Missing Codes Are Guaranteed	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	LSB max	
T_{min} to T_{max} (AD7875 Only)	±1	±1	±1	LSB max	
T_{min} to T_{max} (AD7876 Only)	±1	±1/2	±1	LSB max	
Differential Nonlinearity	±1	±1	−1, +1.5	LSB max	
Unipolar Offset Error (AD7875 Only)	±5	±5	±5	LSB max	
Bipolar Zero Error (AD7876 Only)	±6	±2	±6	LSB max	
Full-Scale Error at +25°C[2]	±8	±8	±8	LSB max	Typical full-scale error is ±1 LSB
Full-Scale TC[2]	±60	±35	±60	ppm/°C max	Typical TC is ±20 ppm/°C
Track/Hold Acquisition Time	2	2	2	μs max	
DYNAMIC PERFORMANCE[3] (AD7875 ONLY)					
Signal-to-Noise Ratio[4] (SNR)					
@ +25°C	70	72	69	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{min} to T_{max}	70	71	69	dB min	Typically 71.5 dB for 0 < V_{IN} < 50 kHz
Total Harmonic Distortion (THD)	−80	−80	−78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	−80	−80	−78	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz Typically −86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)					
Second Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	−80	−80	−78	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
ANALOG INPUT					
AD7875 Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	
AD7875 Input Current	500	500	500	μA max	
AD7876 Input Voltage Range	±10	±10	±10	Volts	
AD7876 Input Current	±600	±600	±600	μA max	
REFERENCE OUTPUT					
REF OUT @ +25°C	2.99 3.01	2.99 3.01	2.99 3.01	V min V max	
REF OUT Tempco	±60	±35	±60	ppm/°C max	Typical Tempco is ±20 ppm/°C
Reference Load Sensitivity (ΔREF OUT/ΔI)	−1	−1	−1	mV max	Reference Load Current Change (0–500 μA) Reference Load Should Not Be Changed During Conversion.
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$/CLK Input Only)	±10	±10	±10	μA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	10	10	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 40 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	10	10	10	μA max	
Floating-State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
External Clock (f_{CLK} = 2.5 MHz)	8	8	8	μs max	
Internal Clock	7/9	7/9	7/9	μs min/μs max	
POWER REQUIREMENTS	As per AD7870/AD7870A				

NOTES

[1]Temperature ranges are as follows: AD7875: K, L Versions, 0 to +70°C; B, C Versions, −40°C to +85°C; T Version, −55°C to +125°C. AD7876: B, C Versions, −40°C to +85°C; T Version, −55°C to +125°C.

[2]Includes internal reference error and is calculated after unipolar offset error (AD7875) or bipolar zero error (AD7876) has been adjusted out. Full-scale error refers to both positive and negative full-scale error for the AD7876.

[3]Dynamic performance parameters are not tested on the AD7876 but these are typically the same as for the AD7875.

[4]SNR calculation includes distortion and noise components.

[5]Sample tested @ +25°C to ensure compliance.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = −5 V ± 5%, AGND = DGND = 0 V. See Figures 9, 10, 11 and 12.)

Parameter	Limit at T_{min}, T_{max} (J, K, L, A, B, C Versions)	Limit at T_{min}, T_{max} (S, T Versions)	Units	Conditions/Comments
t_1	50	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	**75**	ns min	$\overline{RD}$ Pulse Width
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	70	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	**57**	**70**	ns max	Data Access Time after $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	**50**	ns max	
t_8	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	370	370	ns min	SCLK Cycle Time
t_{12}[6]	135	150	ns max	SCLK to Valid Data Delay. C_L=35 pF
t_{13}	20	20	ns min	SCLK Rising Edge to $\overline{SSTRB}$
	100	100	ns max	
t_{14}	10	10	ns min	Bus Relinquish Time after SCLK
	100	100	ns max	
t_{15}	60	60	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 2)
t_{16}	120	120	ns max	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay
t_{17}	200	200	ns min	Data Setup Time Prior to $\overline{BUSY}$
t_{18}	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 2)
t_{19}	0	0	ns min	HBEN to $\overline{CS}$ Setup Time
t_{20}	0	0	ns min	HBEN to $\overline{CS}$ Hold Time

NOTES

[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up on SCLK. The capacitance on all three outputs is 35 pF.

[3]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

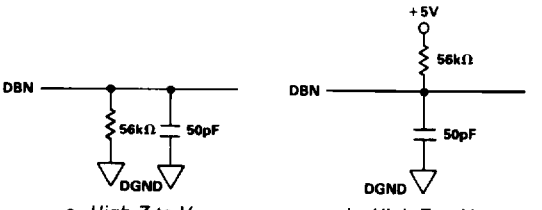
[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.

[6]SDATA will drive higher capacitive loads but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ||C_L) and hence the time to reach 2.4 V. Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

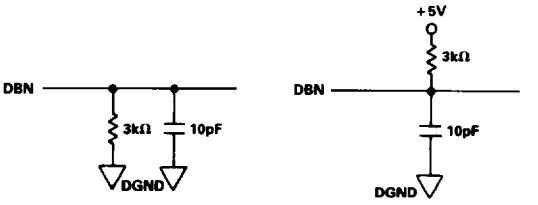
V_{DD} to AGND . . . . . −0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to −7 V
AGND to DGND . . . . . −0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . −15 V to +15 V
REF OUT to AGND . . . . . 0 V to V_{DD}
Digital Inputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J, K, L Versions – AD7870) . . . . . 0 to +70°C
Commercial (K, L Versions – AD7875) . . . . . 0 to +70°C
Industrial (A, B, C Versions – AD7870) . . . −25°C to +85°C
Industrial (B, C Versions – AD7875/AD7876) . . . . . −40°C to +85°C
Extended (S, T Versions) . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

AD7870 ORDERING GUIDE

Model[1, 2]	Temperature Range	V_{IN} Voltage Range (V)	SNR (dBs)	Integral Nonlinearity (LSB)	Package Option[3]
AD7870AJN	0 to +70°C	±3	70 min	±1/2 typ	N-24
AD7870JN	0 to +70°C	±3	70 min	±1/2 typ	N-24
AD7870KN	0 to +70°C	±3	70 min	±1 max	N-24
AD7870LN	0 to +70°C	±3	72 min	±1/2 max	N-24
AD7870JP	0 to +70°C	±3	70 min	±1/2 typ	P-28A
AD7870KP	0 to +70°C	±3	70 min	±1 max	P-28A
AD7870LP	0 to +70°C	±3	72 min	±1/2 max	P-28A
AD7870AQ	−25°C to +85°C	±3	70 min	±1/2 typ	Q-24
AD7870BQ	−25°C to +85°C	±3	70 min	±1 max	Q-24
AD7870CQ	−25°C to +85°C	±3	72 min	±1/2 max	Q-24
AD7870SQ[4]	−55°C to +125°C	±3	69 min	±1/2 typ	Q-24
AD7870TQ[4]	−55°C to +125°C	±3	69 min	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]Contact local sales office for LCCC (Leadless Ceramic Chip Carrier) availability.
[3]N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip. For outline information see Package Information section.
[4]Available to /883B processing only.

AD7875 ORDERING GUIDE

Model[1]	Temperature Range	V_{IN} Voltage Range (V)	SNR (dBs)	Integral Nonlinearity (LSB)	Package Option[2]
AD7875KN	0 to +70°C	0 to +5	70 min	±1 max	N-24
AD7875LN	0 to +70°C	0 to +5	72 min	±1/2 max	N-24
AD7875KR	0 to +70°C	0 to +5	70 min	±1 max	R-24
AD7875KP	0 to +70°C	0 to +5	70 min	±1 max	P-28A
AD7875LP	0 to +70°C	0 to +5	72 min	±1/2 max	P-28A
AD7875BQ	−40°C to +85°C	0 to +5	70 min	±1 max	Q-24
AD7875CQ	−40°C to +85°C	0 to +5	72 min	±1/2 max	Q-24
AD7875TQ[3]	−55°C to +125°C	0 to +5	69 min	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]Available to /883B processing only.

AD7876 ORDERING GUIDE

Model[1]	Temperature Range	V_{IN} Voltage Range (V)	Integral Nonlinearity (LSB)	Package Option[2]
AD7876BN	−40°C to +85°C	±10	±1 max	N-24
AD7876CN	−40°C to +85°C	±10	±1/2 max	N-24
AD7876BR	−40°C to +85°C	±10	±1 max	R-24
AD7876CR	−40°C to +85°C	±10	±1/2 max	R-24
AD7876BQ	−40°C to +85°C	±10	±1 max	Q-24
AD7876CQ	−40°C to +85°C	±10	±1/2 max	Q-24
AD7876TQ[3]	−55°C to +125°C	±10	±1 max	Q-24

NOTES
[1]To order MIL-STD-883, Class B, processed parts, add /883B to part number. Contact local sales office for military data sheet.
[2]N = Narrow Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.
[3]Available to /883B processing only.

PIN FUNCTION DESCRIPTION

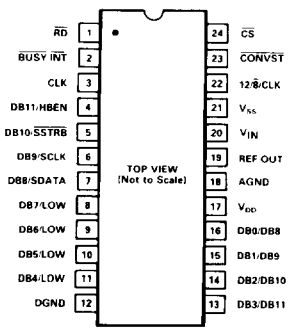
DIP Pin No.	Pin Mnemonic	Function
1	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.
2	$\overline{BUSY}/\overline{INT}$	Busy/Interrupt, Active low logic output indicating converter status. See timing diagrams.
3	CLK	Clock input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed clock oscillator.
4	DB11/HBEN	Data Bit 11 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input (see below). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table I).
5	DB10/$\overline{SSTRB}$	Data Bit 10/Serial Strobe. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ is an active low open-drain output that provides a strobe or framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{SSTRB}$.
6	DB9/SCLK	Data Bit 9/Serial Clock. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If the 12/$\overline{8}$/CLK input is at −5 V, then SCLK runs continuously. If 12/$\overline{8}$/CLK is at 0 V, then SCLK is gated off after serial transmission is complete. SCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
7	DB8/SDATA	Data Bit 8/Serial Data. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is an open-drain serial data output which is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low. An external 4.7 kΩ pull-up resistor is required on SDATA.
8–11	DB7/LOW–DB4/LOW	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB7-DB4. With 12/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table I).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13–16	DB3/DB11–DB0/DB8	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With/12/$\overline{8}$/CLK high, they are always DB3-DB0. With 12/$\overline{8}$/CLK low or −5 V, their function is controlled by HBEN (see Table I).
17	V_{DD}	Positive Supply, +5 V ±5%.
18	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
19	REF OUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 μA.
20	V_{IN}	Analog Input. The analog input range is ±3 V for the AD7870, ±10 V for the AD7876 and 0 to +5 V for the AD7875.
21	V_{SS}	Negative Supply, −5 V ±5%.
22	12/$\overline{8}$/CLK	Three Function Input. Defines the data format and serial clock format. With this pin at +5 V, the output data format is 12-bit parallel only. With this pin at 0 V, either byte or serial data is available and SCLK is not continuous. With this pin at −5 V, byte or serial data is again available but SCLK is now continuous.
23	$\overline{CONVST}$	Convert Start. A low to high transition on this input puts the track/hold into its hold mode and starts conversion. This input is asynchronous to the CLK input.
24	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11 (MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

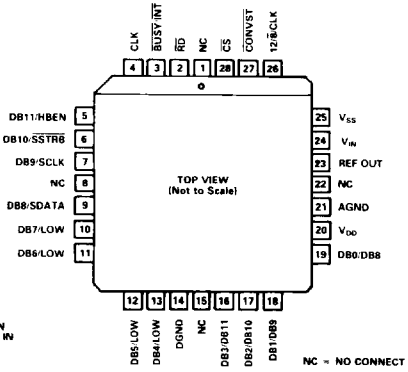
Table I. Output Data for Byte Interfacing

PIN CONFIGURATIONS[1]

DIP and SOIC[2]



PLCC[2]



NC = NO CONNECT

[1]PIN CONFIGURATIONS ARE THE SAME FOR THE AD7870, AD7875 AND AD7876.
[2]THE AD7870 AND AD7875 ARE AVAILABLE IN DIP AND PLCC; THE AD7870A IS AVAILABLE IN PLASTIC DIP; THE AD7875 AND AD7876 ARE AVAILABLE IN SOIC AND DIP.