LOW PHASE NOISE CLOCK MULTIPLIER ICS601-21

Description

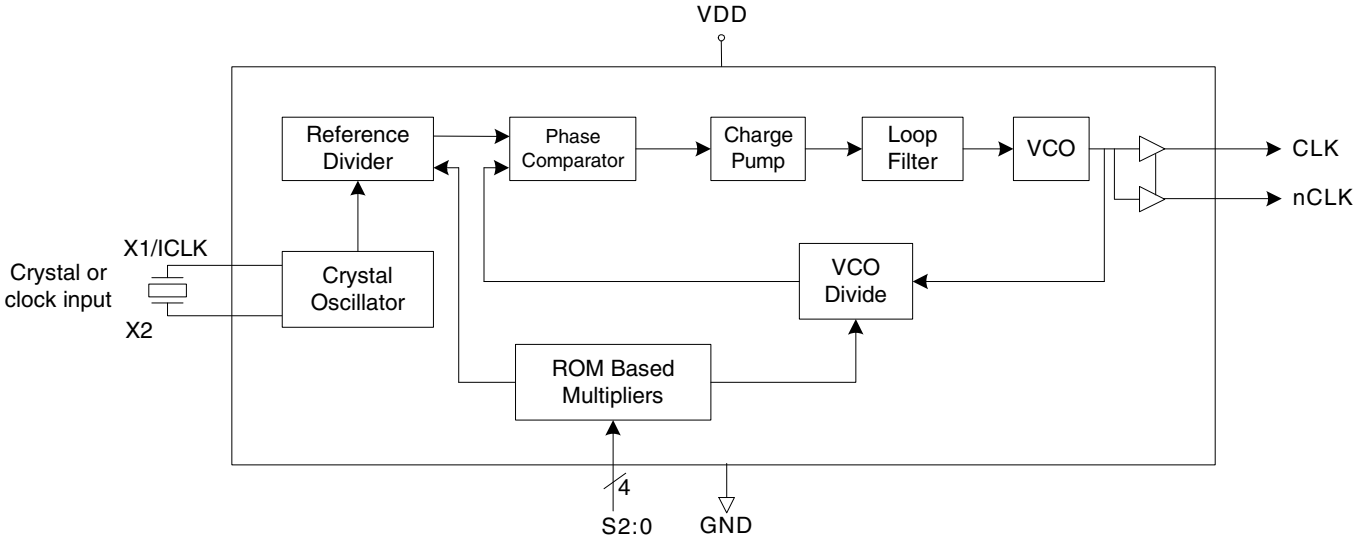
The ICS601-21 is a low-cost, low phase noise, high performance clock synthesizer for applications which require low phase noise and low jitter. It is IDT's lowest phase noise multiplier. Using IDT's patented analog and digital Phase Locked Loop (PLL) techniques, the chip accepts a crystal or clock input, and produces output clocks up to 230 MHz at 3.3 V.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed.

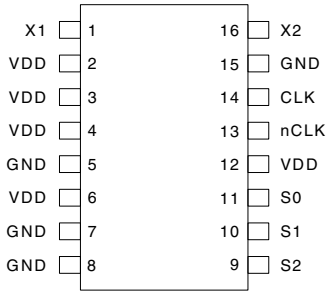
Features

- Fully integrated PLL, no external loop filter required
- Differential 3.3 V LVPECL outputs
- Uses fundamental crystal or clock
  - — Crystal input frequency: 10 to 27MHz
  - — Clock input: 10 to 38MHz (mulitply by 6)
    10 to 31MHz (all other multiply settings)
- Output clocks up to 230 MHz at 3.3 V
- Low phase noise: -122 dBc/Hz at 10 kHz
- Low jitter - 15 ps one sigma typ.
- Powerdown mode lowers power consumption
- Packaged in 16-pin TSSOP, Pb-free
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V
- Commercial temperature range available

Block Diagram



Pin Assignment



16 Pin (173 mil) TSSOP

Multiplier Select Table

S2	S1	S0	Multiplier
0	0	0	x1
0	0	1	x2
0	1	0	x3
0	1	1	x4
1	0	0	x5
1	0	1	x6
1	1	0	x8
1	1	1	x16

0 = connect directly to ground

1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Crystal or clock input. Connect to a fundamental parallel mode crystal or clock input. See electrical tables for input frequenct ranges.
2 - 4	VDD	Power	Connect to +3.3 V.
5	GND	Power	Connect to ground.
6	VDD	Power	Connect to +3.3 V.
7 - 8	GND	Power	Connect to ground.
9	S2	Input	Select pin 2. Internal pull-up resistor.
10	S1	Input	Select pin 1. Internal pull-up resistor.
11	S0	Input	Select pin 0. Internal pull-up resistor.
12	VDD	Power	Connect to +3.3 V.
13	nCLK	Output	Inverted differential clock output.
14	CLK	Output	Differential clock output.
15	GND	Power	Connect to ground.
16	X2	XO	Crystal connection. Connect to a fundamental parallel mode crystal or leave unconnected for clock input. See electrical tables for input frequenct ranges.

External Components

The ICS601-21 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 μF and 0.1 μF should be connected between VDD and GND, as close to the part as possible. A 50 Ω terminating resistor should be used on each clock output. (See termination diagram on page 5). The crystal must be connected as close to the chip as possible. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1 to ground and X2 to ground. In general, the value of these capacitors is given by the following equation, where CL is the crystal load capacitance: Crystal caps (pF) = (CL-5) x 2. So for a crystal with 16 pF load capacitance, two 22 pF caps can be used. For any given board layout, IDT can measure the board capacitance and recommend the exact capacitance value to use.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS601-21. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Commercial version	0 to +70 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	125 °C
Soldering Temperature	260 °C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Electrical Characteristics

VDD=3.3 V ±0.3V, Ambient temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		3.6	V
Input High Voltage	V_{IH}	X1/ICLK pin only	VDD/2+1			V
Input Low Voltage	V_{IL}	X1/ICLK pin only			VDD/2-1	V

DC Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}	Input select pins	2		VDD	V
Input Low Voltage	V_{IL}	Input select pins			0.8	V
Output High Voltage	V_{OH}	Note 1	VDD-1.4		VDD-1.0	V
Output Low Voltage	V_{OL}	Note 1	VDD-2.0		VDD-1.7	V
Output Voltage Swing	V_{swing}	Peak to Peak	0.6		0.95	V
Operating Supply Current	IDD	Note 1, 125 MHz		30	45	mA
Input Capacitance	C_{IN}	Input select pins		5		pF
On Chip Pull-up Resistor	R_{PU}	Input select pins		510		kΩ

Note 1: Outputs terminated with 50Ω to VDD-2V

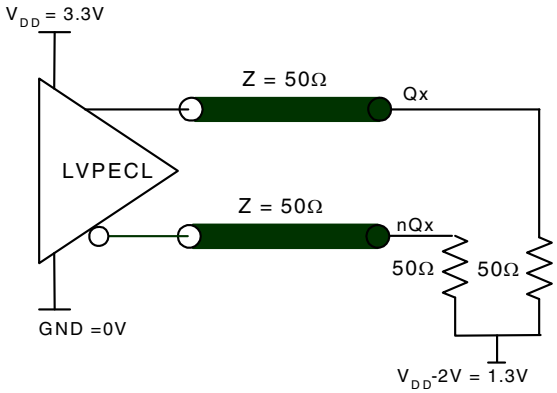
AC Electrical Characteristics

VDD = 3.3 V ±0.3V, Ambient Temperature 0 to +70° C

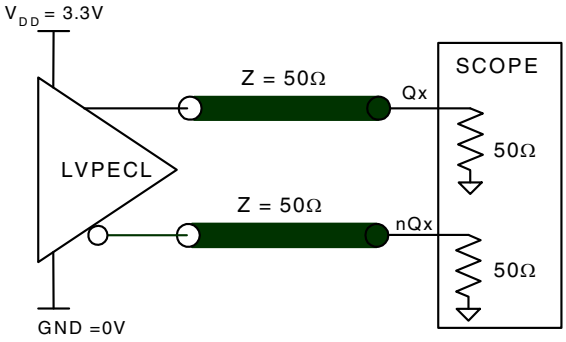
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Crystal Input Frequency	Fin	Note 2	10		27	MHz
Clock Input Frequency	Fin	Note 2, “Multiply by 6” setting	10		38	MHz
		Note 2, excluding “Multiply by 6” setting	10		31	MHz
Output Frequency			10		230	MHz
Output Rise Time	t_{OR}	20% to 80%, no load		600	900	ps
Output Fall Time	t_{OF}	80% to 20%, no load		900	1200	ps
Output Clock Duty Cycle		at VDD/2	45	50	55	%
Maximum Absolute Jitter, short term, 125 MHz		No load		±50	±75	ps
Maximum Jitter, one sigma, 125 MHz (x5)		No load		12	20	ps
Phase Noise, relative to carrier, 125 MHz (x5)		100 Hz offset	-90	-94		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		1 kHz	-116	-120		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		10 kHz offset	-118	-122		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		100 kHz offset	-115	-119		dBc/Hz

Note 2: Input frequency limited by maximum output frequency and multiplication factor (I.e. For 16x, maximum input frequency is 13.75 MHz).

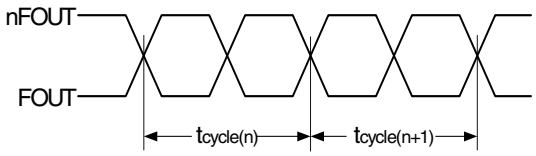
Parameter Measurement Information



3.3V LVPECL Driver Termination



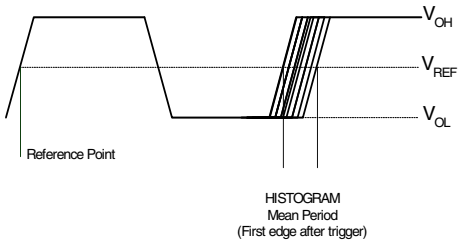
3.3V Output Load AC Test Circuit



$t_{jit(cc)} = t_{cycle(n)} - t_{cycle(n+1)}$

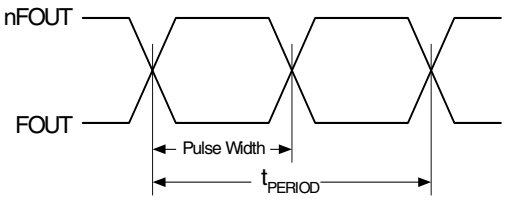
1000 Cycles

CYCLE-TO-CYCLE JITTER



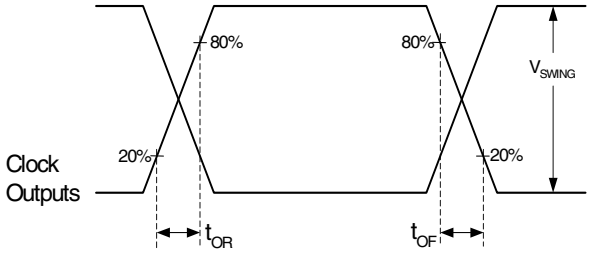
1s contains 68.26% of all measurements
2s contains 95.4% of all measurements
3s contains 99.73% of all measurements
4s contains 99.99366% of all measurements
6s contains (100-1.973x10^{-7})% of all measurements

Period Jitter



$$ODC = \frac{t_{PW}}{t_{PERIOD}}$$

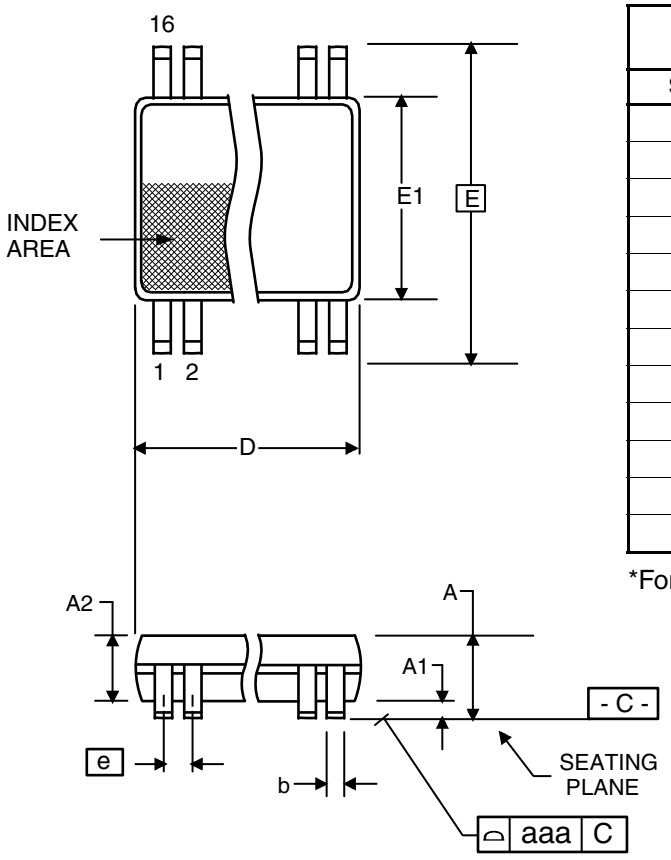
OUTPUT DUTY CYCLE AND t_{PERIOD}

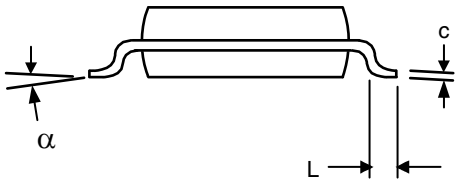


OUTPUT RISE/FALL TIME

Package Outline and Package Dimensions (16-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95





	Millimeters		Inches*	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

*For reference only. Controlling dimensions in mm.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
601G-21LF	601G-21LF	Tubes	16-pin TSSOP	0 to +70° C
601G-21LFT	601G-21LF	Tape and Reel	16-pin TSSOP	0 to +70° C

"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
J	12/14/12	A. Tsui	1. Updated Clock Input and Output frequencies in AC Char table and on front page of DS per characterization report. 2. Removed leaded parts from Orderables table.

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