LC²MOS
Complete, 12-Bit, 100 kHz , Sampling ADC

AD7870A

FEATURES

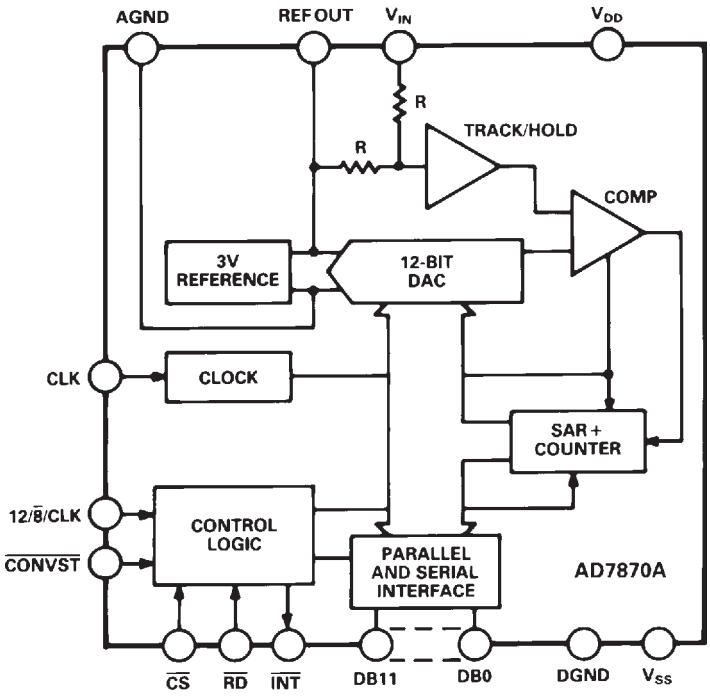
Complete Monolithic 12-Bit ADC with:
- **2 µs Track/Hold Amplifier**
- **8 µs A/D Converter**
- **On-Chip Reference**
- **Laser-Trimmed Clock**
- **Parallel, Byte and Serial Digital Interface**

70 dB SNR at 10 kHz Input Frequency
57 ns Data Access Time
Low Power—60 mW typ

APPLICATIONS

Digital Signal Processing
Speech Recognition and Synthesis
Spectrum Analysis
High Speed Modems
DSP Servo Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7870A is a fast, complete, 12-bit A/D converter. It consists of a track/hold amplifier, 8 µs successive approximation ADC, 3 V buried Zener reference and versatile interface logic. The ADC features a self-contained internal clock that is laser trimmed to guarantee accurate control of conversion time. No external clock timing components are required; the on-chip clock may be overridden by an external clock if required.

AD7870A offers a choice of three data output formats: a single, parallel, 12-bit word, two 8-bit bytes or serial data. Fast bus access times and standard control inputs ensure easy interfacing to modern microprocessors and digital signal processors.

The AD7870A operates from ±5 V power supplies, accepts bipolar input signals of ±3 V and can convert full power signals up to 50 kHz.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the AD7870A is also fully specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7870A is fabricated in Analog Devices' linear compatible CMOS (LC²MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 24-pin, 0.3-inch wide, plastic dual in-line package (DIP).

PRODUCT HIGHLIGHTS

1. Complete 12-bit ADC on a chip.
   The AD7870A is the most complete monolithic ADC available and combines a 12-bit ADC with internal clock, track/hold amplifier and reference on a single chip.
2. Dynamic specifications for DSP users.
   The AD7870A is fully specified and tested for ac parameters, including signal-to-noise ratio, harmonic distortion and intermodulation distortion. Key digital timing parameters are also tested and guaranteed over the full operating temperature range.
3. Fast microprocessor interface.
   Data access times of 57 ns make the AD7870A compatible with modern 8- and 16-bit microprocessors and digital signal processors.

REV. 0

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AD7870A–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V, f_{CLK} is internal, unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	J[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE[2]			
Signal-to-Noise Ratio[3] (SNR)			
@ +25°C	70	dB min	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
T_{MIN} to T_{MAX}	70	dB min	Typically 71.5 dB for 0 < V_{IN} ≤ 50 kHz
Total Harmonic Distortion (THD)	–80	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 100 kHz
			Typically –86 dB for 0 < V_{IN} < 50 kHz
Peak Harmonic or Spurious Noise	–80	dB max	V_{IN} = 10 kHz, f_{SAMPLE} = 100 kHz
			Typically –86 dB for 0 < V_{IN} < 50 kHz
Intermodulation Distortion (IMD)			
Second Order Terms	–80	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Third Order Terms	–80	dB max	fa = 9 kHz, fb = 9.5 kHz, f_{SAMPLE} = 50 kHz
Track/Hold Acquisition Time	2	µs max	
DC ACCURACY			
Resolution	12	Bits	
Minimum Resolution for Which			
No Missing Codes Are Guaranteed	12	Bits	
Integral Nonlinearity	±1/2	LSB typ	
Bipolar Zero Error	±5	LSB max	
Positive Full-Scale Error[4]	±5	LSB max	
Negative Full-Scale Error[4]	±5	LSB max	
ANALOG INPUT			
Input Voltage Range	±3	Volts	
Input Current	±500	µA max	
REFERENCE OUTPUT			
REF OUT @ +25°C	2.99	V min	
	3.01	V max	
REF OUT Tempco	±60	ppm/°C max	
Reference Load Sensitivity (ΔREF OUT/ΔI)	±1	mV max	Reference Load Current Change (0 µA–500 µA)
			Reference Load Should Not Be Change During Conversion
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	µA max	V_{IN} = 0 V to V_{DD}
Input Current (12/$\overline{8}$ CLK Input Only)	±10	µA max	V_{IN} = V_{SS} to V_{DD}
Input Capacitance, C_{IN}[5]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	4.0	V min	I_{SOURCE} = 40 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0			
Floating State Leakage Current	±10	µA max	
Floating-State Output Capacitance[5]	15	pF max	
CONVERSION TIME			
External Clock (f_{CLK} = 2.5 MHz)	7.6/8	µs min/µs max	
Internal Clock	8/10	µs min/µs max	
POWER REQUIREMENTS			
V_{DD}	+5 V	V nom	±5% for Specified Performance
V_{SS}	–5	V non	±5% for Specified Performance
I_{DD}	13	mA max	Typically 8 mA
I_{SS}	6	mA max	Typically 4 mA
Power Dissipation	95	mW max	Typically 60 mW

NOTES
[1]Temperature range is as follow: J Version: 0°C to +70°C.
[2]V_{IN} (pk-pk) = ±3 V.
[3]SNR calculation includes distortion and noise components.
[4]Measured with respect to internal reference and includes bipolar offset error.
[5]Sample tested @ +25°C to ensure compliance.

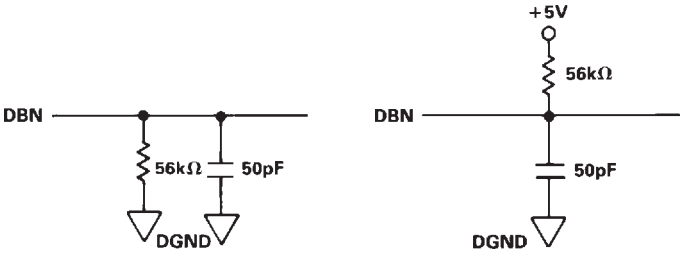
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = –5 V ± 5%, AGND = DGND = 0 V. See Figures 9 and 10.)

Parameter	Limit at T_{MIN}, T_{MAX} (J Version)	Units	Conditions/Comments
t_1	50	ns min	$\overline{CONVST}$ Pulse Width
t_2	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time (Mode 1)
t_3	**60**	ns min	$\overline{RD}$ Pulse Width
t_4	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time (Mode 1)
t_5	70	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_6[3]	57	ns max	Data Access Time after $\overline{RD}$
t_7[4]	5	ns min	Bus Relinquish Time after $\overline{RD}$
	50	ns max	
t_8	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	100	ns min	$\overline{SSTRB}$ to SCLK Falling Edge Setup Time
t_{11}[5]	370	ns min	SCLK Cycle Time
t_{12}[6]	135	ns max	SCLK to Valid Data Delay. C_L = 35 pF
t_{13}	100	ns min	SCLK Rising Edge to $\overline{SSTRB}$
t_{14}	10	ns min	Bus Relinquish Time after SCLK
	100	ns max	

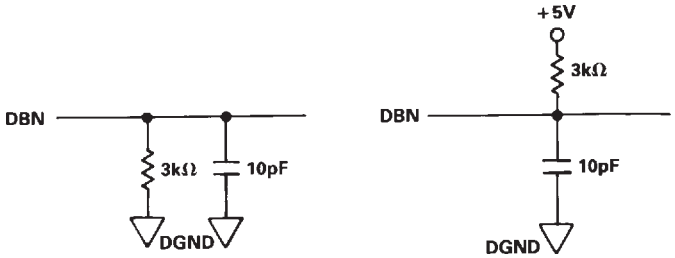
NOTES
[1]Timing specifications in **bold print** are 100% production tested. All other times are sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{SSTRB}$ and a 2 kΩ pull-up on SCLK. The capacitance on all three outputs is 35 pF.
[3]t_6 is measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
[4]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.
[5]SCLK mark/space ratio (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
[6]t_6 SDATA will drive higher capacitive loads but this will add to t_{12} since it increases the external RC time constant (4.7 kΩ‖C_L) and hence the time to reach 2.4 V.

Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{SS} to AGND . . . . . +0.3 V to –7 V
AGND to DGND . . . . . –0.3 V to V_{DD} +0.3 V
V_{IN} to AGND . . . . . –15 V to +15 V
REF OUT to AGND . . . . . 0 V to V_{DD}
Digital Inputs to DGND . . . . . –0.3 V to V_{DD} +0.3 V
Digital Outputs to DGND . . . . . –0.3 V to V_{DD} +0.3 V
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Power Dissipation (Any Package) to +75°C . . . . . 450 mW
Derates above +75°C by . . . . . 10 mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7870A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

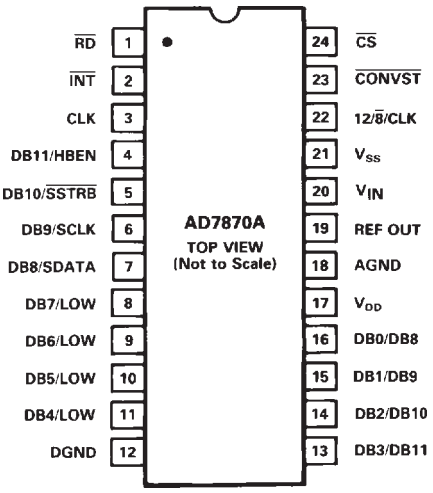
ORDERING GUIDE

Model	Temperature Range	SNR (dBs)	Relative Accuracy (LSB)	Package Option*
AD7870AJN	0°C to +70°C	70 min	±1/2 typ	N-24

*N = Plastic DIP.

PIN CONFIGURATION

DIP



PIN DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	$\overline{RD}$	Read. Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.
2	$\overline{INT}$	Interrupt, Active low logic output indicating converter status. See timing diagrams.
3	CLK	Clock input. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{SS} enables the internal laser-trimmed clock oscillator.
4	DB11/HBEN	Data Bit 11 (MSB)/High Byte Enable. The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input (see below). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table I).
5	DB10/$\overline{SSTRB}$	Data Bit 10/Serial Strobe. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{SSTRB}$ is an active low open-drain output that provides a strobe or framing pulse for serial data. An external 4.7 kΩ pull-up resistor is required on $\overline{SSTRB}$.
6	DB9/SCLK	Data Bit 9/Serial Clock. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If the 12/$\overline{8}$/CLK input is at –5 V, then SCLK runs continuously. If 12/$\overline{8}$/CLK is at 0 V, then SCLK is gated off after serial transmission is complete. SCLK is an open-drain output and requires an external 2 kΩ pull-up resistor.
7	DB8/SDATA	Data Bit 8/Serial Data. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is an open-drain serial data output which is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low. An external 4.7 kΩ pull-up resistor is required on SDATA.
8–11	DB7/LOW–DB4/LOW	Three-state data outputs controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB7–DB4. With 12/$\overline{8}$/CLK low or –5 V, their function is controlled by HBEN (see Table I).
12	DGND	Digital Ground. Ground reference for digital circuitry.
13-16	DB3/DB11–DB0/DB8	Three-state data outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the 12/8/CLK and HBEN inputs. With/12/$\overline{8}$/CLK high, they are always DB3–DB0. With 12/$\overline{8}$/CLK low or –5 V, their function is controlled by HBEN (see Table I).
17	V_{DD}	Positive Supply, +5 V ± 5%.
18	AGND	Analog Ground. Ground reference for track/hold, reference and DAC.
19	REF OUT	Voltage Reference Output. The internal 3 V reference is provided at this pin. The external load capability is 500 μA.
20	V_{IN}	Analog Input. The analog input range is ±3 V.
21	V_{SS}	Negative Supply, –5 V ± 5%.
22	12/$\overline{8}$/CLK	Three Function Input. Defines the data format and serial clock format. With this pin at +5 V, the output data format is 12-bit parallel only. With this pin at 0 V, either byte or serial data is available and SCLK is not continuous. With this pin at –5 V, either byte or serial data is again available but SCLK is now continuous.
23	$\overline{CONVST}$	Convert Start. A high to low transition on this input puts the track/hold into its hold mode and starts conversion. This input is asynchronous to the CLK and independent of $\overline{CS}$ and $\overline{RD}$.
24	$\overline{CS}$	Chip Select. Active low logic input. The device is selected when this input is active.

Table I. Output Data for Byte Interfacing

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11 (MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0 (LSB)

CONVERTER DETAILS

The AD7870A is a complete 12-bit A/D converter, requiring no external components apart from power supply decoupling capacitors. It is comprised of a 12-bit successive approximation ADC based on a fast settling voltage-output DAC, a high speed comparator and SAR, a track/hold amplifier, a 3 V buried Zener reference, a clock oscillator and control logic.

INTERNAL REFERENCE

The AD7870A has an on-chip temperature compensated buried Zener reference that is factory trimmed to 3 V ± 10 mV. Internally it provides both the DAC reference and the dc bias required for bipolar operation. The reference output is available (REF OUT) and capable of providing up to 500 µA to an external load.

The maximum recommended capacitance on REF OUT for normal operation is 50 pF. If the reference is required for use external to the AD7870A, it should be decoupled with a 200 Ω resistor in series with a parallel combination of a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor. These decoupling components are required to remove voltage spikes caused by the AD7870A's internal operation.

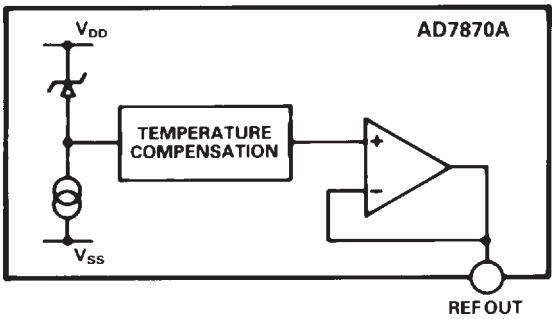


Figure 3. Reference Circuit

TRACK-AND-HOLD AMPLIFIER

The track-and-hold amplifier on the analog input of the AD7870A allows the ADC to accurately convert an input sine wave of 6 V peak-peak amplitude to 12-bit accuracy. The input bandwidth of the track/hold amplifier is much greater than the Nyquist rate of the ADC even when the ADC is operated at its maximum throughput rate. The 0.1 dB cutoff frequency occurs typically at 500 kHz. The track/hold amplifier acquires an input signal to 12-bit accuracy in less than 2 µs. The overall throughput rate is equal to the conversion time plus the track/hold amplifier acquisition time. For a 2.5 MHz input clock the throughput rate is 10 µs max.

The operation of the track/hold is essentially transparent to the user. The track/hold amplifier goes from its tracking mode to its hold mode at the start of conversion. The track-to-hold transition occurs on the falling edge of $\overline{\text{CONVST}}$.

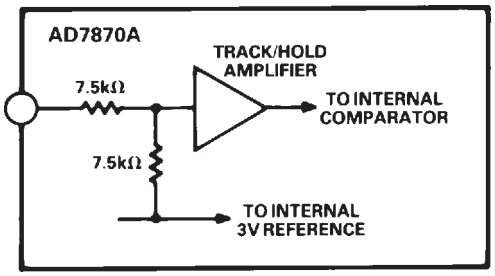


Figure 4. Analog Input

ANALOG INPUT

Figure 4 shows the AD7870A analog input. The analog input range is ±3 V into an input resistance of typically 15 kΩ. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS 3/2 LSBs). The output code is twos complement binary with 1 LSB = FS/4096 = 6 V/4096 = 1.46 mV. The ideal input/output transfer function is shown in Figure 5.

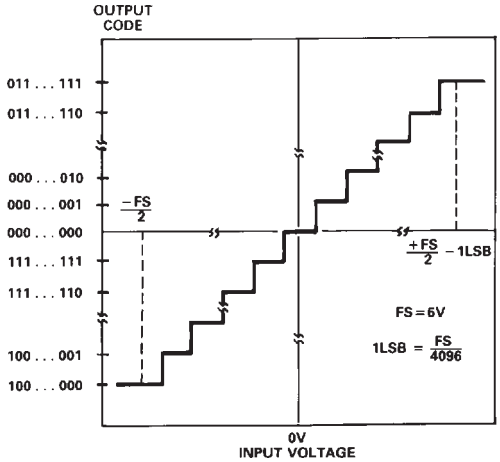


Figure 5. Bipolar Input/Output Transfer Function

BIPOLAR OFFSET AND FULL SCALE ADJUSTMENT

In most digital signal processing (DSP) applications, offset and full-scale errors have little or no effect on system performance. Offset error can always be eliminated in the analog domain by ac coupling. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. Some applications will require that the input signal span the full analog input dynamic range. In such applications, offset and full-scale error will have to be adjusted to zero.

Where adjustment is required, offset error must be adjusted before full-scale error. This is achieved by trimming the offset of the op amp driving the analog input of the AD7870A while the input voltage is 1/2 LSB below ground. The trim procedure is as follows: apply a voltage of 0.73 mV (–1/2 LSB) at V_1 in Figure 6 and adjust the op amp offset voltage until the ADC output code flickers between 1111 1111 1111 and 0000 0000 0000. Gain error can be adjusted at either the first code transition (ADC negative full scale) or the last code transition (ADC positive full scale). The trim procedures for both cases are as follows (see Figure 6).

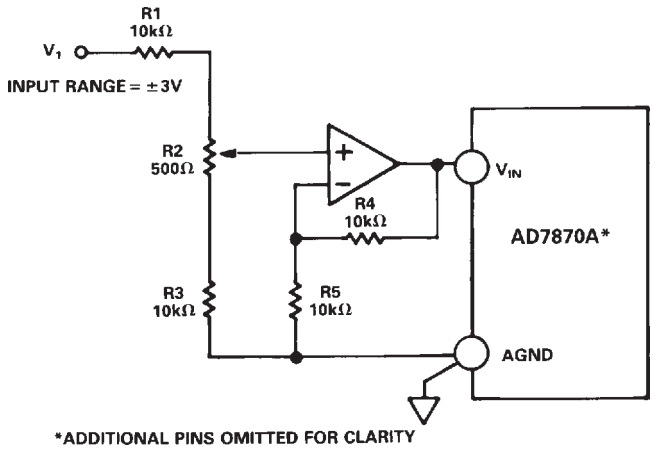


Figure 6. Full-Scale Adjust Circuit

Positive Full-Scale Adjust
Apply a voltage of 2.9978 V (FS/2 – 3/2 LSBs) at V_1. Adjust R2 until the ADC output code flickers between 0111 1111 1110 and 0111 1111 1111.

Negative Full-Scale Adjust
Apply a voltage of –2.9993 V (–FS/2 +1/ 2 LSB) at V_1 and adjust R2 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001.

UNIPOLAR OPERATION

A typical unipolar circuit is shown in Figure 7. The AD7870A REF OUT is used to offset the analog input by 3 V. The analog input range is determined by the ratio of R3 to R4. The minimum range with which the circuit will work is 0 V to +3 V (R3 = 0, R4 = O/C). The resistor values are given in Figure 7 for input ranges of 0 V to +5 V and 0 V to +10 V. R5 and R6 are included for offset and full-scale adjust only and should be omitted if adjustment is not required.

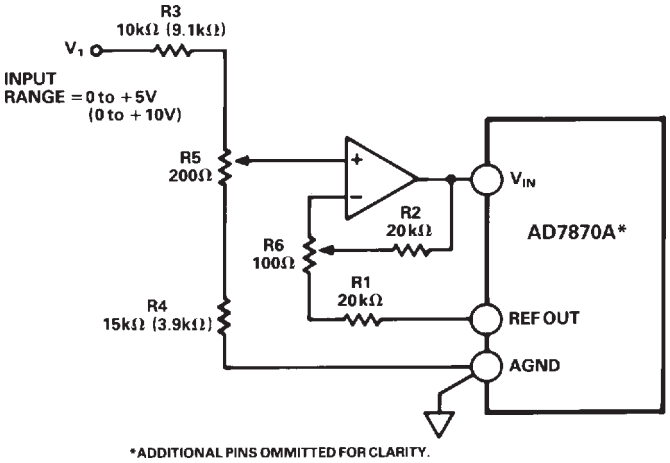


Figure 7. Unipolar Circuit

The ideal input/output transfer function is shown in Figure 8. The output can be converted to natural binary by inverting the MSB.

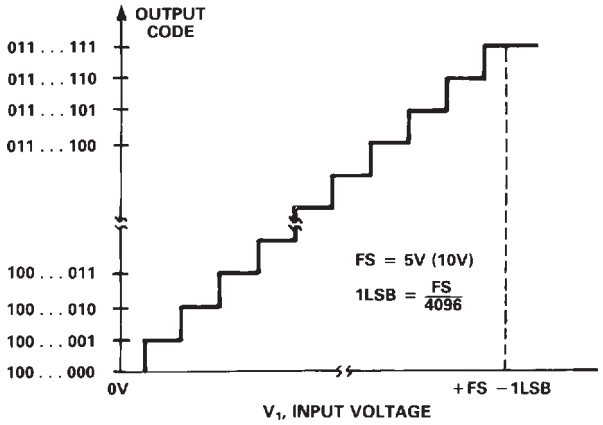


Figure 8. Unipolar Transfer Function

UNIPOLAR OFFSET AND FULL-SCALE ADJUSTMENT

When absolute accuracy is required, offset and full-scale error can be adjusted to zero. Offset must be adjusted before full scale. This is achieved by applying an input voltage of (1/2 LSB) to V_1 and adjust R6 until the ADC output code flickers between 1000 0000 0000 and 1000 0000 0001. For full-scale adjustment, apply an input voltage of (FS–3/2 LSBs) to V_1 and adjust R5 until the output code flickers between 0111 1111 1110 and 0111 11111111.

TIMING AND CONTROL

The AD7870A is capable of one basic interfacing mode. In this mode (Mode 1), the $\overline{\text{CONVST}}$ line is used to start conversion and drive the track/hold into its hold mode. At the end of conversion the track/hold returns to its tracking mode. It is principally intended for digital signal processing and other applications where precise sampling in time is required. In these applications, it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. For these cases, the $\overline{\text{CONVST}}$ line is driven by a timer or some precise clock source.

DATA OUTPUT FORMATS

The AD7870A offers a choice of three data output formats, one serial and two parallel. The parallel data formats are a single, 12-bit parallel word for 16-bit data buses and a two-byte format for 8-bit data buses. The data format is controlled by the 12/$\overline{8}$/CLK input. A logic high on this pin selects the 12-bit parallel output format only. A logic low or –5 V applied to this pin allows the user access to either serial or byte formatted data. Three of the pins previously assigned to the four MSBs in parallel form are now used for serial communications while the fourth pin becomes a control input for the byte-formatted data.

Parallel Output Format

The two parallel formats available on the AD7870A are a 12-bit wide data word and a two-byte data word. In the first, all 12 bits of data are available at the same time on DB11 (MSB) through DB0 (LSB). In the second, two reads are required to access the data. When this data format is selected, the DB11/HBEN pin assumes the HBEN function. HBEN selects which byte of data is to be read from the AD7870A. When HBEN is low, the lower eight bits of data are placed on the data bus during a read operation; with HBEN high, the upper four bits of the 12-bit word are placed on the data bus. These four bits are right justified and thereby occupy the lower nibble of data while the upper nibble contains four zeros.

Serial Output Format

Serial data is available on the AD7870A when the 12/$\overline{8}$/CLK input is at 0 V or –5 V and in this case the DB10/$\overline{\text{SSTRB}}$, DB9/SCLK and DB8/SDATA pins assume their serial functions. Serial data is available during conversion with a word length of 16 bits; four leading zeros, followed by the 12-bit conversion result starting with the MSB. The data is synchronized to the serial clock output (SCLK) and framed by the serial strobe ($\overline{\text{SSTRB}}$). Data is clocked out on a low to high transition of the serial clock and is valid on the falling edge of this clock while the $\overline{\text{SSTRB}}$ output is low. $\overline{\text{SSTRB}}$ goes low within three clock cycles after $\overline{\text{CONVST}}$, and the first serial data bit (the first leading zero) is valid on the first falling edge of SCLK after $\overline{\text{SSTRB}}$ goes low. All three serial lines are open-drain outputs and require external pull-up resistors.

The serial clock out is derived from the ADC clock source, which may be internal or external. Normally, SCLK is required during the serial transmission only. In these cases, it can be shut down at the end of conversion to allow multiple ADCs to share a common serial bus. However, some serial systems (e.g., TMS32020) require a serial clock that runs continuously. Both options are available on the AD7870A using the 12/8/CLK input. With this input at –5 V, the serial clock (SCLK) runs continuously; when 12/$\overline{8}$/CLK is at 0 V, SCLK is turned off at the end of transmission.

MODE 1 INTERFACE

Conversion is initiated by a low going pulse on the $\overline{\text{CONVST}}$ input. The falling edge of this $\overline{\text{CONVST}}$ pulse starts conversion and drives the track/hold amplifier into its hold mode. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. This $\overline{\text{INT}}$ line can be used to interrupt the microprocessor. A read operation to the AD7870A accesses the data and the $\overline{\text{INT}}$ line is reset high on the falling edge of $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Trying to exercise $\overline{\text{CS}}$ and RD during a conversion can cause errors to the conversion in progress. In applications where precise sampling is not critical, the CONVST pulse can be generated from a microprocessor $\overline{\text{WR}}$ line OR-gated with a decoded address.

Figure 9 shows the timing diagram for a 12-bit parallel data output format (12/$\overline{8}$/CLK = +5 V). A read to the AD7870A at the end of conversion accesses all 12 bits of data at the same time. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ control the output three-state drivers. If $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are high, the databus is three-state. If $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are hardwired low, data from the previous conversion will remain on the databus. This data will be updated approximately $t_{CONVERT}$ after the falling edge of $\overline{\text{CONVST}}$. With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ hardwired low, the INT line will remain low. Serial data is not available for this data output format.

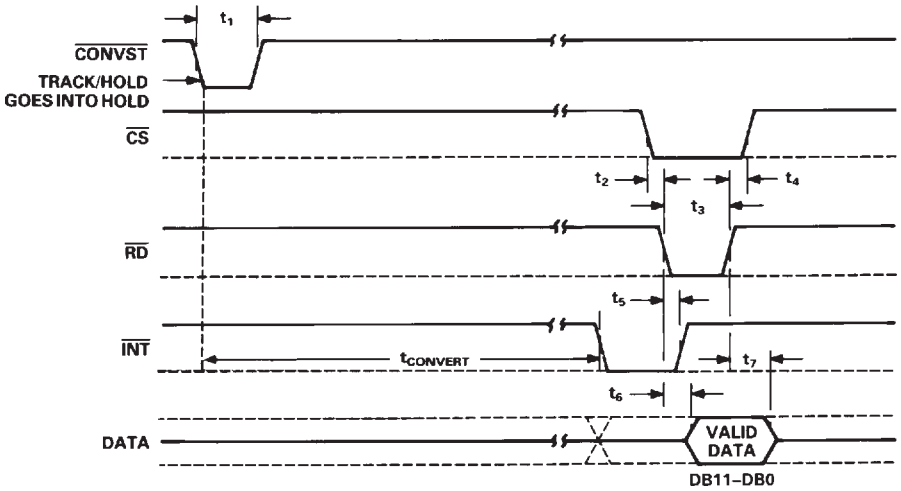


Figure 9. Mode 1 Timing Diagram, 12-Bit Parallel Read

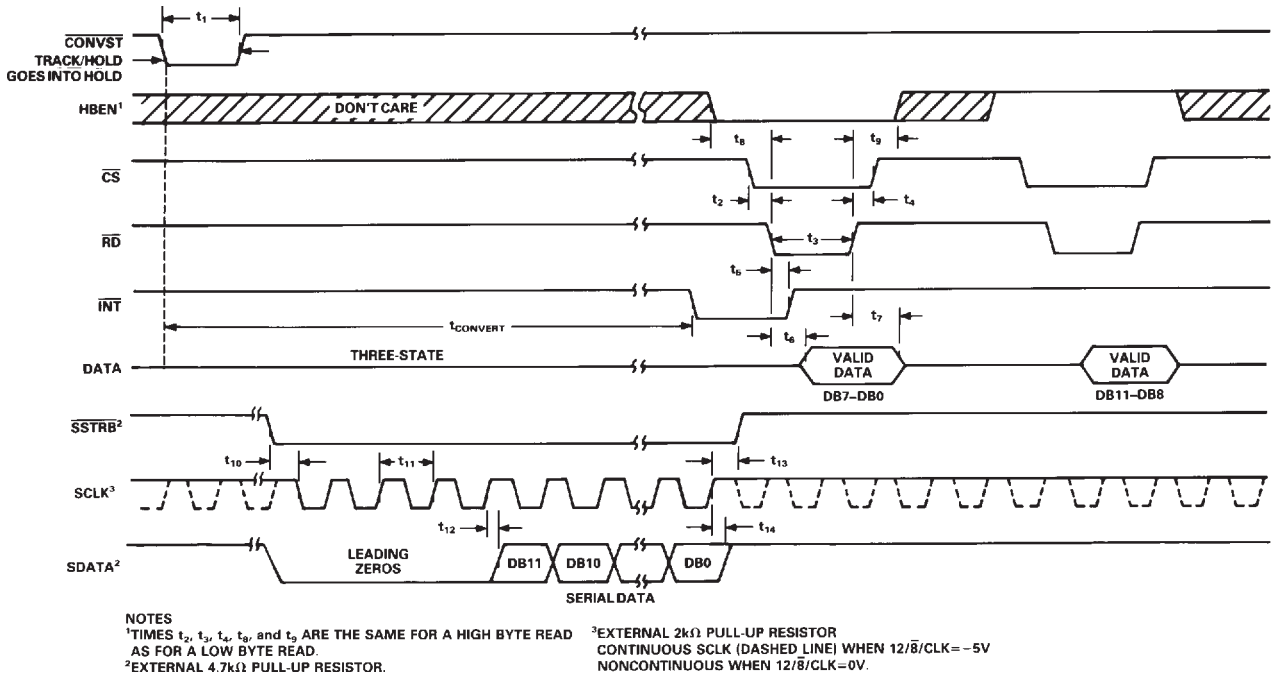


Figure 10. Mode 1 Timing Diagram, Byte or Serial Read

The timing diagram for byte and serial data is shown in Figure 10. $\overline{INT}$ goes low at the end of conversion and is reset high by the first falling edge of $\overline{CS}$ and $\overline{RD}$. This first read at the end of conversion can either access the low byte or high byte of data depending on the status of $\overline{HBEN}$ (Figure 10 shows low byte only for example). The diagram shows both a noncontinuously and a continuously running clock (dashed line).

AD7870A DYNAMIC SPECIFICATIONS

The AD7870A is specified and 100% tested for dynamic performance specifications. These ac specifications are required for signal processing applications such as speech recognition, spectrum analysis and high speed modems. These applications require information on the ADC's effect on the spectral content of the input signal. Hence, the parameters for which the AD7870A is specified include SNR, harmonic distortion, intermodulation distortion and peak harmonics. These terms are discussed in more detail in the following sections.

Signal-to-Noise Ratio (SNR)

SNR is the measured signal-to-noise ratio at the output of the ADC. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency (FS/2) excluding dc. SNR is dependent upon the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise ratio for a sine wave input is given by

$$SNR = (6.02N + 1.76)\ dB \qquad (1)$$

where N is the number of bits. Thus for an ideal 12-bit converter, SNR = 74 dB.

The output spectrum from the ADC is evaluated by applying a sine-wave signal of very low distortion to the V_{IN} input which is sampled at a 100 kHz sampling rate. A Fast Fourier Transform (FFT) plot is generated from which the SNR data can be obtained. Figure 11 shows a typical 2048 point FFT plot of the AD7870AJN with an input signal of 25 kHz and a sampling frequency of 100 kHz. The SNR obtained from this graph is 72.6 dB. It should be noted that the harmonics are taken into account when calculating the SNR.

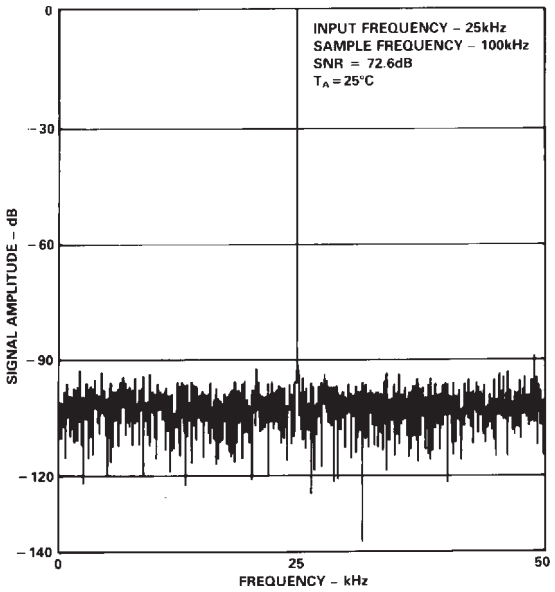


Figure 11. FFT Plot

Effective Number of Bits

The formula given in (1) relates the SNR to the number of bits. Rewriting the formula, as in (2), it is possible to obtain a measure of performance expressed in effective number of bits (N).

$$N = \frac{SNR - 1.76}{6.02} \qquad (2)$$

The effective number of bits for a device can be calculated directly from its measured SNR.

Figure 12 shows a typical plot of effective number of bits versus frequency for an AD7870AJN, with a sampling frequency of 100 kHz. The effective number of bits typically falls between 11.7 and 11.85 corresponding to SNR figures of 72.2 dB and 73.1 dB.

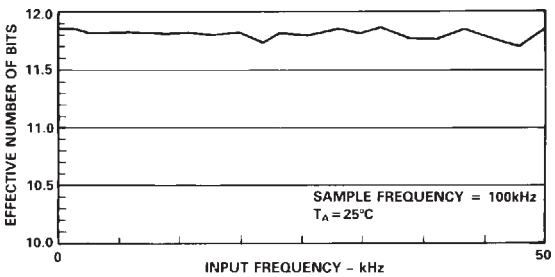


Figure 12. Effective Number of Bits vs. Frequency

Harmonic Distortion

Harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. For the AD7870A, total harmonic distortion (THD) is defined as

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonic. The THD is also derived from the FFT plot of the ADC output spectrum.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa + nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). Using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs. In this case, the input consists of two, equal amplitude, low distortion sine waves. Figure 13 shows a typical IMD plot for the AD7870A.

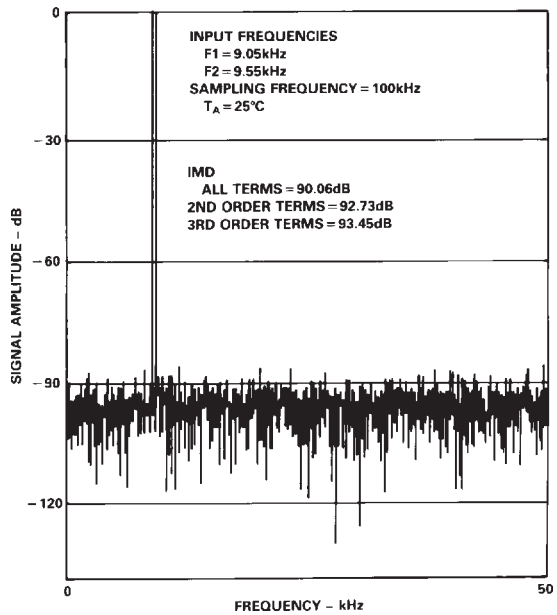


Figure 13. IMD Plot

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to FS/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification will be determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor the peak will be a noise peak.

AC Linearity Plot

When a sine wave of specified frequency is applied to the V_{IN} input of the AD7870A, and several million samples are taken, a histogram showing the frequency of occurrence of each of the 4096 ADC codes can be generated. From this histogram data it is possible to generate an ac integral linearity plot as shown in Figure 14. This shows very good integral linearity performance from the AD7870A at an input frequency of 25 kHz. The absence of large spikes in the plot shows good differential linearity. Simplified versions of the formulae used are outlined below.

$$INL(i) = \left[\frac{V(i) - V(o)}{V(fs) - V(o)} \times 4096 \right] - i$$

where $INL(i)$ is the integral linearity at code i. $V(fs)$ and $V(o)$ are the estimated full-scale and offset transitions and $V(i)$ is the estimated transition for the ith code.

V(i) the estimated code transition point is derived as follows:

$$V(i) = -A \times Cos \frac{\pi \times cum(i)}{N}$$

where A is the peak signal amplitude,
N is the number of histogram samples
and $cum(i) = \sum_{n=0}^{i} V(n)$ occurrences

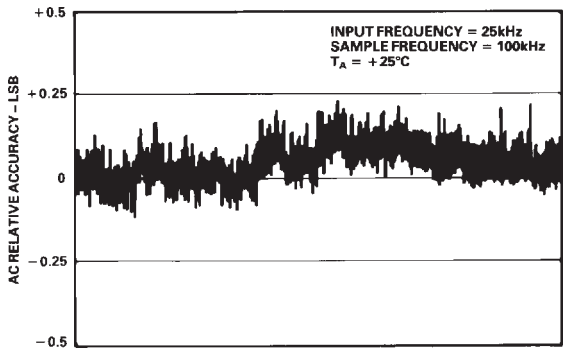


Figure 14. AC INL Plot

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the overall circuit design itself in achieving high speed A/D performance. The AD7870A is required to make bit decisions on an LSB size of 1.465 mV. Thus, the designer has to be conscious of noise both in the ADC itself and in the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors that influence any ADC, and a proper PCB layout that minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at the AD7870A AGND pin or as close as possible to the AD7870A. Connect all other grounds and the AD7870A DGND to this single analog ground point. Do not connect any other digital grounds to this analog ground point.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths and also guards the analog circuitry from digital noise.

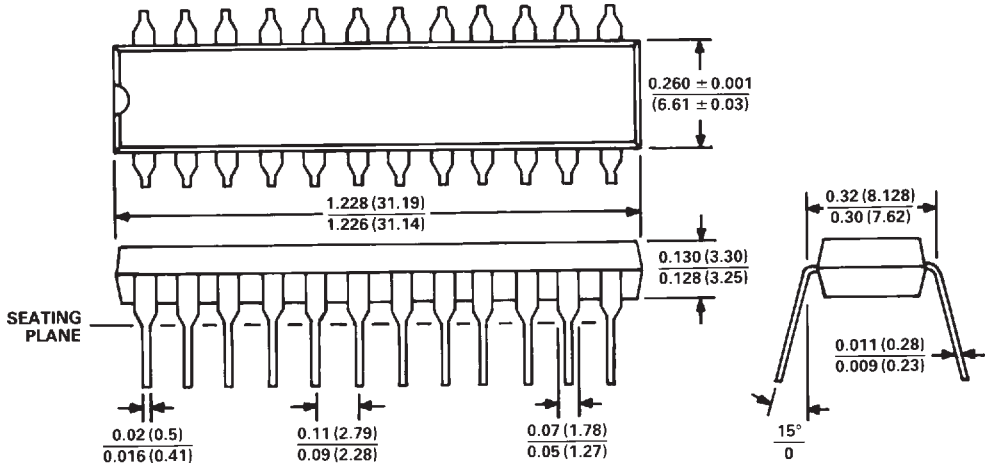
NOISE

Keep the input signal leads to V_{IN} and signal return leads from AGND as short as possible to minimize input noise coupling. In applications where this is not possible, use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Pin Plastic DIP (N-24)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

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