The ISL5857 is a 12-bit, 260+MSPS (Mega Samples Per Second), CMOS, high speed, low power, D/A (digital-to-analog) converter designed specifically for use in high performance communication systems such as base transceiver stations utilizing 2.5 G or 3 G cellular protocols.

This device complements the ISL5x57 family of high speed converters, which include 10, 12, and 14-bit devices.

## Applications

- Cellular Infrastructure - single or multicarrier: IS-136, IS-95, GSM, EDGE, CDMA2000, WCDMA, TDS-CDMA
- BWA infrastructure
- Medical/test instrumentation
- Wireless communication systems
- High resolution imaging systems
- Arbitrary waveform generators


## Features

- Low power. . . . . . . 103mW with 20mA output at 130MSPS
- Adjustable full scale output current. . . . . . . . . 2mA to 20 mA
- +3.3V power supply
- 3V LVCMOS compatible inputs
- Excellent spurious free dynamic range ( 73 dBc to Nyquist, $\mathrm{f}_{\mathrm{S}}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=10 \mathrm{MHz}$ )
- UMTS adjacent channel power $=70 \mathrm{~dB}$ at 19.2 MHz
- EDGE/GSM SFDR $=90 \mathrm{dBc}$ at 11 MHz in 20 MHz window
- Pin compatible, 3.3 V , lower power replacement for the AD9752 and HI5860
- Pb-free (RoHS compliant)


FIGURE 1. TYPICAL APPLICATIONS CIRCUIT

Functional Block Diagram


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

## Pin Configuration

|  |  |  |
| :---: | :---: | :---: |
| D11 (MSB) 1 | 28 | CLK |
| D10 2 | 27 | DV ${ }_{\text {D }}$ |
| D9 3 | 26 | DCOM |
| D8 4 | 25 | NC |
| D7 5 | 24 | $A V_{\text {D }}$ |
| D6 6 | 23 | COMP |
| D5 7 | 22 | IOUTA |
| D4 8 | 21 | IOUTB |
| D3 9 | 20 | ACOM |
| D2 10 | 19 | NC |
| D1 11 | 18 | FSADJ |
| D0 (LSB) 12 | 17 | REFIO |
| DCOM 13 | 16 | REFLO |
| DCOM 14 | 15 | SLEEP |

## Pin Descriptions

| PIN NO. | PIN NAME | DESCRIPTION |
| :---: | :---: | :---: |
| 1 through 12 | D11 (MSB) Through DO (LSB) | Digital data Bit 11, (Most Significant Bit) through Digital Data Bit 0, (Least Significant Bit). |
| 15 | SLEEP | Control pin for power-down mode. Sleep Mode is active high; Connect to ground for Normal Mode. Sleep pin has internal $20 \mu \mathrm{~A}$ active pull-down current. |
| 16 | REFLO | Connect to analog ground to enable internal 1.2V reference or connect to $\mathrm{AV}_{\mathrm{DD}}$ to disable internal reference. |
| 17 | REFIO | Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use $0.1 \mu \mathrm{~F}$ capacitor to ground when internal reference is enabled. |
| 18 | FSADJ | Full scale current adjust. Use a resistor to ground to adjust full scale output current. Full scale output current $=32$ $x V_{\text {FSAD }} / R_{\text {SET }}$. |
| 19, 25 | NC | No Connect. These should be grounded, but can be left disconnected. |
| 21 | IOUTB | The complementary current output of the device. Full scale output current is achieved when all input bits are set to binary 0. |
| 22 | IOUTA | Current output of the device. Full scale output current is achieved when all input bits are set to binary 1. |
| 23 | COMP | Connect $0.1 \mu \mathrm{~F}$ capacitor to ACOM. |
| 24 | AV DD | Analog supply (+3.0V to +3.6 V ). |
| 20 | ACOM | Connect to analog ground. |
| 26, 13, 14 | DCOM | Connect to digital ground. |
| 27 | DV ${ }_{\text {DD }}$ | Digital supply ( +3.0 V to +3.6 V ). |
| 28 | CLK | Clock input. |

## Ordering Information

| PART NUMBER <br> (Notes 1, 2) | PART <br> MARKING | TEMP RANGE <br> $\left({ }^{\circ} \mathrm{C}\right)$ | PACKAGE <br> (RoHS Compliant) | PKG. <br> DWG. \# | CLOCK <br> SPEED |
| :--- | :---: | :---: | :---: | :---: | :---: |
| ISL5857IBZ No longer available <br> or supported, recommended <br> replacement part: ISL5857IAZ | ISL5857IBZ | -40 to +85 | 28 Ld SOIC | M28.3 |  |
| ISL5857IAZ |  |  | 260 MHz |  |  |

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and $100 \%$ matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb -free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), please see product information page for ISL5857. For more information on MSL, please see tech brief TB363.

## Absolute Maximum Ratings

| Digital Supply Voltage DV ${ }_{\text {DD }}$ to DCOM | +3.6V |
| :---: | :---: |
| Analog Supply Voltage AV ${ }_{\text {DD }}$ to ACOM. | +3.6V |
| Grounds, ACOM TO DCOM . | -0.3V to +0.3V |
| Digital Input Voltages (D9-DO, CLK, SLEEP) | DV $\mathrm{DD}^{+0.3 V}$ |
| Reference Input Voltage Range | $\mathrm{AV}_{\mathrm{DD}}+0.3 \mathrm{~V}$ |
| Analog Output Current (lout) | 24mA |

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{\text {JA }}\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ |
| :---: | :---: |
| SOIC Package . | 75 |
| TSSOP Package | 110 |
| Maximum Junction Temperature | $.150^{\circ} \mathrm{C}$ |
| Maximum Storage Temperature Range | ${ }^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$ |
| Pb-free Reflow Profile | see TB493 |

## Operating Conditions

Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$
CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:
3. $\theta_{\mathrm{JA}}$ is measured with the component mounted on an evaluation PC board in free air. See Tech Brief TB379.

Electrical Specifications $A V_{D D}=D V_{D D}=+3.3 \mathrm{~V}, V_{R E F}=$ Internal $1.2 \mathrm{~V}, 10 U T F S=20 \mathrm{~mA}, T_{A}=+25^{\circ} \mathrm{C}$ for all typical values. Boldface limits apply across the operating temperature range, $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.

| PARAMETER | TEST CONDITIONS | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \mathrm{TO} 85^{\circ} \mathrm{C}$ |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX |  |
| SYSTEM PERFORMANCE |  |  |  |  |  |
| Resolution |  | 12 | - | - | Bits |
| Integral Linearity Error, INL | "Best fit" straight line (Note 10) | -1.25 | $\pm 0.5$ | +1.25 | LSB |
| Differential Linearity Error, DNL | (Note 10) | -1 | $\pm 0.5$ | +1 | LSB |
| Offset Error, Ios | IOUTA (Note 10) | -0.006 |  | +0.006 | \% FSR |
| Offset Drift Coefficient | (Note 10) | - | 0.1 | - | $\begin{gathered} \mathrm{ppm} \\ \text { FSR } /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Full Scale Gain Error, FSE | With external reference (Notes 4, 10) | -3 | $\pm 0.5$ | +3 | \% FSR |
|  | With internal reference (Notes 4, 10) | -3 | $\pm 0.5$ | +3 | \% FSR |
| Full Scale Gain Drift | With external reference (Note 10) | - | $\pm 50$ | - | $\begin{gathered} \mathrm{ppm} \\ \text { FSR } /{ }^{\circ} \mathrm{C} \end{gathered}$ |
|  | With internal reference (Note 10) | - | $\pm 100$ | - | $\begin{gathered} \text { ppm } \\ \text { FSR } /{ }^{\circ} \mathrm{C} \end{gathered}$ |
| Full Scale Output Current, ${ }_{\text {I }}$ S |  | 2 | - | 20 | mA |
| Output Voltage Compliance Range | (Note 5) | -1.0 | - | 1.25 | V |
| DYNAMIC CHARACTERISTICS |  |  |  |  |  |
| Maximum Clock Rate, feLK |  | 260 | 300 | - | MHz |
| Output Rise Time | Full scale step | - | 1.5 | - | ns |
| Output Fall Time | Full scale step | - | 1.5 | - | ns |
| Output Capacitance |  | - | 10 | - | pF |
| Output Noise | IOUTFS $=20 \mathrm{~mA}$ | - | 50 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |
|  | IOUTFS $=2 \mathrm{~mA}$ | - | 30 | - | $\mathrm{pA} / \sqrt{\mathrm{Hz}}$ |

AC CHARACTERISTICS (Using Figure 15 with $\mathrm{R}_{\text {DIFF }}=50 \Omega$ and $\mathrm{R}_{\text {LOAD }}=50 \Omega$, Full scale output $=-2.5 \mathrm{dBm}$ )
Spurious Free Dynamic Range, SFDR Within a Window

| $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=80.8 \mathrm{MHz}, 30 \mathrm{MHz} \mathrm{span}(\underline{\text { Notes 6 }}$, 10) | - | 73 | - | dBc |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=40.4 \mathrm{MHz}, 30 \mathrm{MHz}$ span $($ Notes 6, 10) | - | 80 | - | dBc |
| $\mathrm{f}_{\mathrm{CLK}}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=20.2 \mathrm{MHz}, 20 \mathrm{MHz}$ span $(\underline{\text { Notes 6 }}$, 10) | - | 85 | - | dBc |

Electrical Specifications $\quad A V_{D D}=D V_{D D}=+3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}=\operatorname{Interna1} 1.2 \mathrm{~V}, 10 \mathrm{OTFS}=20 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ for all typical values. Boldface limits apply across the operating temperature range, $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. (Continued)

| PARAMETER | TEST CONDITIONS | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ T0 $85^{\circ} \mathrm{C}$ |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX |  |
| Spurious Free Dynamic Range, SFDR to Nyquist (fcLK/2) | $\mathrm{f}_{\text {CLK }}=260 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=80.8 \mathrm{MHz}($ Notes 6, 10) | - | 47 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=260 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=40.4 \mathrm{MHz}(\underline{\text { Notes 6 6, 10 }}$ ) | - | 60 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=260 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=20.2 \mathrm{MHz}($ Notes 6, 10) | - | 62 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=80.8 \mathrm{MHz}$ ( (Notes 6, 10) | - | 51 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=210 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=40.4 \mathrm{MHz}$ ( (Notes 6, 10, 12) | - | 60 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=200 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=20.2 \mathrm{MHz}, \mathrm{T}=25^{\circ} \mathrm{C}$ ( Notes 6, 10) | 60 | 62 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=200 \mathrm{MSPS}, \mathrm{fout}^{\text {a }} \mathbf{2 0 . 2} \mathbf{M H z}, \mathrm{T}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ( ( otes 6, 10) | 58 | - | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=50.5 \mathrm{MHz}($ Notes 6, 10) | - | 57 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=40.4 \mathrm{MHz}(\underline{\text { Notes 6 }}$, 10) | - | 62 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=20.2 \mathrm{MHz}($ Notes 6, 10) | - | 69 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=10.1 \mathrm{MHz}$ ( Notes 6, 10) | - | 73 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=5.05 \mathrm{MHz}, \mathrm{T}=25^{\circ} \mathrm{C}$ ( Notes 6, 10) | 70 | 77 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=5.05 \mathrm{MHz}, \mathrm{T}=-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$ ( Notes 6, 10) | 68 | - | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=100 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=40.4 \mathrm{MHz}($ Notes 6, 10) | - | 60 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=30.3 \mathrm{MHz}($ Notes 6, 10) | - | 63 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=20.2 \mathrm{MHz}($ Notes 6, 10) | - | 69 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=10.1 \mathrm{MHz}$ (Notes 6, 10, 12) | - | 70 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=80 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=5.05 \mathrm{MHz}(\underline{\text { Notes 6, }}$, 10) | - | 76 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=50 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=20.2 \mathrm{MHz}($ Notes 6, 10) | - | 68 | - | dBc |
|  | $\mathrm{f}_{\text {CLK }}=50 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=10.1 \mathrm{MHz}($ Notes 6, 10) | - | 73 | - | dBc |
|  | $\mathrm{f}_{\mathrm{CLK}}=50 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=5.05 \mathrm{MHz}($ Notes 6, 10) | - | 77 | - | dBc |
| Spurious Free Dynamic Range, SFDR in a Window with Eight Tones | $\mathrm{f}_{\mathrm{CLK}}=210 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=28.3 \mathrm{MHz}$ to $45.2 \mathrm{MHz}, 2.1 \mathrm{MHz}$ spacing, 50 MHz Span (Notes 6, 10, 12) | - | 65 | - | dBc |
|  | $\mathrm{f}_{\mathrm{CLK}}=130 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=17.5 \mathrm{MHz}$ to 27.9 MHz , 1.3MHz spacing, 35 MHz Span (Notes 6, 10) | - | 68 | - | dBc |
|  | $\mathrm{f}_{\mathrm{CLK}}=80 \mathrm{MSPS}, \mathrm{f}_{\text {Out }}=10.8 \mathrm{MHz}$ to $17.2 \mathrm{MHz}, 811 \mathrm{kHz}$ spacing, 15 MHz Span (Notes 6, 10) | - | 75 | - | dBc |
|  | $\mathrm{f}_{\mathrm{CLK}}=50 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=6.7 \mathrm{MHz}$ to $10.8 \mathrm{MHz}, 490 \mathrm{kHz}$ spacing, 10 MHz Span (Notes 6, 10) | - | 77 | - | dBc |
| Spurious Free Dynamic Range, SFDR in a Window with EDGE or GSM | $\mathrm{f}_{\mathrm{CLK}}=78 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=11 \mathrm{MHz}$, in a 20 MHz window, $\mathrm{RBW}=30 \mathrm{kHz}$ (Notes 6, 10, 12) | - | 90 | - | dBc |
| Adjacent Channel Power Ratio, ACPR with UMTS | $\mathrm{f}_{\text {CLK }}=76.8 \mathrm{MSPS}, \mathrm{f}_{\text {OUT }}=19.2 \mathrm{MHz}, \mathrm{RBW}=30 \mathrm{kHz}$ ( (Notes 6, 10, 12) | - | 70 | - | dB |
| VOLTAGE REFERENCE |  |  |  |  |  |
| Internal Reference Voltage, $\mathrm{V}_{\text {FSADJ }}$ | Pin 18 voltage with internal reference | 1.2 | 1.23 | 1.3 | V |
| Internal Reference Voltage Drift |  | - | $\pm 40$ | - | ppm/ ${ }^{\circ} \mathrm{C}$ |
| Internal Reference Output Current Sink/Source Capability | Reference is not intended to be externally loaded | - | 0 | - | $\mu \mathrm{A}$ |
| Reference Input Impedance |  | - | 1 | - | M $\Omega$ |
| Reference Input Multiplying Bandwidth | (Note 10) | - | 1.0 | - | MHz |

Electrical Specifications $\quad A V_{D D}=D V_{D D}=+3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{REF}}=$ Internal $1.2 \mathrm{~V}, I O U T F S=20 \mathrm{~mA}, \mathrm{~T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ for all typical values. Boldface limits apply across the operating temperature range, $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$. (Continued)

| PARAMETER | TEST CONDITIONS | $\mathrm{T}_{\mathrm{A}}=-40^{\circ} \mathrm{C} \mathrm{TO} 85^{\circ} \mathrm{C}$ |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX |  |
| DIGITAL INPUTS D11-D0, CLK |  |  |  |  |  |
| Input Logic High Voltage with 3.3V Supply, $\mathrm{V}_{\mathrm{IH}}$ | (Note 5) | 2.3 | 3.3 | - | V |
| Input Logic Low Voltage with 3.3V Supply, VIL | (Note 5) | - | 0 | 1.0 | V |
| Sleep Input Current, $\mathrm{I}_{\mathbf{I H}}$ |  | -25 | - | +25 | $\mu \mathrm{A}$ |
| Input Logic Current, $\mathrm{I}_{\text {IH, }}$, $\mathrm{I}_{\text {IL }}$ |  | -20 | - | +20 | $\mu \mathrm{A}$ |
| Clock Input Current, $\mathrm{I}_{\mathbf{I H},} \mathrm{I}_{\text {IL }}$ |  | -10 | - | +10 | $\mu \mathrm{A}$ |
| Digital Input Capacitance, $\mathrm{C}_{\text {IN }}$ |  | - | 5 | - | pF |
| TIMING CHARACTERISTICS |  |  |  |  |  |
| Data Setup Time, $\mathrm{t}_{\text {SU }}$ | See Figure 17 | - | 1.5 | - | ns |
| Data Hold Time, $\mathrm{t}_{\text {HLD }}$ | See Figure 17 | - | 1.5 | - | ns |
| Propagation Delay Time, $\mathrm{t}_{\text {PD }}$ | See Figure 17 | - | 1 | - | Clock <br> Period |
| CLK Pulse Width, ${ }_{\text {PW1 }}$, t $_{\text {PW2 }}$ | See Figure 17 (Note 5) | 0.9 | - | - | ns |
| POWER SUPPLY CHARACTERISTICS |  |  |  |  |  |
| AV DD Power Supply | (Note 11) | 2.7 | 3.3 | 3.6 | V |
| DV ${ }_{\text {DD }}$ Power Supply | (Note 11) | 2.7 | 3.3 | 3.6 | V |
| Analog Supply Current ( ${ }_{\text {AVDD }}$ ) | $3.3 \mathrm{~V}, 10 \mathrm{~T}$ 仿 $=20 \mathrm{~mA}$ | - | 27.5 | 28.5 | mA |
|  | 3.3 V, IOUTFS $=2 \mathrm{~mA}$ | - | 10 | - | mA |
| Digital Supply Current (IDVDD) | 3.3V (Note 7) | - | 3.7 | 5 | mA |
|  | 3.3 V (Note 8) | - | 6.5 | 8 | mA |
| Supply Current (lavid ${ }^{\text {d }}$ ) Sleep Mode | 3.3V, IOUTFS = Don't Care | - | 1.5 | - | mA |
| Power Dissipation | 3.3 V, IOUTFS $=20 \mathrm{~mA}$ ( (ote 7) | - | 103 | 111 | mW |
|  | 3.3 V, IOUTFS $=20 \mathrm{~mA}$ ( (10te 8) | - | 110 | 120 | mW |
|  | 3.3 V, IOUTFS $=20 \mathrm{~mA}$ ( Note 9) | - | 157 | - | mW |
|  | 3.3 V, IOUTFS $=2 \mathrm{~mA}$ ( Note 7) | - | 45 | - | mW |
| Power Supply Rejection | Single supply (Note 10) | -0.125 | - | +0.125 | \%FSR/V |

## NOTES:

4. Gain Error measured as the error in the ratio between the full scale output current and the current through RSET (typically $625 \mu \mathrm{~A})$. Ideally the ratio should be 32.
5. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
6. Spectral measurements made with differential transformer coupled output and no external filtering. For multitone testing, the same pattern was used at different clock rates, producing different output frequencies but at the same ratio to the clock rate.
7. Measured with the clock at 130MSPS and the output frequency at 5 MHz .
8. Measured with the clock at 200 MSPS and the output frequency at 20 MHz .
9. Measured with the clock at 260 MSPS and the output frequency at 40 MHz .
10. See "Definition of Specifications" on page 9.
11. Recommended operation is from 3.0 V to 3.6 V . Operation below 3.0 V is possible with some degradation in spectral performance. Reduction in analog output current may be necessary to maintain spectral performance.
12. See "Typical Performance Plots" on page 7.

## Typical Performance Plots

$\left(+3.3 V\right.$ Supply, Using Figure 15 with $R_{\text {DIFF }}=100 \Omega$ and $\left.R_{\text {LOAD }}=50 \Omega\right)$


FIGURE 3. EDGE AT 11MHz, 78MSPS CLOCK $(91+d B c$ AT $\Delta f=+6 \mathrm{MHz})$


FIGURE 5. GSM AT 11MHz, 78MSPS CLOCK
$(90+d B c$ AT $\Delta f=+6 \mathrm{MHz}, 3 \mathrm{~dB}$ PAD)


FIGURE 7. FOUR EDGE CARRIERS AT 12.4 to $15.6 \mathrm{MHz}, 800 \mathrm{kHz}$ SPACING, 78MSPS (71dBc - 20MHz WINDOW)


FIGURE 4. EDGE AT 11MHz, 78MSPS CLOCK (75dBc -NYQUIST, 6dB PAD)


FIGURE 6. GSM AT 11MHz, 78MSPS CLOCK (75dBc - NYQUIST, 9dB PAD)


FIGURE 8. FOUR GSM CARRIERS AT 12.4 to $15.6 \mathrm{MHz}, \mathbf{7 8 M S P S}$
(73dBc - 20MHz WINDOW, 6dB PAD)

Typical Performance Plots ${ }_{(+3,3 v}$ Supply, Using Eigure 15 with Rolff $=1000$ and R Rioad $\left.=500\right)$ (Continued)


FIGURE 9. UMTS AT 19.2MHz, 76.8MSPS (70dB 1st ACPR, 70 dB 2nd ACPR)


FIGURE 11. ONE TONE AT 40.4MHz, 210MSPS CLOCK (61dBc - NYQUIST, 6dB PAD)


FIGURE 13. TWO TONES (CF = 6) AT 8.5MHz, 50MSPS CLOCK, 500kHz SPACING (82dBc - 10MHz WINDOW, 6dB PAD)


FIGURE 10. ONE TONE AT 10.1MHz, 80MSPS CLOCK (71dBc - NYQUIST, 6dB PAD)


FIGURE 12. EIGHT TONES (CREST FACTOR = 8.9) AT 37MHz, 210MSPS CLOCK, 2.1MHz SPACING (65dBc - NYQUIST)


FIGURE 14. FOUR TONES (CF = 8.1) AT 14MHz, 80MSPS CLOCK, 800kHz SPACING (70dBc - NYQUIST, 6dB PAD)

## Definition of Specifications

Adjacent Channel Power Ratio, ACPR, is the ratio of the average power in the adjacent frequency channel (or offset) to the average power in the transmitted frequency channel.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

EDGE, Enhanced Data for Global Evolution, a TDMA standard for cellular applications which uses 200kHz BW, 8-PSK modulated carriers.

Full Scale Gain Drift, is measured by setting the data inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from $\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$. It is defined as the maximum deviation from the value measured at room temperature to the value measured at either $\mathrm{T}_{\text {MIN }}$ or $\mathrm{T}_{\text {MAX }}$. The units are ppm of FSR (full scale range) per ${ }^{\circ} \mathrm{C}$.

Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R $\mathrm{R}_{\mathrm{SET}}$ ).

GSM, Global System for Mobile Communication, a TDMA standard for cellular applications which uses 200 kHz BW, GMSK modulated carriers.

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Internal Reference Voltage Drift, is defined as the maximum deviation from the value measured at room temperature to the value measured at either $\mathrm{T}_{\text {MIN }}$ or $\mathrm{T}_{\text {MAX }}$. The units are ppm per ${ }^{\circ} \mathrm{C}$.

Offset Drift, is measured by setting the data inputs to all logic low (all Os) and measuring the output voltage at IOUTA through a known resistance as the temperature is varied from $\mathrm{T}_{\text {MIN }}$ to $\mathrm{T}_{\text {MAX }}$. It is defined as the maximum deviation from the value measured at room temperature to the value measured at either $\mathrm{T}_{\text {MIN }}$ or $\mathrm{T}_{\text {MAX }}$. The units are ppm of FSR (full scale range) per ${ }^{\circ} \mathrm{C}$.

Offset Error, is measured by setting the data inputs to all logic low (all Os) and measuring the output voltage of IOUTA through a known resistance. Offset error is defined as the maximum deviation of the IOUTA output current from a value of OmA.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed does not violate the compliance range.

Power Supply Rejection, is measured using a single power supply. The nominal supply voltage is varied $\pm 10 \%$ and the change in the DAC full scale output is noted.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the
amplitude of the output waveform is $0.707(-3 \mathrm{~dB})$ of its original value.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental signal to the largest harmonically or non-harmonically related spur within the specified frequency window.

Total Harmonic Distortion, THD, is the ratio of the RMS value of the fundamental output signal to the RMS sum of the first five harmonic components.

UMTS, Universal Mobile Telecommunications System, a W-CDMA standard for cellular applications which uses 3.84MHz modulated carriers.

## Detailed Description

The ISL5857 is a 12-bit, current out, CMOS, digital to analog converter. The maximum update rate is at least $260+$ MSPS and can be powered by a single power supply in the recommended range of +3.0 V to +3.6 V . It consumes less than 120 mW of power when using a +3.3 V supply, the maximum 20 mA of output current, and the data switching at 210MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter might have a substantially larger amount of current turning on and off at certain worst-case transition points, such as midscale and quarter scale transitions. By greatly reducing the amount of current switching at these major transitions, the overall glitch of the converter is dramatically reduced, improving settling time, transient problems and accuracy.

## Digital Inputs and Termination

The ISL5857 digital inputs are guaranteed to 3V LVCMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are long $50 \Omega$ lines, then $50 \Omega$ termination resistors should be placed as close to the converter inputs as possible connected to the digital ground plane (if separate grounds are used). These termination resistors are not likely needed as long as the digital waveform source is within a few inches of the DAC. For pattern drivers with very high speed edge rates, it is recommended that the user consider series termination ( $50 \Omega$ to $200 \Omega$ ) prior to the DAC's inputs in order to reduce the amount of noise.

## Power Supply

Separate digital and analog power supplies are recommended. The allowable supply range is +2.7 V to +3.6 V . The recommended supply range is +3.0 V to 3.6 V (nominally +3.3 V ) to maintain optimum SFDR. However, operation down to +2.7 V is possible with some degradation in SFDR. Reducing the analog output current can help the SFDR at +2.7V. The SFDR values stated in the table of specifications were obtained with $\mathrm{a}+3.3 \mathrm{~V}$ supply.

## Ground Planes

Separate digital and analog ground planes should be used. All of the digital functions of the device and their corresponding components should be located over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane.

## Noise Reduction

To minimize power supply noise, $0.1 \mu \mathrm{~F}$ capacitors should be placed as close as possible to the converter's power supply pins, $A V_{D D}$ and $D V_{D D}$. Also, the layout should be designed using separate digital and analog ground planes and these capacitors should be terminated to the digital ground for $\mathrm{DV}_{\mathrm{DD}}$ and to the analog ground for $\mathrm{AV}_{\mathrm{DD}}$. Additional filtering of the power supplies on the board is recommended.

## Voltage Reference

The internal voltage reference of the device has a nominal value of +1.23 V with a $\pm 40 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ drift coefficient over the full temperature range of the converter. It is recommended that a $0.1 \mu \mathrm{~F}$ capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin (16) selects the reference. The internal reference can be selected if pin 16 is tied low (ground). If an external reference is desired, then pin 16 should be tied high (the analog supply voltage) and the external reference driven into REFIO, pin 17. The full scale output current of the converter is a function of the voltage reference used and the value of $\mathrm{R}_{\text {SET }}$. I OUT should be within the 2 mA to 20 mA range, though operation below 2 mA is possible with performance degradation.

If the internal reference is used, $\mathrm{V}_{\text {FSADJ }}$ will equal approximately 1.2 V (pin 18). If an external reference is used, $\mathrm{V}_{\text {FSADJ }}$ will equal the external reference. The calculation for IOUT (Full Scale) is:
$I_{\text {OUT }}($ Full Scale $)=\left(\mathrm{V}_{\text {FSADJ }} /\right.$ R $_{\text {SET }} \times 32$
If the full scale output current is set to 20 mA by using the internal voltage reference (1.2V) and a $1.91 \mathrm{k} \Omega \mathrm{R}_{\mathrm{SET}}$ resistor, then the input coding to output current will resemble the following:

TABLE 1. INPUT CODING vs OUTPUT CURRENT WITH INTERNAL REFERENCE AND RSET $=1.91 \mathrm{k} \Omega$

| INPUT CODE (D11-D0) | IOUTA (mA) | IOUTB (mA) |
| :---: | :---: | :---: |
| 111111111111 | 20 | 0 |
| 100000000000 | 10 | 10 |
| 000000000000 | 0 | 20 |

## Analog Output

IOUTA and IOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single-ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -1.0 V to 1.25 V . $\mathrm{R}_{\text {OUT }}$ (the impedance loading each current output)
should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:
$V_{\text {OUT }}=I_{\text {OUT }} \times R_{\text {OUT }}$.
The most effective method for reducing the power consumption is to reduce the analog output current, which dominates the supply current. The maximum recommended output current is 20 mA .

## Differential Output

IOUTA and IOUTB can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. With $R_{\text {DIFF }}=50 \Omega$ and $R_{\text {LOAD }}=50 \Omega$, the circuit in Figure 15 will provide a 500 mV signal at the output of the transformer if the full scale output current of the DAC is set to 20 mA (used for the electrical specifications table). Values of RDIFF $=100 \Omega$ and $R_{\text {LOAD }}=50 \Omega$ were used for the typical performance curves. The center tap in Figure 15 must be grounded.

In the circuit in Figure 16, the user is left with the option to ground or float the center tap. The DC voltage that will exist at either IOUTA or IOUTB if the center tap is floating is IOUT ${ }_{D C} \times$ $\left(R_{A} / / R_{B}\right) V$ because $R_{\text {DIFF }}$ is DC shorted by the transformer. If the center tap is grounded, the DC voltage is OV . Recommended values for the circuit in Figure 16 are $R_{A}=R_{B}=50 \Omega, R_{\text {DIFF }}=100 \Omega$, assuming $R_{\text {LOAD }}=50 \Omega$. The performance of Figures 15 and 16 is basically the same, however leaving the center tap of Figure 16 floating allows the circuit to find a more balanced virtual ground, theoretically improving the even order harmonic rejection, but likely reducing the signal swing available due to the output voltage compliance range limitations.
$R_{E Q}=0.5 \times\left(R_{\text {LOAD }} / / R_{\text {DIFF }}\right)$
AT EACH OUTPUT


RLOAD REPRESENTS THE LOAD SEEN BY THE TRANSFORMER

FIGURE 15. OUTPUT LOADING FOR DATASHEET MEASUREMENTS

## Propagation Delay

The converter requires two clock rising edges for data to be represented at the output. Each rising edge of the clock captures the present data word and outputs the previous data. The propagation delay is therefore $1 /$ CLK, plus $<2$ ns of processing. See Figure 17.

## Test Service

Intersil offers customer-specific testing of converters with a service called Testdrive. To submit a request, fill out the Testdrive form. The form can be found by doing an 'entire site search' at www.intersil.com on the words 'DAC Testdrive'. Or, send a request to the technical support center.
$R_{E Q}=0.5 \times\left(R_{\text {LOAD }} / / R_{\text {DIFF }} / / R_{A}\right)$, WHERE $R_{A}=R_{B}$


FIGURE 16. ALTERNATIVE OUTPUT LOADING

## Timing Diagram



FIGURE 17. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
| :---: | :---: | :---: |
| October 7, 2015 | FN6079.3 | Updated Ordering Information on page 3. |
| May 14, 2015 | FN6079.2 | Updated entire datasheet applying Intersil's new standards. <br> Moved the Typical Application Circuit to page 1, Pin Configuration to page 2, and Ordering Information Table to page 3. <br> Removed obsolete products from the ordering information table on page 3. <br> Added Notes 2 and 3 to the Ordering Information Table. <br> Added the Part Marking column to the Ordering Information Table. <br> Removed ( -2.5 dBm ) from the following sentence under "Differential Output" on page 10: "With RDIFF = 50 RLOAD $=50 \Omega$, the circuit in Figure 13 will provide a $500 \mathrm{mV}(-2.5 \mathrm{dBm})$ signal at the output of the transformer if the full scale output current of the DAC is set to 20 mA (used for the electrical specifications table)." <br> Added Revision History and About Intersil Verbiage <br> Updated POD M28.3 to latest revision. <br> -Change made from Rev 0 to Rev 1 was adding land pattern <br> Updated POD M28.173 to latest revision. <br> -Changes made from Rev 0 to Rev 1 was converting to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes. |

## About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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## Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

| SYMBOL | INCHES |  | MILLIMETERS |  | NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX |  |
| A | 0.0926 | 0.1043 | 2.35 | 2.65 | - |
| A1 | 0.0040 | 0.0118 | 0.10 | 0.30 | - |
| B | 0.013 | 0.0200 | 0.33 | 0.51 | 9 |
| C | 0.0091 | 0.0125 | 0.23 | 0.32 | - |
| D | 0.6969 | 0.7125 | 17.70 | 18.10 | 3 |
| E | 0.2914 | 0.2992 | 7.40 | 7.60 | 4 |
| e | 0.05 BSC |  | 1.27 BSC |  | - |
| H | 0.394 | 0.419 | 10.00 | 10.65 | - |
| h | 0.01 | 0.029 | 0.25 | 0.75 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 28 |  | 28 |  | 7 |
| $\alpha$ | $0^{\circ}$ | $8^{\circ}$ | $0^{\circ}$ | $8^{\circ}$ | - |

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension " $D$ " does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15 mm ( 0.006 inch) per side.
4. Dimension " $E$ " does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25 mm ( 0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. " $L$ " is the length of terminal for soldering to a substrate.
7. " N " is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width " $B$ ", as measured 0.36 mm ( 0.014 inch ) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm ( 0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

## Package Outline Drawing

M28.173
28 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 1, 5/10


TOP VIEW
END VIEW


SIDE VIEW


DETAIL " X "


NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs.

Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H .
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08 mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07 mm .
6. Dimension in () are for reference only.
7. Conforms to JEDEC MO-153.

