High-Speed CMOS 16K x 16 Asynchronous Dual-Port RAM

QS70261A
QS7026A

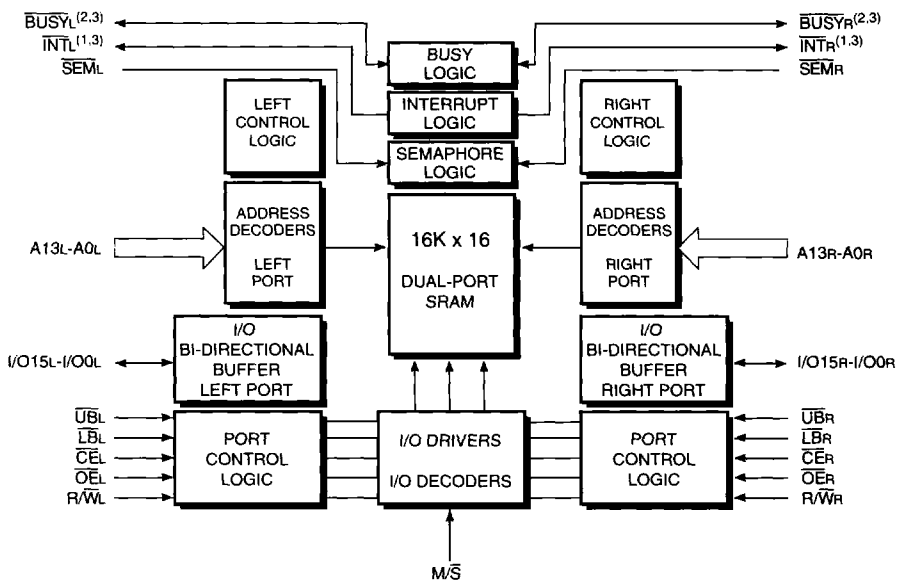
FEATURES

- High-speed asynchronous dual-port architecture
- Access times from either port, 17[1]/20/25/35/55 ns
- Industry standard pin-out
- Independent port access and control
- Separate byte controls for bus muxing
- Master/slave pin, for width expansion
- Depth expandable
- Low-noise outputs, for quiet operation
- Integrated arbitration:
  - Semaphores
  - Interrupts (QS70261A Only)
  - Busy Flags
- Industrial temperature range available (-40°C to 85°C)
- 100-pin TQFP (QS70261A Only) and 84-pin PLCC (QS72026A Only)

DESCRIPTION

The QS70261A/26A is an asynchronous 16K x 16 Dual-Port RAM. This device can be used as a stand-alone 256K-bit Dual-Port RAM, or multiple devices can be interconnected for 32-bit or more word systems without adding discrete logic. Both ports can be written to and read from simultaneously. Coincidental address matches are arbitrated internally using the busy flag. Other arbitration schemes are catered for, such as semaphores and interrupts. $\overline{CE}$ powers down the memory array, permitting the device to enter very low power standby mode. This device can be used in DSP applications, data communications, networking, graphics and multiprocessing. The use of multiple power and ground pins and output waveform control and input noise filters dramatically reduces noise susceptibility and ground bounce.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM



Notes:
1. Only available on QS70261A.
2. M/$\overline{S}$ HIGH, $\overline{BUSY}$ is output, M/$\overline{S}$ LOW, $\overline{BUSY}$ is intput.
3. $\overline{BUSY}$ and $\overline{INT}$ outputs are non-tri-stated push-pull.

FIGURE 2. 100-PIN TQFP PINOUT (QS70261A ONLY) (Top view)

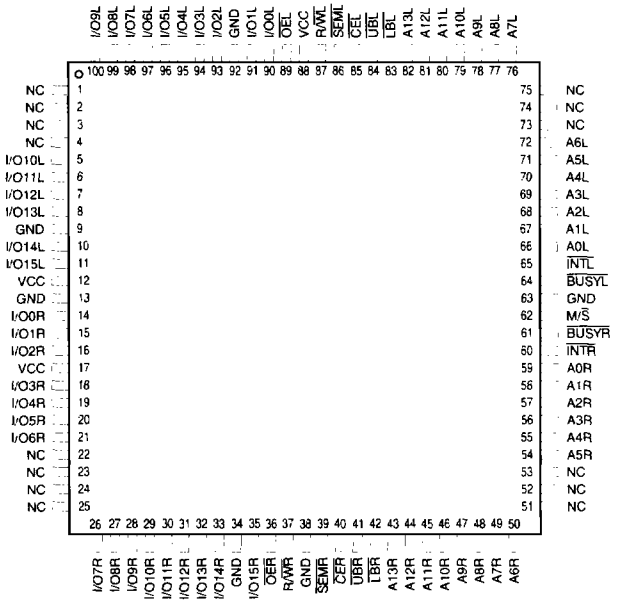
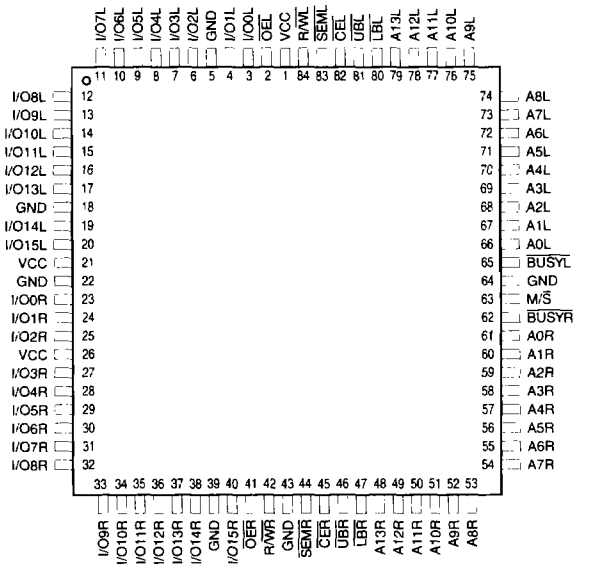


FIGURE 3. 84-PIN PLCC PINOUT (QS7026A ONLY) (Top view)



FUNCTIONAL DESCRIPTION

The QS70261A/26A provides two ports with separate controls, address buses and data buses that permit independent read and write accesses to any memory location. The QS70261A/26A has an automatic power-down feature controlled by $\overline{CE}$. When this is inactive, the RAM array and sense amplifiers are turned off and the part enters standby mode.

POWER-DOWN OPERATION

These devices have an automatic power-down feature controlled by $\overline{CE}$, the dual-port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power-down circuitry that permits the respective port to go into standby mode when not selected. This is the condition shown in the TABLE 2. NON-CONTENTIOUS READ AND WRITE where $\overline{CE}$ and $\overline{SEM}$ are both HIGH or both LOW.

TABLE 1. PIN DESCRIPTIONS, QS70261A AND QS7026A

Left Port	Right Port	Input Or Output	Pin Description	Active State
I/O_{NL}	I/O_{NR}	Input & Output	Bi-directional Data Port	X
A_{NL}	A_{NR}	Input	Address Bus	X
$R/\overline{W}_L$	$R/\overline{W}_R$	Input	Read/Write Select Pin	Note 1
$\overline{OE}_L$	$\overline{OE}_R$	Input	Output Enable	L
$\overline{UB}_L$	$\overline{UB}_R$	Input	Upper Byte Select	L
$\overline{LB}_L$	$\overline{LB}_R$	Input	Lower Byte Select	L
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Input & Output	Busy Flag	L
$\overline{SEM}_L$	$\overline{SEM}_R$	Input	Semaphore Enable	L
$\overline{INT}_L$	$\overline{INT}_R$	Output	Interrupt Flag	L
$\overline{CE}_L$	$\overline{CE}_R$	Input	Chip Enable	L
$M/\overline{S}$		Input	Master/$\overline{Slave}$	Note 2

Notes:
1. Write when LOW, read when HIGH.
2. Slave when LOW, master when HIGH.
3. Interrupt Flags available on QS70261A only.

TABLE 2. NON-CONTENTIOUS READ/WRITE

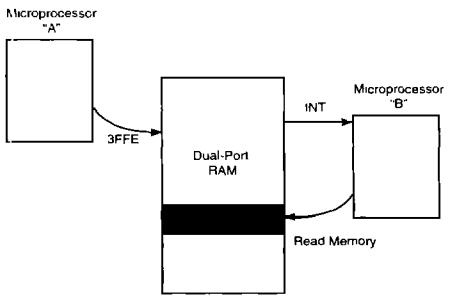
$R/\overline{W}$	$\overline{UB}$	$\overline{LB}$	$\overline{CE}$	$\overline{OE}$	$\overline{SEM}$	I/O15-8	I/O7-0	Mode
X	X	X	H	X	H	HIGH-Z	HIGH-Z	Power-Down HIGH-Z
X	X	X	L	X	L	HIGH-Z	HIGH-Z	Power-Down HIGH-Z
X	H	H	X	X	H	HIGH-Z	HIGH-Z	Both Bytes Deselected
X	X	X	X	H	X	HIGH-Z	HIGH-Z	Outputs Disabled
L	H	L	L	X	H	HIGH-Z	WR I/O	Data Write Lower Byte Only
L	L	H	L	X	H	WR I/O	HIGH-Z	Data Write Upper Byte Only
L	L	L	L	X	H	WR I/O	WR I/O	Data Write Both Bytes
H	H	L	L	L	H	HIGH-Z	RD I/O	Data Read Lower Byte Only
H	L	H	L	L	H	RD I/O	HIGH-Z	Data Read Upper Byte Only
H	L	L	L	L	H	RD I/O	RD I/O	Data Read Both Bytes

INTERRUPTS ($\overline{INT}$)

When the left port wants to interrupt the right port, the left port writes to location 3FFF(HEX) setting the $\overline{INT}_R$ flag. The flag is cleared by reading 3FFF from the right port. A 16-bit message at these locations is user defined.

When the right port wants to interrupt the left port, the right port writes to location 3FFE(HEX) which sets the $\overline{INT}_L$ flag. The flag is cleared by reading 3FFE from the left port.

FIGURE 4. USE OF INTERRUPTS IN A MULTIPROCESSING APPLICATION



BUSY LOGIC ($\overline{BUSY}$)

$\overline{BUSY}$ logic prevents writes to the same address. Writes are arbitrated so that one port will gain access to write, and the other port will be prevented from writing by $\overline{BUSY}$ being asserted. This condition only happens on writes and prevents data corruption due to simultaneous address accesses. This feature can be disabled when the part is put into slave mode.

TABLE 3. BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	$A13_L$-$A0_L$ $A13_R$-$A0_R$	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	No Match	H	H	Normal
H	X	Match	H	H	Normal
X	H	Match	H	H	Normal
L	L	Match	—	—	Write Inhibit[2]

Notes:
1. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are outputs when the device is in master mode. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are inputs when the device is in slave mode.
2. Write inhibit occurs on same port as $\overline{BUSY}$ output LOW.

TABLE 4. INTERRUPT FLAG TRUTH TABLE[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A13_L$-$A0_L$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A13_R$-$A0_R$	$\overline{INT}_R$	Function
L	L	X	3FFF	X	X	X	X	X	L[2]	Set $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF	H[3]	Reset $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FFE	X	Set $\overline{INT}_L$ Flag
X	L	L	3FFE	H[2]	X	X	X	X	X	Reset $\overline{INT}_L$ Flag

Notes:
1. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

WIDTH AND DEPTH EXPANSION WITH QS70261A/26A DUAL-PORT RAMS

If the write inhibit function of busy logic is not enabled, the busy logic can be disabled by placing the part into slave mode with the M/$\overline{S}$ pin. Once in slave mode, the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the QS70261A/26A RAM in master mode are push-pull type outputs and do not require pull-up resistors to operate. If these RAMs are being expanded in depth, then $\overline{BUSY}$ indication for the resulting array requires the use of an external AND gate.

ENHANCED SEMAPHORES

The QS70261A/26A is an extremely fast dual-port x16 CMOS static RAM with an additional eight address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the dual-port RAM to claim a privilege over the other processor for functions defined by the system designer's software. For example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the dual-port RAM or any other shared resource, for example to protect blocks of data (see Figure 5).

The dual-port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS static RAMs and can be read from or written to at the same time with the only possible conflict arising from the simultaneous writing or a simultaneous read/write of a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the dual-port RAM.

SEMAPHORE APPLICATION

Systems which can best use the QS70261A/26A contain multiple processors or controllers and are typically very high speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the QS70261A/26A's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The QS70261A/26A does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high speed systems.

In addition, the use of the $\overline{UB}$ and $\overline{LB}$ controls allows individual byte control of the I/O bus when in semaphore mode and hence adds the ability to be tristated.

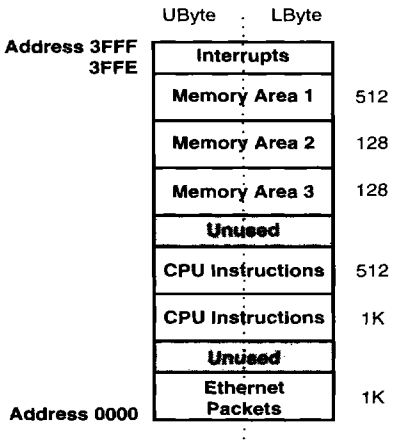
TABLE 5. SEMAPHORES

$\overline{SEM}$	$\overline{UB}$	$\overline{LB}$	MSBYTES	LSBYTES
L	L	L	DDDD DDDD[1]	DDDD DDDD[1]
L	L	H	DDDD DDDD[1]	ZZZZ ZZZZ
L	H	L	ZZZZ ZZZZ	DDDD DDDD[1]
L	H	H	ZZZZ ZZZZ	ZZZZ ZZZZ

Note:
1. "D" means active outputs

For example, use of this method of memory segmentation in Figure 5 allows Ethernet packets to be stored in a 1K memory area and CPU instructions to be stored in two blocks of 1K and 512, etc. The granularity is extremely flexible and can be from one word to the full memory map.

FIGURE 5. TYPICAL MEMORY PARTITIONING USING ENHANCED SEMAPHORES



SEMAPHORE ACCESS

The eight semaphore flags reside within the QS70261A/26A in a separate memory space from the dual-port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (address, $\overline{UB}$, $\overline{LB}$, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A2-A0.

When the semaphores are being accessed, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a "0" on that side and a "1" on the other side. That semaphore can now only be modified by the side showing the "0." When a "1" is written into the same location from the same side, the flag will be set to a "1" for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a "0" into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. A "0" written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a "1" reads as a "1" in all data bits, the semaphore flag will force its side of the semaphore flag and the other side HIGH. This condition will continue until a "0" is written to the same semaphore request latch. Should the other side's semaphore request latch have been written "0" in the meantime, the semaphore flag will flip over to other side as soon as a "1" is written into the first-side request latch. These flags will now stay LOW until the semaphore request latch is written to a "1." If a semaphore is requested and a processor which requested it no longer needs the resource, the entire system can hang up until a "1" is written into the semaphore request latch.

The critical case of semaphore timing is when both request a single token by attempting to write a "0" at the same time. The semaphore logic is specially designed to resolve this problem if simultaneous requests are made.

TABLE 6. SEMAPHORE ADDRESSING

AX...A3	A2	A1	A0	Semaphore Flag
X	0	0	0	1
X	0	0	1	2
X	0	1	0	3
X	0	1	1	4
X	1	0	0	5
X	1	0	1	6
X	1	1	0	7
X	1	1	1	8

SEMAPHORE OPERATION

When a semaphore flag is read, its value is spread into all data so that a flag that is a "1" reads as a "1" in all data bits, and a flag containing a "0" reads as all "0"s.

A sequence write/read must be used by the semaphore in order to guarantee that no system-level contention will occur. A processor requests access to shared resources by attempting to write a "0" into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a "0," yet the semaphore flag will appear as "1," a fact which the processor will verify by the subsequent read.

SEMAPHORE ARCHITECTURE

The semaphore logic is a set of eight latches (see Figure 6) which are independent of the dual-port RAM.

These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "token passing allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch.

This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a "0" into a semaphore latch and is released when the same side writes a "1" to that latch.

FIGURE 6. SEMAPHORE LATCHES

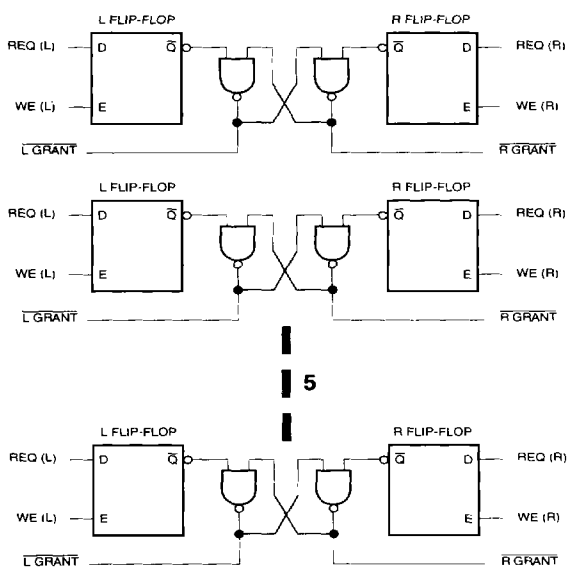


TABLE 7. SEMAPHORE READ/WRITE

R/$\overline{W}$	$\overline{UB}$	$\overline{LB}$	$\overline{CE}$	$\overline{OE}$	$\overline{SEM}$	I/O15-8	I/O7-0	Output Mode
H	L	L	H	L	L	DOUT	DOUT	Read Data in Semaphore Flag
H	H	H	X	L	L	HIGH-Z	HIGH-Z	Read Data in Semaphore Flag
↑	X	X	H	X	L	DIN	DIN	Write Data (D0) into Semaphore Location
↑	H	H	H	X	L	DIN	DIN	Write Data (D0) into Semaphore Location
X	X	L	L	X	L	HIGH-Z	HIGH-Z	Power-Down HIGH-Z
X	L	X	L	X	L	HIGH-Z	HIGH-Z	Power-Down HIGH-Z
H	L	H	H	L	L	DOUT	HIGH-Z	DOUT Semaphore Upper Byte
H	H	L	H	L	L	HIGH-Z	DOUT	DOUT Semaphore Lower Byte

TABLE 8. SEMAPHORE WRITE SEQUENCE (one of the eight semaphores)

Function Port	Action Writes	Left I/O15-0	Right I/O15-0	Status
No Action	—	1	1	Semaphore Free
Left	0	0	1	Left Port Obtains Semaphore Token
Right	0	0	1	No Change. Right Port Has No Write Access to Semaphore
Left	1	1	0	Right Port Obtains Semaphore Token
Left	0	1	0	No Change. Left Port Has No Write Access to Semaphore
Right	1	0	1	Left Port Obtains Semaphore Token
Left	1	1	1	Semaphore Free
Right	0	1	0	Right Port Obtains Semaphore Token
Right	1	1	1	Semaphore Free
Left	0	0	1	Left Port Obtains Semaphore Token
Left	1	1	1	Semaphore Free

TABLE 9. RECOMMENDED OPERATING CONDITIONS

Commercial T_A = 0°C to 70°C, Industrial T_A = -40°C to 85°C

Symbol	Description	Min	Max
V_{CC}	Supply Voltage	4.5V	5.5V
GND	Ground	0V	0V

TABLE 10. ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to Vcc + 0.5V
DC Input Voltage V_{IN}	–0.5V to Vcc + 0.5V
AC Input Voltage (Pulse Width ≤ 20 ns)	–3.0V
DC Input Diode Current with V_{IN} < 0	–50 mA
DC Output Diode Current V_{OUT}< 0	–50 mA
DC Output Diode Current V_{OUT}>Vcc	+50 mA
DC Output Current Max. Sink Current/Pin	-70 mA
DC Output Current Max. Source Current/Pin	70 mA
T_{STG} Storage Temperature	–65°C to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may *cause permanent damage* to this device resulting in functional or reliability type failures.

TABLE 11. DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A = 0°C to 70°C, Industrial T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage		2.2	—	V
V_{IL}	Input LOW Voltage		—	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4 mA, Vcc = MIN	2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 4 mA, Vcc = MIN	—	0.4	V
$\lvert I_{OZ} \rvert$	Output Leakage	$\overline{CE}$ = V_{IH}, Vcc = MAX, V_{OUT} = Vcc or 0V	—	10	µA
$\lvert I_{IL} \rvert$	Input Leakage	Vcc = MAX, GND < V_{IN} < Vcc	—	10	µA

TABLE 12. CAPACITANCE

T_A = 25°C, f = 1.0 MHz TQFP (TF) Package

Name	Description	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz	4	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1 MHz	8	10	pF

Note: Capacitance is guaranteed but not tested.

TABLE 13. DC POWER-SUPPLY CHARACTERISTICS OVER OPERATING TEMPERATURE AND SUPPLY VOLTAGE

			-17		-20		-25		
	Parameter	**Test Condition**	**Typ[1]**	**Max**	**Typ[1]**	**Max**	**Typ[1]**	**Max**	**Units**
I_{CC}	Dynamic Operating Current	$\overline{CE} \le V_{IL}$, $\overline{SEM} \le V_{IH}$ Outputs Open f = f_{MAX}[2]	200	295	180	275	170	265	mA
I_{SE1}	Standby Current Both Ports - TTL Level Inputs	$\overline{SEM} \ge V_{IH}$ $\overline{CE} \ge V_{IH}$ f = f_{MAX}[2]	35	85	30	85	25	85	mA
I_{SE2}	Standby Current One Port - TTL Level Inputs	$\overline{SEM}_R$ or $\overline{SEM}_L \ge V_{IH}$ $\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$ f = f_{MAX}[2]	125	220	115	210	105	200	mA
I_{SB3}	Full Standby Current Both Ports - All CMOS Level Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0[3], $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC} - 0.2V$	1	15	1	15	1	15	mA
I_{SB4}	Full Standby Current One Port - All CMOS Level Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, $\overline{SEM}_R$ = $\overline{SEM}_L$ $\ge V_{CC} - 0.2V$, Active Port Outputs Open, f = f_{MAX}[2]	120	200	110	185	100	170	mA

Notes:

1. V_{CC} = 5V, T_A = +25°C, and not production tested.
2. At f = f_{MAX}, address and control lines are cycling at the maximum read cycle frequency 1/t_{RC}, output enable is high. AC TEST CONDITIONS of input levels of 0V to 3V.
3. f = 0 means no address or control lines change.

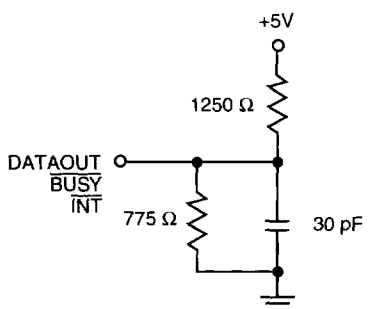
TABLE 13. DC POWER-SUPPLY CHARACTERISTICS OVER OPERATING TEMPERATURE AND SUPPLY VOLTAGE (Continued)

			-35		-55		
	Parameter	**Test Condition**	**Typ[1]**	**Max**	**Typ[1]**	**Max**	**Units**
I_{CC}	Dynamic Operating Current	$\overline{CE} \le V_{IL}$, $\overline{SEM} \le V_{IH}$ Outputs Open f = f_{MAX}[2]	160	255	150	230	mA
I_{SB1}	Standby Current Both Ports - TTL Level Inputs	$\overline{SEM} \ge V_{IH}$ $\overline{CE} \ge V_{IH}$ f = f_{MAX}[2]	20	85	13	85	mA
I_{SB2}	Standby Current One Port - TTL Level Inputs	$\overline{SEM}_R$ or $\overline{SEM}_L \ge V_{IH}$ $\overline{CE}_R$ or $\overline{CE}_L \ge V_{IH}$ f = f_{MAX}[2]	95	185	85	165	mA
I_{SB3}	Full Standby Current Both Ports - All CMOS Level Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \ge V_{CC} - 0.2V$ $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, f = 0[3], $\overline{SEM}_R$ = $\overline{SEM}_L \ge V_{CC} - 0.2V$	1	15	1	15	mA
I_{SB4}	Full Standby Current One Port - All CMOS Level Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC} - 0.2V$, $V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$, $\overline{SEM}_R = \overline{SEM}_L \ge V_{CC} - 0.2V$, Active Port Outputs Open, f = f_{MAX}[2]	90	160	90	135	mA

Notes:

1. V_{CC} = 5V, T_A = +25°C, and not production tested.
2. At f = f_{MAX}, address and control lines are cycling at the maximum read cycle frequency 1/t_{RC}, output enable is high. AC TEST CONDITIONS of input levels of 0V to 3V.
3. f = 0 means no address or control lines change.

FIGURE 7. AC TEST CONDITIONS



Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

Output Load.
5 pF for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}.
Includes jig and scope.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE AND SUPPLY VOLTAGE

TABLE 14. READ CYCLE TIMING

Sym	Parameter	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max
t_{RC}	Read Cycle Time	17	—	20	—	25	—
t_{AA}	Address Access Time	—	17	—	20	—	25
t_{ACE}	Chip Enable Access Time	—	17	—	20	—	25
t_{ABE}	Byte Enable Access Time	—	17	—	20	—	25
t_{AOE}	Output Enable Access Time	—	10	—	12	—	13
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—
t_{LZ}	Output LOW-Z Time[1]	3	—	3	—	3	—
t_{HZ}	Output HIGH-Z Time[1]	—	10	—	12	—	15
t_{PU}	Chip Enable to Power-Up Time[1]	0	—	0	—	0	—
t_{PD}	Chip Disable to Power-Down Time[1]	—	17	—	20	—	25
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—
t_{SAA}	Semaphore Address Access	—	17	—	20	—	25

Sym	Parameter	-35 Min	-35 Max	-55 Min	-55 Max
t_{RC}	Read Cycle Time	35	—	55	—
t_{AA}	Address Access Time	—	35	—	55
t_{ACE}	Chip Enable Access Time	—	35	—	55
t_{ABE}	Byte Enable Access Time	—	35	—	55
t_{AOE}	Output Enable Access Time	—	20	—	30
t_{OH}	Output Hold from Address Change	3	—	3	—
t_{LZ}	Output LOW-Z Time[1]	3	—	3	—
t_{HZ}	Output HIGH-Z Time[1]	—	15	—	25
t_{PU}	Chip Enable to Power-Up Time[1]	0	—	0	—
t_{PD}	Chip Disable to Power-Down Time[1]	—	35	—	50
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—
t_{SAA}	Semaphore Address Access	—	35	—	55

TABLE 15. WRITE CYCLE TIMING

Sym	Parameter	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max
t_{WC}	Write Cycle Time	17	—	20	—	25	—
t_{EW}	Chip Enable to End of Write	12	—	15	—	20	—
t_{AW}	Address Valid to End of Write	12	—	15	—	20	—
t_{AS}	Address Setup Time	0	—	0	—	0	—
t_{WP}	Write Pulse Width	12	—	15	—	20	—
t_{WR}	Write Recovery Time	0	—	0	—	0	—
t_{DW}	Data Valid to End of Write	10	—	15	—	15	—
t_{HZ}	Output HIGH-Z Time[1]	—	10	—	12	—	15
t_{DH}	Data Hold Time	0	—	0	—	0	—
t_{WZ}	Write Enable to Output in HIGH-Z[1]	—	10	—	12	—	15
t_{OW}	Output Active from End of Write[1]	0	—	0	—	0	—
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—

Sym	Parameter	-35 Min	-35 Max	-55 Min	-55 Max
t_{WC}	Write Cycle Time	35	—	55	—
t_{EW}	Chip Enable to End of Write	30	—	45	—
t_{AW}	Address Valid to End of Write	30	—	45	—
t_{AS}	Address Setup Time	0	—	0	—
t_{WP}	Write Pulse Width	25	—	40	—
t_{WR}	Write Recovery Time	0	—	0	—
t_{DW}	Data Valid to End of Write	15	—	30	—
t_{HZ}	Output HIGH-Z Time[1]	—	15	—	25
t_{DH}	Data Hold Time	0	—	0	—
t_{WZ}	Write Enable to Output in HIGH-Z[1]	—	15	—	25
t_{OW}	Output Active from End of Write[1]	0	—	0	—
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—

Note:
1. Transition is measured ± 500 mV from low- or high-impedance voltage with load (see AC TEST CONDITIONS). Guaranteed but not tested.

TABLE 16. BUSY TIMING (M/$\overline{S}$ = H)

Sym	Parameter	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max
t_{BAA}	Busy Access Address Match	—	17	—	20	—	20
t_{BDA}	Busy Disable Address Mismatch	—	17	—	20	—	20
t_{BAC}	Busy Access from $\overline{CE}$ LOW	—	17	—	20	—	20
t_{BDC}	Busy Disable from $\overline{CE}$ HIGH	—	17	—	17	—	20
t_{APS}	Arbitration Setup[1]	5	—	5	—	5	—
t_{BDD}	Busy Disable to Valid Data[2]	—	17	—	20	—	25
t_{WB}	Busy Setup Stop Write[4]	0	—	0	—	0	—
t_{WH}	Busy Hold Stop Write[5]	13	—	15	—	17	—
t_{WDD}	Write Pulse to Data Delay[3]	—	30	—	45	—	50
t_{DDD}	Write Data, Read Data[3]	—	25	—	30	—	35

Sym	Parameter	-35 Min	-35 Max	-55 Min	-55 Max
t_{EAA}	Busy Access Address Match	—	20	—	45
t_{EDA}	Busy Disable Address Mismatch	—	20	—	40
t_{BAC}	Busy Access from $\overline{CE}$ LOW	—	20	—	40
t_{BDC}	Busy Disable from $\overline{CE}$ HIGH	—	20	—	35
t_{APS}	Arbitration Setup[1]	5	—	5	—
t_{BDD}	Busy Disable to Valid Data[2]	—	35	—	55
t_{WB}	Busy Setup Stop Write[4]	0	—	0	—
t_{WH}	Busy Hold Stop Write[5]	25	—	25	—
t_{WDD}	Write Pulse to Data Delay[3]	—	60	—	80
t_{DDD}	Write Data, Read Data[3]	—	45	—	65

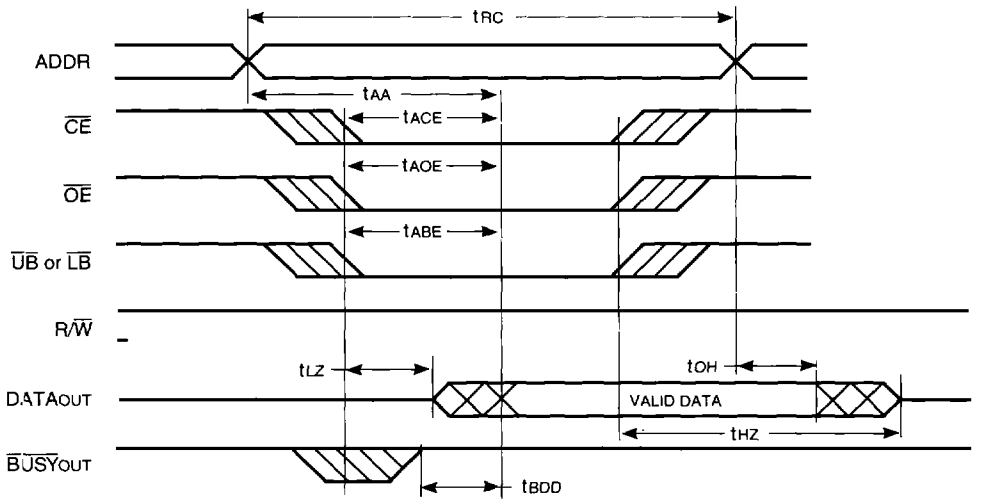
Notes:
1. To ensure that the earlier of the two ports wins.
2. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read with $\overline{BUSY}$ (M/$\overline{S}$ = H)" or "Timing Waveform of Write with Port-to-Port Delay (M/$\overline{S}$ = L)."
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.

TABLE 17. INTERRUPT TIMING

Sym	Parameter	-17 Min	-17 Max	-20 Min	-20 Max	-25 Min	-25 Max
t_{AS}	Address Set-up Time	0	—	0	—	0	—
t_{WR}	Write Recovery Time	0	—	0	—	0	—
t_{INS}	Interrupt Set Time	—	15	—	20	—	20
t_{INR}	Interrupt Reset Time	—	15	—	20	—	20

Sym	Parameter	-35 Min	-35 Max	-55 Min	-55 Max
t_{AS}	Address Set-up Time	0	—	0	—
t_{WR}	Write Recovery Time	0	—	0	—
t_{INS}	Interrupt Set Time	—	25	—	40
t_{INR}	Interrupt Reset Time	—	25	—	40

FIGURE 8. READ CYCLE TIMING WAVEFORM



Note:
1. $\overline{SEM}$ = H.

FIGURE 9. R/$\overline{W}$ CONTROLLED WRITE CYCLE TIMING WAVEFORM[1,3,5,8]

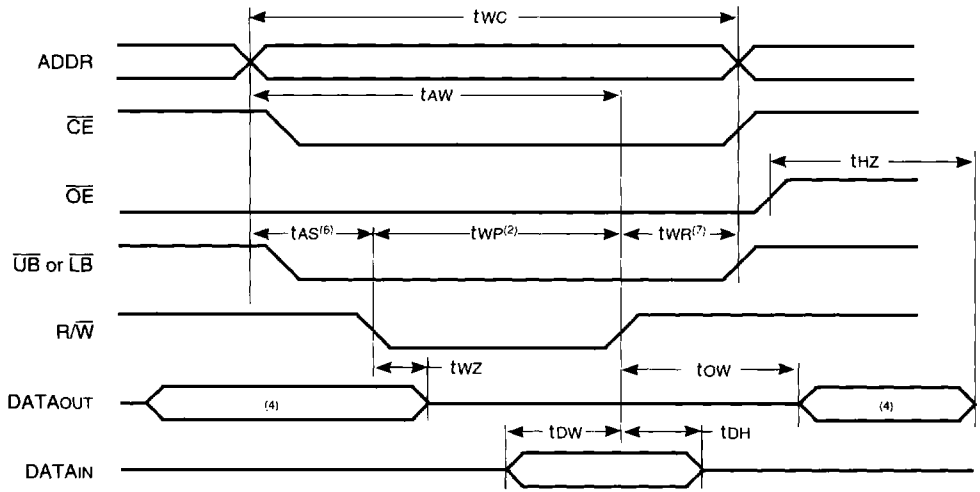
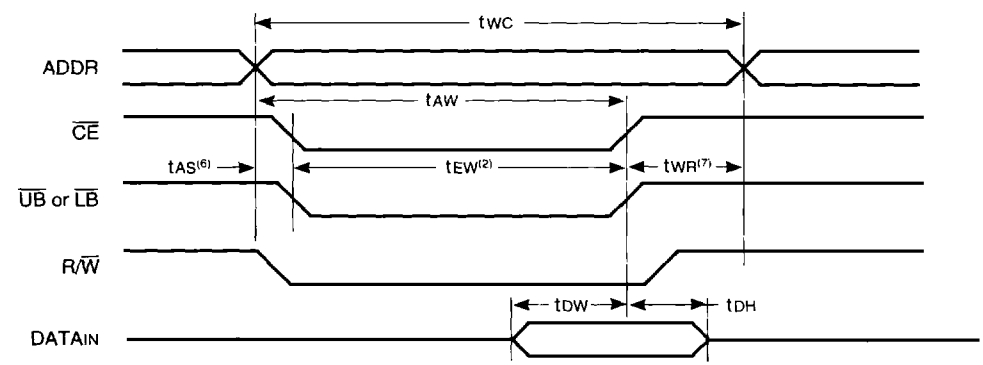


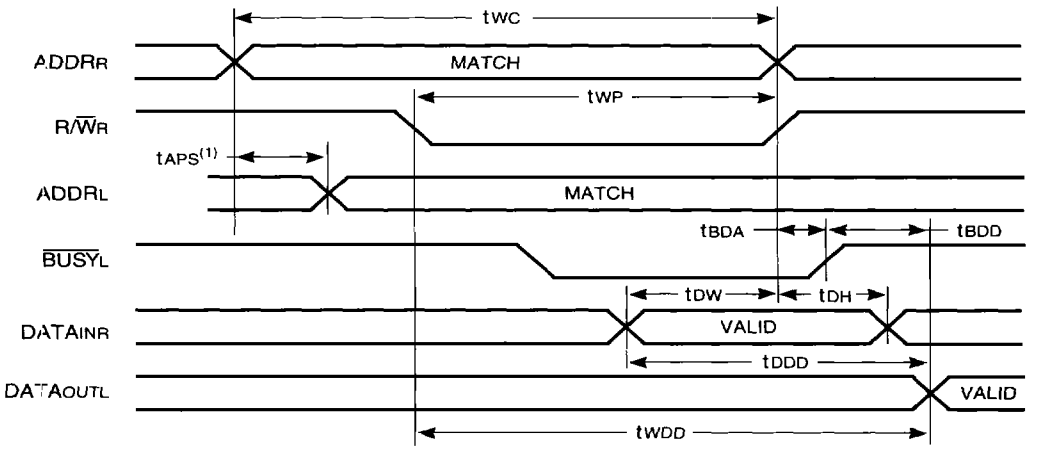
FIGURE 10. $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED WRITE CYCLE TIMING WAVEFORM[1,3,5,8]



Notes to Figures 9 and 10:

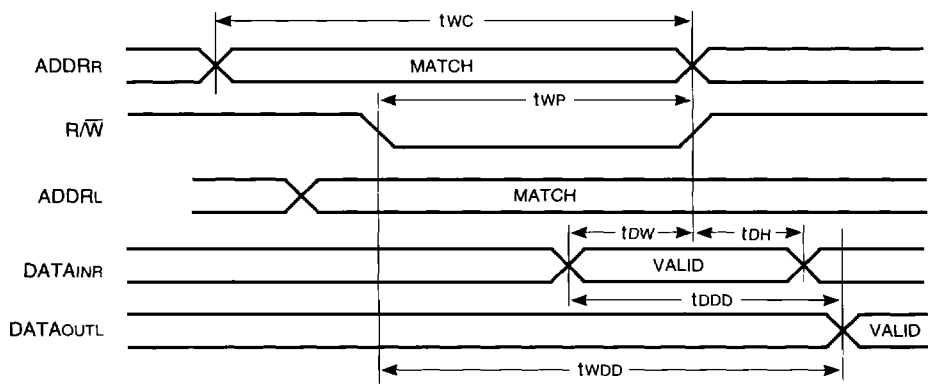
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a LOW $\overline{UB}$ or $\overline{LB}$ and a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last: $\overline{CE}$, R/$\overline{W}$, or byte control.
7. Timing depends on which enable signal is de-asserted first: $\overline{CE}$, R/$\overline{W}$, or byte control.
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or t_{WZ} + t_{DW} to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

FIGURE 11. $\overline{BUSY}$ TIMING WAVEFORM (M/$\overline{S}$ = H)



Note:
1. If tAPS is violated, no guarantee on which port will write.

FIGURE 12. PORT-TO-PORT WRITE TIMING DELAY WAVEFORM (M/$\overline{S}$ = L)[1,2]



Note:
1. $\overline{BUSY}$ input is HIGH for the writing port.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L.

FIGURE 13. SLAVE WRITE TIMING WAVEFORM (M/$\overline{S}$ = L)

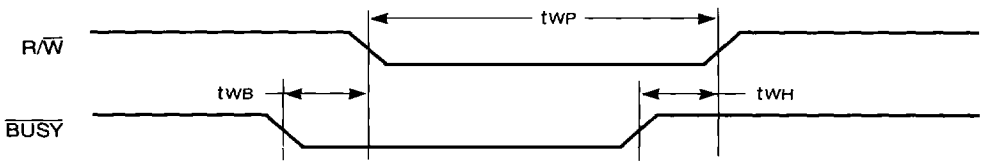
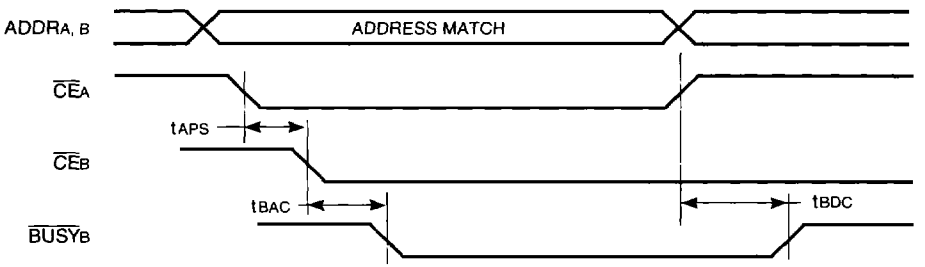
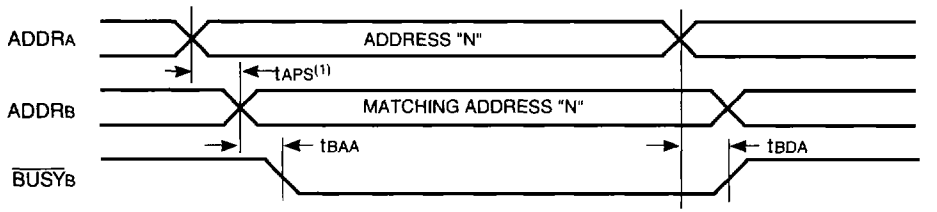


FIGURE 14. $\overline{BUSY}$ ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING (M/$\overline{S}$ = H)[1]



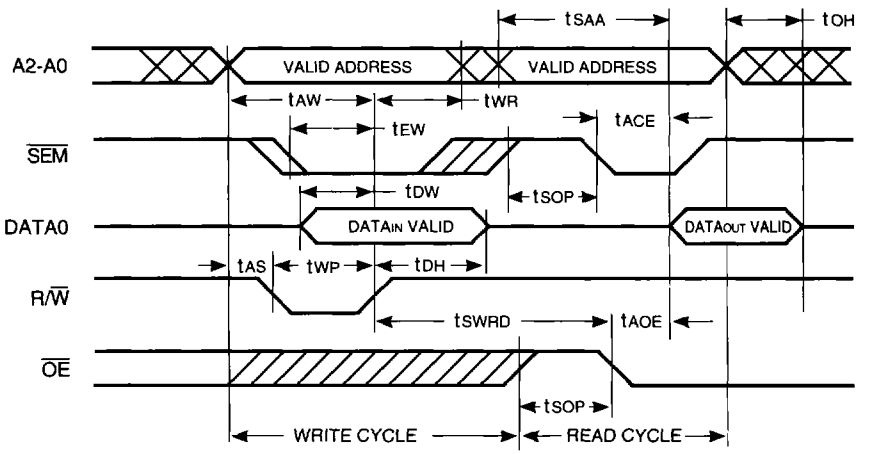
Note:
1. If tAPS is not satisfied, there is no guarantee on which $\overline{BUSY}$ will be asserted.

FIGURE 15. $\overline{BUSY}$ ARBITRATION CONTROLLED BY ADDRESS MATCH CONTROLLED BY $\overline{CE}$ TIMING (M/$\overline{S}$ = H)



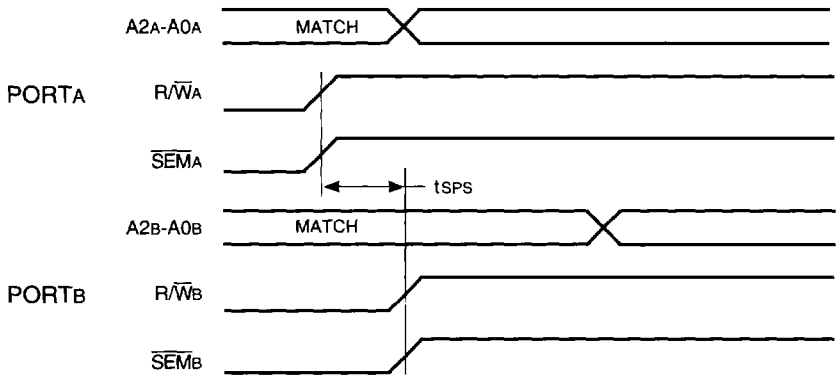
Note:
1 If tAPS is not satisfied, there is no guarantee on which $\overline{BUSY}$ will be asserted.

FIGURE 16. SEMAPHORE READ-AFTER-WRITE TIMING WAVEFORM, EITHER SIDE



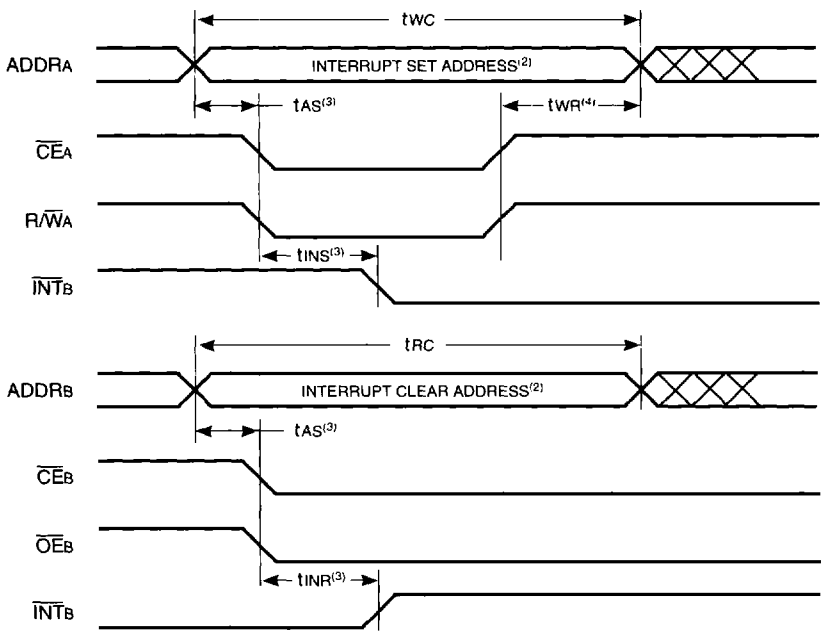
Note:
1. $\overline{CE}$ = H or $\overline{UB}$ and $\overline{LB}$ = H for the above.

FIGURE 17. SEMAPHORE WRITE CONTENTION TIMING WAVEFORM



Notes:
1. $D_{OR} = D_{OL} = L$, $\overline{CE}_R = \overline{CE}_L = H$, semaphore flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right. "B" is the opposite port from "A."
3. This parameter is measured from R/W̄A or SEMA going HIGH to R/W̄B or SEMB going HIGH.
4. If t_{SPS} is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FIGURE 18. INTERRUPT TIMING WAVEFORM[1]



Notes:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A."
2. See TABLE 4. INTERRUPT FLAG TRUTH TABLE.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

PACKAGING INFORMATION

The QS7026A is offered in the JEDEC-standard 84-pin PLCC package and the QS70261A is offered in the JEDEC-standard 100-pin TQFP (Thin QFP) plastic package. This package offers the best combination of small footprint, manufacturability and low cost. Test sockets are available from Yamaichi and may be available from ITT Pomona as of this writing. TQFP products are shipped in plastic trays. θ_{JA} for the TQFP is 64°C/W.

As with all large plastic packages, care should be taken to avoid moisture-related mechanical failure. This typically occurs when moisture absorbed into the porous molding compound vaporizes during reflow operations. To prevent moisture-related assembly problems, it is recommended that customers perform a baking operation prior to assembly. Baking the units for 24 hours at 125°C removes excess moisture from the part. In a typical environment of 60% relative humidity at <30°C, parts can sit up to 48 hours before assembly. In higher-humidity environments, the time between bake and solder reflow should be shorter. In dry environments (<20% RH), or when sealed in moisture-barrier bags with dessicant, shelf life is indefinite.

ORDERING INFORMATION

Example: