TPS22917 1 V–5.5-V, 2-A, 80-mΩ Ultra-Low Leakage Load Switch

1 Features

- Input Operating Voltage Range (V_{IN}): 1 V to 5.5 V
- Maximum Continuous Current (I_{MAX}): 2 A
- On-Resistance (R_{ON}):
  - 5 V_{IN} = 80 mΩ (Typical)
  - 1.8 V_{IN} = 120 mΩ (Typical)
  - 1 V_{IN} = 220 mΩ (Typical)
- Ultra-Low Power Consumption:
  - ON State (I_Q): 0.5 µA (Typical)
  - OFF State (I_{SD}): 10 nA (Typical)
- Smart ON Pin Pull Down (R_{PD}):
  - ON ≥ VIH (I_{ON}): 10 nA (Maximum)
  - ON ≤ VIL (R_{PD}): 750 kΩ (Typical)
- Adjustable Turn ON Limits Inrush Current (t_{ON}):
  - 5-V t_{ON} = 100 µs at 72 mV/µs (C_T = Open)
  - 5-V t_{ON} = 4000 µs at 2.3 mV/µs (C_T = 1000 pF)
- Adjustable Output Discharge and Fall Time:
  - Optional QOD Resistance ≥ 150 Ω (Internal)
- Always-ON True Reverse Current Blocking (RCB):
  - Activation Current (I_{RCB}): –500 mA (Typical)
  - Reverse Leakage ($I_{IN,RCB}$): –1 µA (Maximum)

2 Applications

- Industrial Systems
- Set Top Box
- Blood Glucose Meters
- Electronic Point of Sale

3 Description

The TPS22917 device is a small, single channel load switch utilizing a low leakage P-Channel MOSFET for minimum power loss. Advanced gate control design supports operating voltages as low as 1 V with minimal increase in ON-Resistance and power loss.

The Rise and Fall times can be independently adjusted with external components for system level optimizations. The timing capacitor (C_T) and turn on time can be adjusted to manage inrush current without adding unnecessary system delays. The output discharge resistance (QOD) can be used to adjust the output fall time. Connect the QOD pin directly to the output for a fastest fall time or leave it open for the slowest fall time.

The switch ON state is controlled by a digital input that can interface directly with low-voltage control signals. When power is first applied, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the ON pin is deliberately driven high (≥V_{IH}), the Smart Pull Down (R_{PD}) is disconnected to prevent unnecessary power loss.

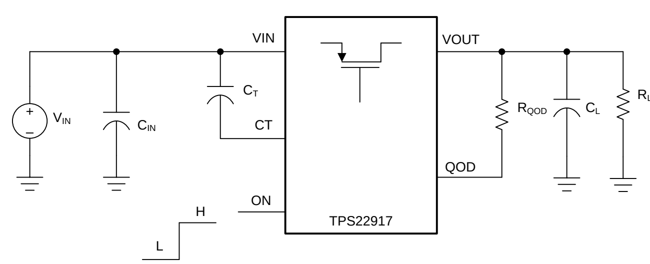
The TPS22917 device is available in a small, leaded SOT-23 package (DBV) which allows visual inspection of solder joints. The device is characterized for operation over a temperature range of –40°C to +125°C.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22917	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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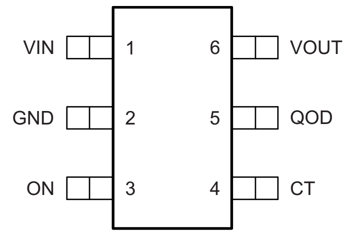
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2017) to Revision A	Page
• Changed product status from Advanced Information to Production Data	1

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input.
2	GND	—	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	CT	O	Switch slew rate control. Connect capacitor from this pin to VIN to inrease output slew rate and turn on time. Can be left floating for fastest timing.
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. • Placing an external resistor between VOUT and QOD • Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for more information.
6	VOUT	O	Switch output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{ON}	Enable voltage	–0.3	6	V
V_{QOD}	QOD pin voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		2	A
I_{PLS}	Maximum pulsed switch current, pulse < 300-µs, 2% duty cycle		2.5	A
$T_{J,MAX}$	Maximum junction temperature		125	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Maximum Lead temperature (10-s soldering time)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1	5.5	V
V_{OUT}	Output voltage	0	5.5	V
V_{IH}	High-level input voltage, ON	1	5.5	V
V_{IL}	Low-level input voltage, ON	0	0.35	V
V_{QOD}	QOD Pin Voltage	0	5.5	V
V_{CT}	Timing Capacitor Voltage Rating	7		V

6.4 Thermal Information

Thermal Parameters[1]		TPS22917 DBV (SOT-23) 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	183	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	152	°C/W
θ_{JB}	Junction-to-board thermal resistance	34	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies for all variants over the entire recommended power supply voltage range of 1 V to 5.5 V. Typical Values are at 25°C.

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP	MAX	UNIT
INPUT SUPPLY(VIN)								
$I_{Q,VIN}$	V_{IN} Quiescent current	$V_{ON} \geq V_{IH}$, V_{OUT} = Open		–40°C to +85°C		0.5	1.0	µA
				–40°C to +125°C			1.2	µA
$I_{SD,VIN}$	V_{IN} Shutdown current	$V_{ON} \leq V_{IL}$, V_{OUT} = GND		–40°C to +85°C		10	100	nA
				–40°C to +105°C			250	nA
ON-RESISTANCE(R_{ON})								
R_{ON}	ON-Resistance	I_{OUT} = 200 mA	V_{IN} = 5 V	25°C		80	100	mΩ
				–40°C to +85°C			120	
				–40°C to +105°C			130	
				–40°C to +125°C			140	
			V_{IN} = 3.6 V	25°C		90	110	
				–40°C to +85°C			140	
				–40°C to +105°C			150	
				–40°C to +125°C			160	
			V_{IN} = 1.8 V	25°C		120	150	
				–40°C to +85°C			175	
				–40°C to +105°C			185	
				–40°C to +125°C			200	
			V_{IN} = 1.2 V	25°C		170	220	
				–40°C to +85°C			265	
				–40°C to +105°C			280	
				–40°C to +125°C			300	
			VIN = 1.0 V	25°C		220	300	
				–40°C to +85°C			350	
				–40°C to +105°C			370	
				–40°C to +125°C			390	
ENABLE PIN(ON)								
I_{ON}	ON Pin leakage	$V_{ON} \geq V_{IH}$		–40°C to +125°C	–10		10	nA
R_{PD}	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$		–40°C to +105°C		750		kΩ
REVERSE CURRENT BLOCKING(RCB)								
I_{RCB}	RCB Activation Current	$V_{ON} \geq V_{IH}$, $V_{OUT} > V_{IN}$		–40°C to +125°C		-0.5	-1	A
t_{RCB}	RCB Activation time	$V_{ON} \geq V_{IH}$, $V_{OUT} > V_{IN}$ + 200mV		–40°C to +125°C		10		µs
V_{RCB}	RCB Release Voltage	$V_{ON} \geq V_{IH}$, $V_{OUT} > V_{IN}$		–40°C to +125°C		25		mV
$I_{IN,RCB}$	VIN Reverse Leakage Current	0 V ≤ $V_{IN} + V_{RCB} \leq V_{OUT}$ ≤ 5.5 V		–40°C to +105°C	–1			µA
QUICK OUTPUT DISCHARGE(QOD)								
QOD	Output discharge resistance	$V_{ON} \leq V_{IL}$		–40°C to +105°C		150		Ω

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table applies over the entire recommended power supply voltage range of 1 V to 5.5 V at 25°C with a load of C_L = 1 µF, R_L = 10 Ω

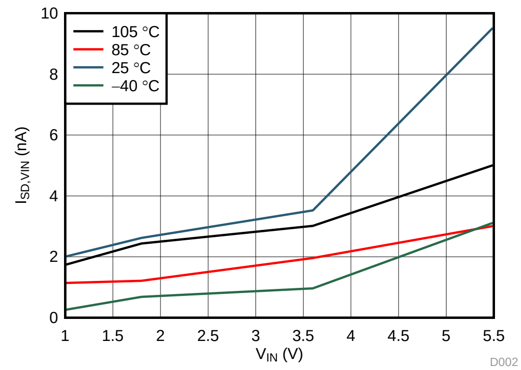
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	V_{IN} = 5.0 V	C_T = Open		100		µs
			C_T ≥ 100 pF		4		µs/pF
		V_{IN} = 3.6 V	C_T = Open		120		µs
			C_T ≥ 100 pF		3.8		µs/pF
		V_{IN} = 1.8 V	C_T = Open		200		µs
			C_T ≥ 100 pF		3.6		µs/pF
		V_{IN} = 1.2 V	C_T = Open		300		µs
			C_T ≥ 200 pF		3.4		µs/pF
		V_{IN} = 1.0 V	C_T = Open		400		µs
			C_T ≥ 400 pF		3		µs/pF
t_R	Output Rise Time	V_{IN} = 5.0 V	C_T = Open		55		µs
			C_T ≥ 100 pF		1.8		µs/pF
		V_{IN} = 3.6 V	C_T = Open		65		µs
			C_T ≥ 100 pF		1.6		µs/pF
		V_{IN} = 1.8 V	C_T = Open		100		µs
			C_T ≥ 100 pF		1.2		µs/pF
		V_{IN} = 1.2 V	C_T = Open		150		µs
			C_T ≥ 200 pF		0.95		µs/pF
		V_{IN} = 1.0 V	C_T = Open		200		µs
			C_T ≥ 400 pF		0.6		µs/pF
SR_{ON}	Turn ON Slew Rate(1)	V_{IN} = 5.0 V	C_T = Open		72		mV/µs
			C_T ≥ 100 pF		2300		(mV/µs)*pF
		V_{IN} = 3.6 V	C_T = Open		44		mV/µs
			C_T ≥ 100 pF		1900		(mV/µs)*pF
		V_{IN} = 1.8 V	C_T = Open		14		mV/µs
			C_T ≥ 100 pF		1100		(mV/µs)*pF
		V_{IN} = 1.2 V	C_T = Open		6.2		mV/µs
			C_T ≥ 200 pF		1000		(mV/µs)*pF
		V_{IN} = 1.0 V	C_T = Open		3.9		mV/µs
			C_T ≥ 400 pF		1100		(mV/µs)*pF
t_{OFF}	Turn OFF Time				10		µs
t_{FALL}	Output Fall Time(2)	R_L = 10 Ω	C_L = 1uF, R_{QOD} = Short		22		µs
		R_L = Open	C_L = 10uF, R_{QOD} = Short		3.8		ms
			C_L = 10uF, R_{QOD} = 100 Ω		5.9		ms
			C_L = 220uF, R_{QOD} = Short		72		ms

(1) SR_{ON} is the fastest Slew Rate during the turn on time (t_{ON})
(2) Output may not discharge completely if QOD is not connected to VOUT.

6.7 Typical Characteristics

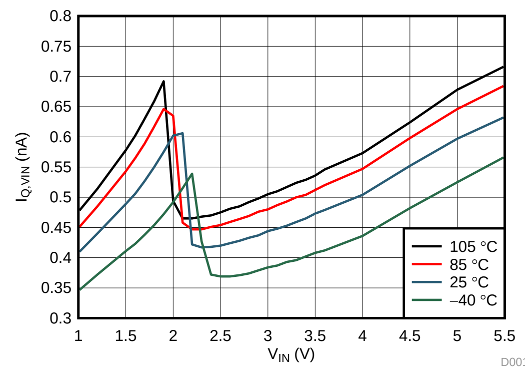
6.7.1 Typical Electrical Characteristics

The typical characteristics curves in this section apply at 25°C unless otherwise noted.



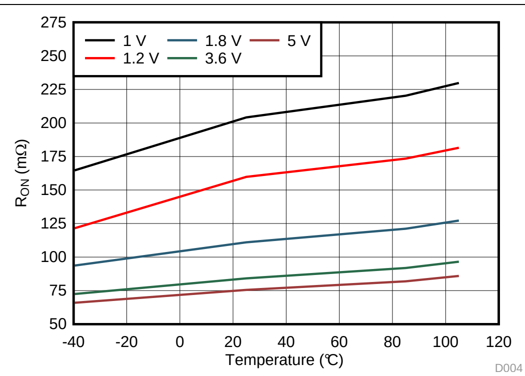
$V_{ON} \leq V_{IL}$

Figure 1. Shutdown Current (I_{SD})



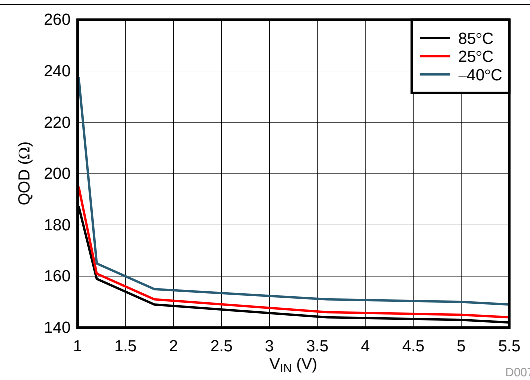
$V_{ON} \geq V_{IH}$

Figure 2. Quiescent Current (I_Q)



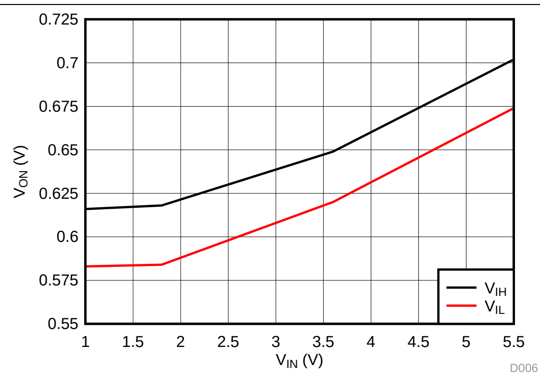
$V_{ON} \geq V_{IH}$

Figure 3. ON-Resistance (R_{ON})



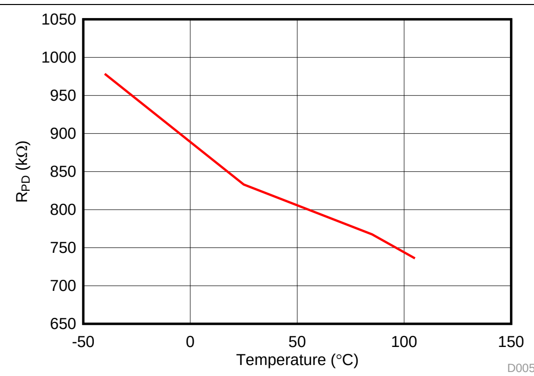
$V_{ON} \leq V_{IL}$

Figure 4. Quick Output Discharge (QOD)



–40°C to +105°C

Figure 5. ON Pin Threshold



$V_{ON} \leq V_{IL}$

Figure 6. ON Pin Smart Pull Down (R_{PD})

6.7.2 Typical Switching Characteristics

The typical data in this section apply at 25°C with a load of C_L = 1 µF, R_L = 10 Ω, and QOD shorted to VOUT unless otherwise noted.

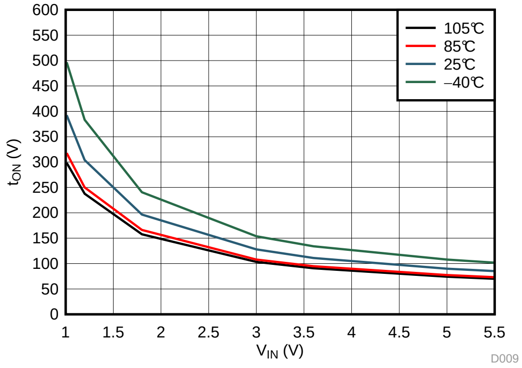


Figure 7. Turn On Time (CT = Open)

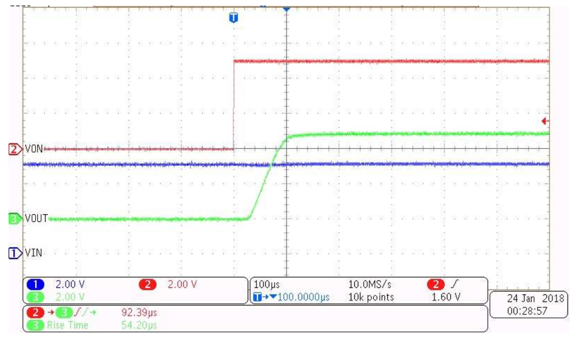


Figure 8. Turn On at 5 V (CT = Open)

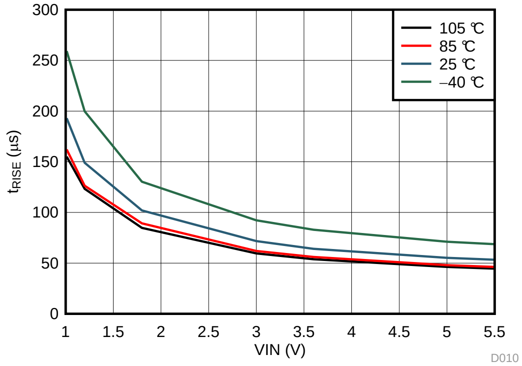


Figure 9. Rise Time (CT = Open)

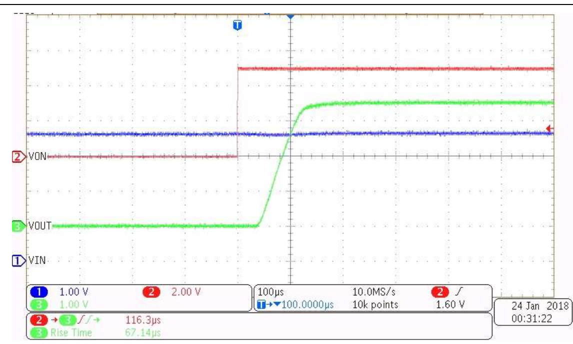


Figure 10. Turn On at 3.6 V (CT = Open)

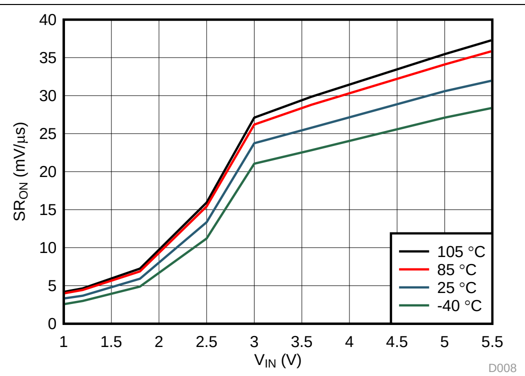


Figure 11. Slew Rate (CT = Open)

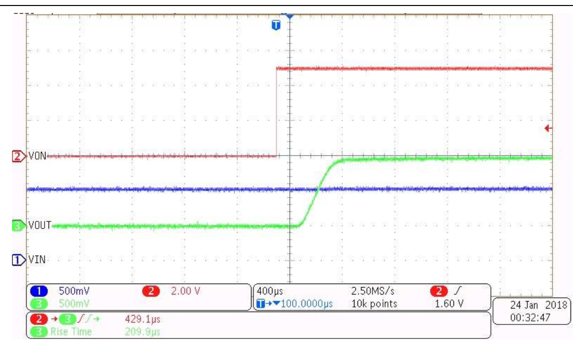


Figure 12. Turn On at 1 V (CT = Open)

Typical Switching Characteristics (continued)

The typical data in this section apply at 25°C with a load of C_L = 1 µF, R_L = 10 Ω, and QOD shorted to VOUT unless otherwise noted.

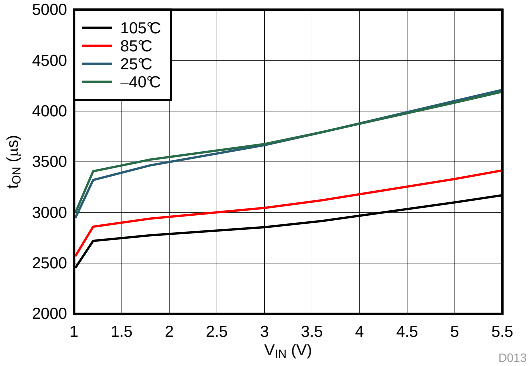


Figure 13. Turn On Time (CT = 1000 pF)

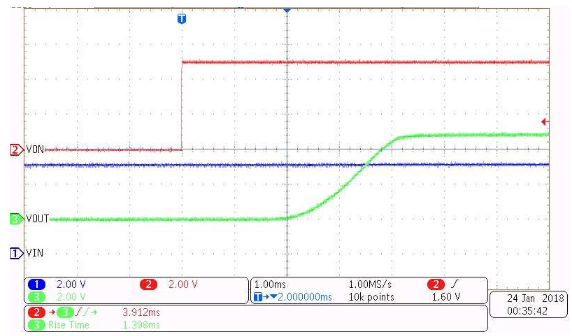


Figure 14. Turn On at 5 V (CT = 1000 pF)

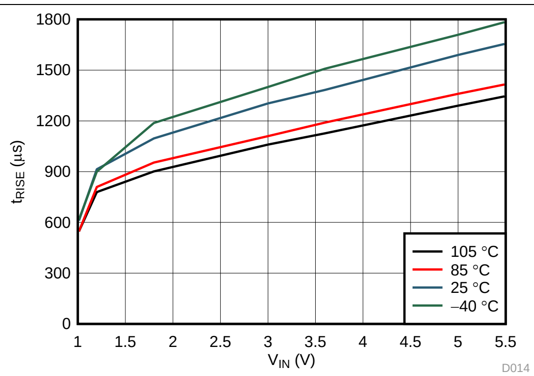


Figure 15. Rise Time (CT = 1000 pF)

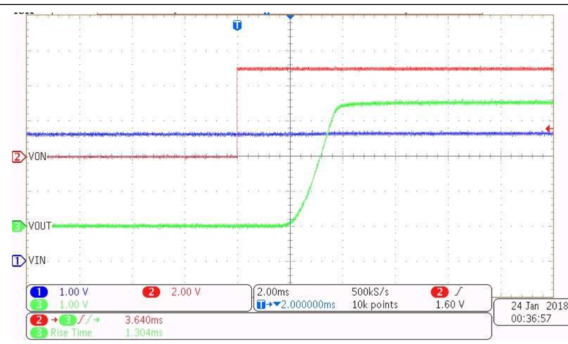


Figure 16. Turn On at 3.6 V (CT = 1000 pF)

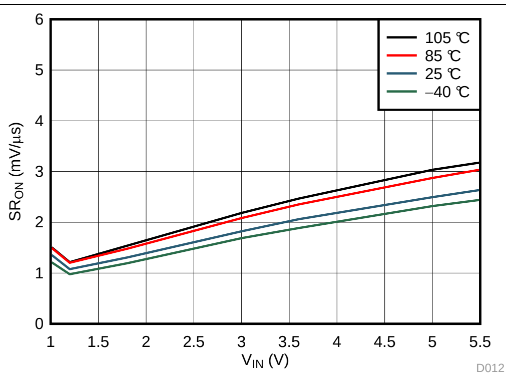


Figure 17. Slow Slew Rate (CT = 1000 pF)

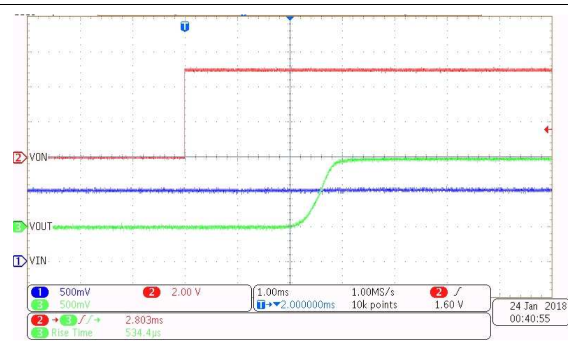
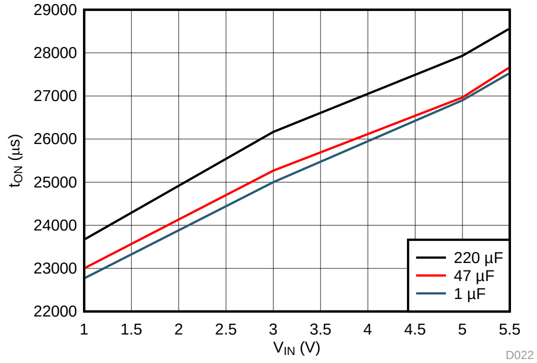


Figure 18. Turn On at 1 V (CT = 1000 pF)

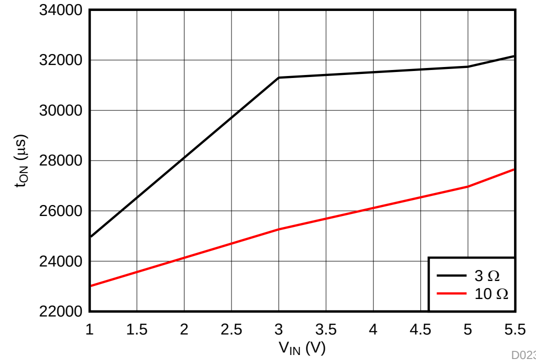
Typical Switching Characteristics (continued)

The typical data in this section apply at 25°C with a load of C_L = 1 µF, R_L = 10 Ω, and QOD shorted to VOUT unless otherwise noted.



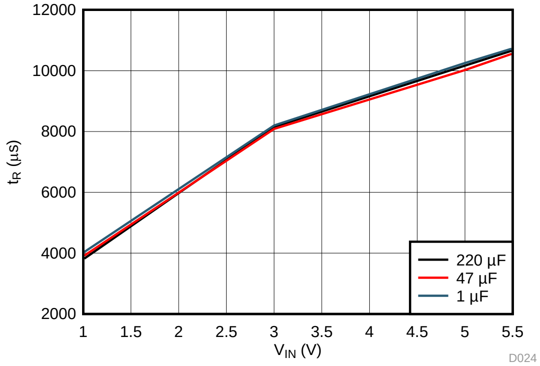
R_L = 10 Ω

Figure 19. Turn On vs Load Capacitance (CT = 10000 pF)



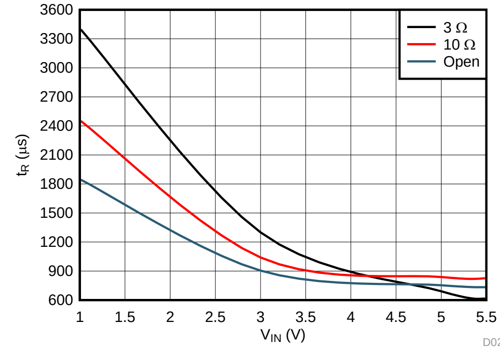
C_L = 47 µF

Figure 20. Turn On vs Load Resistance (CT = 10000 pF)



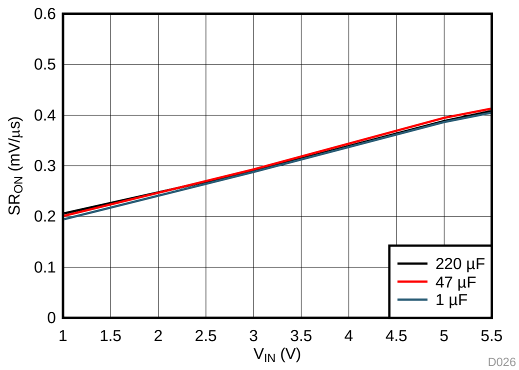
R_L = 10 Ω

Figure 21. Rise Time vs Load Capacitance (CT = 10000 pF)



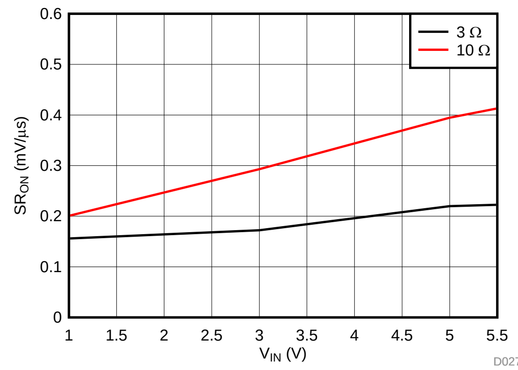
C_L = 47 µF

Figure 22. Rise Time vs Load Resistance (CT = 10000 pF)



R_L = 10 Ω

Figure 23. Slew Rate vs Load Capacitance (CT = 10000 pF)



C_L = 47 µF

Figure 24. Slew Rate vs Load Resistance (CT = 10000 pF)

Typical Switching Characteristics (continued)

The typical data in this section apply at 25°C with a load of C_L = 1 µF, R_L = 10 Ω, and QOD shorted to VOUT unless otherwise noted.

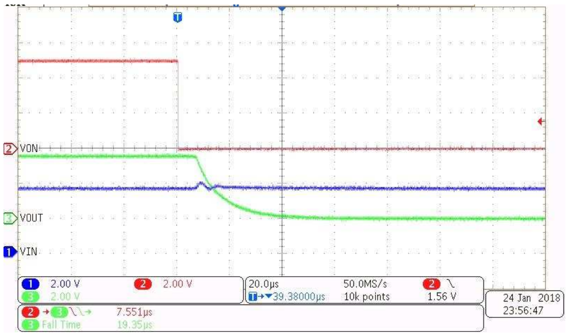
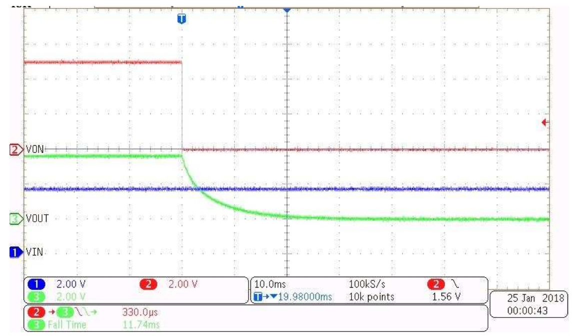
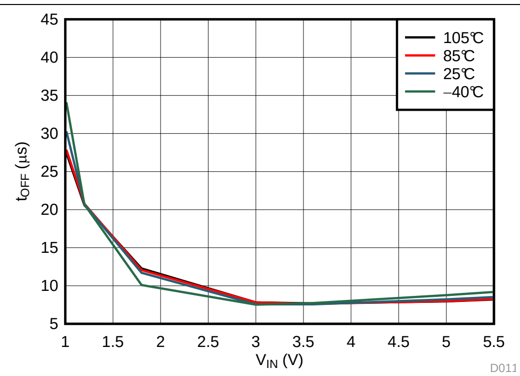


Figure 25. Turn Off at 3.6 V



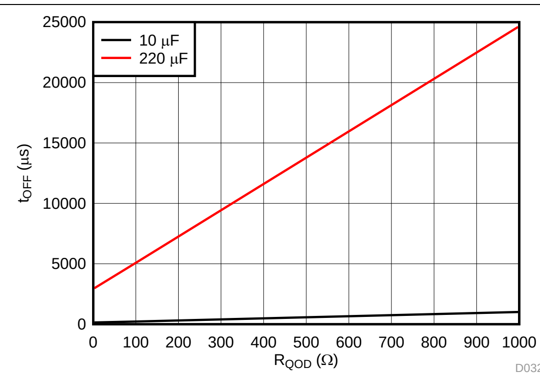
R_L = Open C_L = 47 µF

Figure 26. Turn Off at 3.6 V (Open Load)



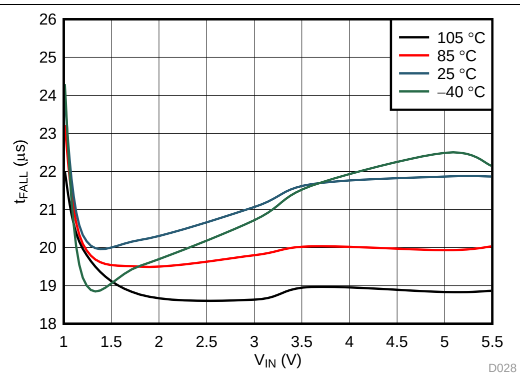
V_{IN} = 1 V to 5.5 V

Figure 27. Turn Off Time



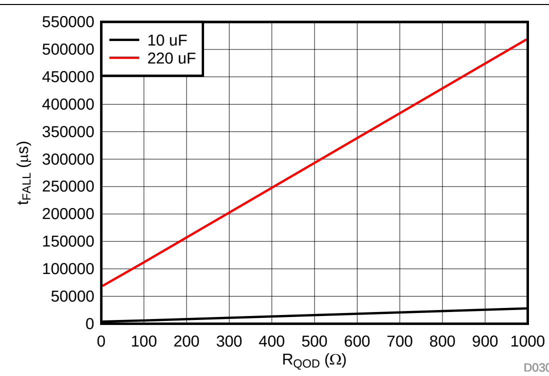
V_{IN} = 1 V to 5.5 V R_L = Open

Figure 28. Turn Off Time (Open Load)



V_{IN} = 1 V to 5.5 V

Figure 29. Fall Time

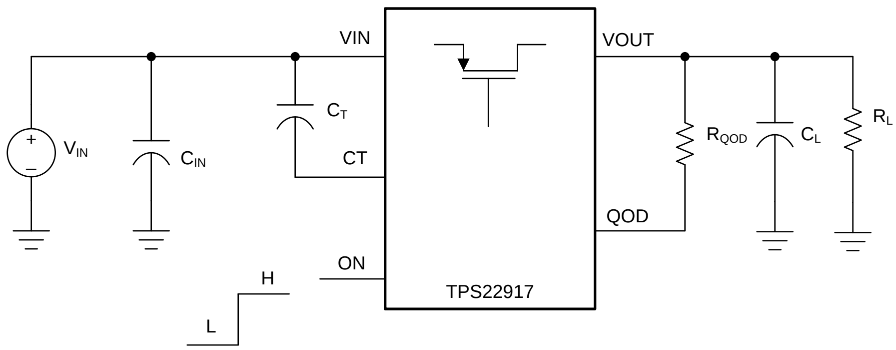


V_{IN} = 1 V to 5.5 V R_L = Open

Figure 30. Fall Time (Open Load)

7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams



(1) Rise and fall times of the control signal are 100 ns

(2) Turn-off times and fall times are dependent on the time constant at the load. For TPS22917, the internal pull-down resistance QOD is enabled when the switch is disabled. The time constant is (R_{QOD} + QOD || R_L) × C_L.

Figure 31. Test Circuit

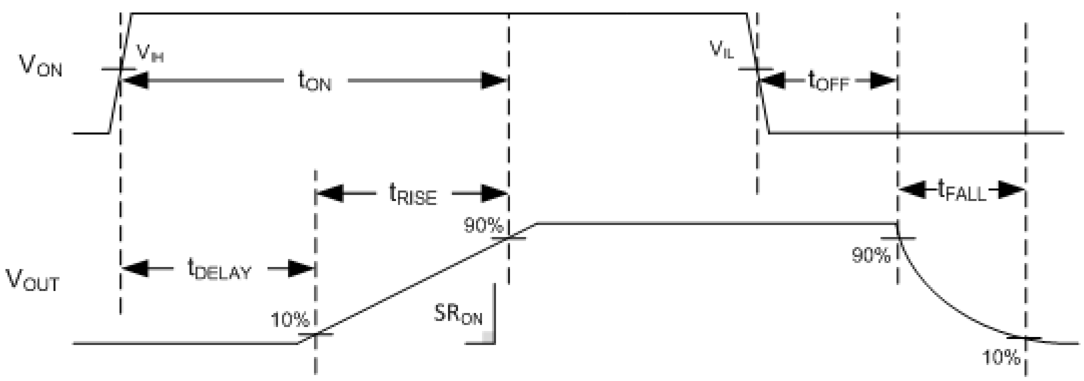


Figure 32. Timing Waveforms

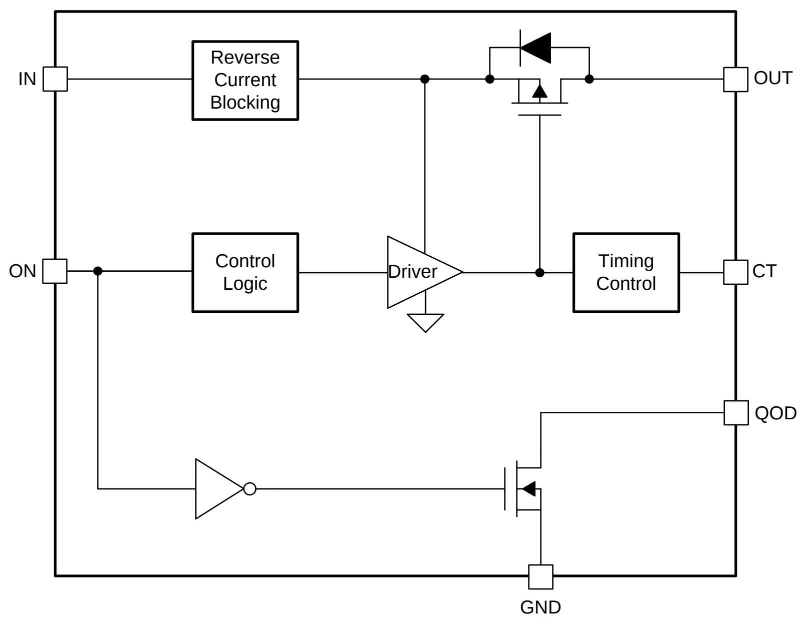
8 Detailed Description

8.1 Overview

The TPS22917 device is a 5.5-V, 2-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance P-channel MOSFET which reduces the drop out voltage across the device.

The TPS22917 device has a configurable slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pull Down is used to keep the ON pin from floating until system sequencing is complete. Once the ON pin is deliberately driven high ($\geq V_{IH}$), the Smart Pull Down is disconnected to prevent unnecessary power loss. Table 1 shown then the ON Pin Smart Pull Down is active.

Table 1. Smart-ON Pull Down

VON	Pull Down
$\leq V_{IL}$	Connected
$\geq V_{IH}$	Disconnected

8.3.2 Turn On Time (t_{ON}) and Adjustable Slew Rate (CT)

A capacitor to VIN on the CT pin sets the slew rate of V_{OUT}. The CT capacitor voltage will ramp until shortly after the switch is turned on and V_{OUT} becomes stable.

Leaving the CT pin open will result in the highest slew rate and fastest turn on time. These values can be found in the Switching Characteristics Table. For slower slew rates the required CT capacitor can be found using Equation 1:

$$CT = (\text{Slew Rate}) \div SR_{ON}$$

where

- Slew Rate = Desired slew rate (mV/us)
- CT = The capacitance value on the CT pin (pF)
- SR_{ON} = Slew Rate Constant from Table ((mV/µs) × pF) (1)

The total turn on time has a direct correlation to the output slew rate. The fastest turn on times (t_{ON}), with CT pin open, can be found in the Switching Characteristics. For slower slew rates, the resulting turn on time can be found with Equation 2:

$$\text{Turn On time} = CT \times t_{ON}$$

where

- Turn On Time = Total Time from Enable until V_{OUT} rises to 90% of V_{IN} (µs)
- CT = The capacitance value on the CT pin (pF)
- t_{ON} = Turn On Time Constant (µs/pF) (2)

8.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22917 device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance QOD.
- QOD pin connected to VOUT pin using an external resistor R_{QOD}. After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, Equation 3 can be used:

  $$R_{DIS} = QOD + R_{QOD}$$

  Where:

  - R_{DIS} = Total output discharge resistance (Ω)
  - QOD = Internal pulldown resistance (Ω)
  - R_{QOD} = External resistance placed between the VOUT and QOD pins (Ω) (3)
- QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality, and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_L). To calculate the approximate fall time of V_{OUT} use Equation 4.

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L$$

Where:

- t_{FALL} = Output Fall Time from 90% to 10% (µs)
- R_{DIS} = Total QOD + R_{QOD} Resistance (Ω)
- R_L = Output Load Resistance (Ω)
- C_L = Output Load Capacitance (µF) (4)

8.3.3.1 QOD when System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN}. Past a certain V_{IN} level, the strength of the R_{PD} will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the *Setting Fall Time for Shutdown Power Sequencing* section.

8.4 Full-Time Reverse Current Blocking

In a scenario where the device is enabled and V_{OUT} is greater than V_{IN} there is potential for reverse current to flow through the pass FET or the body diode. When the reverse current threshold (I_{RCB}) is exceeded, the switch is disabled within t_{RCB}. The Switch will remain off and block reverse current as long as the reverse voltage condition exists. Once V_{OUT} has dropped below the V_{RCB} release threshold the device will turn back on with slew rate control.

8.5 Device Functional Modes

Table 2 describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

Table 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22917 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND (via QOD + R_{QOD})
L	QOD pin tied to VOUT directly	GND (via QOD)
L	QOD pin left open	Floating
H	N/A	VIN

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22917 device can be used to power downstream modules.

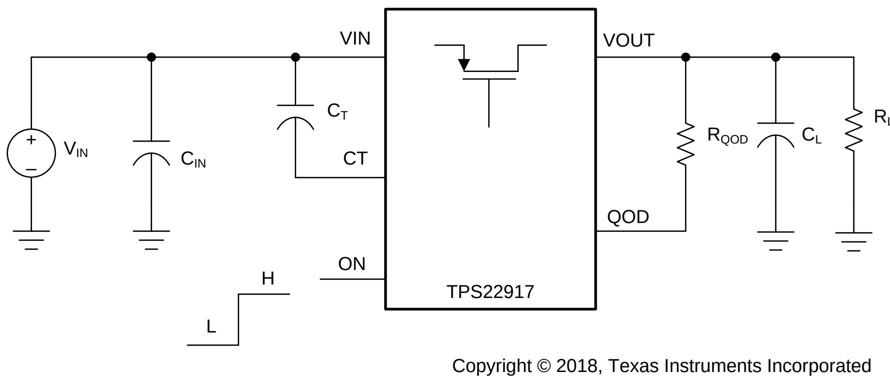


Figure 33. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Table 3 as the design parameters:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	3.6 V
Load Current / Resistance (R_L)	1 kΩ
Load Capacitance (C_L)	47 µF
Minimum Fall Time (t_F)	40 ms
Maximum Inrush Current (I_{RUSH})	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use Equation 5 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$(\text{Slew Rate}) = I_{RUSH} \div C_L$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_L = capacitance on VOUT (μF)
- Slew Rate = Output Slew Rate during turn on (mV/μs) (5)

Once the required slew rate shown in Equation 1 can be used to find the minimum CT capacitance

$$CT = SR_{ON} \div (\text{Slew Rate}) \quad (6)$$

$$CT = 1900 \div 3.2 = 594 \text{ pF} \quad (7)$$

To ensure an inrush current of less than 150 mA, choose a CT value greater than 594 pF. An appropriate value should be placed on such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

9.2.2.2 Application Curves

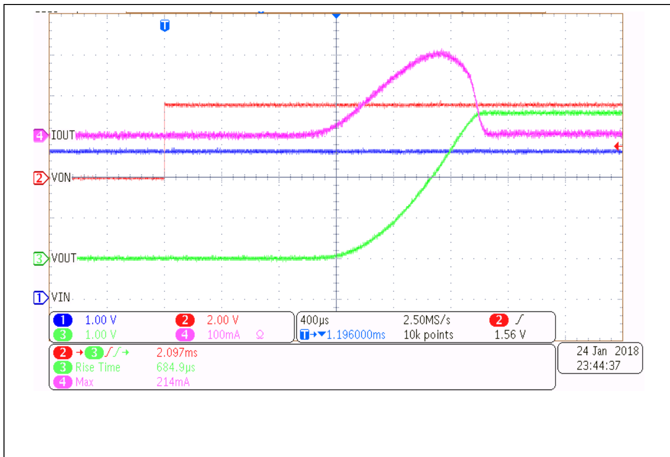


Figure 34. Inrush Current (CT = 470 pF)

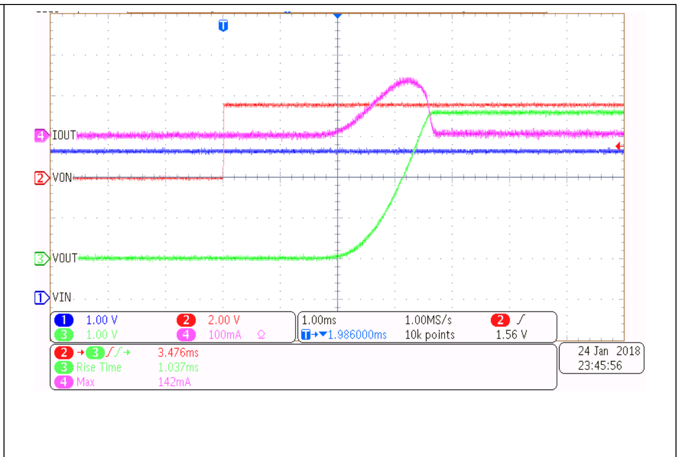


Figure 35. Inrush Current (CT = 1000 pF)

9.2.2.3 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22917, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using Equation 4:

$$t_{FALL} = 2.2 \times (R_{DIS} \,||\, R_L) \times C_L \quad (8)$$

$$R_{DIS} = 630\ \Omega \quad (9)$$

Equation 3 can then be used to calculate the R_{QOD} resistance needed to acheive a particular discharge value:

$$R_{DIS} = QOD + R_{QOD} \quad (10)$$

$$R_{QOD} = 480\ \Omega \quad (11)$$

To ensure a fall time greater than, choose an R_{QOD} value greater than 480 Ω.

9.2.2.4 Application Curves

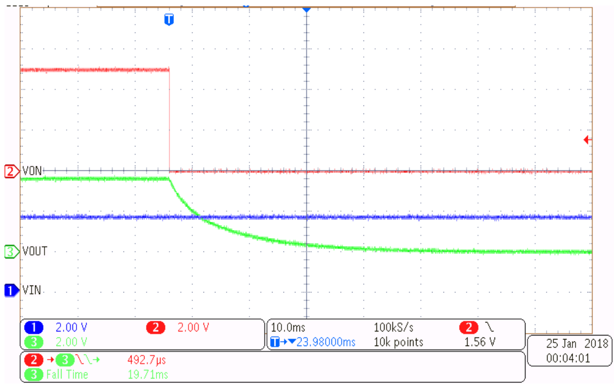


Figure 36. Fall Time (R_{QOD} = 100 Ω)

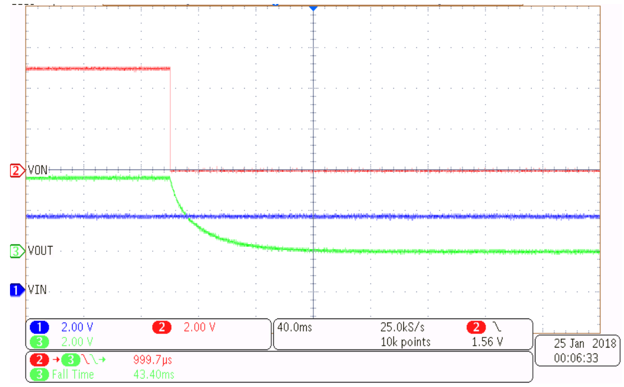


Figure 37. Fall Time (R_{QOD} = 1 kΩ)

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 µF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

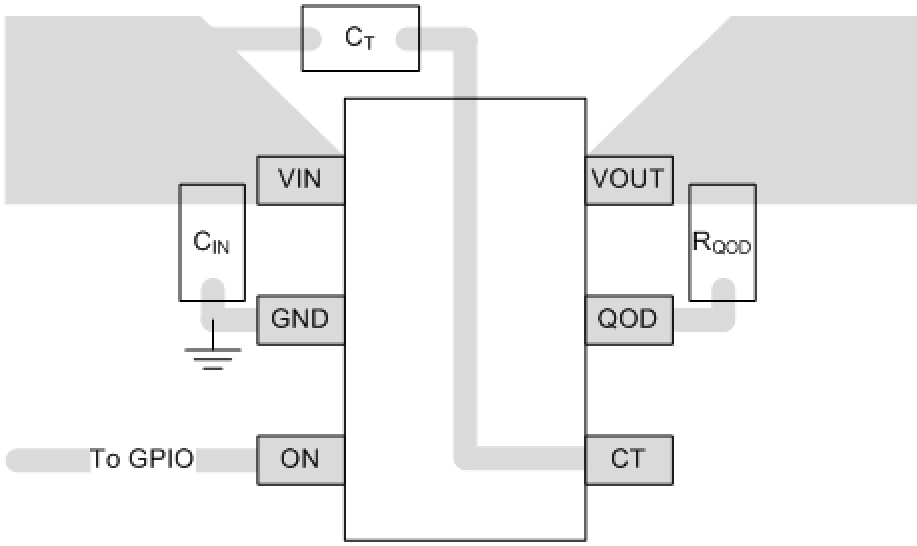


Figure 38. Recommended Board Layout

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use Equation 12:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22917)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the table. This parameter is highly dependent upon board layout. (12)

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22917DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1IAF	Samples
TPS22917DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1IAF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

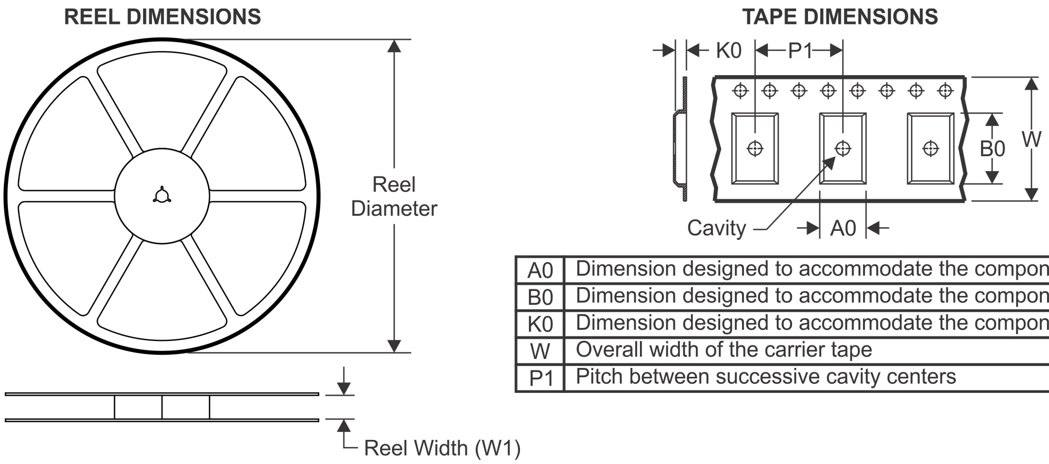
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

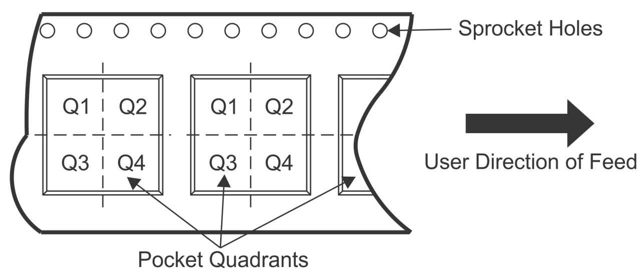
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

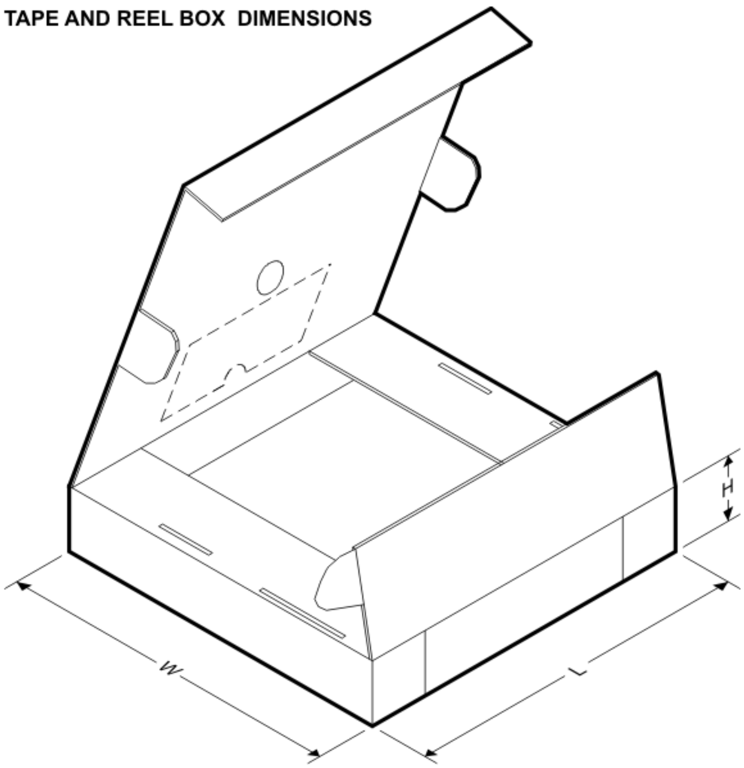
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22917DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS22917DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



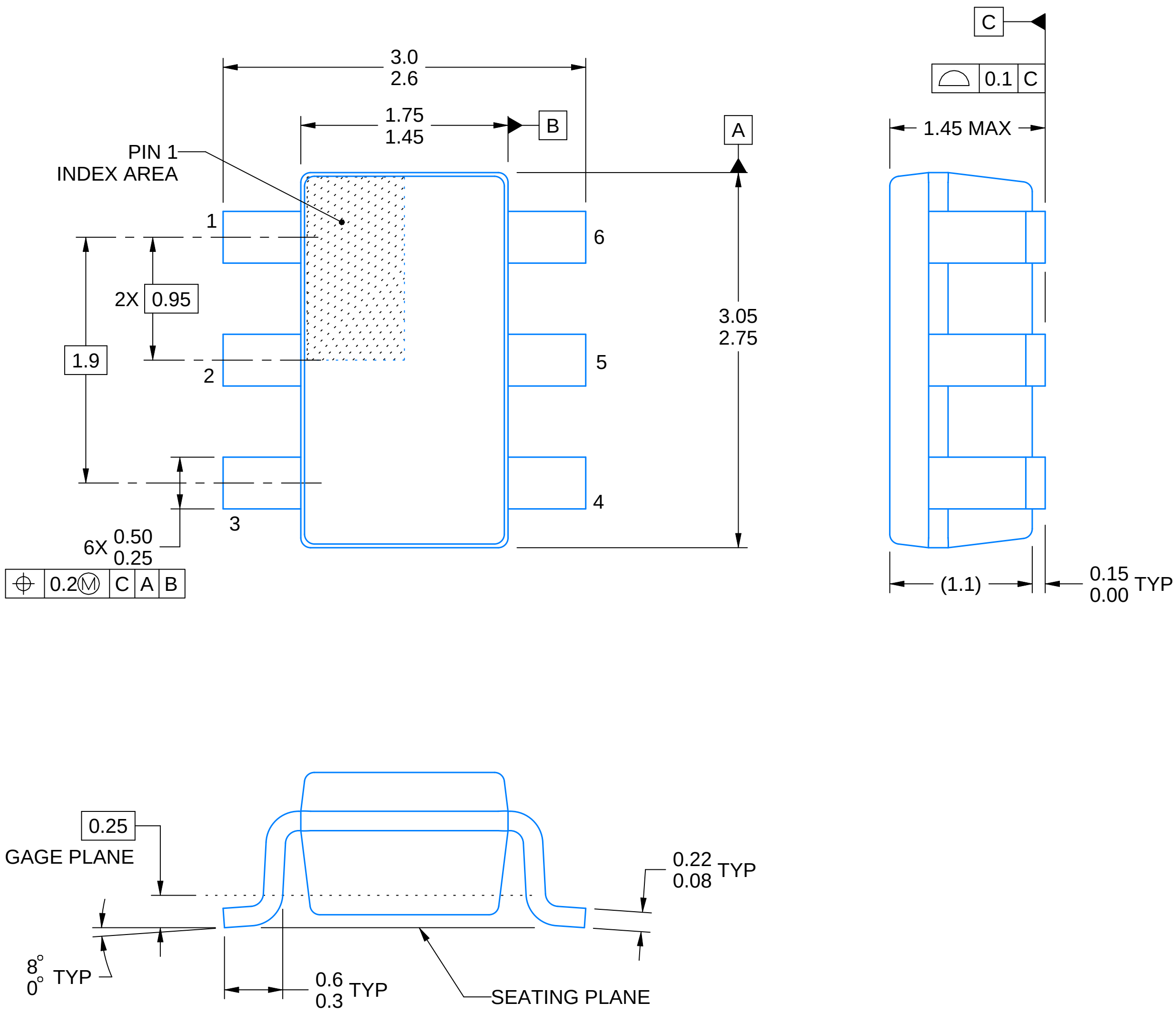
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22917DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS22917DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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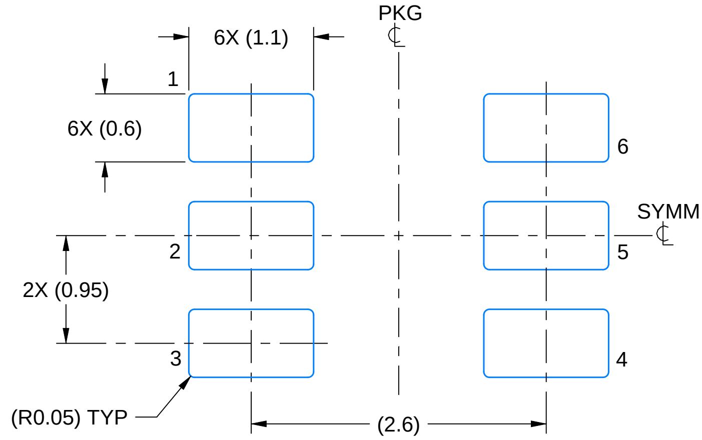
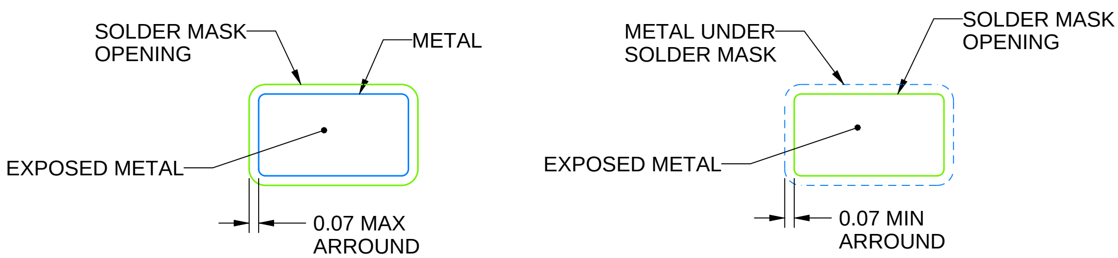
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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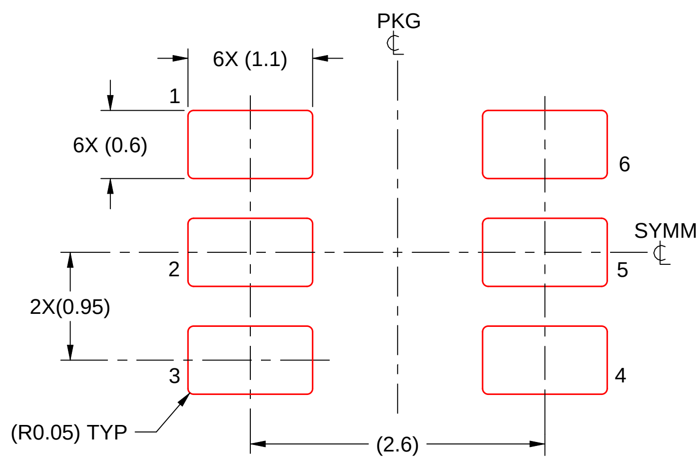
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.