Unitrode Products
from Texas Instruments

application INFO available

UC1842A/3A/4A/5A
UC2842A/3A/4A/5A
UC3842A/3A/4A/5A

Current Mode PWM Controller

FEATURES

- Optimized for Off-line and DC to DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low RO Error Amp

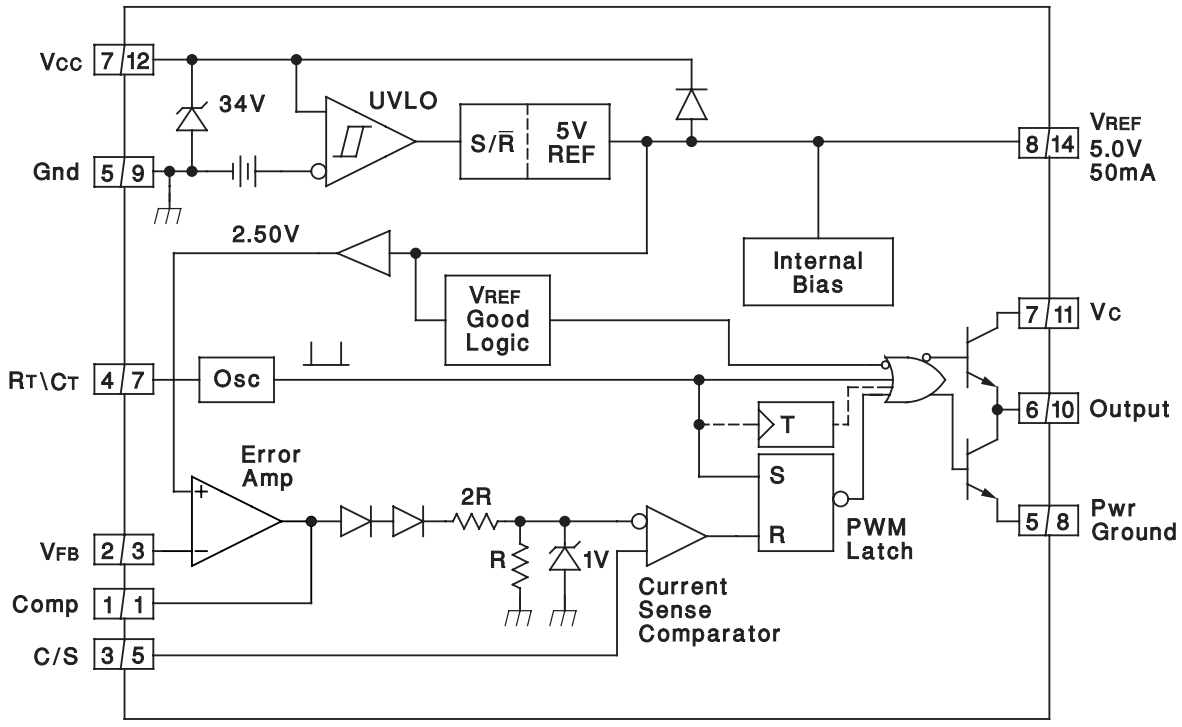
DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for VCC over 5V.

The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844A and 1845A.

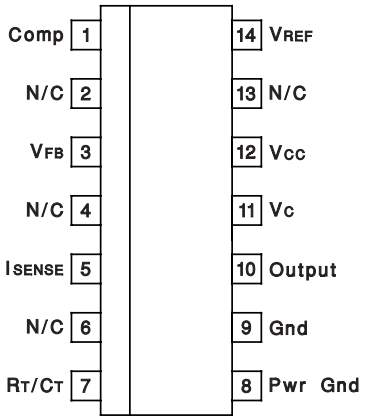
CONNECTION DIAGRAMS

ABSOLUTE MAXIMUM RATINGS (Note 1)

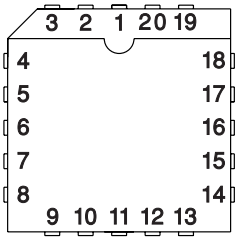
Supply Voltage (Low Impedance Source) 30V
Supply Voltage (I_{CC} mA) . . . . . Self Limiting
Output Current. . . . . ±1A
Output Energy (Capacitive Load). 5µJ
Analog Inputs (Pins 2, 3). . . . . -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Storage Temperature Range. . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only.

SOIC-14 (TOP VIEW)
D Package

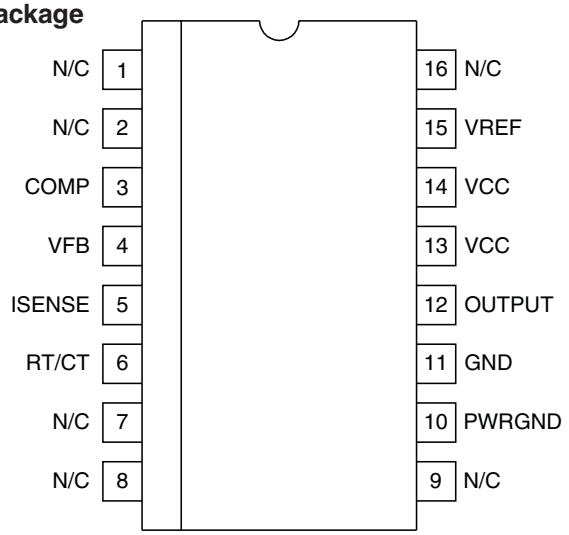


PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages

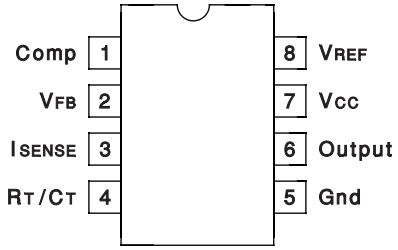


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Comp	2
N/C	3-4
V_{FB}	5
N/C	6
I_{SENSE}	7
N/C	8-9
R_T/C_T	10
N/C	11
Pwr Gnd	12
Gnd	13
N/C	14
Output	15
N/C	16
V_C	17
V_{CC}	18
N/C	19
V_{REF}	20

SOIC-WIDE16 (TOP VIEW)
DW Package



DIL-8, SOIC-8 (TOP VIEW)
J or N, D8 Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ 125°C for the UC184xA; –40°C ≤ T_A ≤ 125°C for the UC284xAQ; –40°C ≤ T_A ≤ 85°C for the UC284xA; 0 ≤ T_A ≤ 70°C for the UC384xA; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF; T_A = T_J; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{IN} 25V		6	20		6	20	mV
Load Regulation	1 ≤ I_O ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz T_J = 25°C (Note 2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak (Note 2)		1.7			1.7		V
Discharge Current	T_J = 25°C, $V_{PIN\ 4}$ = 2V (Note 8)	7.8	8.3	8.8	7.8	8.3	8.8	mA
	$V_{PIN\ 4}$ = 2V (Note 8)	7.5		8.8	7.6		8.8	mA
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	T_J = 25°C (Note 2)	0.7	1		0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3V, R_L = 15k to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7V, R_L = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25V (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	$V_{PIN\ 3}$ = 0 to 2V (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		15	2.2		15	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
UVLO Saturation	V_{CC} = 5V, I_{SINK} = 10mA		0.7	1.2		0.7	1.2	V

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PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After	x842A/4A	9	10	11	8.5	10	11.5	V
Turn On	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0V		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA	30	34		30	34		V

Note 2: *Ensured by design, but not 100% production tested.*
Note 3: *Parameter measured at trip point of latch with V_{PIN2} = 0.*
Note 4: *Gain defined as: $A = \frac{\Delta VPIN\ 1}{\Delta VPIN\ 3}$; 0 ≤ $V_{PIN\ 3}$ ≤ 0.8V.*

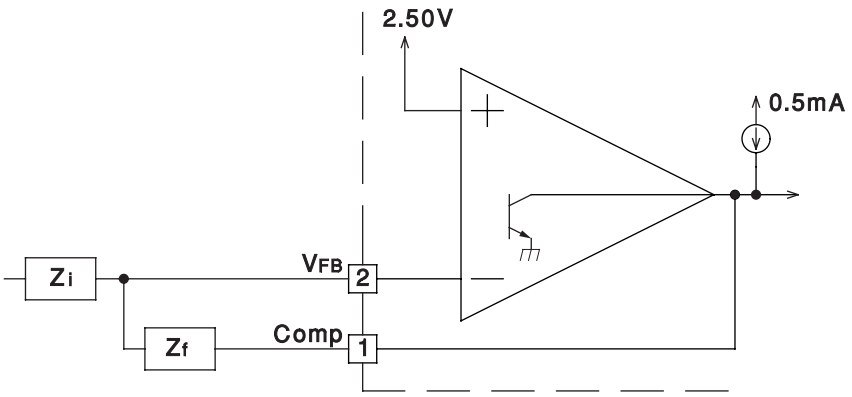
Note 5: *Adjust V_{CC} above the start threshold before setting at 15V.*
Note 6: *Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.*
Note 7: *"Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:*

$$Temp\ Stability = \frac{VREF\ (max) - VREF\ (min)}{TJ\ (max) - TJ\ (min)}$$

. V_{REF} (max) and V_{REF} (min) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

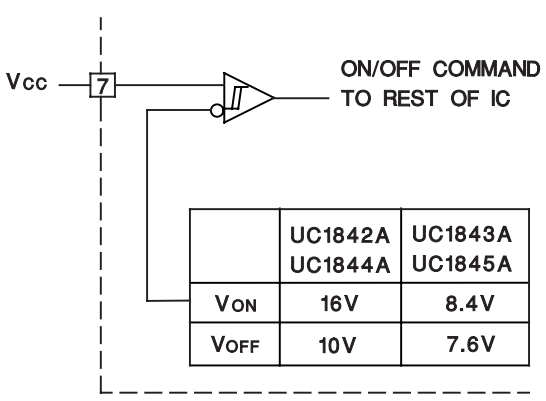
Note 8: *This parameter is measured with R_T = 10kΩ to V_{REF}. This contributes approximately 300μA of current to the measurement. The total current flowing into the R_T/C pin will be approximately 300μA higher than the measured value.*

Error Amp Configuration

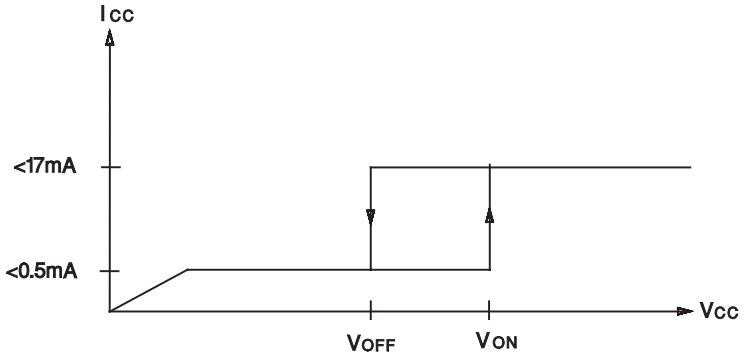


Error Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Under-Voltage Lockout

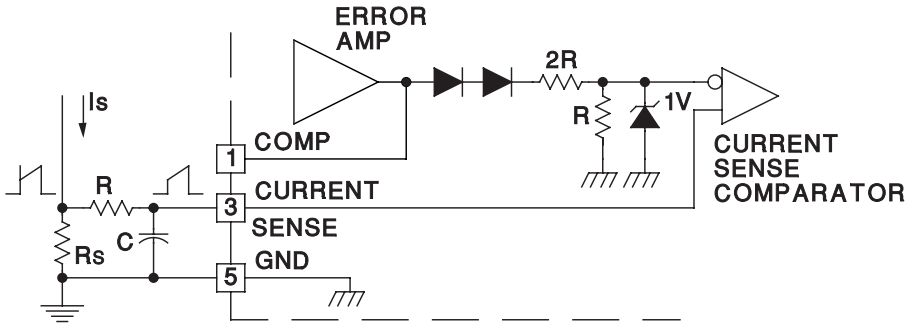


	UC1842A UC1844A	UC1843A UC1845A
VON	16V	8.4V
VOFF	10V	7.6V



During UVLO, the Output is low.

Current Sense Circuit

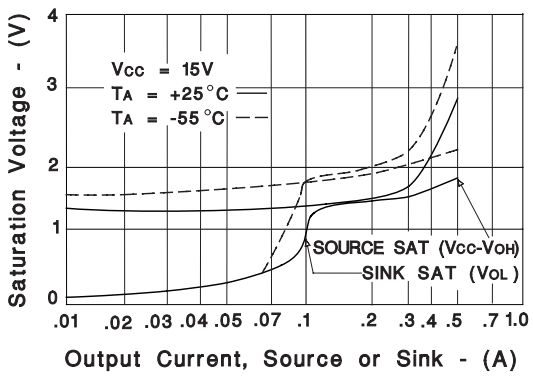


Peak Current (Is) is Determined By The Formula

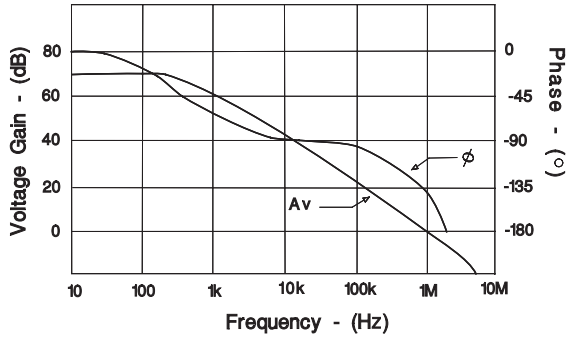
$$I_{SMAX} \approx \frac{1.0V}{RS}$$

A small RC filter may be required to suppress switch transients.

Output Saturation Characteristics

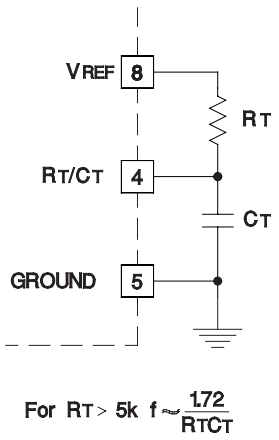


Error Amplifier Open-Loop Frequency Response

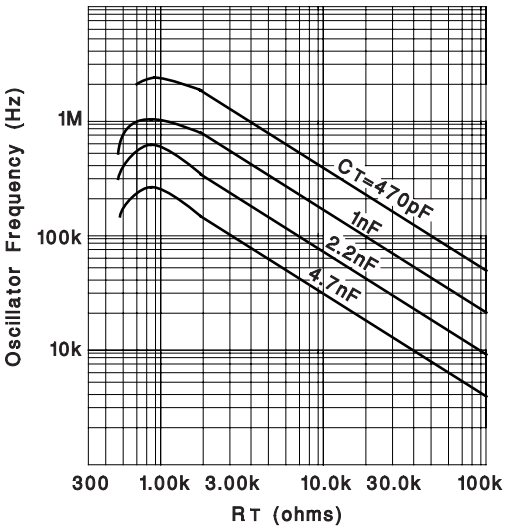


APPLICATIONS DATA (cont.)

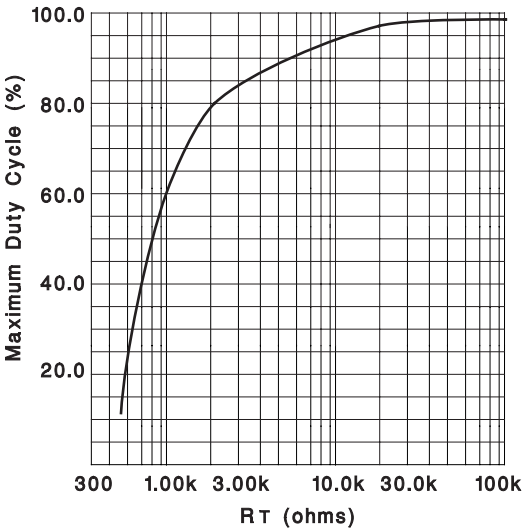
Oscillator Section



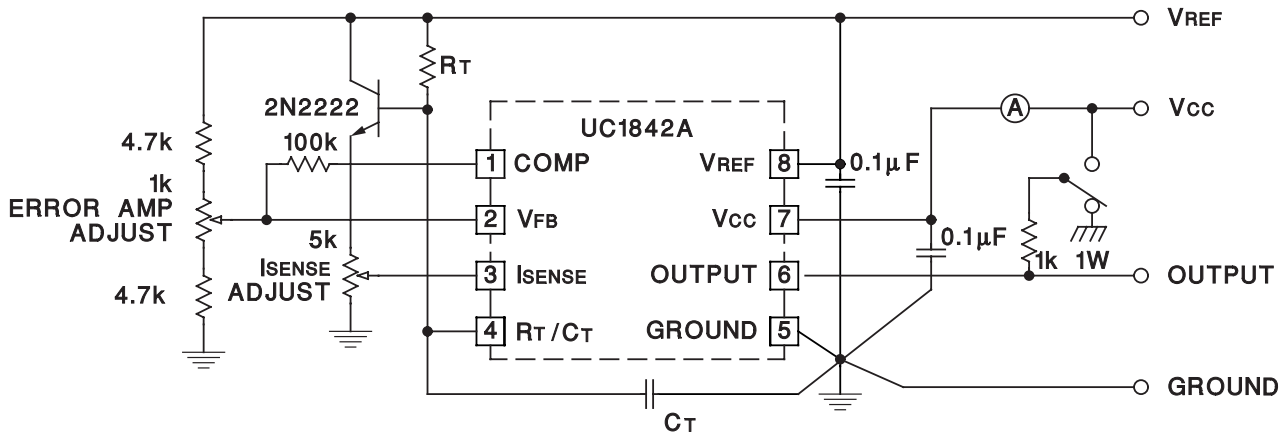
Oscillator Frequency vs Timing Resistance



Maximum Duty Cycle vs Timing Resistor

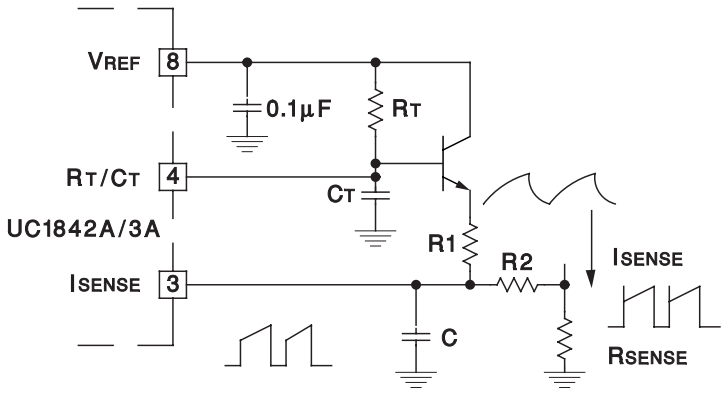


Open-Loop Laboratory Test Fixture



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

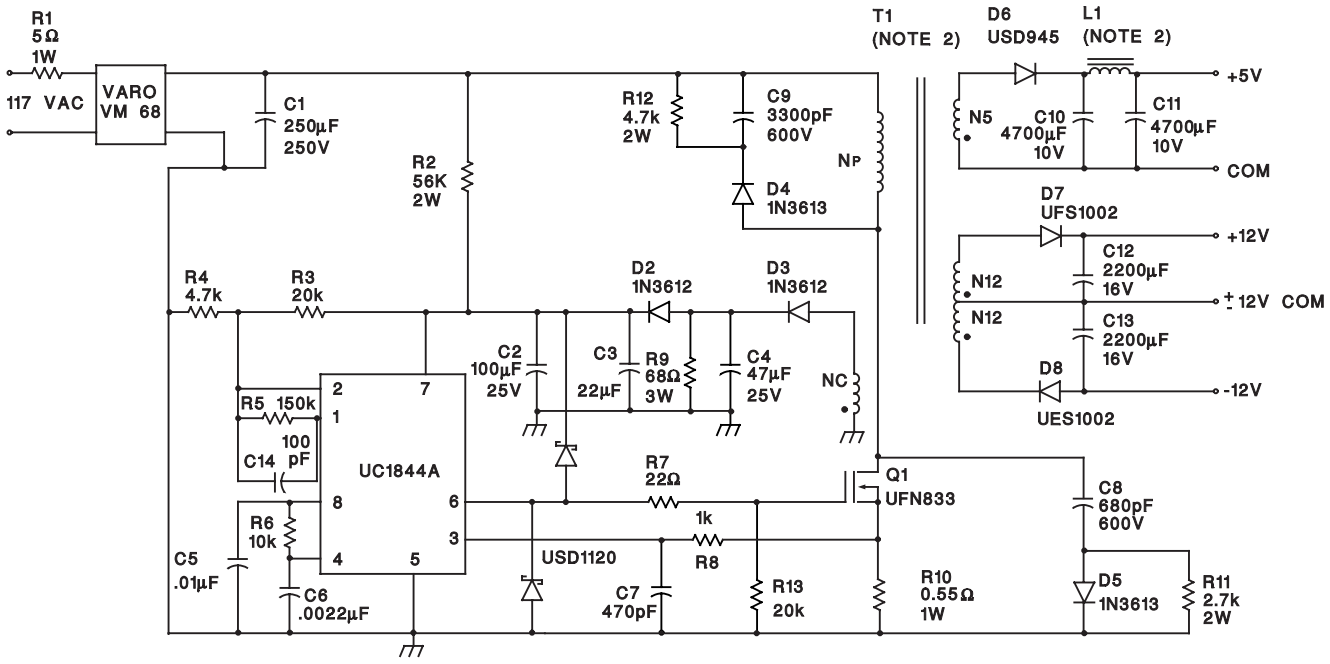
Slope Compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

APPLICATIONS DATA (cont.)

Off-line Flyback Regulator



Power Supply Specifications

1. Input Voltage		*95VAC to 130VA (50 Hz/60Hz)*
2. Line Isolation		*3750V*
3. Switching Frequency		*40kHz*
4. Efficiency	*Full Load*	*70%*

5. Output Voltage:
A. +5V, ±5%; 1A to 4A load
Ripple voltage: 50mV P-P Max
B. +12V, ±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max
C. -12V ,±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max