

NM93C46

1K-Bit Serial CMOS EEPROM (MICROWIRE™ Bus Interface)

General Description

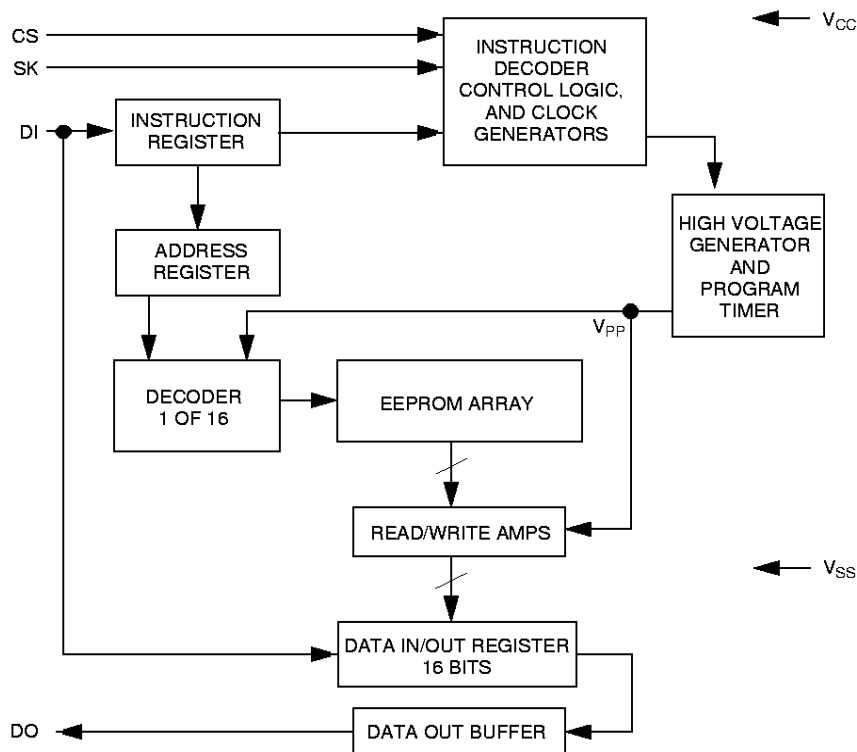
The NM93C46 devices are 1024 bits of CMOS non-volatile electrically erasable memory divided into 64 16-bit registers. They are fabricated using Fairchild Semiconductor's floating-gate CMOS process for high reliability, high endurance and low power consumption. These memory devices are available in an 8-pin SOIC or 8-pin TSSOP package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions which control this device: Read, Write Enable, Erase, Erase All, Write, Write All, and Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Device status during programming mode
- Typical active current of 200µA
10µA standby current typical
1µA standby current typical (L)
0.1µA standby current typical (LZ)
- No erase required before write
- Reliable CMOS floating gate technology
- 2.7V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Block Diagram



DS500080-1

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	NM93C46	0°C to +70°C
	NM93C46E	-40°C to +85°C
	NM93C46V	-40°C to +125°C
Power Supply (V _{CC})		4.5V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I _{CCA}	Operating Current		CS = V _{IH} , SK = 1MHz		1	mA
I _{CCS}	Standby Current		CS = V _{IL}		50	μA
I _{IL} I _{OL}	Input Leakage Output Leakage		V _{IN} = 0V to V _{CC} (Note 2)		±1	μA
V _{IL} V _{IH}	Input Low Voltage Input High Voltage			-0.1 2	0.8 V _{CC} +1	V
V _{OL1} V _{OH1}	Output Low Voltage Output High Voltage		I _{OL} = 2.1mA I _{OH} = -400 μA	2.4	0.4	V
V _{OL2} V _{OH2}	Output Low Voltage Output High Voltage		I _{OL} = 10 μA I _{OH} = -10 μA	V _{CC} -0.2	0.2	V
f _{SK}	SK Clock Frequency		(Note 3)	0	1	MHz
t _{SKH}	SK High Time	NM93C46 NM93C46E/V		250 300		ns
t _{SKL}	SK Low Time			250		ns
t _{SKS}	SK Setup Time		SK must be at V _{IL} for t _{SKS} before CS goes high	50		ns
t _{CS}	Minimum CS Low Time		(Note 4)	250		ns
t _{CSS}	CS Setup Time			50		ns
t _{DH}	DO Hold Time			70		ns
t _{DIS}	DI Setup Time	NM93C46 NM93C46E/V		100 200		ns
t _{CSH}	CS Hold Time			0		ns
t _{DIH}	DI Hold Time			20		ns
t _{PD1}	Output Delay to "1"				500	ns
t _{PD0}	Output Delay to "0"				500	ns
t _{SV}	CS to Status Valid				500	ns
t _{DF}	CS to DO in TRI-STATE		CS = V _{IL}		100	ns
t _{WP}	Write Cycle Time				10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	NM93C46L/LZ	0°C to +70°C
	NM93C46LE/LZE	-40°C to +85°C
	NM93C46LV/LZV	-40°C to +125°C
Power Supply (V _{CC})		2.7V to 4.5V

Low V_{CC} (2.7V to 4.5V) DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min.	Max.	Units
I _{CCA}	Operating Current		CS = V _{IH} , SK = 250KHz		1	mA
I _{CCS}	Standby Current		CS = V _{IL}		10	μA
	L				1	μA
	LZ					
I _{IL}	Input Leakage		V _{IN} = 0V to V _{CC}		±1	μA
I _{OL}	Output Leakage		(Note 2)			
V _{IL}	Input Low Voltage			-0.1	0.15 V _{CC}	V
V _{IH}	Input High Voltage			0.8 V _{CC}	V _{CC} + 1	V
V _{OL}	Output Low Voltage		I _{OL} = 10 μA		0.1 V _{CC}	V
V _{OH}	Output High Voltage		I _{OH} = -10 μA	0.9 V _{CC}		V
f _{SK}	SK Clock Frequency		(Note 3)	0	250	KHz
t _{SKH}	SK High Time			1		μs
t _{SKL}	SK Low Time			1		μs
t _{SKS}	SK Setup Time		SK must be at V _{IL} for t _{SKS} before CS goes high	0.2		μs
t _{CS}	Minimum CS Low Time		(Note 4)	1		μs
t _{CSS}	CS Setup Time			0.2		μs
t _{DH}	DO Hold Time			70		ns
t _{DIS}	DI Setup Time			0.4		μs
t _{CSH}	CS Hold Time			0		ns
t _{DIH}	DI Hold Time			0.4		μs
t _{PD1}	Output Delay to "1"				2	μs
t _{PD0}	Output Delay to "0"				2	μs
t _{SV}	CS to Status Valid				1	μs
t _{DF}	CS to DO in TRI-STATE		CS = V _{IL}		0.4	μs
t _{WP}	Write Cycle Time				15	ms

Capacitance T_A = 25°C, f = 1 MHz (Note 5)

Symbol	Test	Typ	Max	Units
C _{OUT}	Output Capacitance		5	pF
C _{IN}	Input Capacitance		5	pF

AC Test Conditions

V _{CC} Range	V _{IL} /V _{IH} Input Levels	V _{IL} /V _{IH} Timing Level	V _{OL} /V _{OH} Timing Level	I _{OL} /I _{OH}
2.7V ≤ V _{CC} ≤ 5.5V (Extended Voltage Levels)	.03V/1.8V	1.0V	0.8V/1.5V	±10μA
4.5V ≤ V _{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	-2.1mA/0.4mA

Output Load: 1 TTL Gate (C_L = 100 pF)

Note 1 Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 Typical leakage values are in the 20nA range.

Note 3 The shortest allowable SK clock period = 1/f_{SK} (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set 1/f_{SK} = t_{SKHminimum} + t_{SKLminimum} for shorter SK cycle time operation.

Note 4 CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5 This parameter is periodically sampled and not 100% tested.

Functional Description

The NM93C46 device has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Write Enable (WEN):

When V_{CC} is applied to the part, it 'powers-up' in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum time of t_{CS} . DO = logical "0" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by the address and 16 bits of data to be written into the specified address. After the last bit of data is put in the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of t_{CS} . DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

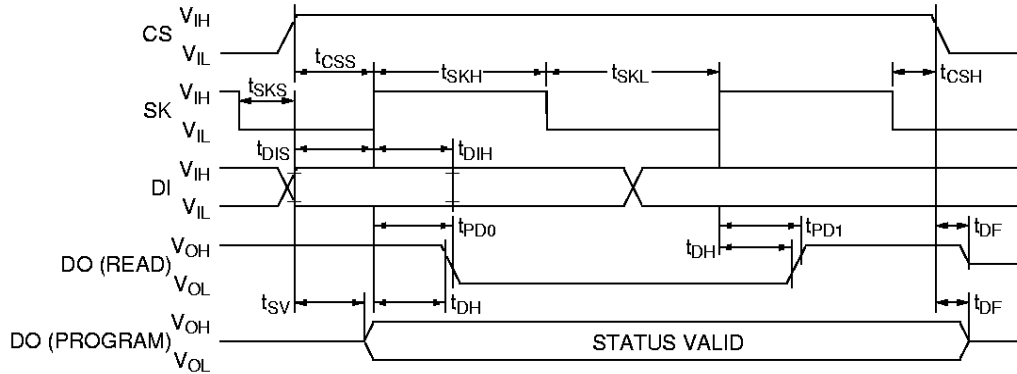
Note: The Fairchild CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C46

Instruction	SB	Op. Code	Address	Data	Comments
READ	1	10	A5-A0		Reads data stored in memory, at specified address.
WEN	1	00	11xxxx		Write enable must precede all programming modes.
ERASE	1	11	A5-A0		Erase selected register.
WRITE	1	01	A5-A0	D15-D0	Writes selected register.
ERAL	1	00	10xxxx		Erases all registers.
WRALL	1	00	01xxxx	D15-D0	Writes all registers.
WDS	1	00	00xxxx		Disables all programming instructions.

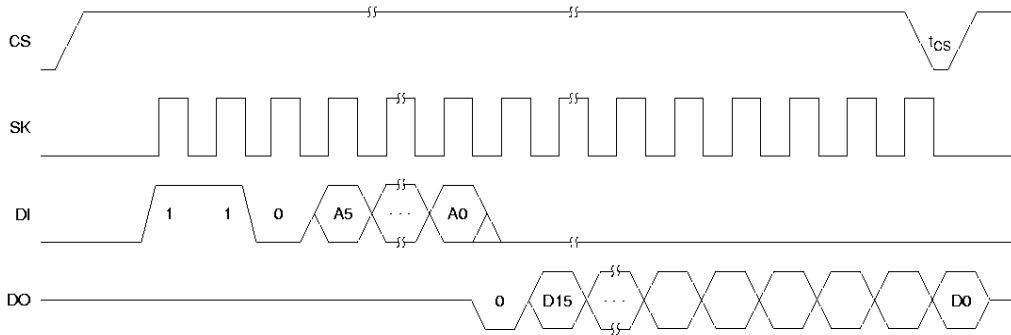
Timing Diagrams

Synchronous Data Timing



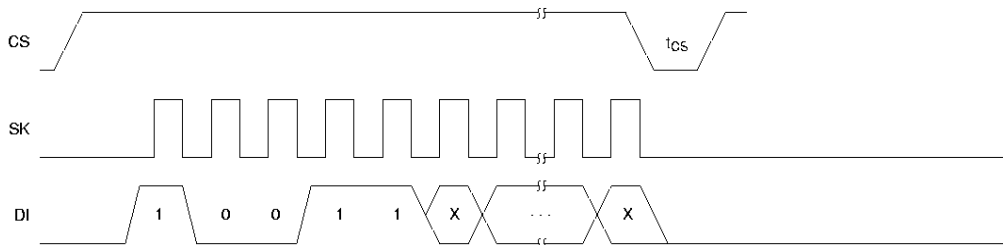
DS500080-4

READ



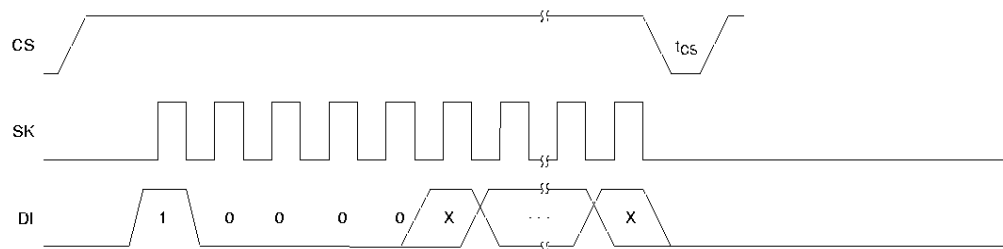
DS500080-5

WEN



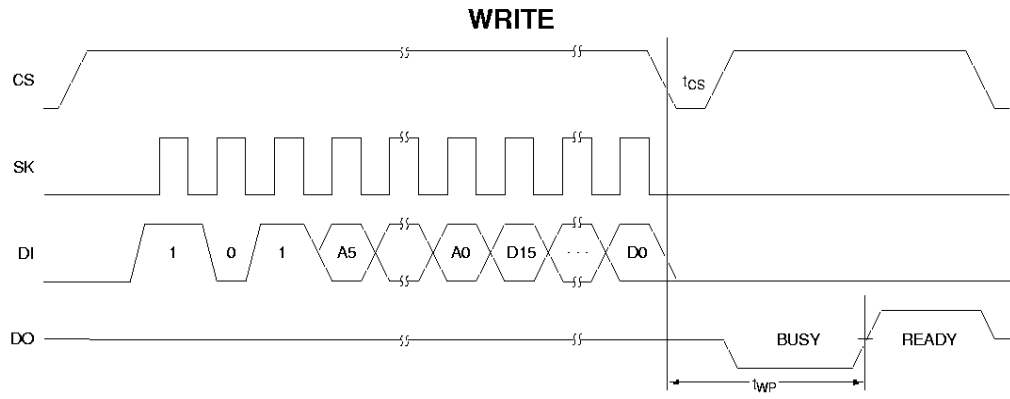
DS500080-6

WDS

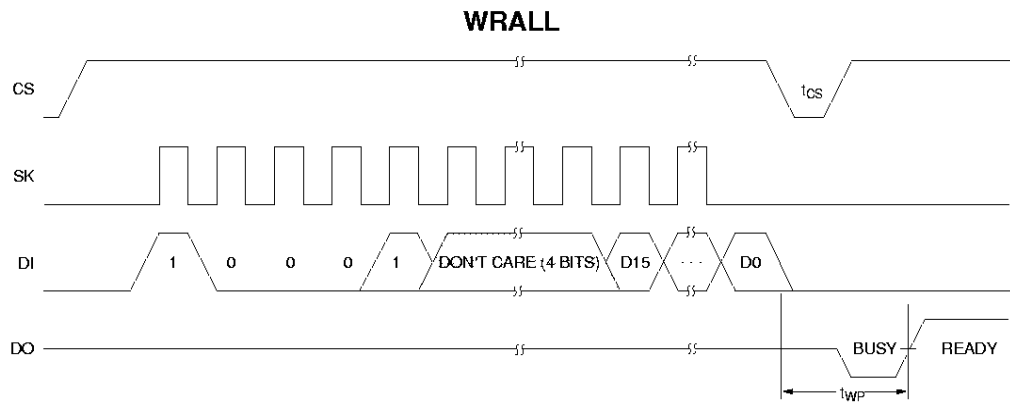


DS500080-7

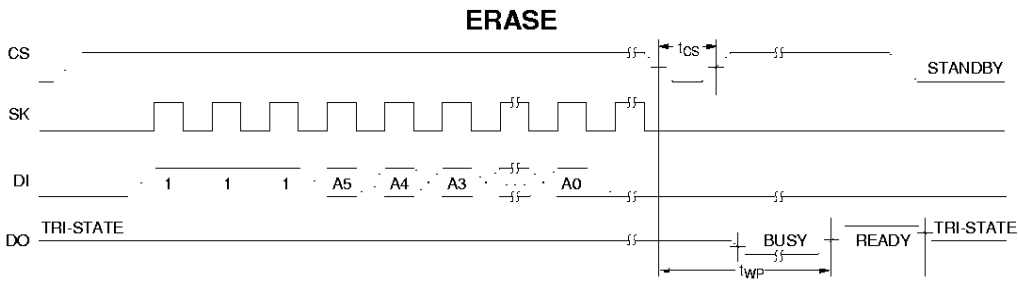
Timing Diagrams (Continued)



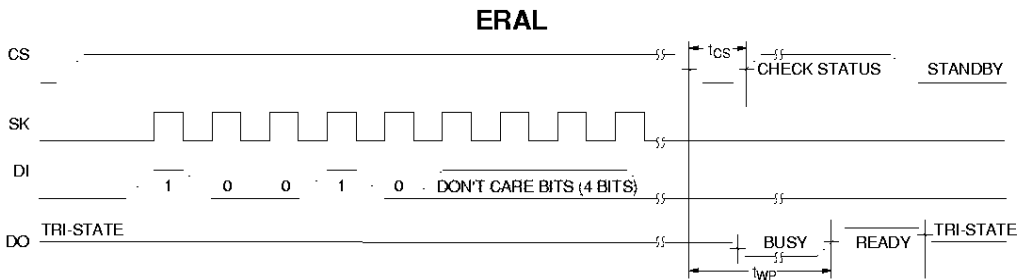
DS500080-8



DS500080-9

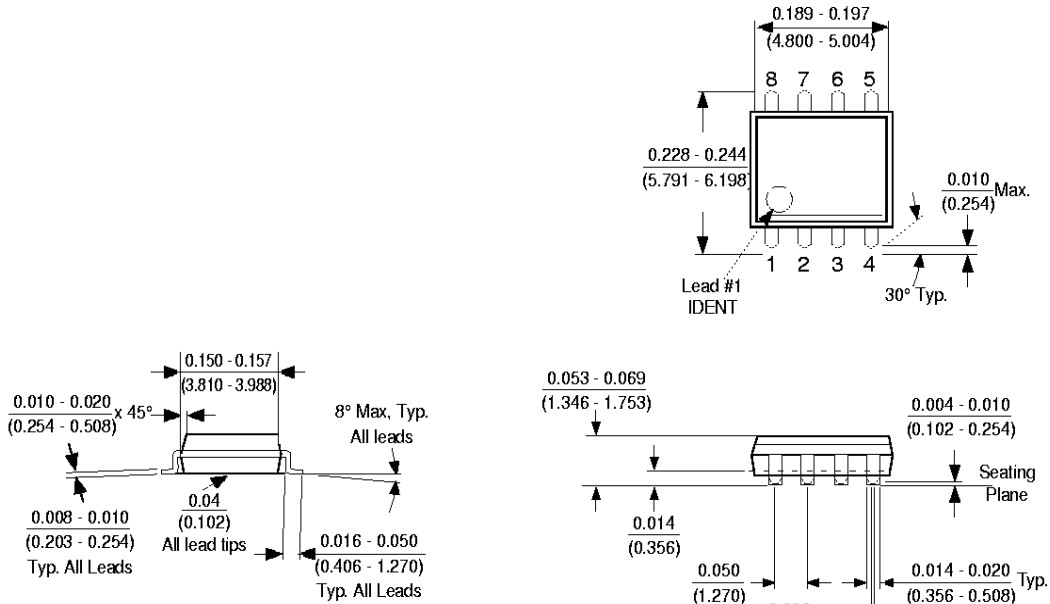


DS500080-10

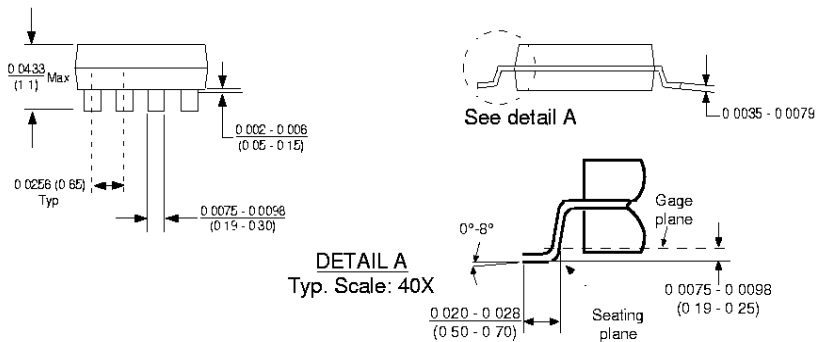
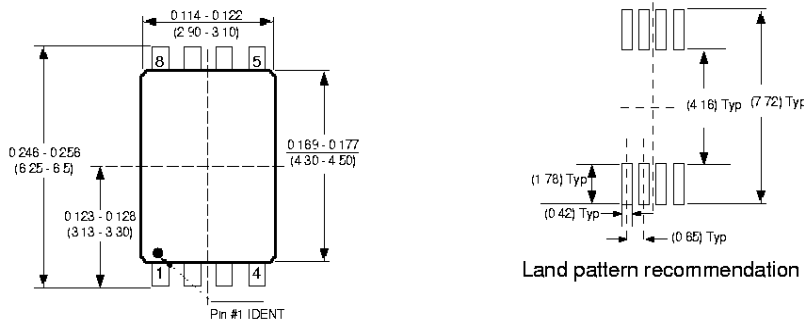


DS500080-11

Physical Dimensions inches (millimeters) unless otherwise noted



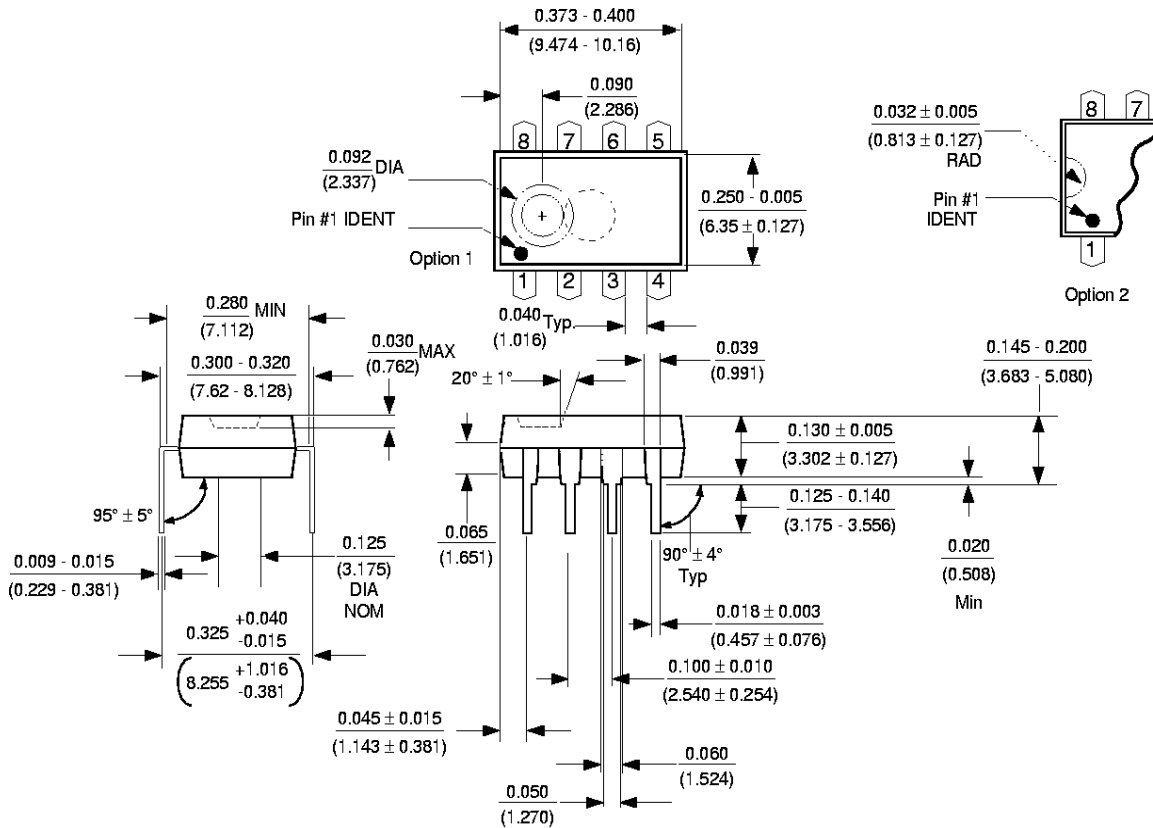
**Molded Small Out-Line Package (M8)
Package Number M08A**



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

**8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08**

Physical Dimensions inches (millimeters) unless otherwise noted



**Molded Dual-In-Line Package (N)
Package Number N08E**

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Americas
Customer Response Center
Tel 1-888-522-5372

Fairchild Semiconductor Europe
Fax +44 (0) 1793-856856
Tel +49 (0) 8141-6102-0
English Tel +44 (0) 1793-856856
Français Tel +33 (0) 1-6930-3696
Italiano Tel +39 (0) 2-249111-1

Fairchild Semiconductor Hong Kong
8/F, Room 808, Empire Centre
68 Mody Road, Tsimshatsui East
Kowloon Hong Kong
Tel, +852-2722-8338
Fax +852-2722-8383

Fairchild Semiconductor Japan Ltd.
4F, Natsume Bldg
2-18-6, Yushima, Bunkyo-ku
Tokyo, 113-0034 Japan
Tel 81-3-3818-8640
Fax 81-3-3818-8641

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.