

March 2006

Features

- 450 MHz small signal bandwidth
- 1500 V/μs slew rate
- 5.2 mA/channel static supply current
- 65 mA output current
- 120 MHz gain flatness to +/- 0.1 dB
- 14 pin SOIC

Applications

- Video switchers/routers
- Video line drivers
- Twisted pair driver/receiver
- Active filters

Description

The ZL40122 is a high speed, quad, current feedback operational amplifier offering high performance at a low cost. The device has a very high output current drive capability of 65 mA while requiring only 5.2 mA of static supply current. This feature makes the ZL40122

Ordering Information

ZL40122/DCA	14 lead SOIC	Tubes
ZL40122/DCB	14 lead SOIC	Tape & Reel
ZL40122DCF1	14 lead SOIC*	Tape & Reel, Bake & Drypack
ZL40122DCE1	14 lead SOIC*	Tubes, Bake & Drypack
*Pb Free Matte Tin		
-40°C to +85°C		

the ideal choice where a high density of high speed devices is required.

The flat gain response to 120 MHz, 450 MHz small signal bandwidth and 1500 V/μs slew rate make the device an excellent solution for video applications such as driving video signals down significant cable lengths.

Other applications which may take advantage of the ZL40122 superior dynamic performance features include low cost high order active filters and twisted pair driver/receivers.

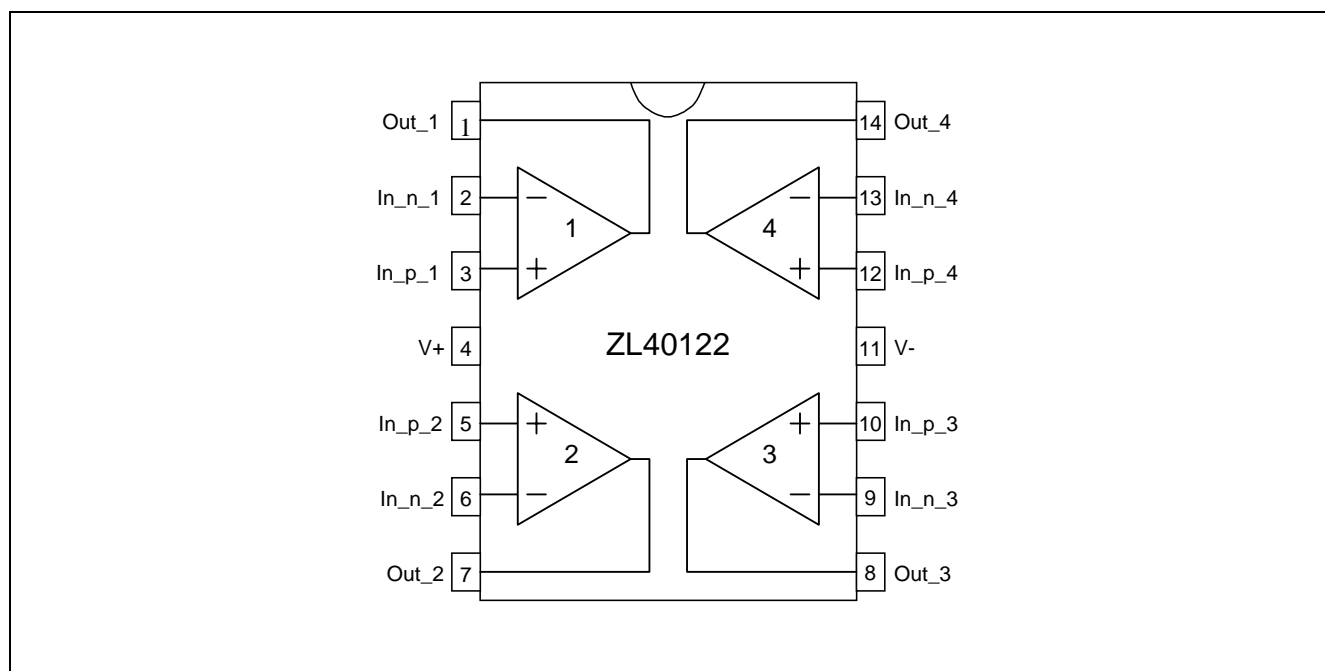


Figure 1 - Functional Block Diagram and Pin Connection

Change Summary

Changes from November 2004 Issue to March 2006 Issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1		Updated Ordering Information

Application Notes

Current Feedback Op Amps

Current feedback op amps offer several advantages over voltage feedback amplifiers:

- AC bandwidth not dependent on closed loop gain
- High Slew Rate
- Fast settling time

The architecture of the current feedback opamp consists of a high impedance non-inverting input and a low impedance inverting input which is always feedback connected. The error current is amplified by a transimpedance amplifier which can be considered to have gain

$$Z(f) = \frac{Z_o}{1 + j\left(\frac{f}{f_o}\right)}$$

where Z_o is the DC gain.

It can be shown that the closed loop non-inverting gain is given by

$$\frac{V_{out}}{V_{in}} = \frac{A_v}{1 + j\left(\frac{fR_f}{f_oZ_o}\right)}$$

where A_v is the DC closed loop gain, R_f is the feedback resistor. The closed loop bandwidth is therefore given by

$$BW_{CL} = \frac{f_oZ_o}{R_f} = \frac{GB_{OL}}{R_f}$$

and for low values of closed loop gain A_v depends only on the feedback resistor R_f and not the closed loop gain.

Increasing the value of R_f

- Increases closed loop stability
- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking
- Reduces overshoot

Using a resistor value of $R_f=510 \Omega$ for $A_v=+2$ V/V gives good stability and bandwidth. However since requirements for stability and bandwidth vary it may be worth experimentation to find the optimal R_f for a given application.

Layout Considerations

Correct high frequency operation requires a considered PCB layout as stray capacitances have a strong influence over high frequency operation for this device. The Zarlink evaluation board serves as a good example layout that should be copied. The following guidelines should be followed:

- Include 6.8 uF tantalum and 0.1 uF ceramic capacitors on both positive and negative supplies
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitances
- Minimize all trace lengths to reduce series inductance

Application Diagrams

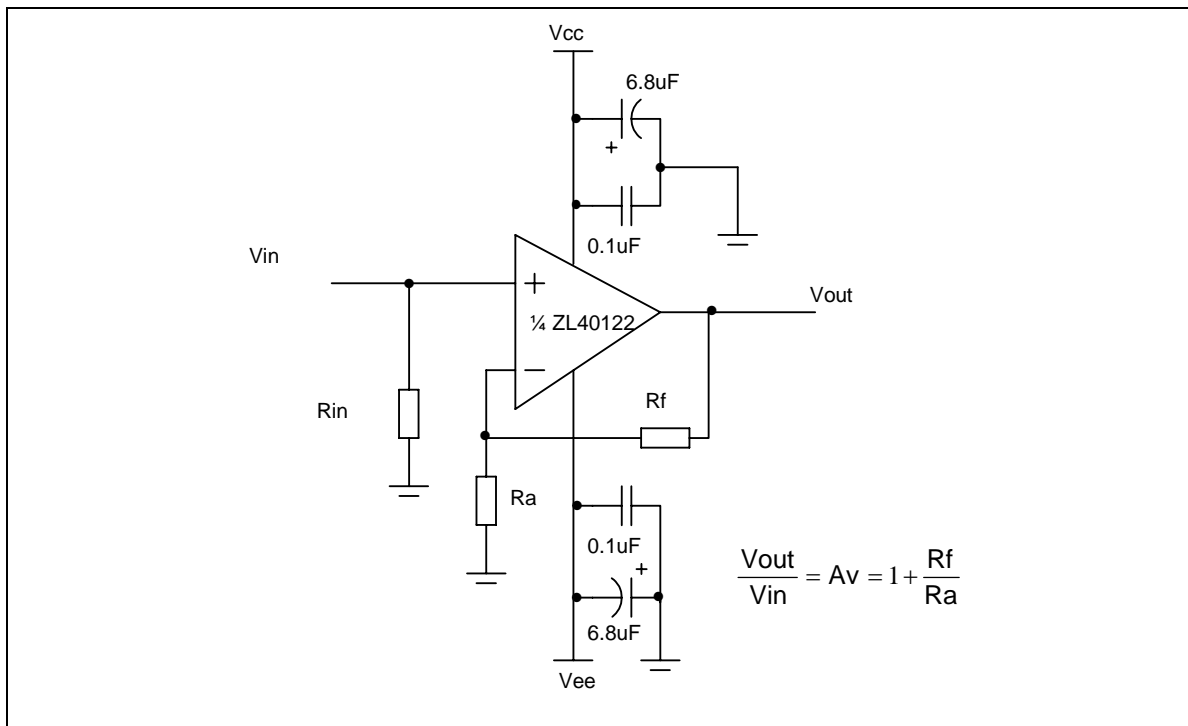


Figure 2 - Non-inverting Gain

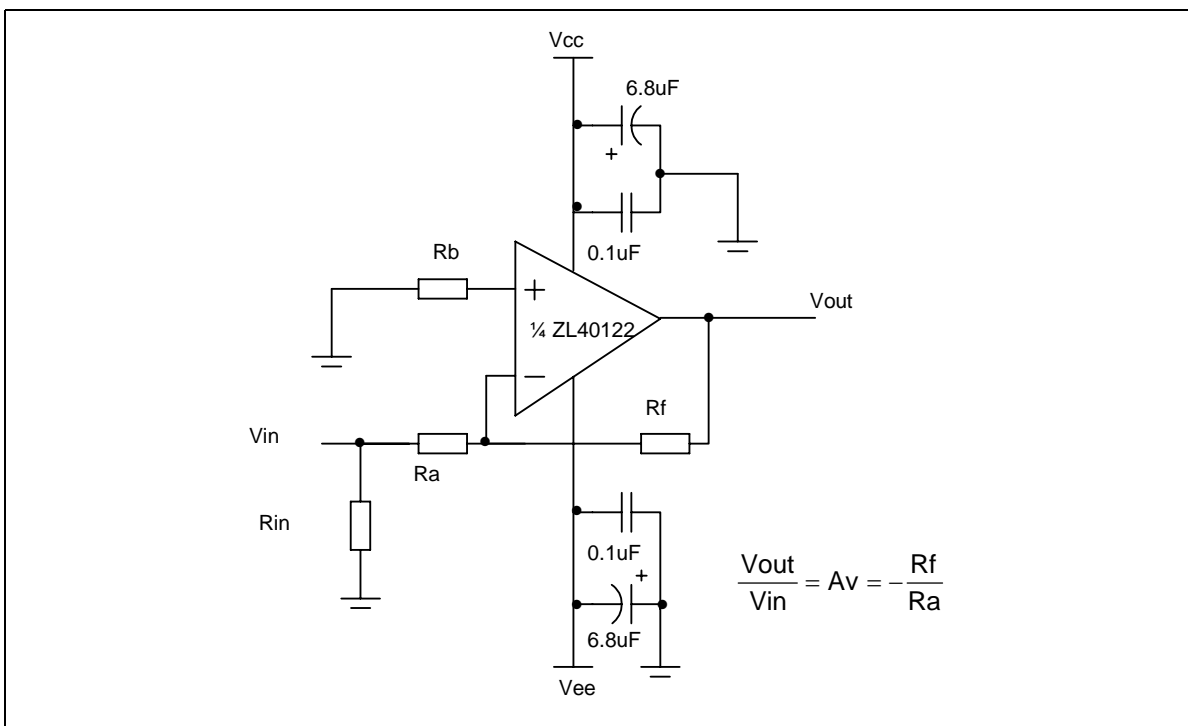


Figure 3 - Inverting Gain

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units
1	Vin Differential	V_{IN}		± 1.2	V
2	Output Short Circuit Protection	$V_{OS/C}$		See Apps Note in this data sheet	
3	Supply voltage	V+, V-		± 6.5	V
4	Voltage at Input Pins	$V_{(+IN)}, V_{(-IN)}$	V-	V+	V
5	Voltage at Output Pins	V_O	V-	V+	V
6	EDS Protection (HBM Human Body Model) (see Note 2)		2	(see Note 3)	kV
7	Storage Temperature		-55	+150	°C
8	Latch-up test		± 100 mA for 100 ms	(see Note 4)	
9	Supply transient test		20% pulse for 100 ms	(see Note 5)	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF. Machine model, 20 Ω in series with 100 pF.

Note 3: 0.8 kV between the pairs of +INA, -INA and +INB pins only. 2 kV between supply pins, OUTA or OUTB pins and any input pin.

Note 4: ± 100 mA applied to input and output pins to force the device to go into "latch-up". The device passes this test to JEDEC spec 17.

Note 5: Positive and Negative supply transient testing increases the supplies by 20% for 100 ms.

Operating Range

Characteristic	Min.	Typ.	Max.	Units	Comments
Supply Voltage (Vcc)	± 4.0		± 6.0	V	
Operating Temperature (Ambient)	-40		+85	°C	
Junction to Ambient resistance	Rth(j-a)	150		°C 4 layer FR4 board	
Junction to Case resistance	Rth(j-c)	60		°C 4 layer FR4 board	

Electrical Characteristics - $V_{CC}=\pm 5\text{ V}$, $T_{amb}=25\text{C}(\text{typ.})$, $T_{amb}=-40\text{C}$ to $+85\text{C}(\text{min-max})$, $A_v=+2\text{V/V}$, $R_f=510\ \Omega$, $R_{load}=100\ \Omega$ unless specified.

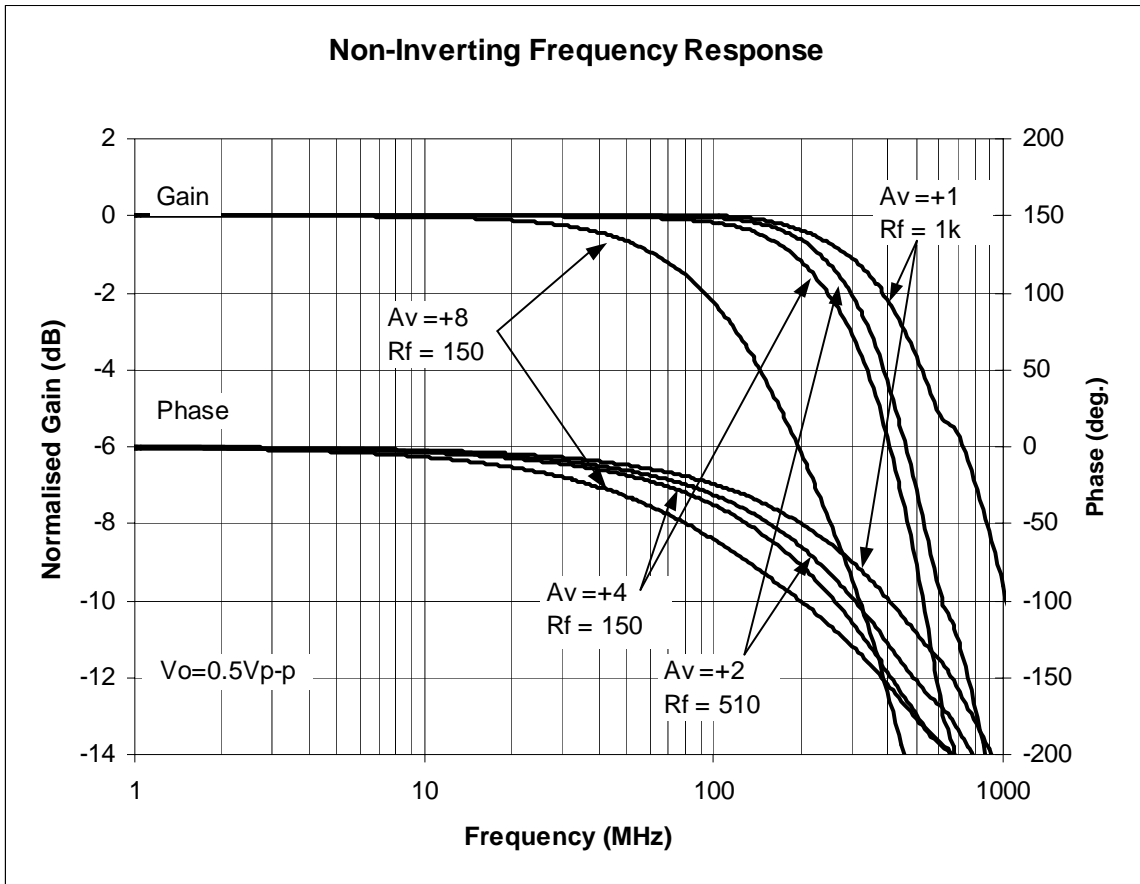
Characteristic	Conditions	Typ 25C	Min/ Max 25C	Min/ Max -40 to +85C	Units	Test Type ¹
Frequency Domain Response						
-3 dB Bandwidth	$A_v=+1$; $V_o < 0.5\text{ V}_{p-p}$; $R_f=1.5\text{ k}\Omega$	450	-	-	MHz	C
	$A_v=+2$; $V_o < 0.5\text{ V}_{p-p}$; $R_f=510\ \Omega$	380	-	-	MHz	C
	$A_v=+2$; $V_o < 5\text{ V}_{p-p}$; $R_f=510\ \Omega$	170	-	-	MHz	C
+/- 0.1 dB Flatness	$A_v=+2$; $V_o < 0.5\text{ V}_{p-p}$; $R_f=510\ \Omega$	120	-	-	MHz	C
Differential Gain (NTSC)	$R_{load}=150\ \Omega$	0.01	-	-	%	C
Differential Phase (NTSC)	$R_{load}=150\ \Omega$	0.015	-	-	deg.	C
Time Domain Response						
Rise and Fall Time	$V_{out}=0.5\text{ V Step}$	1	-	-	ns	C
	$V_{out}=5\text{ V Step}$	2.8	-	-	ns	C
Settling Time to 0.1%	$V_{out}=2\text{ V Step}$	6	-	-	ns	C
Overshoot	$V_{out}=0.5\text{ V Step}$	4	-	-	%	C
Slew Rate	$V_{out}=5\text{ V Step}$	1500	-	-	V/ μs	C
Noise and Distortion						
2 nd Harmonic Distortion	$V_{out}=2\text{ V}_{p-p}$, 1 MHz	-84	-	-	dBc	C
3 rd Harmonic Distortion	$V_{out}=2\text{ V}_{p-p}$, 1 MHz	-85	-	-	dBc	C
Equivalent Input Noise						
Voltage	>1 MHz	5.5	-	-	nV $\sqrt{\text{Hz}}$	C
Non-Inverting Current	>1 MHz	1.3	-	-	pV $\sqrt{\text{Hz}}$	C
Inverting Current	>1 MHz	11	-	-	pA $\sqrt{\text{Hz}}$	C
Static, DC Performance						
Input Offset Voltage		2.7	± 6.3	± 7.7	mV	A
Average Drift		-	-	15	$\mu\text{V}/\text{deg. C}$	C
Input Bias Current – Non-inverting		2.6	± 5.6	± 6	μA	A
Average Drift		-	-	6	nA/deg. C	C

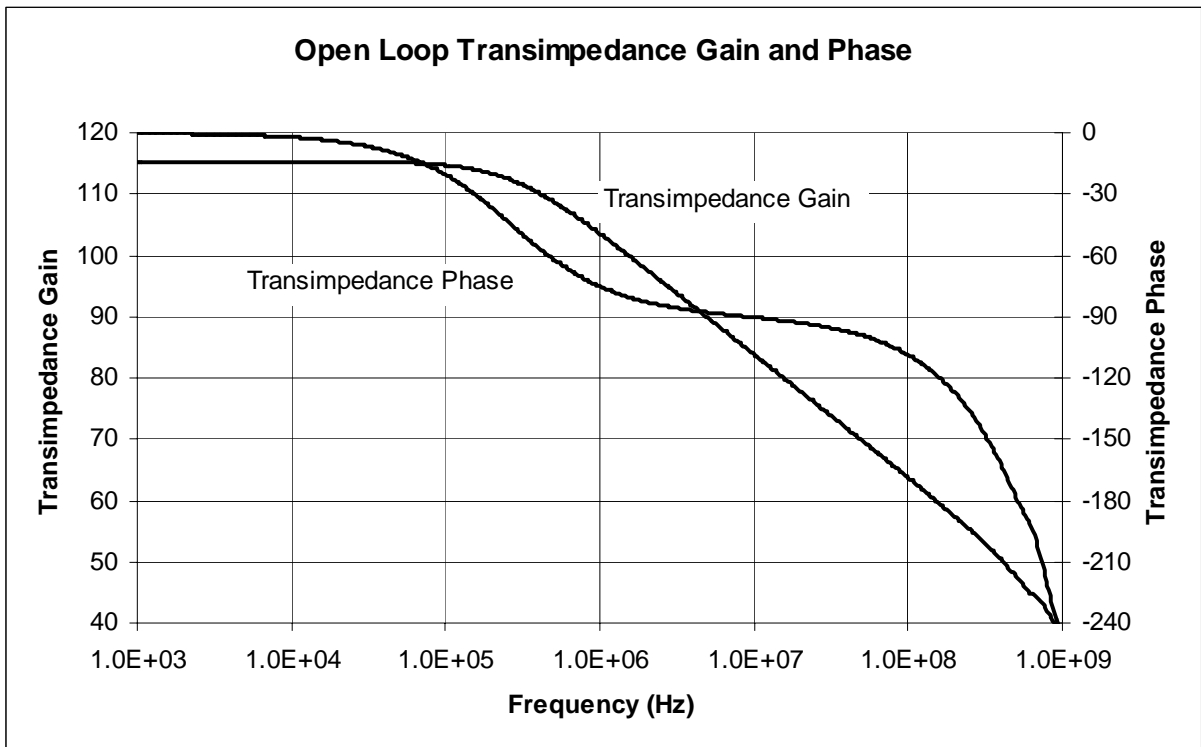
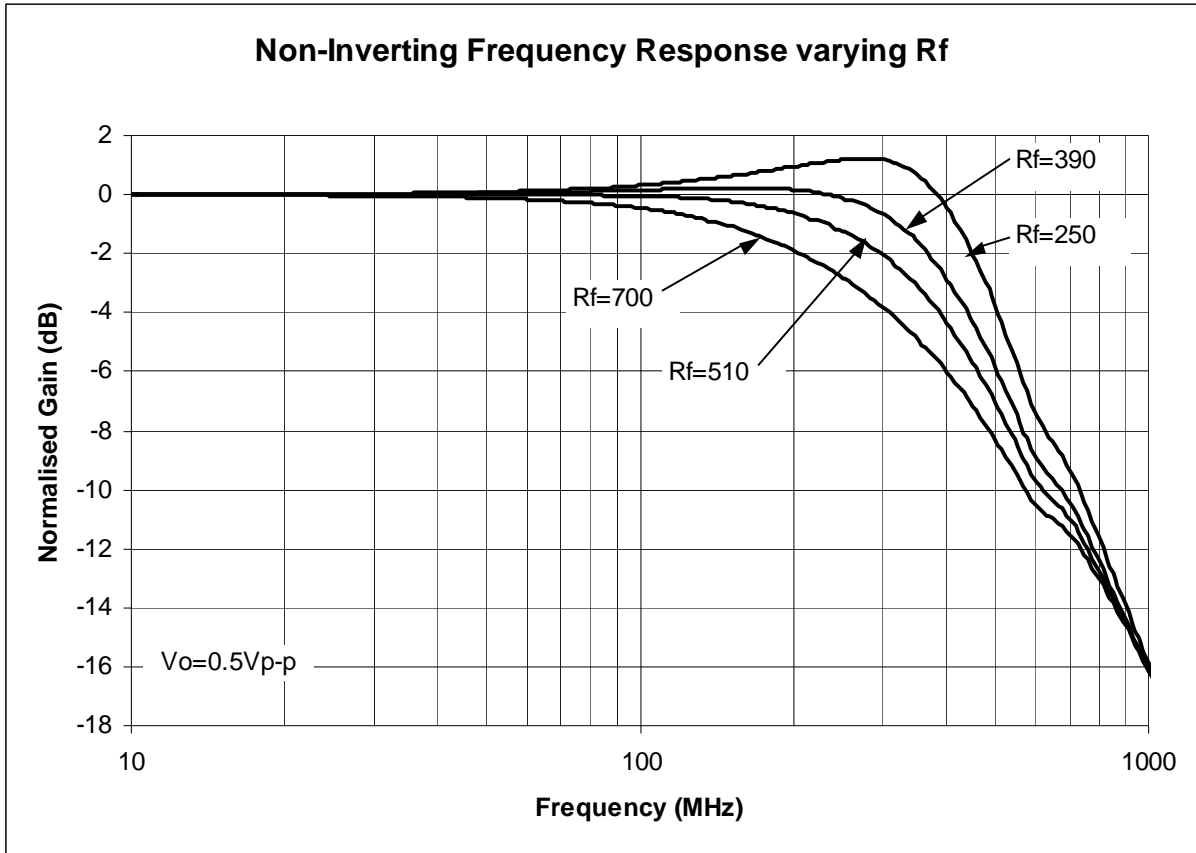
Characteristic	Conditions	Typ 25C	Min/ Max 25C	Min/ Max -40 to +85C	Units	Test Type ¹
Input Bias Current – Inverting		7.4	±25	±28	μA	A
Average Drift		-	-	15	nA/deg. C	C
Power Supply Rejection Ratio (+ve)	DC	61	58	57	dB	A
Power Supply Rejection Ratio (-ve)	DC	58	56	55	dB	A
Common Mode Rejection Ratio	DC	54	50	49	dB	A
Supply Current (per Channel)	Quiescent	5.2	6.5	6.7	mA	A
Miscellaneous Performance						
Input Resistance (Non-inverting)		8	-	-	MΩ	C
Input Capacitance (Non-inverting)		1	-	-	pF	C
Common Mode Input Range		±2.4	±2.2	±2.0	V	A
Output Voltage Range	Rload=100 Ω	±2.8	±2.7	±2.6	V	A
Output Current (max)		65	-	-	mA	C
Output Resistance, Closed Loop	DC	90	-	-	mΩ	C

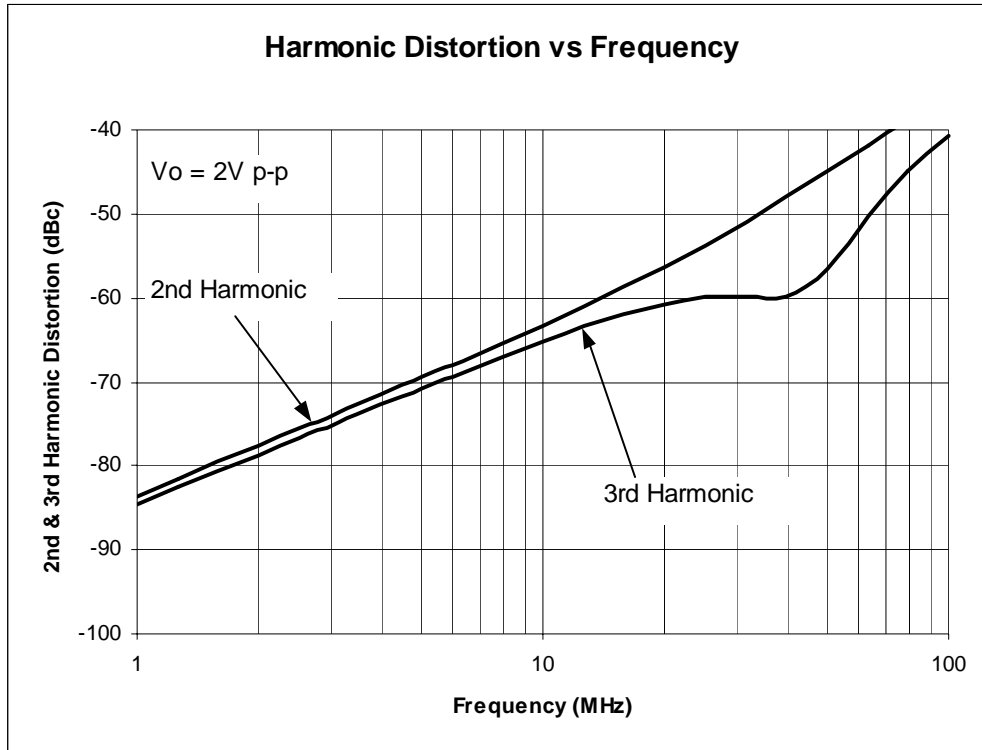
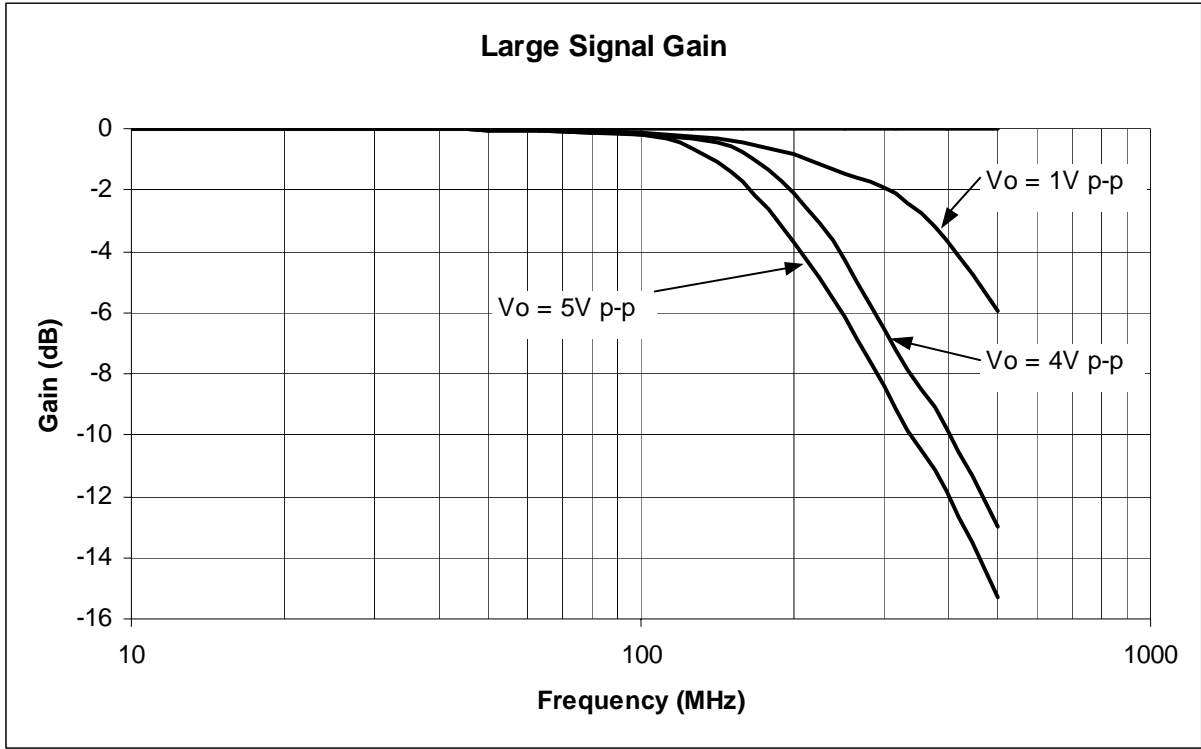
Note: Test Types:

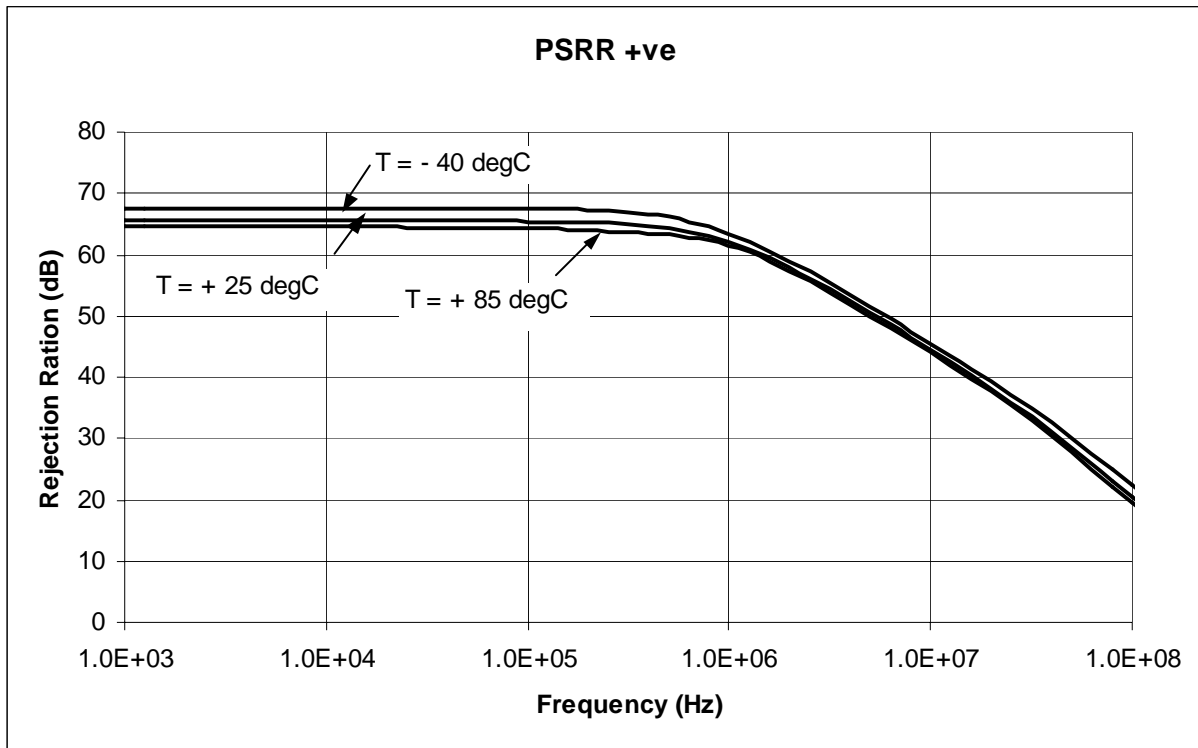
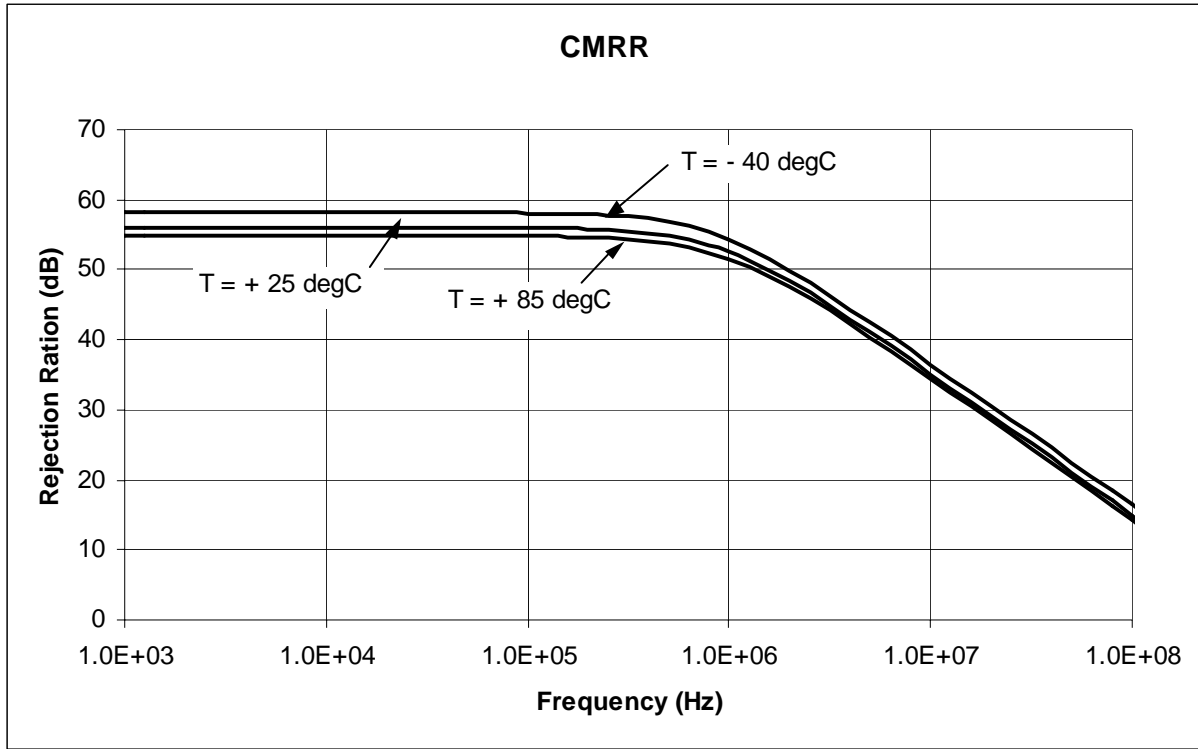
- (A) 100% tested at 25°C. Over temperature limits are set by characterization and simulation.
- (B) Limits set by characterization or simulation.
- (C) Typical value only for information.

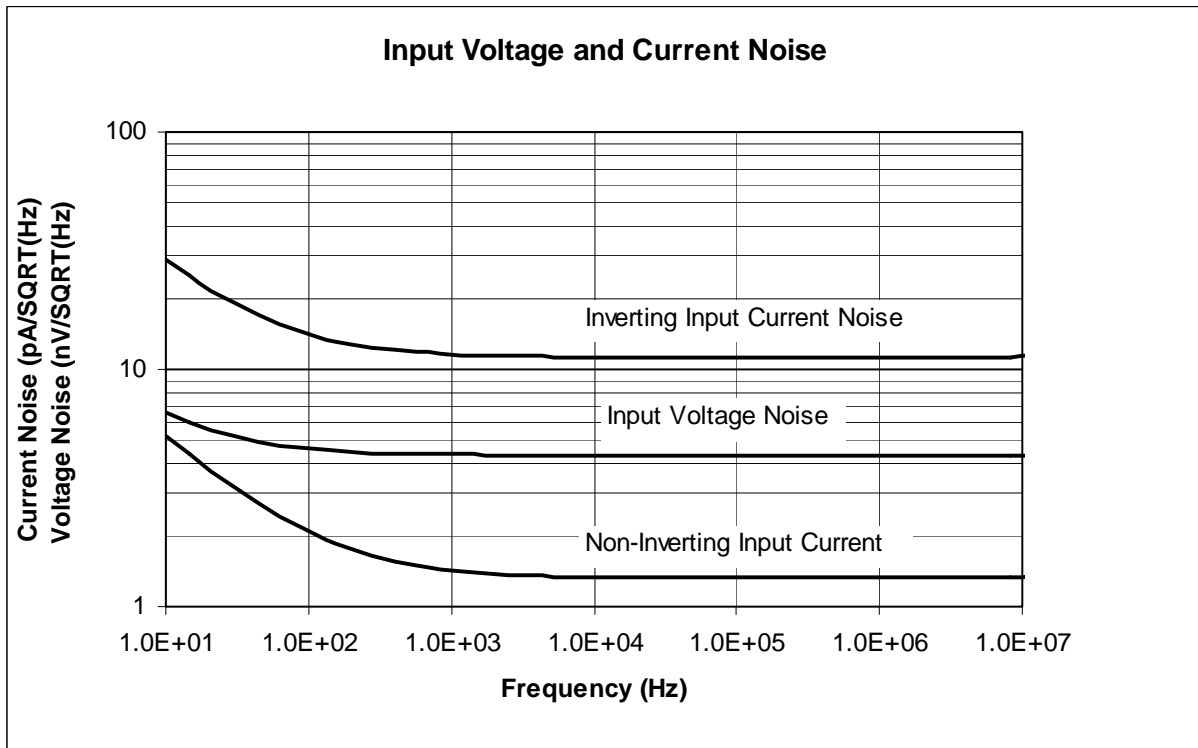
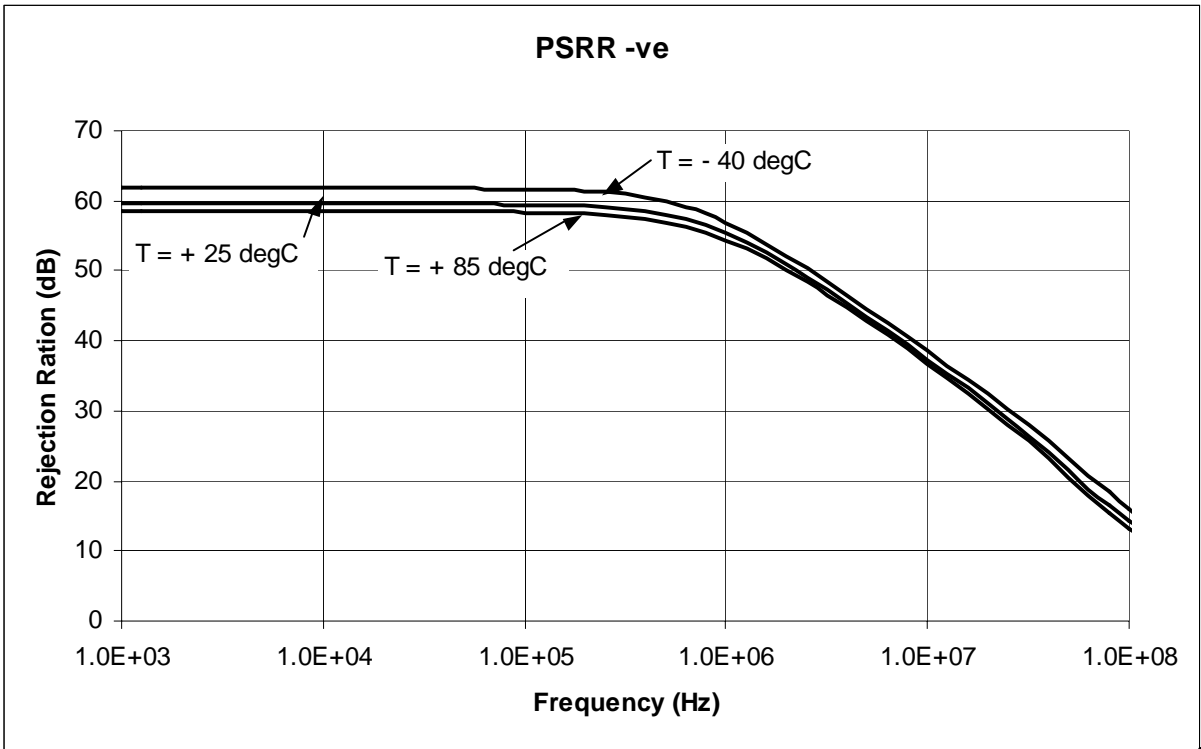
Typical Performance Characteristics - $T_{amb}=25\text{degC}$, $V_{supply}=\pm 5\text{ V}$, $R_{load}=100\ \Omega$, $A_v=+2V/V$, $R_f=510\ \Omega$, unless otherwise specified.

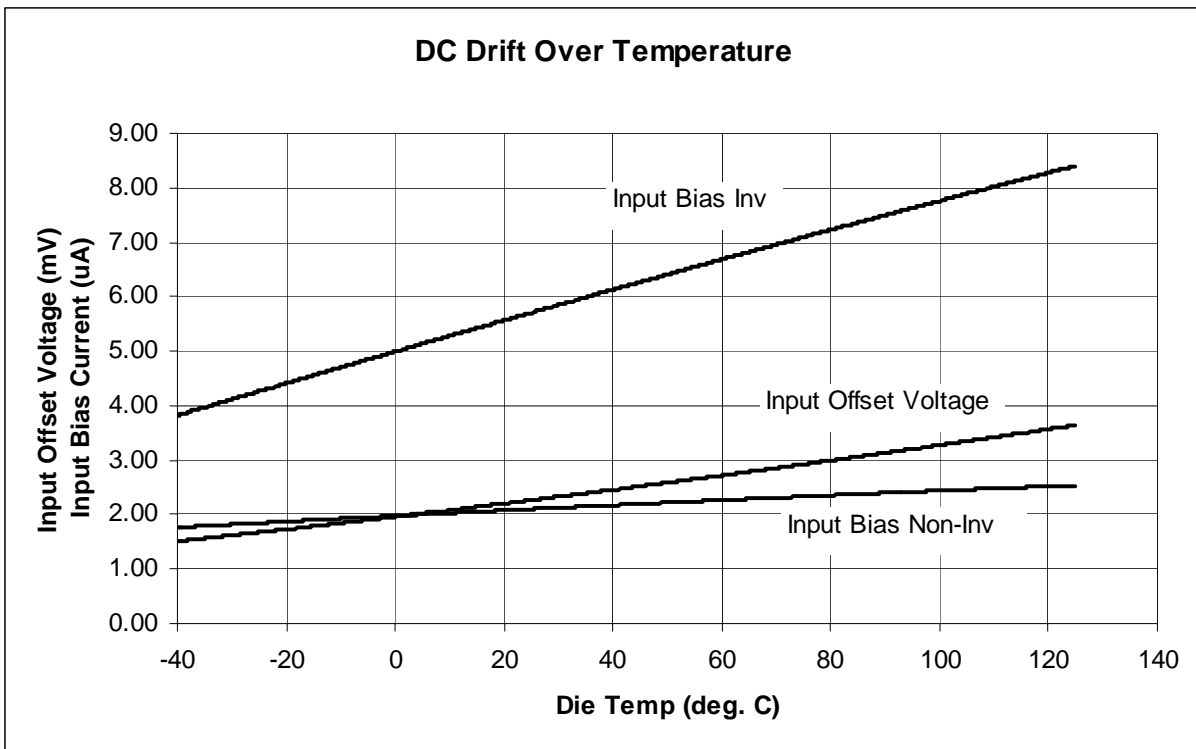
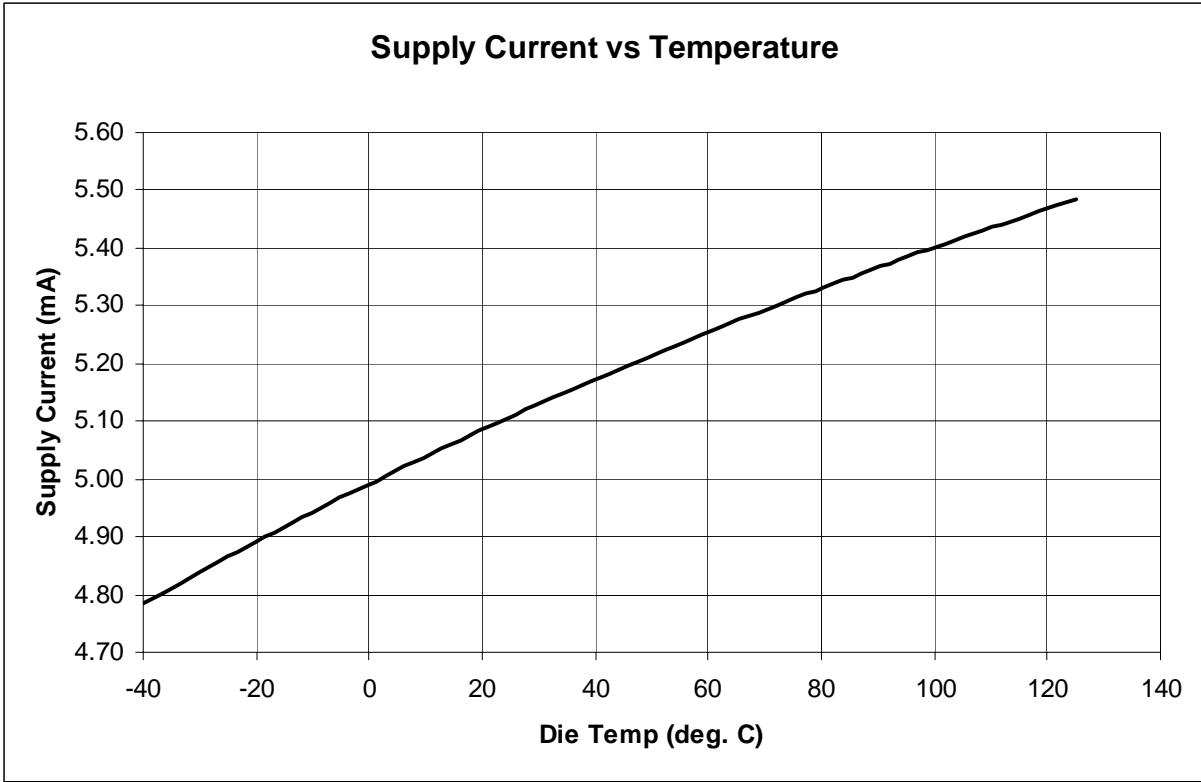


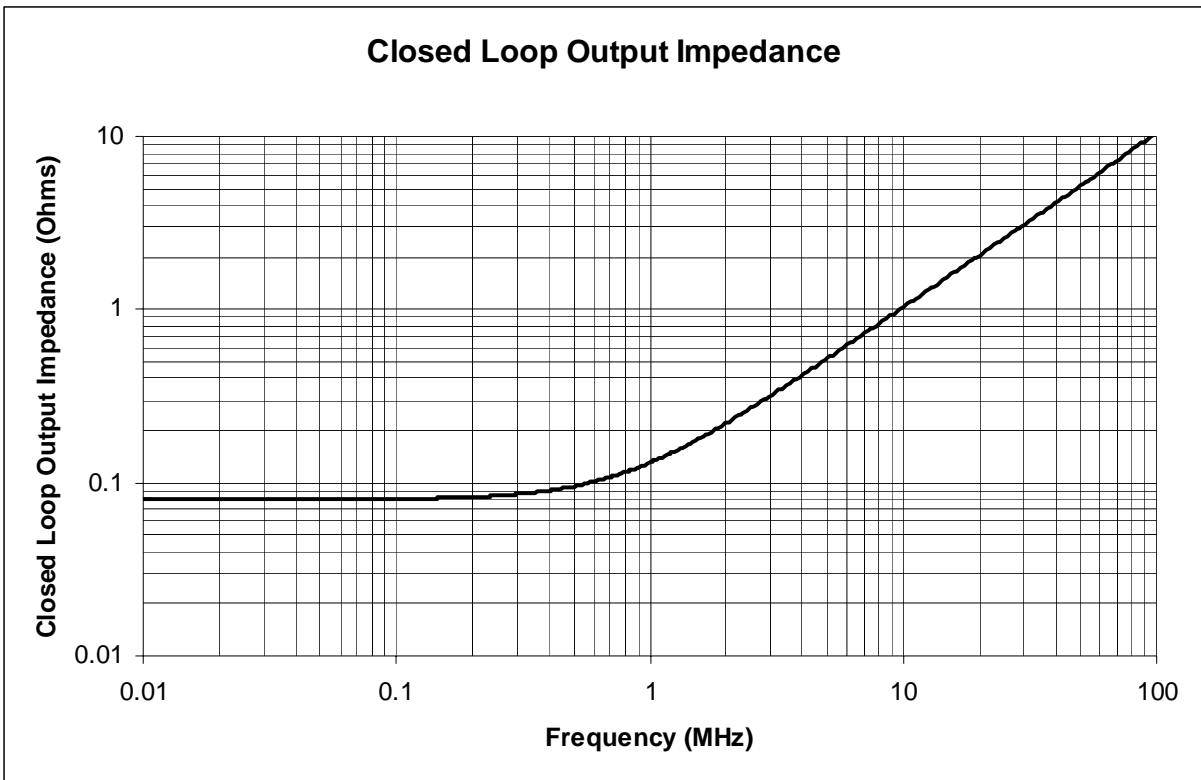
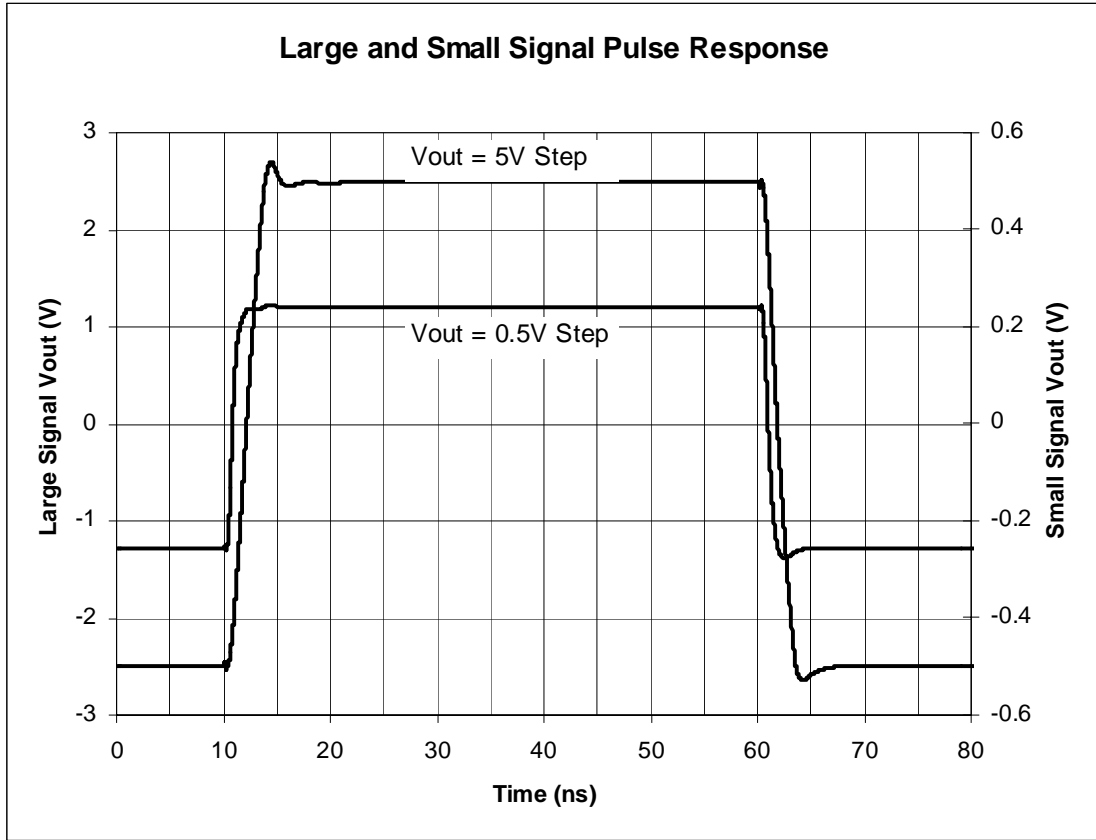


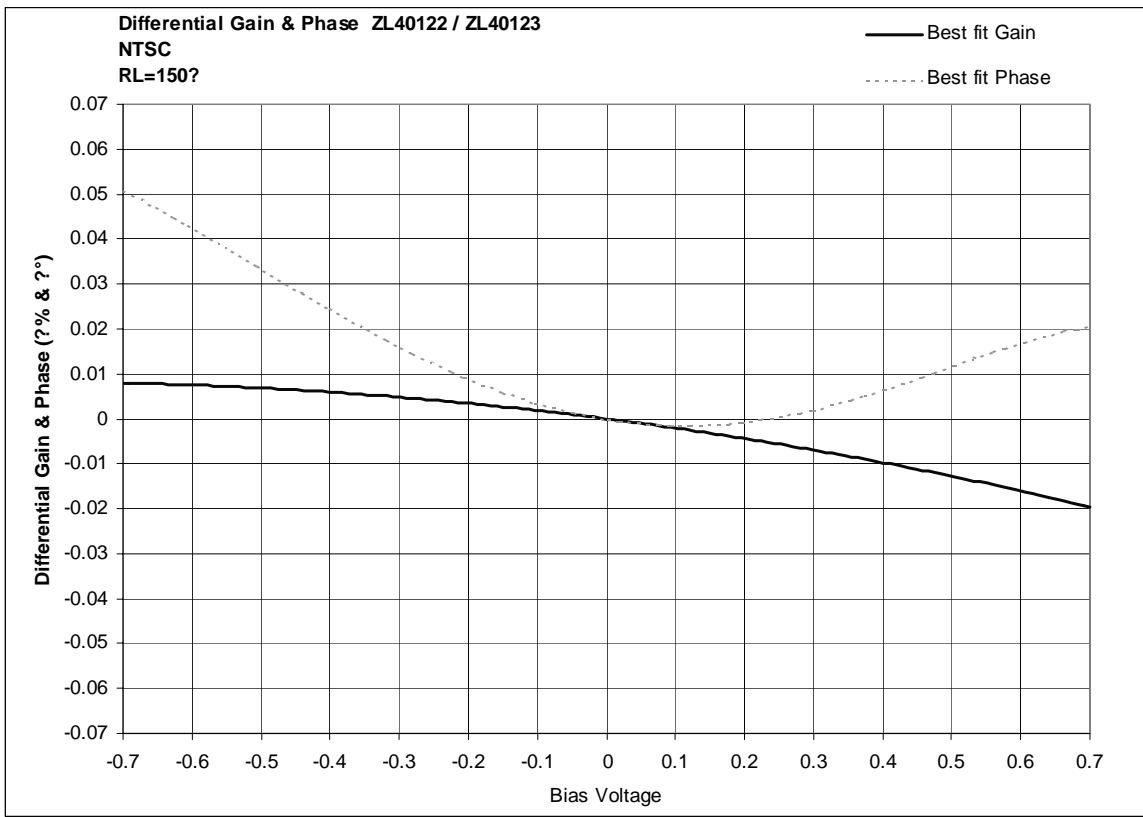


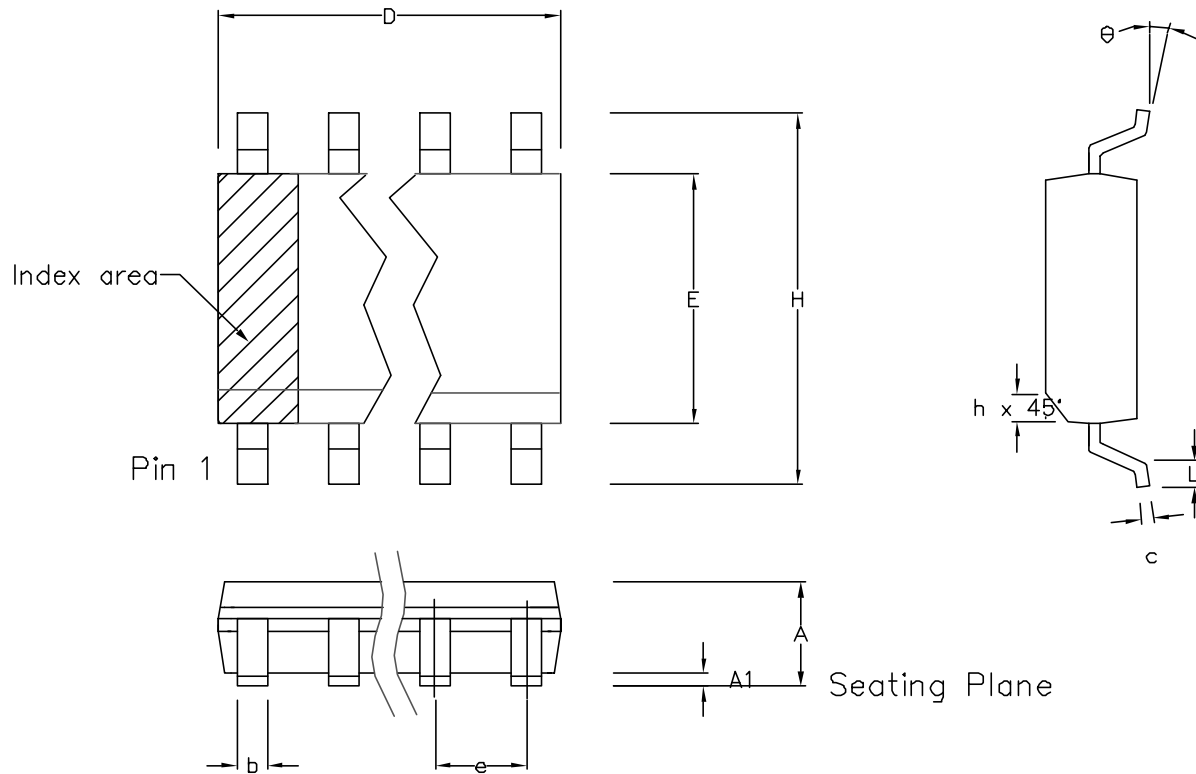












	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
Pin Features				
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension $E1$ do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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APPRD.					



Previous package codes

MP / S

Package Code DC

Package Outline for
14 lead SOIC
(0.150" Body Width)

GPD00011



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