

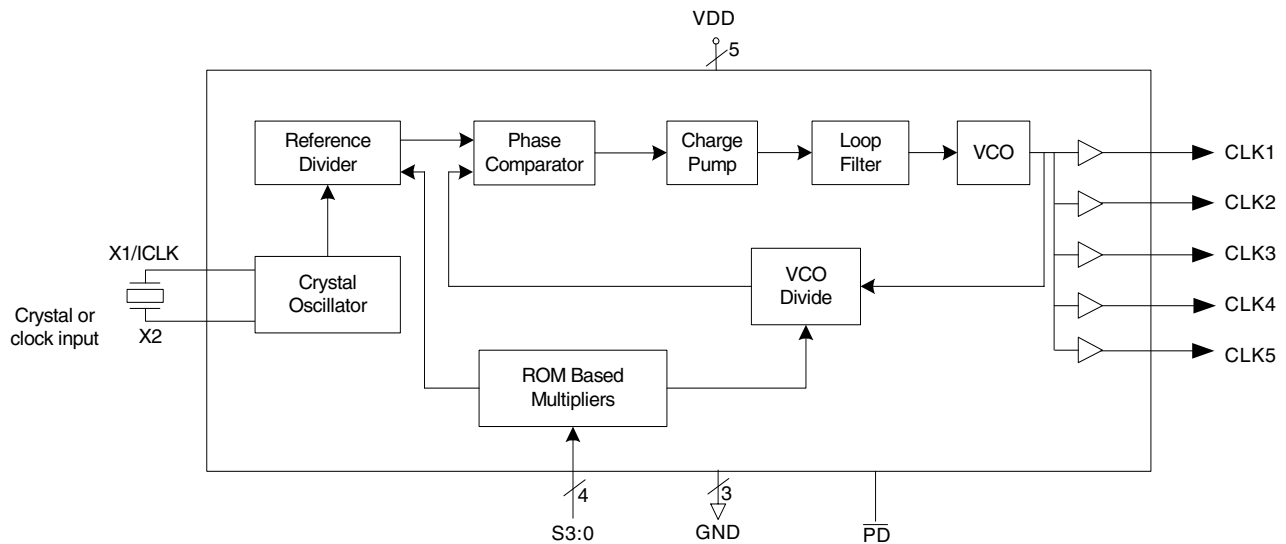
Description

The ICS601-25 is a low-cost, low phase noise, high performance clock synthesizer for applications which require low phase noise, low jitter, and low skew fanout. It is IDT's lowest phase noise multiplier, and also the lowest CMOS part in the industry. Using IDT's patented analog and digital Phase Locked Loop (PLL) techniques, the chip accepts a 10-27 MHz crystal or clock input, and produces output clocks up to 156 MHz.

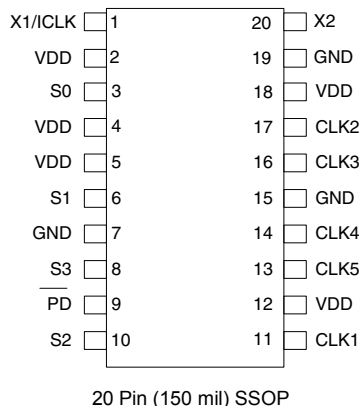
Features

- Packaged in 20-pin SSOP
- Uses fundamental 10 - 27 MHz crystal or clock
- Output clocks up to 156 MHz
- Low phase noise: -132 dBc/Hz at 10 kHz
- Five low skew (<250 ps) outputs
- Low jitter - 18 ps one sigma at 125 MHz
- Full swing CMOS outputs with 25 mA drive capability at TTL levels
- Powerdown mode lowers power consumption
- Advanced, low power, sub-micron CMOS process
- Industrial temperature version available
- Pb (lead) free package
- Operating voltage of 3.3 V

Block Diagram



Pin Assignment



Output Select Table

S3	S2	S1	S0	Multiplier
0	0	0	0	x1
0	0	0	1	x2
0	0	1	0	x3
0	0	1	1	x4
0	1	0	0	x5
0	1	0	1	x6
0	1	1	0	x8
0	1	1	1	x16
1	0	0	0	x7
1	0	0	1	x9
1	0	1	0	x10
1	0	1	1	x11
1	1	0	0	x12
1	1	0	1	output tristates
1	1	1	0	x14
1	1	1	1	x15

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	XI	Crystal or clock input. Connect to a 10-27 MHz fundamental parallel mode crystal or clock input.
2	VDD	Power	Connect to +3.3 V.
3	S0	Input	Select pin 0. Internal pull-up.
4, 5	VDD	Power	Connect to +3.3 V.
6	S1	Input	Select pin 1. Internal pull-up.
7	GND	Power	Connect to ground.
8	S3	Input	Select pin 3. Internal pull-down.
9	$\overline{\text{PD}}$	Input	Powerdown when held low. Internal pull-up.
10	S2	Input	Select pin 2. Internal pull-up.
11	CLK1	Output	Clock output.
12	VDD	Power	Connect to +3.3 V.
13	CLK5	Output	Clock output.
14	CLK4	Output	Clock output.
15	GND	Power	Connect to ground.
16	CLK3	Output	Clock output.
17	CLK2	Output	Clock output.
18	VDD	Power	Connect to +3.3 V.
19	GND	Power	Connect to ground.
20	X2	XO	Crystal connection. Connect to a 10-27 MHz fundamental parallel mode crystal or leave unconnected for clock input.

External Components

The ICS601-25 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 μF and 0.1 μF should be connected between VDD and GND, as close to the part as possible. A 33 Ω series terminating resistor should be used on each clock output. The crystal must be connected as close to the chip as possible. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1 to ground and X2 to ground. In general, the value of these capacitors is given by the following equation, where CL is the crystal load capacitance: Crystal caps (pF) = $(\text{CL}-5) \times 2$. So for a crystal with 16 pF load capacitance, two 22 pF caps can be used. For any given board layout, ICS can measure the board capacitance and recommend the exact capacitance value to use.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS601-25. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Commercial version	0 to +70 °C
Ambient Operating Temperature, Industrial version	-40 to +85 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	125 °C
Soldering Temperature	260 °C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (commercial)	0		+70	°C
Ambient Operating Temperature (industrial)	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+2.97		+3.63	V

DC Electrical Characteristics

VDD=3.3 V \pm 10%, Ambient temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.97		3.63	V
Input High Voltage	V _{IH}	X1/ICLK pin only	VDD/2+1			V
Input Low Voltage	V _{IL}	X1/ICLK pin only			VDD/2-1	V

DC Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input High Voltage	V_{IH}		2		VDD	V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage, CMOS level	V_{OH}	$I_{OH} = -4$ mA	VDD-0.4			V
Output High Voltage	V_{OH}	$I_{OL} = -12$ mA	2.4			V
Output Low Voltage	V_{OL}	$I_{OL} = 12$ mA			0.4	V
Operating Supply Current	IDD	No load, 125 MHz		45	60	mA
Short Circuit Current	I_{OS}	Each output	± 40	± 60		mA
Input Capacitance		Select pins		5		pF
Output Impedance	Z_{OUT}			20		Ω
On Chip Pull-up Resistor	R_{PU}	S2, S1, S0, \overline{PD} pins		510		k Ω
On Chip Pull-down Resistor	R_{PD}	S3 pin		240		k Ω

AC Electrical Characteristics

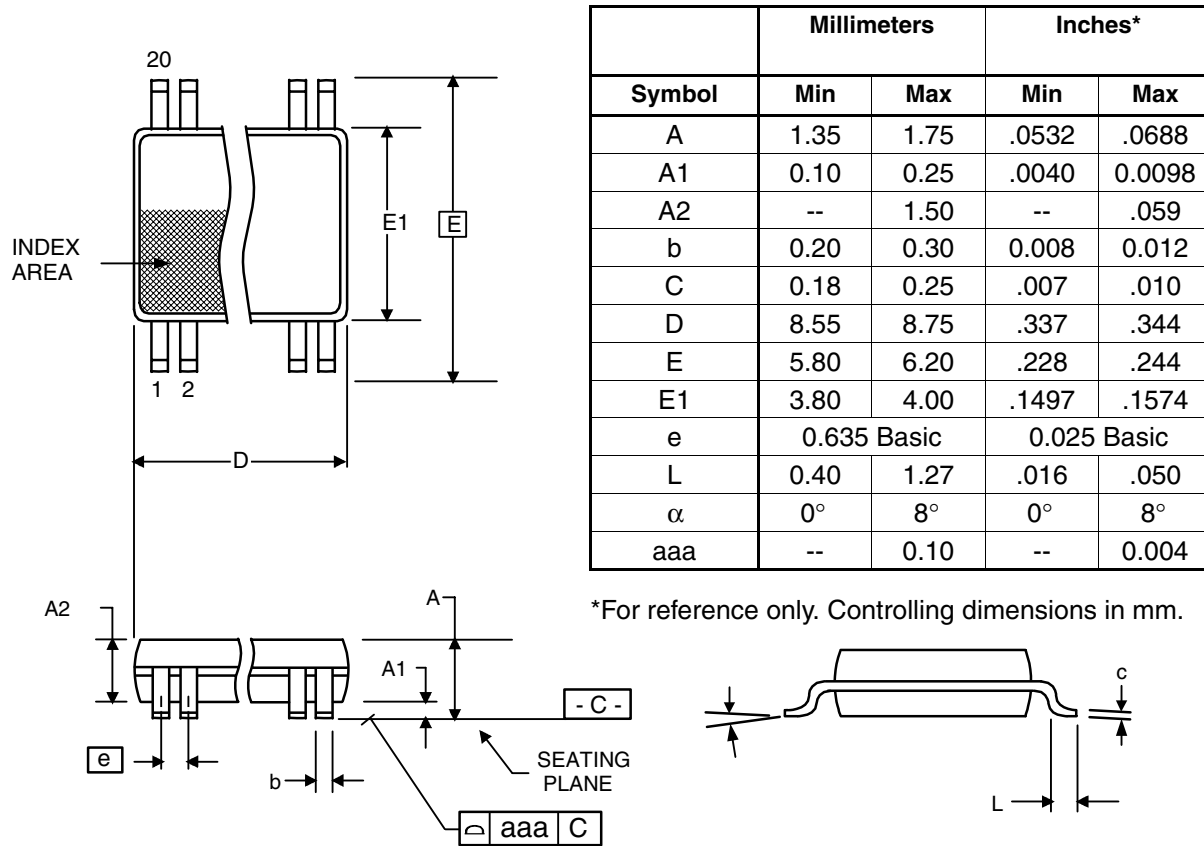
VDD = 3.3V $\pm 10\%$, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			10		27	MHz
Output Frequency		At 3.3V			156	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, Note 1			1.5	ns
Output Fall Time	t_{OF}	0.8 to 2.0 V, Note 1			1.5	ns
Output Clock Duty Cycle		At VDD/2, Note 1	45	50	55	%
Maximum Absolute jitter, short term, 125 MHz		Note 1		± 50	± 75	ps
Maximum jitter, one sigma, 125 MHz (x5)		Note 1		18	25	ps
Phase Noise, relative to carrier, 125 MHz (x5)		100 Hz offset	-90	-95		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		1 kHz	-115	-120		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		10 kHz offset	-118	-123		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		100 kHz offset	-115	-120		dBc/Hz
Output to Output Skew		25M in, 125M out, Note 1			250	ps

Note 1: Measured with 15 pF load

Package Outline and Package Dimensions (20-pin SSOP, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
601R-25LF	601R-25LF	Tubes	20-pin SSOP	0 to +70° C
601R-25LFT	601R-25LF	Tape and Reel	20-pin SSOP	0 to +70° C
601R-25ILF	601R-25ILF	Tubes	20-pin SSOP	-40 to 85° C
601R-25ILFT	601R-25ILF	Tape and Reel	20-pin SSOP	-40 to 85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Circuit Systems (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.