

## General Description

The 842023 is an Ethernet Clock Generator. For Ethernet applications, a 25MHz crystal is used to generate 250MHz. The 842023 uses IDT 3<sup>rd</sup> generation low phase noise VCO technology and can achieve <1ps rms phase jitter, easily meeting Ethernet jitter requirements. The 842023 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

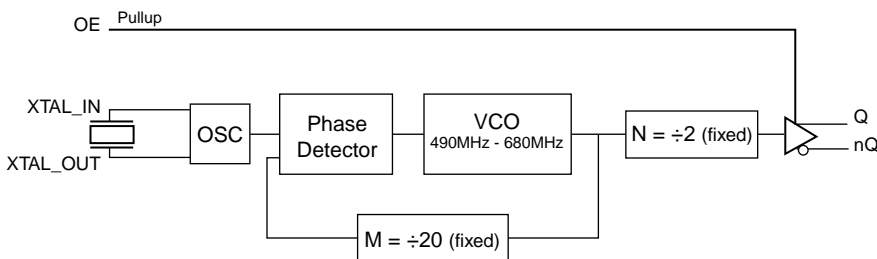
## Features

- One differential HSTL output pair
- Crystal oscillator interface, 18pF parallel resonant crystal (24.5MHz – 34MHz)
- Output frequency range: 245MHz – 340MHz
- VCO range: 490MHz – 680MHz
- RMS phase jitter at: 250MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.36ps (typical)
- Full 3.3V or 2.5V output supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

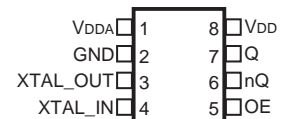
## Frequency Table

Inputs				Output Frequency (MHz)
Crystal Frequency (MHz)	M	N	Multiplication Value M/N	
25	20	2	10	250

## Block Diagram



## Pin Assignment



**842023**

**8 Lead TSSOP**

**4.40mm x 3.0mm x 0.925 package body**

**G Package**

**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	V <sub>DDA</sub>	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Output enable pin. When HIGH, Q/nQ outputs are active. When LOW, the Q/nQ outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. HSTL interface levels.
8	V <sub>DD</sub>	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V <sub>DD</sub>	4.6V
Inputs, V <sub>I</sub>	-0.5V to V <sub>DD</sub> + 0.5V
Outputs, I <sub>O</sub> Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, θ <sub>JA</sub>	129.5°C/W (0 mps)
Storage Temperature, T <sub>STG</sub>	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics, V<sub>DD</sub> = 3.3V ± 5%, T<sub>A</sub> = 0°C to 70°C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V <sub>DD</sub>	Power Supply Voltage		3.135	3.3	3.465	V
V <sub>DDA</sub>	Analog Supply Voltage		V <sub>DD</sub> - 0.11	3.3	V <sub>DD</sub>	V
I <sub>DD</sub>	Power Supply Current				84	mA
I <sub>DDA</sub>	Analog Supply Current				11	mA

**Table 3B. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.11$	2.5	$V_{DD}$	V
$I_{DD}$	Power Supply Current				80	mA
$I_{DDA}$	Analog Supply Current				11	mA

**Table 3C. LVC MOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	OE $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	OE $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$

**Table 3D. HSTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		1.0		1.8	V
$V_{OL}$	Output Low Voltage; NOTE 1		0		0.6	V
$V_{OX}$	Output Crossover Voltage; NOTE 2		$40\% \times (V_{OH} - V_{OL}) + V_{OL}$		$60\% \times (V_{OH} - V_{OL}) + V_{OL}$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.4		1.8	V

NOTE 1: Outputs terminated with  $50\Omega$  to GND.

NOTE 2: Defined with respect to output voltage swing at a given condition.

**Table 3E. HSTL DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		0.9		1.4	V
$V_{OL}$	Output Low Voltage; NOTE 1				0.4	V
$V_{OX}$	Output Crossover Voltage; NOTE 2		$40\% \times (V_{OH} - V_{OL}) + V_{OL}$		$60\% \times (V_{OH} - V_{OL}) + V_{OL}$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.4		1.4	V

NOTE 1: Outputs terminated with  $50\Omega$  to GND.

NOTE 2: Defined with respect to output voltage swing at a given condition.

**Table 4. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		24.5		34	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE: It is not recommended to overdrive the crystal input with an external clock.

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		245		340	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 1	250MHz Integration Range: 1.875MHz – 20MHz		0.36		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		48		52	%

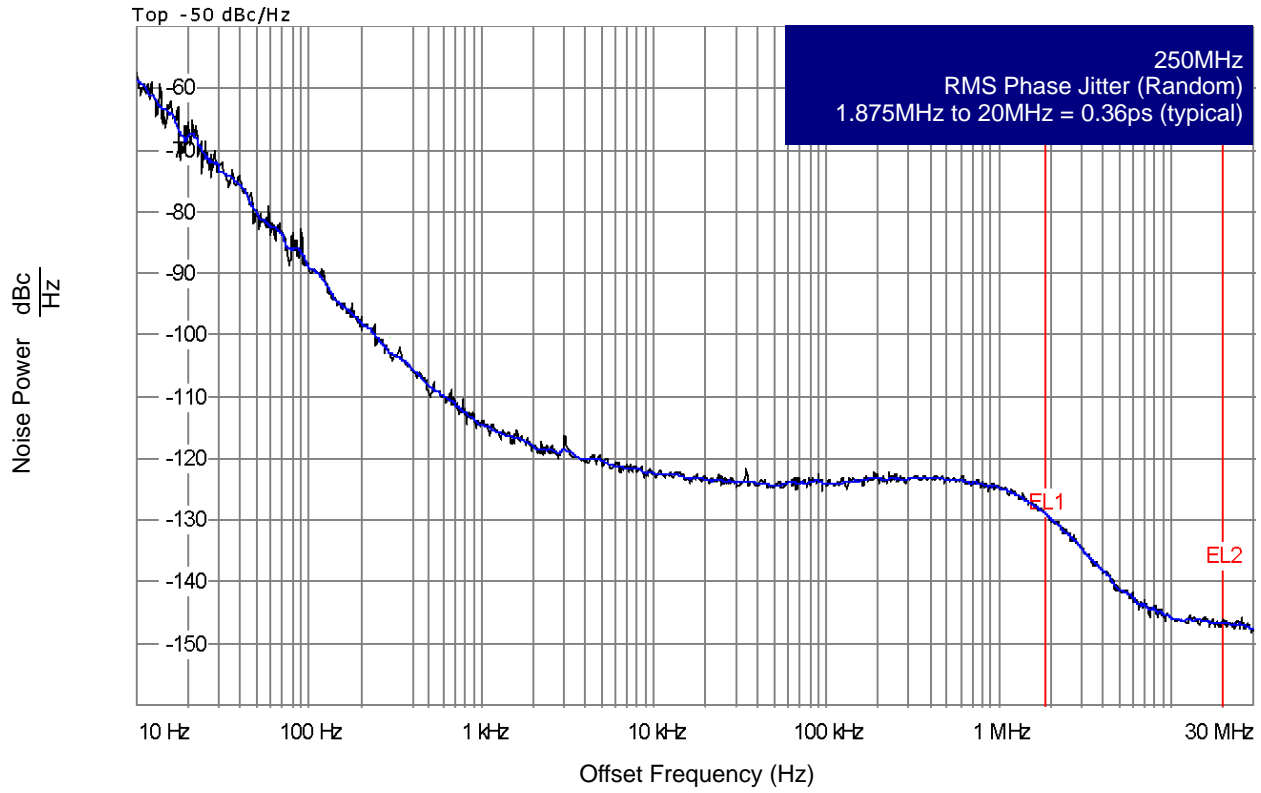
NOTE 1: Please refer to Phase Noise Plots.

**Table 5B. AC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$** 

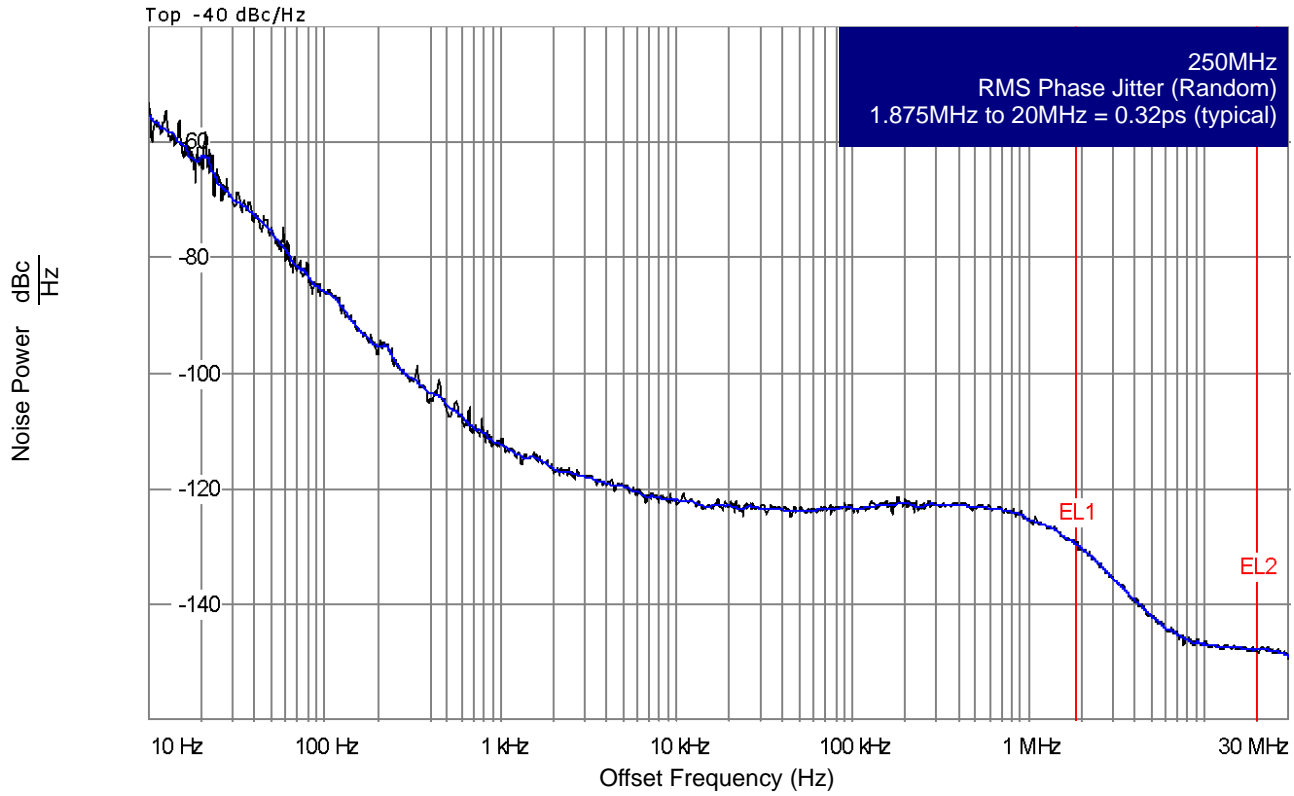
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		245		340	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 1	250MHz Integration Range: 1.875MHz – 20MHz		0.32		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to Phase Noise Plots.

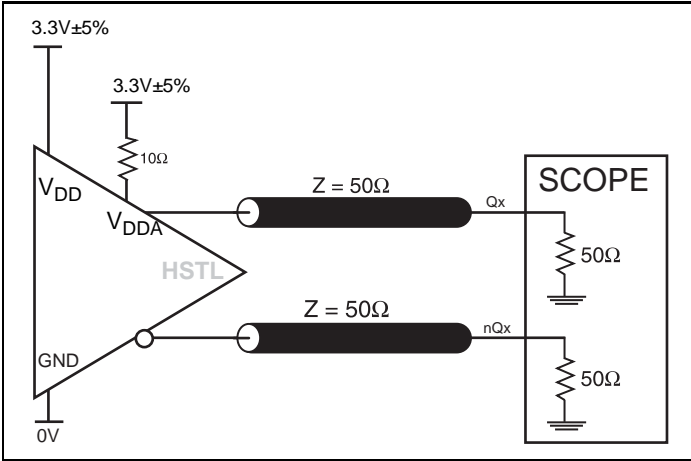
### Typical Phase Noise at 250MHz (3.3V)



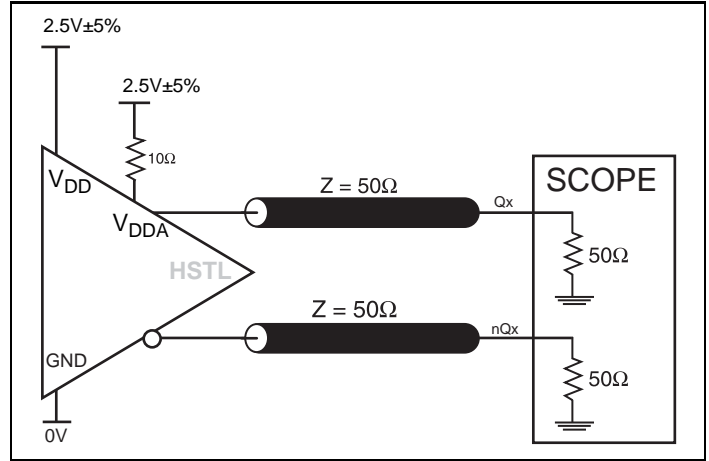
## Typical Phase Noise at 250MHz (2.5V)



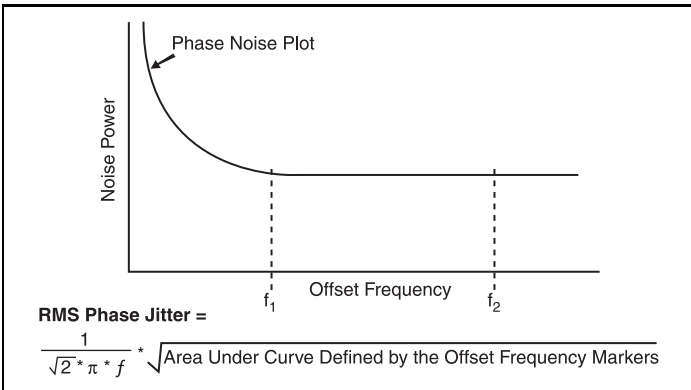
## Parameter Measurement Information



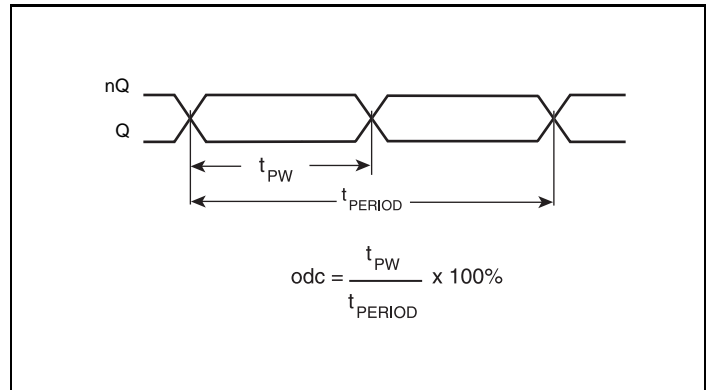
3.3V HSTL Output Load AC Test Circuit



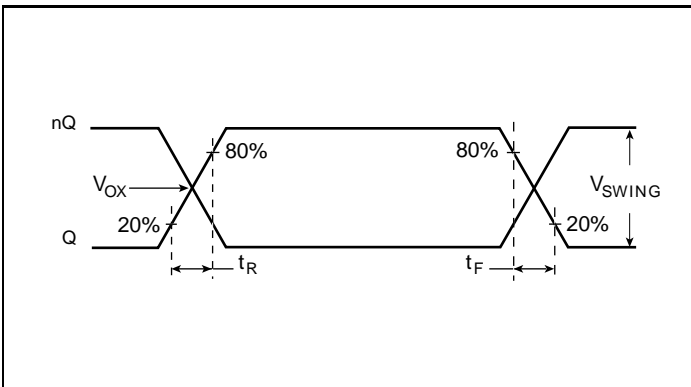
2.5V HSTL Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



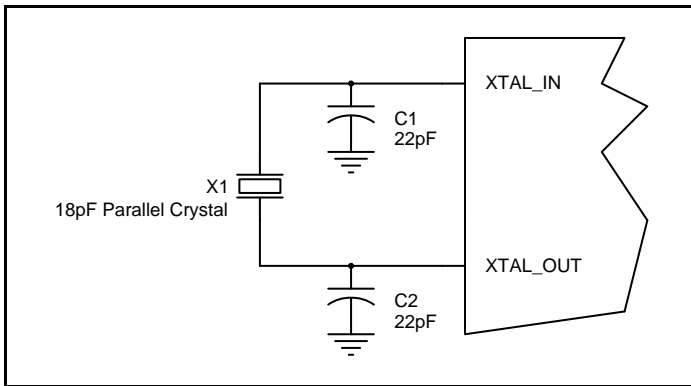
Output Rise/Fall Time

## Application Information

### Crystal Input Interface

The 842023 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel

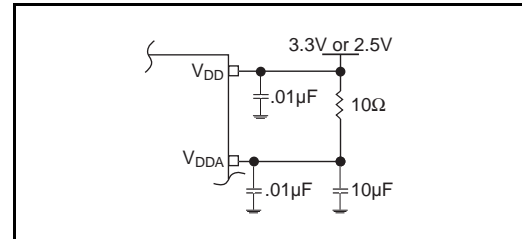
resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.



**Figure 1. Crystal Input Interface**

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 842023 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and 0.01 $\mu$ F bypass capacitors should be used for each pin. *Figure 3* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional 10 $\Omega$  resistor along with a 10 $\mu$ F bypass capacitor be connected to the  $V_{DDA}$  pin.



**Figure 3. Power Supply Filtering**



## Termination for HSTL Outputs

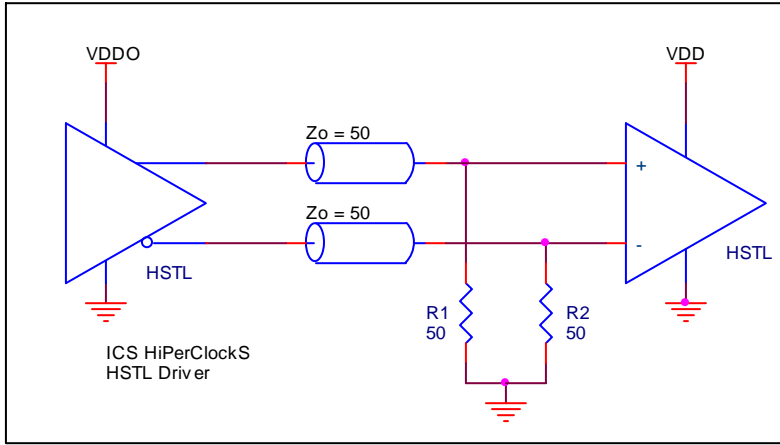


Figure 4. HSTL Output Termination

## Schematic Example

Figure 5 shows an example of the 842023 application schematic. In this example, the device is operated at  $V_{DD} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The  $C1 = 22pF$  and  $C2 = 22pF$  are recommended for frequency accuracy. For different

board layouts, the  $C1$  and  $C2$  may be slightly adjusted for optimizing frequency accuracy. An example of HSTL termination is shown in this schematic.

Note: Thermal pad (E-pad) must be connected to ground (GND).

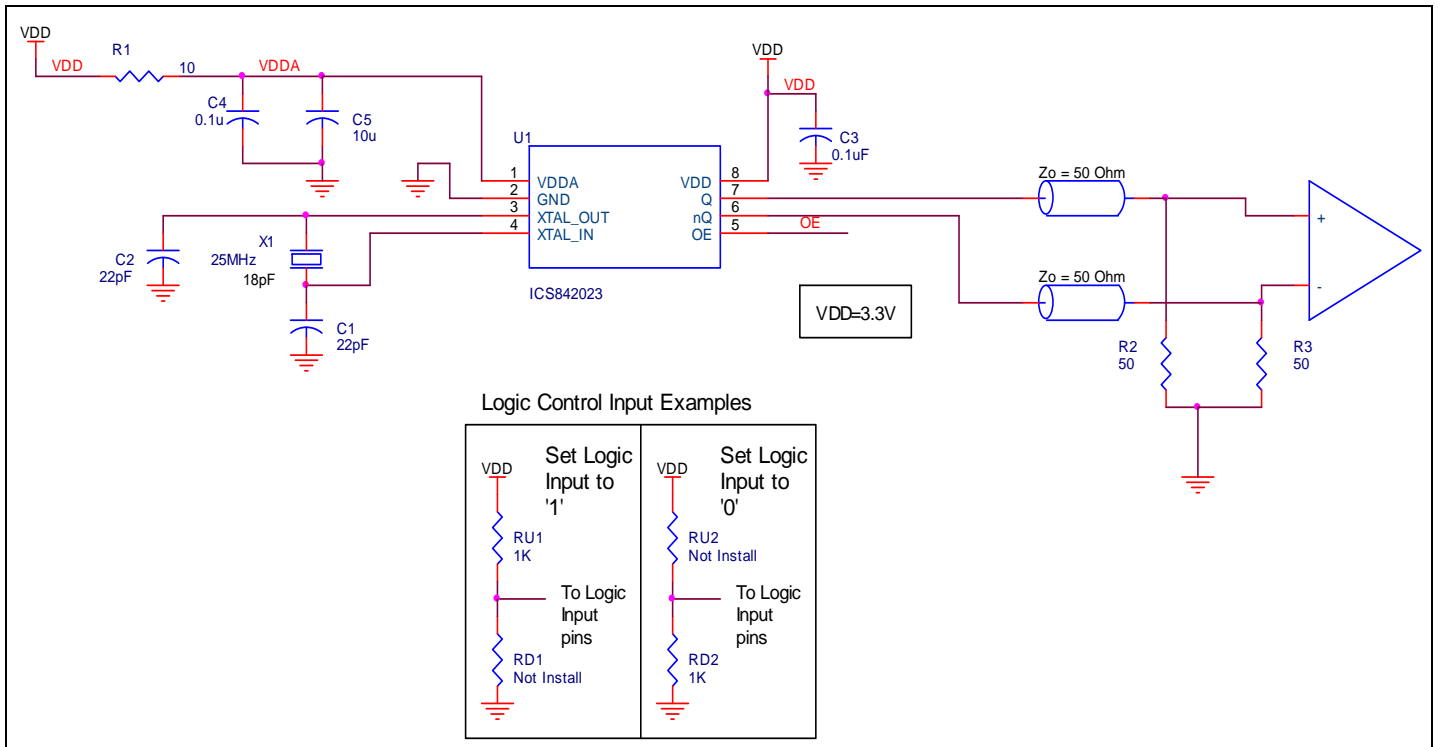


Figure 5. 842023 Schematic Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the 842023. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 842023 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (84mA + 11mA) = \mathbf{329.18mW}$
- Power (outputs)<sub>MAX</sub> = **94.32mW/Loaded Output pair**

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) = 329.18mW + 94.32mW = **423.49mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.423\text{W} * 129.5^\circ\text{C/W} = 124.8^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

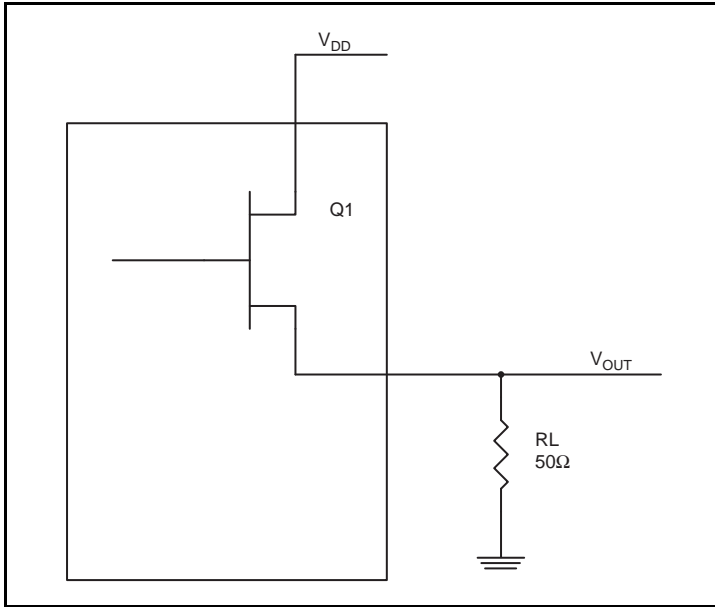
**Table 7. Thermal Resistance  $\theta_{JA}$  for 8 Lead TSSOP, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 6*.



**Figure 6. HSTL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd\_H is power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

$$Pd_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$$

$$Pd_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$$

$$Pd_H = (1.8V/50\Omega) * (3.465 - 1.8V) = 59.94mW$$

$$Pd_L = (0.6V/50\Omega) * (3.465 - 0.6V) = 34.38mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{94.32mW}$$

## Reliability Information

Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 8 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

## Transistor Count

The transistor count for 842023 is: 2538

## Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

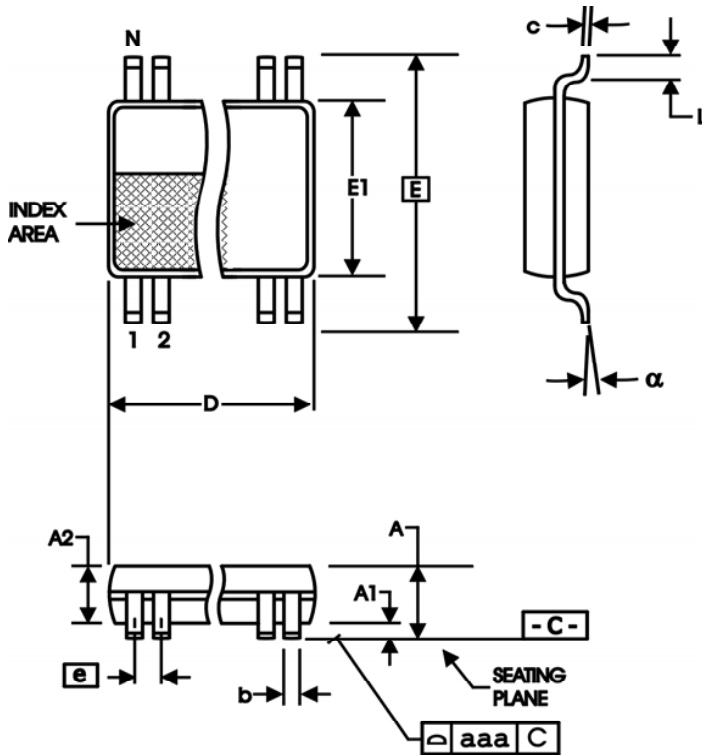


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 10. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
842023BGLF	023BL	"Lead-Free" 8 Lead TSSOP	Tube	0°C to 70°C
842023BGLFT	023BL	"Lead-Free" 8 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T4	1	Deleted HiPerClockS references throughout.	11/2/12
		4	Crystal Characteristics Table - added note.	
		7	Deleted application note, <i>LVC MOS to XTAL Interface</i> .	
		8	Added Note: Thermal pad (E-pad) must be connected to ground (GND).	
		12	Deleted quantity from tape and reel.	
A			Product Discontinuation Notice - Last time buy expires August 14, 2016. PDN CQ-15-04	8/14/15



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.