

FDMD8630

MOSFET – N-Channel, POWERTRENCH[®], Dual

30 V, 167 A, 1.0 m Ω

General Description

This package integrates two N-Channel devices connected internally in common-source configuration. This enables very low package parasitics and optimized thermal path to the common source pad on the bottom. Provides a very small footprint (5 x 6 mm) for higher power density.

Features

- Common Source Configuration to Eliminate PCB Routing
- Large Source Pad on Bottom of Package for Enhanced Thermals
- Max $r_{DS(on)} = 1.0\text{ m}\Omega$ at $V_{GS} = 10\text{ V}$, $I_D = 38\text{ A}$
- Max $r_{DS(on)} = 1.3\text{ m}\Omega$ at $V_{GS} = 4.5\text{ V}$, $I_D = 33\text{ A}$
- Ideal for Flexible Layout in Secondary Side Synchronous Rectification
- 100% UIL Tested
- This Device is Pb-Free and is RoHS Compliant

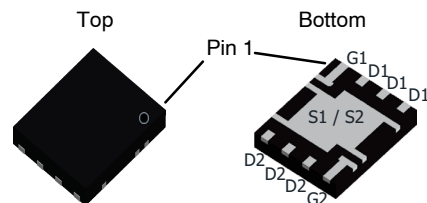
Applications

- Isolated DC-DC Synchronous Rectifiers
- Common Ground Load Switches



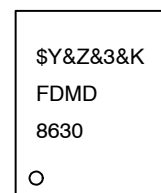
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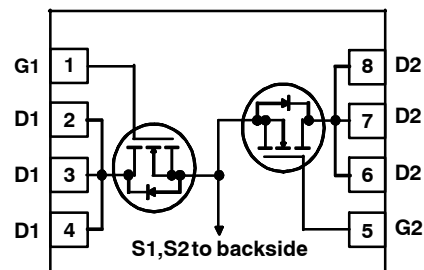
**PQFN8 5X6, 1.27P
CASE 483AS**

MARKING DIAGRAM



&Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDMD8630	= Specific Device Code

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMD8630

MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ Unless Otherwise Noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous – $T_C = 25^\circ\text{C}$ (Note 5)	167	A
	– Continuous – $T_C = 100^\circ\text{C}$ (Note 5)	106	
	– Continuous – $T_A = 25^\circ\text{C}$ (Note 1a)	38	
	– Pulsed – (Note 4)	1178	
EAS	Single Pulse Avalanche Energy (Note 3)	726	mJ
P_D	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$	43	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	55	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMD8630	FDMD8630	Power 5 x 6	13"	12 mm	3000 Units

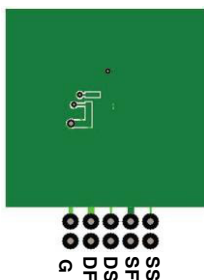
ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	30			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		15		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\ \text{V}, V_{DS} = 0\ \text{V}$			100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0	1.6	3.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 38\ \text{A}$		0.6	1.0	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 33\ \text{A}$		0.8	1.3	
		$V_{GS} = 4.5\ \text{V}, I_D = 33\ \text{A}, T_J = 125^\circ\text{C}$		0.9	1.5	
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}, I_D = 38\ \text{A}$		281		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = 15\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		7090	9930	pF
C_{oss}	Output Capacitance			2025	2835	pF
C_{rss}	Reverse Transfer Capacitance			212	300	pF
R_g	Gate Resistance		0.1	1.9	3.8	Ω
SWITCHING CHARACTERISTICS						

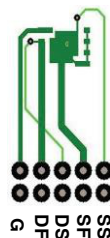
FDMD8630

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $55^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- E_{AS} of 726 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 22\text{ A}$, $V_{DD} = 30\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.1\text{ mH}$, $I_{AS} = 70\text{ A}$.
- Pulsed I_d please refer to Fig 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

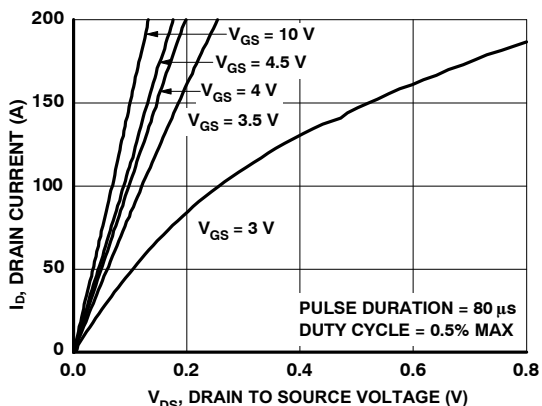
 $T_J = 25^\circ\text{C}$ Unless Otherwise Noted

Figure 1. On-Region Characteristics

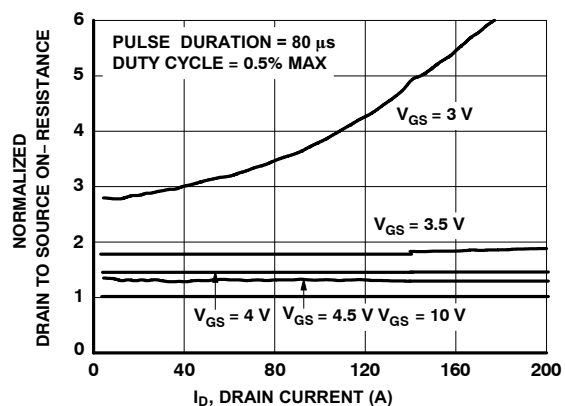


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

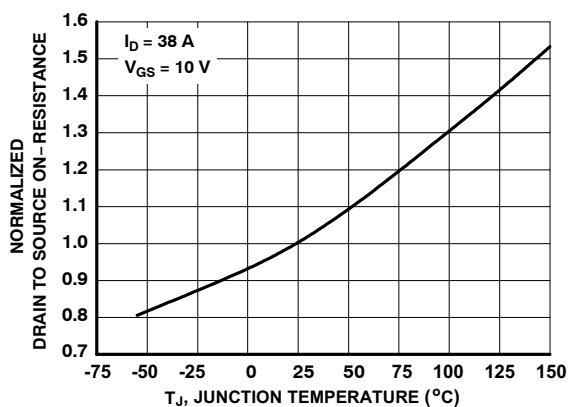


Figure 3. Normalized On Resistance vs Junction Temperature

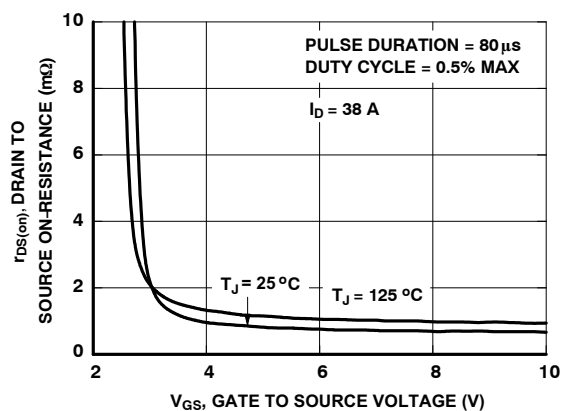


Figure 4. On-Resistance vs Gate to Source Voltage

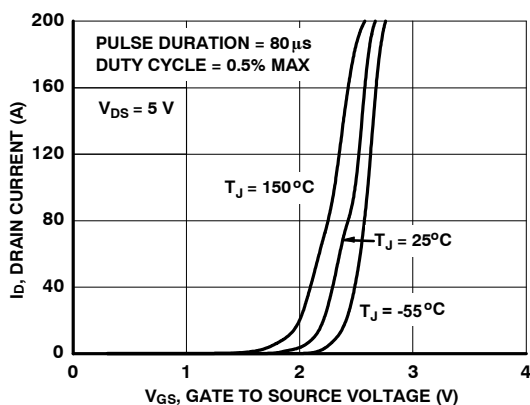


Figure 5. Transfer Characteristics

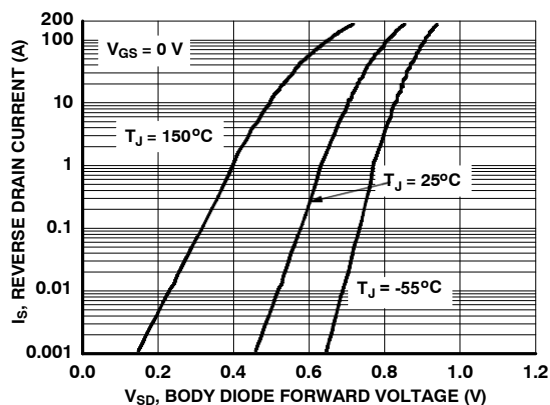


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

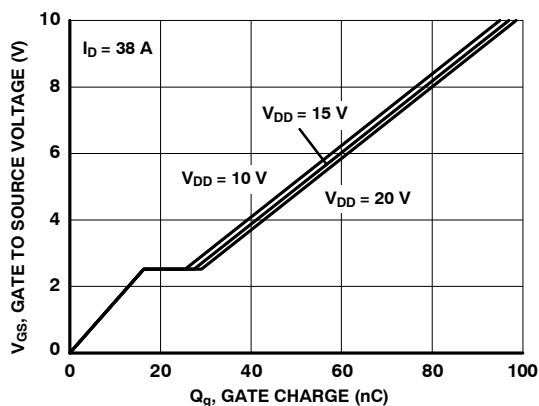


Figure 7. Gate Charge Characteristics

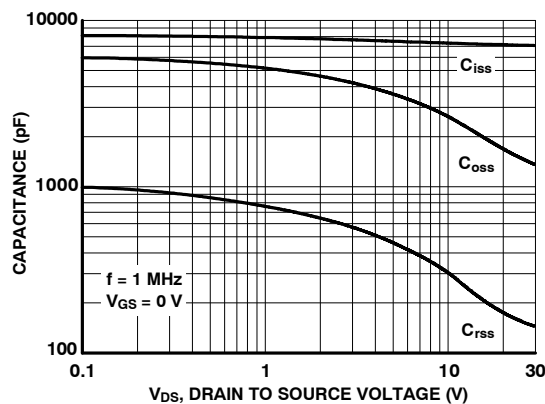


Figure 8. Capacitance vs Drain to Source Voltage

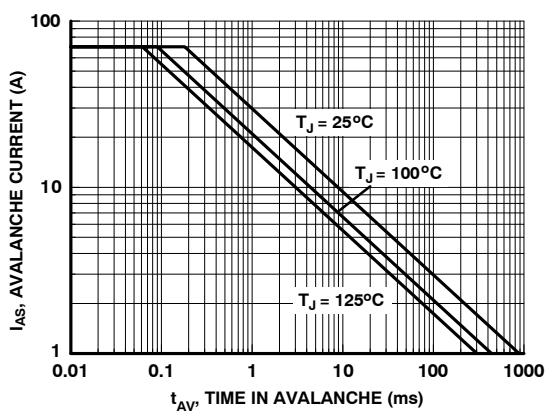


Figure 9. Unclamped Inductive Switching Capability

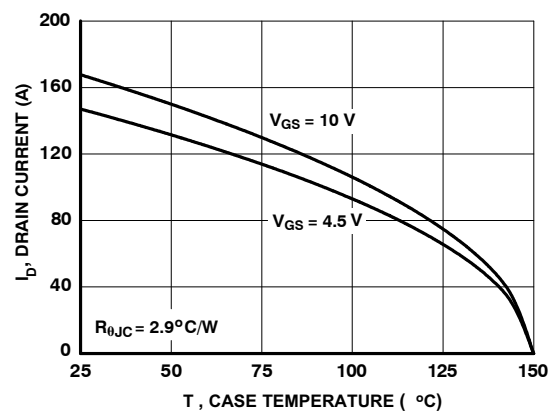


Figure 10. Maximum Continuous Drain Current vs Case Temperature

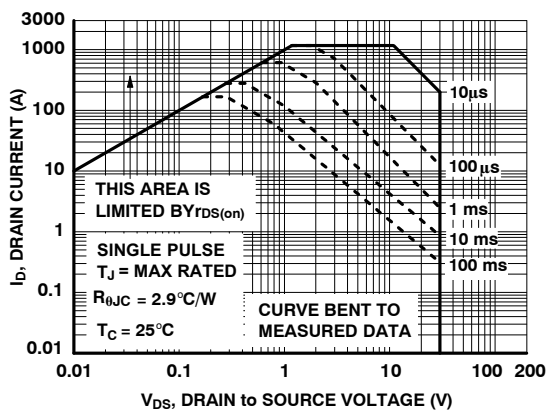


Figure 11. Forward Bias Safe Operating Area

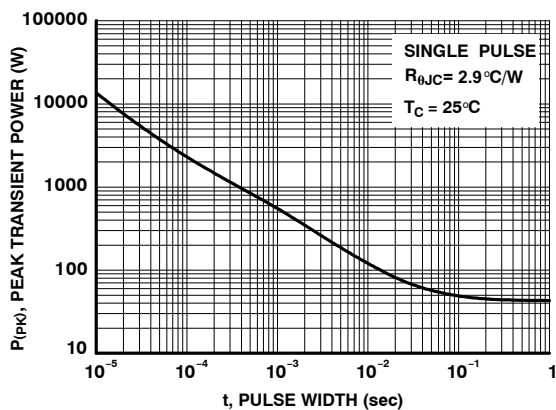


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

$T_J = 25^\circ\text{C}$ Unless Otherwise Noted (continued)

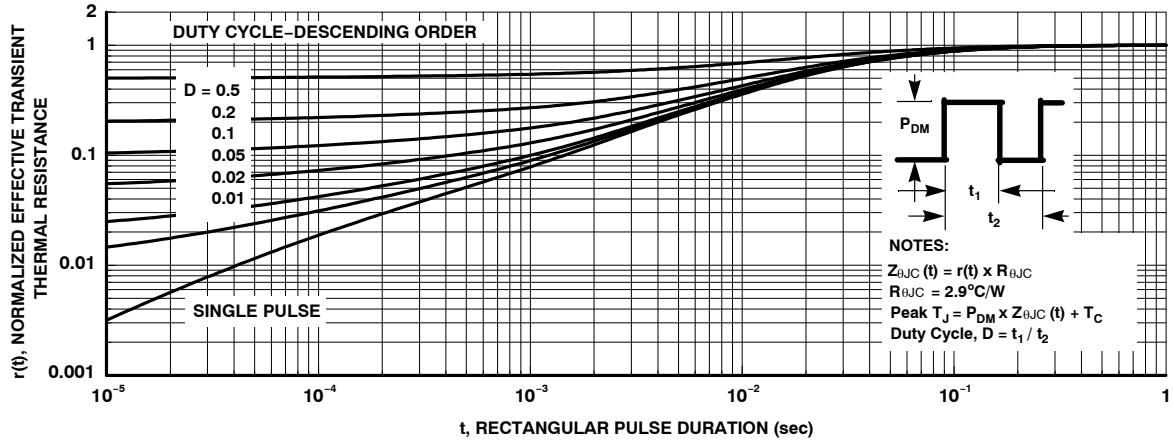
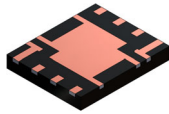


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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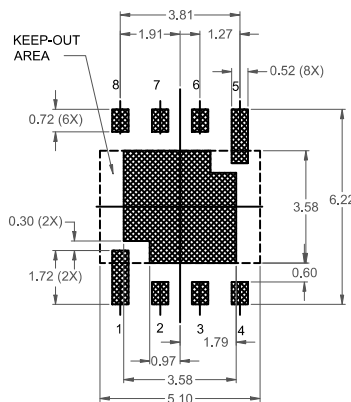
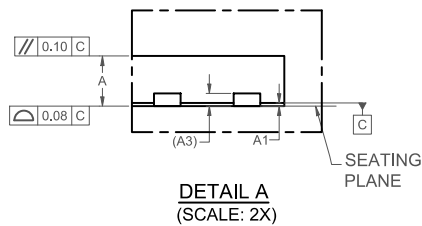
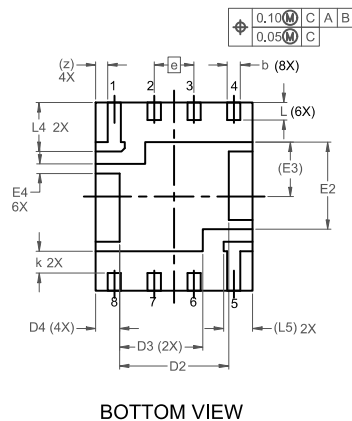
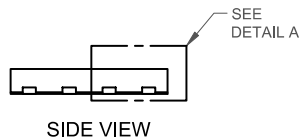
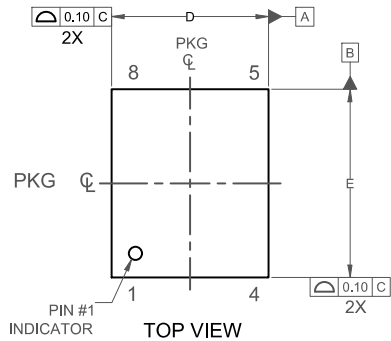


PQFN8 5X6, 1.27P CASE 483AS ISSUE A

DATE 17 MAY 2021

NOTES:

- A) PACKAGE REFERENCE :
TO JEDEC REGISTRATION, MO-240B, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME
Y14.5M-2009
- E) IT IS RECOMMENDED TO HAVE NO
TRACES OR VIAS WITHIN THE KEEP-OUT AREA



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PB-FREE STRATEGY AND SOLDERING
DETAILS, PLEASE DOWNLOAD THE ON
SEMICONDUCTOR SOLDERING AND
MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
b	0.37	0.42	0.47
A3	0.20 REF		
D	4.90	5.00	5.10
D2	3.38	3.48	3.58
D3	2.55	2.65	2.75
D4	0.66	0.76	0.86
E	5.90	6.00	6.10
E2	2.68	2.78	2.88
E3	1.74 REF		
E4	0.25	0.30	0.35
e	1.27 BSC		
k	0.60	0.70	0.80
L	0.46	0.56	0.66
L4	1.46	1.56	1.66
L5	0.82	0.92	1.02
z	0.39 REF		

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