FPC401 Quad Port Controller

1 Features

- Supports Control Signal Management and I2C Aggregation Across Four Ports
- Combine Multiple FPC401s to Control 56 Total Ports Through a Single Host Interface
- Eliminates Need for Discrete I2C Muxes, LED Drivers, and High-Pin-Count FPGA/CPLD Control Devices
- Reduces PCB Routing Complexity by Handling All Low-Speed Control Signals Close to the Port
- Selectable I2C (Up to 1 MHz) or SPI (Up to 10 MHz) Host Control Interface
- Automatic Pre-Fetching of Critical, User-Specified Data From the Modules
- Low Single-Port and Multi-Port Read/Write Latency: <50 µs for SPI Mode, <400 µs for I2C Mode
- Broadcast Mode Allows Writes to All Ports Simultaneously Across All FPC401 Controllers
- Advanced LED Features for Port Status Indication, Including Programmable Blinking and Dimming
- Customizable Interrupt Events
- Separate Host-Side I/O Voltage: 1.8-V to 3.3-V
- Small QFN Package Enabling Placement on Bottom Side of PCB Underneath Ports

2 Applications

- ToR/Aggregation/Core Switch and Router SFP+/QSFP+ Port Control
- SAS External Cable Management Interface Control
- Video Switch & Router SFP+/QSFP+ Port Control

3 Description

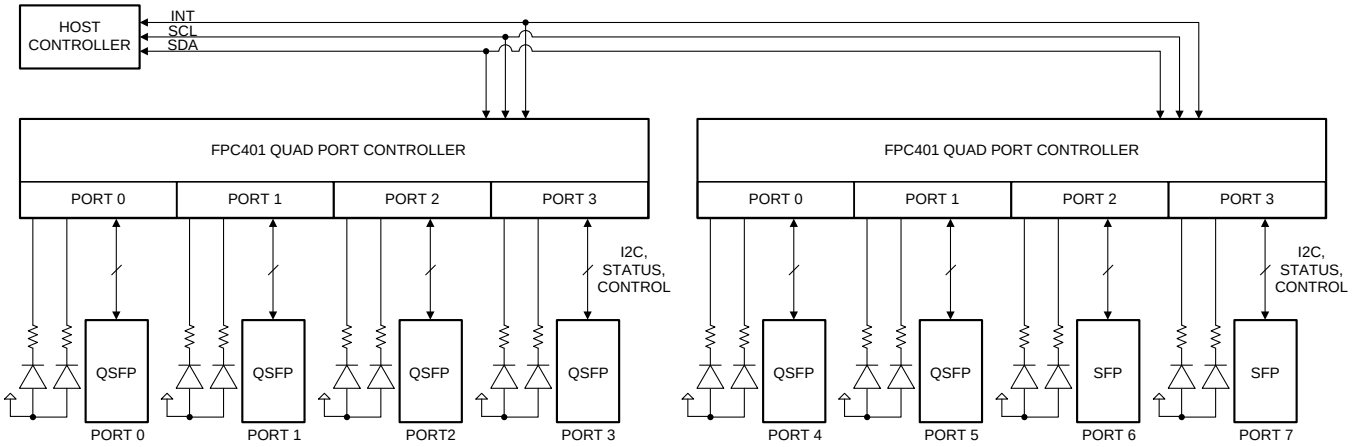
The FPC401 quad port controller serves as a low-speed signal aggregator for common port types such as SFP+, QSFP+, and SAS. The FPC401 aggregates all low-speed control and I2C signals across four ports and presents a single easy-to-use management interface to the host (I2C or SPI). Multiple FPC401s can be used in high-port-count applications with one common control interface to the host. The FPC401 is designed to allow placement on the bottom side of the PCB, underneath the press fit connector, to simplify routing. This localized control of the ports' low-speed signals cuts system BOM cost by enabling the use of smaller IO count control devices (FPGAs, CPLDs, MCUs) and by reducing routing layer congestion.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
FPC401	QFN (56)	5.00 mm × 11.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2016	*	Initial release.

5 Description (continued)

The FPC401 is compatible with standard SFF-8431, SFF-8436, and SFF-8449 low-speed management interfaces, including a dedicated 100-kHz and 400-kHz I2C interface to each port. Additional general-purpose pins are available to perform functions such as driving port status LEDs or controlling power switches. The LED drivers have convenience features such as programmable blinking and dimming. The interface to the host controller can operate on a separate supply voltage between 1.8-V and 3.3-V to support low-voltage I/Os.

The FPC401 can prefetch data from user-specified registers in each module, making the data readily accessible to the host through a fast I2C (up to 1 MHz) or SPI (up to 10 MHz) interface. In addition, the FPC401 can trigger an interrupt to the host whenever critical, user-configurable events occur associated with any of the ports under its control. This eliminates the need to continuously poll the modules.

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation, see the following:

- *FPC401 Programmer's Guide* (SNLU221)
- *FPC401 Evaluation Module (EVM) User's Guide* (SNLU222)

Click here to request access to these documents in the FPC401 MySecure folder.

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
FPC401RHUR	ACTIVE	WQFN	RHU	56	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	FPC401	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

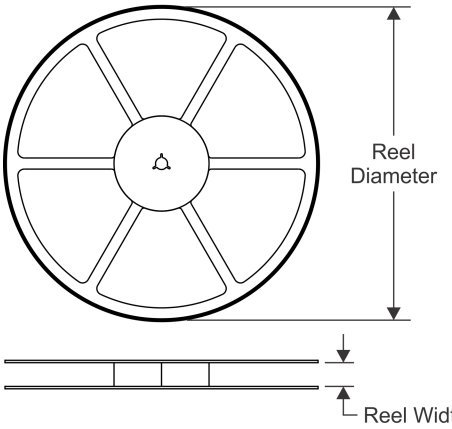
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

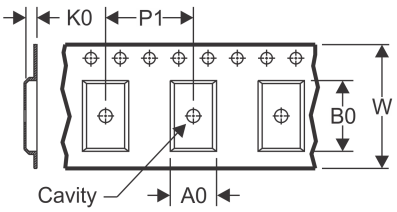
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

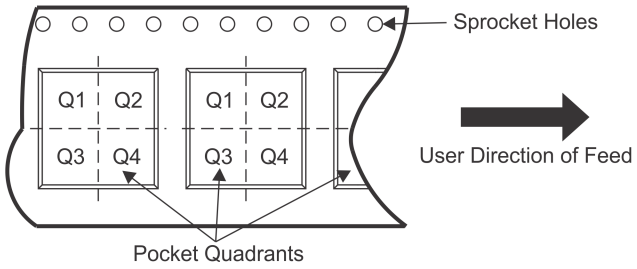


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

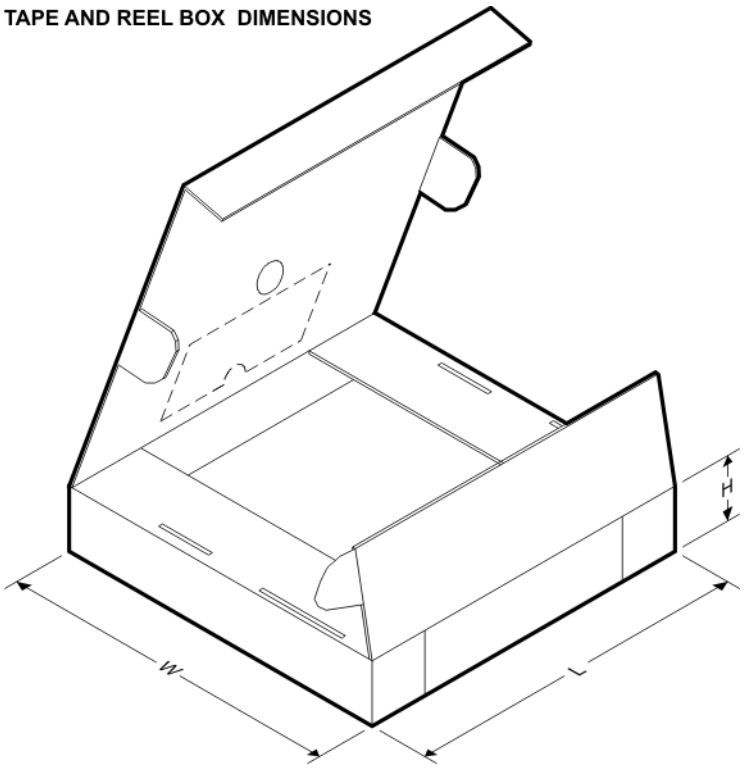
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
FPC401RHUR	WQFN	RHU	56	2000	330.0	24.4	5.3	11.3	1.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

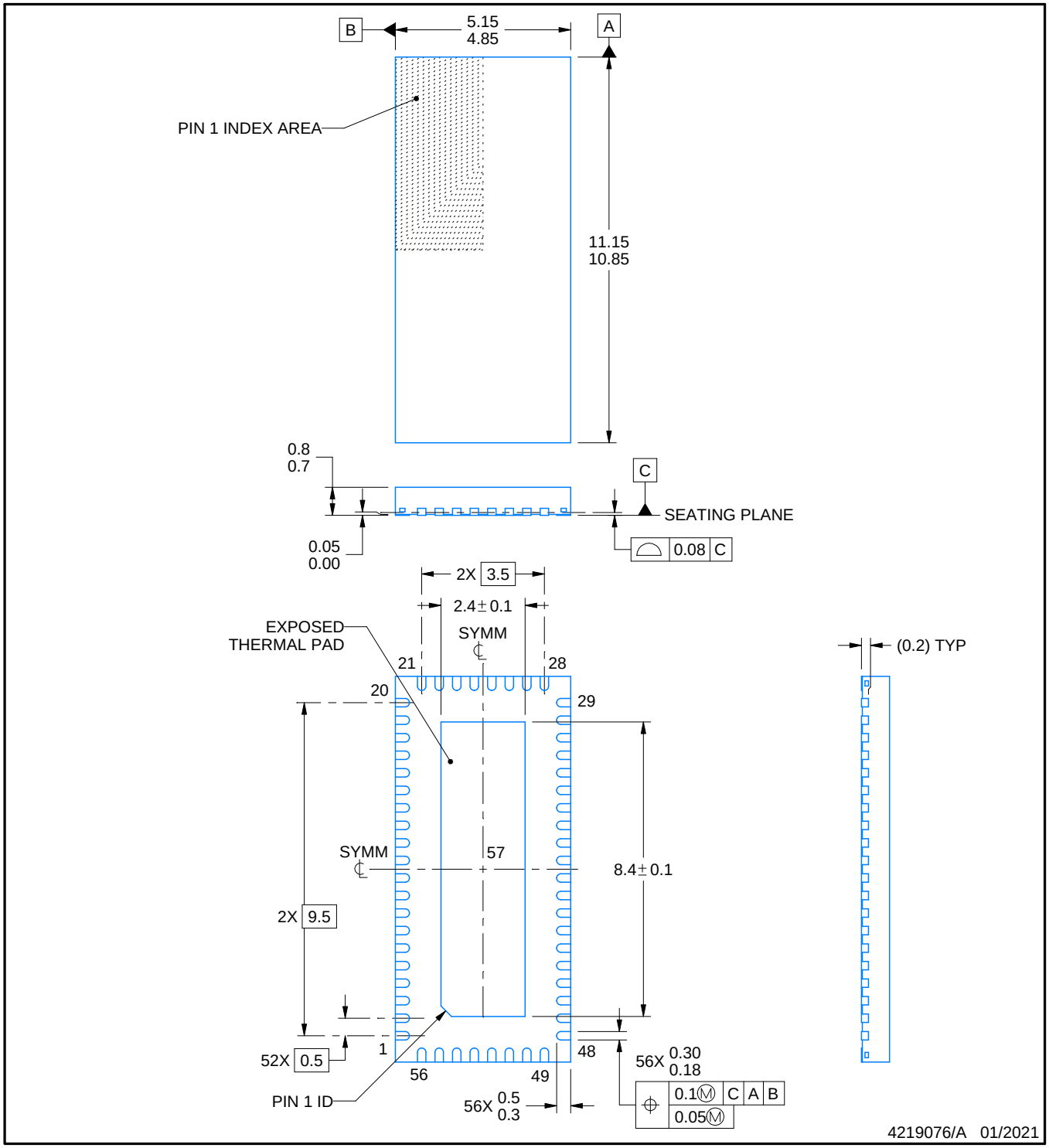
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
FPC401RHUR	WQFN	RHU	56	2000	367.0	367.0	45.0

PACKAGE OUTLINE

RHU0056A

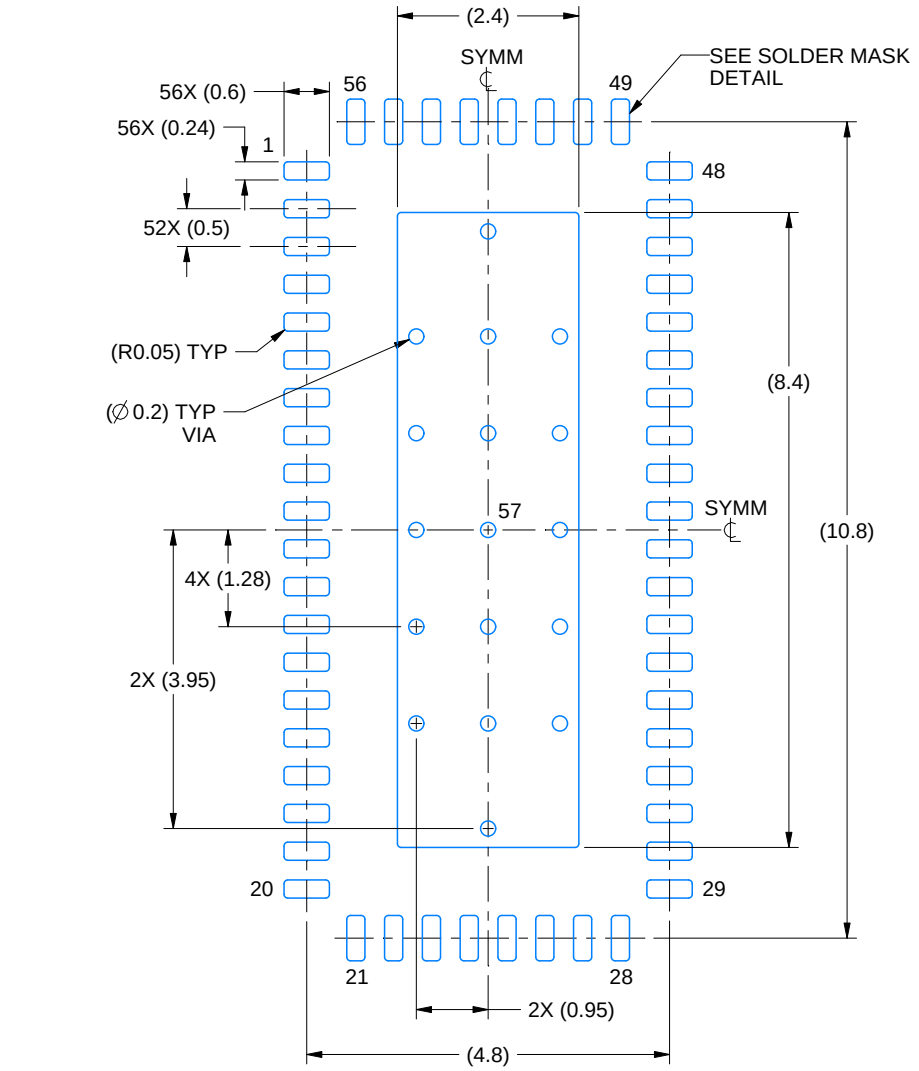
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

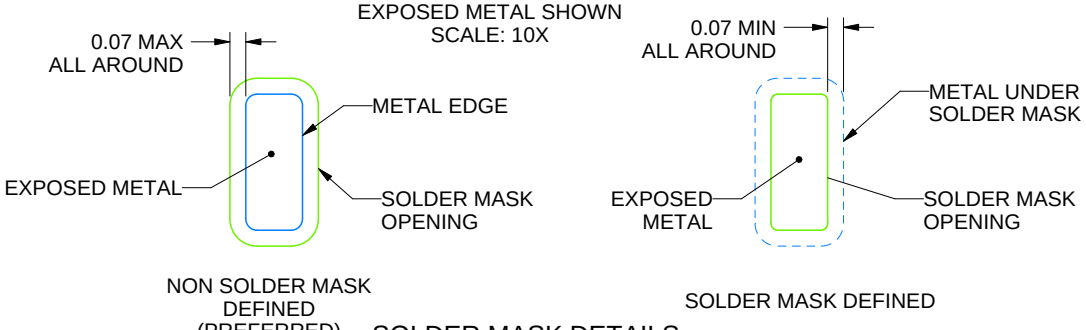
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 10X



SOLDER MASK DETAILS

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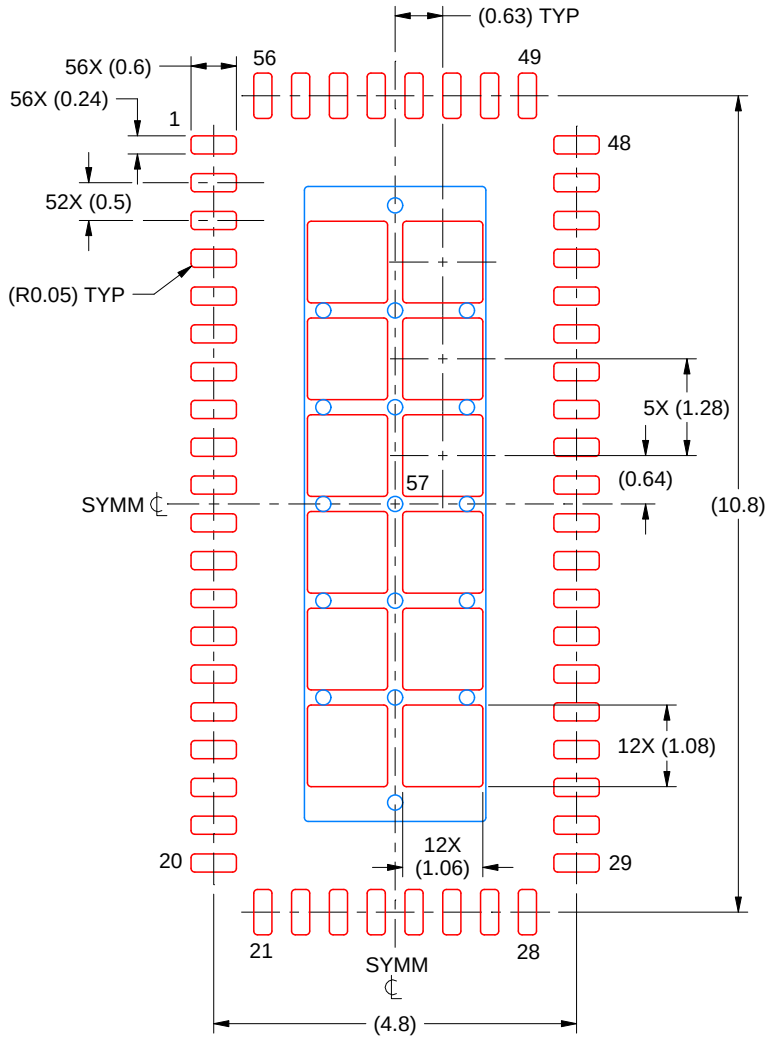
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 57
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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