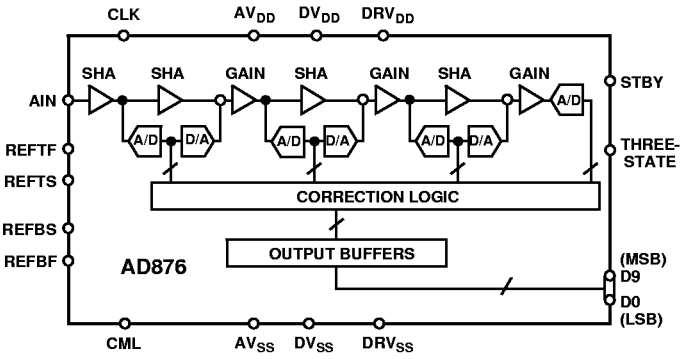
10-Bit 20 MSPS 160 mW CMOS A/D Converter

AD876

FEATURES

CMOS 10-Bit 20 MSPS Sampling A/D Converter
Pin-Compatible 8-Bit Option
Power Dissipation: 160 mW
+5 V Single Supply Operation
Differential Nonlinearity: 0.5 LSB
Guaranteed No Missing Codes
Power Down (Standby) Mode
Three-State Outputs
Digital I/Os Compatible with +5 V or +3.3 V Logic
Adjustable Reference Input
Small Size: 28-Lead SOIC, 28-Lead SSOP, or 48-Lead Thin Quad Flatpack (TQFP)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD876 is a CMOS, 160 mW, 10-bit, 20 MSPS analog-to-digital converter (ADC). The AD876 has an on-chip input sample-and-hold amplifier. By implementing a multistage pipelined architecture with output error correction logic, the AD876 offers accurate performance and guarantees no missing codes over the full operating temperature range. Force and sense connections to the reference inputs minimize external voltage drops.

The AD876 can be placed into a standby mode of operation reducing the power below 50 mW. The AD876's digital I/O interfaces to either +5 V or +3.3 V logic. Digital output pins can be placed in a high impedance state; the format of the output is straight binary coding.

The AD876's speed, resolution and single-supply operation ideally suit a variety of applications in video, multimedia, imaging, high speed data acquisition and communications. The AD876's low power and single-supply operation satisfy requirements for high speed portable applications. Its speed and resolution ideally suit charge coupled device (CCD) input systems such as color scanners, digital copiers, electronic still cameras and camcorders.

The AD876 comes in a space saving 28-lead SOIC and 48-lead thin quad flatpack (TQFP) and is specified over the commercial (0°C to +70°C) temperature range.

PRODUCT HIGHLIGHTS

Low Power

The AD876 at 160 mW consumes a fraction of the power of presently available 8- or 10-bit, video speed converters. Power-down mode and single-supply operation further enhance its desirability in low power, battery operated applications such as electronic still cameras, camcorders and communication systems.

Very Small Package

The AD876 comes in a 28-lead SOIC, 28-lead SSOP, and 48-lead surface mount, thin quad flat package. The TQFP package is ideal for very tight, low headroom designs.

Digital I/O Functionality

The AD876 offers three-state output control.

Pin Compatible Upgrade Path

The AD876 offers the option of laying out designs for eight bits and migrating to 10-bit resolution if prototype results warrant.

REV. B

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AD876–SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFB} = +4.0 V, V_{REFB} = +2.0 V, f_{CLOCK} = 20 MSPS, unless otherwise noted)

Parameter	AD876JR-8 Min	AD876JR-8 Typ	AD876JR-8 Max	AD876 Min	AD876 Typ	AD876 Max	Units
RESOLUTION		8			10		Bits
DC ACCURACY							
Integral Nonlinearity (INL)		±0.3	±1.0		±1.0		LSB
Differential Nonlinearity (DNL)		±0.1	±0.75		±0.5	±1	LSB
No Missing Codes		GUARANTEED			GUARANTEED		
Offset Error		0.1			0.4		% FSR
Gain Error		0.1			0.2		% FSR
ANALOG INPUT							
Input Range		2			2		V p-p
Input Capacitance		5.0			5.0		pF
REFERENCE INPUT							
Reference Top Voltage	3.5	4.0	4.5	3.5	4.0	4.5	V
Reference Bottom Voltage	1.6	2.0	2.5	1.6	2.0	2.5	V
Reference Input Resistance		250			250		Ω
Reference Input Current		8.0			8.0		mA
Reference Top Offset		35			35		mV
Reference Bottom Offset		35			35		mV
DYNAMIC PERFORMANCE							
Effective Number of Bits							
f_{IN} = 1 MHz		7.8			9.0		Bits
f_{IN} = 3.58 MHz	7.4	7.8		8.2	9.0		Bits
f_{IN} = 10 MHz		7.5			8.2		Bits
Signal-to-Noise and Distortion (S/N+D) Ratio							
f_{IN} = 1 MHz		49			56		dB
f_{IN} = 3.58 MHz	46	49		51	56		dB
f_{IN} = 10 MHz		47			51		dB
Total Harmonic Distortion (THD)							
f_{IN} =1 MHz		–62			–62		dB
f_{IN} = 3.58 MHz		–62	–56		–62	–56	dB
f_{IN} =10 MHz		–60			–60		dB
Spurious Free Dynamic Range[2]		–65			–65		dB
Full Power Bandwidth		150			150		MHz
Differential Phase		0.5			0.5		Degree
Differential Gain		1			1		%
POWER SUPPLIES							
Operating Voltage							
AV_{DD}[1]	+4.5		+5.25	+4.5		+5.25	Volts
DV_{DD}[1]	+4.5		+5.25	+4.5		+5.25	Volts
DRV_{DD}	+3.0		+5.25	+3.0		+5.25	Volts
Operating Current							
IAV_{DD}		20	25		20	25	mA
IDV_{DD}		12	16		12	16	mA
$IDRV_{DD}$		0.1	1		0.1	1	mA
POWER CONSUMPTION		160	190		160	190	mW
TEMPERATURE RANGE							
Specified	0		+70	0		+70	°C

NOTES

[1]AV_{DD} and DV_{DD} must be within 0.5 V of each other to maintain specified performance levels.

[2]3.58 MHz Input Frequency.

Specifications subject to change without notice. See Definition of Specifications for additional information.

DIGITAL SPECIFICATIONS

(T_{MIN} to T_{MAX} with AV_{DD} = +5.0 V, DV_{DD} = +5.0 V, DRV_{DD} = +3.3 V, V_{REFT} = +4.0 V, V_{REFB} = +2.0 V, f_{CLOCK} = 20 MSPS, C_L = 20 pF unless otherwise noted)

Parameter	Symbol	DRV_{DD}	AD876 Min	AD876 Typ	AD876 Max	Units
LOGIC INPUT						
High Level Input Voltage	V_{IH}	3.0	2.4			V
		5.0	4.0			V
		5.25	4.2			V
Low Level Input Voltage	V_{IL}	3.0			0.6	V
		5.0			1.0	V
		5.25			1.05	V
High Level Input Current	I_{IH}	5.0	–10		+10	µA
Low Level Input Current	I_{IL}	5.0	–50		+50	µA
Low Level Input Current (CLK Only)	I_{IL}	5.0	–10		+10	µA
Input Capacitance	C_{IN}			5		pF
LOGIC OUTPUTS						
High Level Output Voltage	V_{OH}					
(I_{OH} = 50 µA)		3.0	2.4			V
		5.0	3.8			V
(I_{OH} = 0.5 mA)		5.0	2.4			V
Low Level Output Voltage	V_{OL}					
(I_{OL} = 50 µA)		3.6			0.7	V
		5.25			1.05	V
(I_{OL} = 0.6 mA)		5.25			0.4	V
Output Capacitance	C_{OUT}			5		pF
Output Leakage Current	I_{OZ}		–10		10	µA

Specifications subject to change without notice.

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate[1]		20			MHz
Clock Period	t_C		50		ns
Clock High	t_{CH}	23	25		ns
Clock Low	t_{CL}	23	25		ns
Output Delay	t_{OD}	10	20		ns
Pipeline Delay (Latency)				3.5	Clock Cycles
Aperture Delay Time			4		ns
Aperture Jitter			22		ps

NOTE
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.

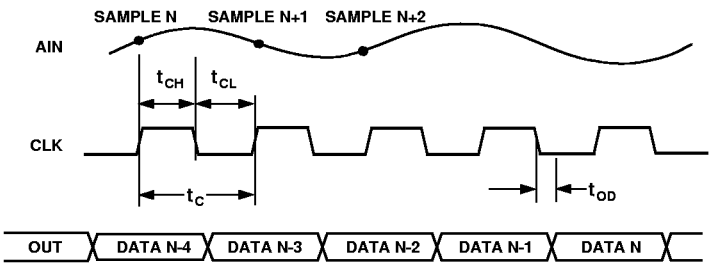


Figure 1. Timing Diagram

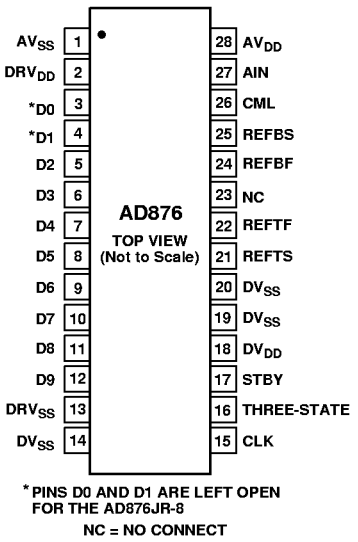
PIN FUNCTION DESCRIPTIONS

Symbol	SOIC Pin No.	TQFP Pin No.	Type	Name and Function
D0 (LSB)	3	1	DO	Least Significant Bit.
D1–D4	4–7	2–5	DO	Data Bits 1 through 4.
D5–D8	8–11	8–11		Data Bits 5 through 8.
D9 (MSB)	12	12	DO	Most Significant Bit.
THREE-STATE	16	23	DI	THREE-STATE = LOW or N/C: Normal Operating Mode; THREE-STATE = HIGH: High Impedance Outputs
STBY	17	24	DI	STBY = LOW or N/C: Normal Operating Mode; STBY = HIGH: Standby Mode
CLK	15	22	DI	Clock Input.
CML	26	38	AO	Bypass Pin for an Internal Bias Point.
REFTF	22	30	AI	Reference Top Force.
REFBF	24	34	AI	Reference Bottom Force.
REFTS	21	29	AI	Reference Top Sense.
REFBS	25	35	AI	Reference Bottom Sense.
AIN	27	39	AI	Analog Input.
AV_{DD}	28	42	P	+5 V Analog Supply.
AV_{SS}	1	44	P	Analog Ground.
DV_{DD}	18	26	P	+5 V Digital Supply.
DV_{SS}	14, 19, 20	17, 27, 28	P	Digital Ground.
DRV_{DD}	2	45	P	+3.3 V/+5 V Digital Supply. Supply for digital input and output buffers.
DRV_{SS}	13	16	P	+3.3 V/+5 V Digital Ground. Ground for digital input and output buffers.

Type: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power.

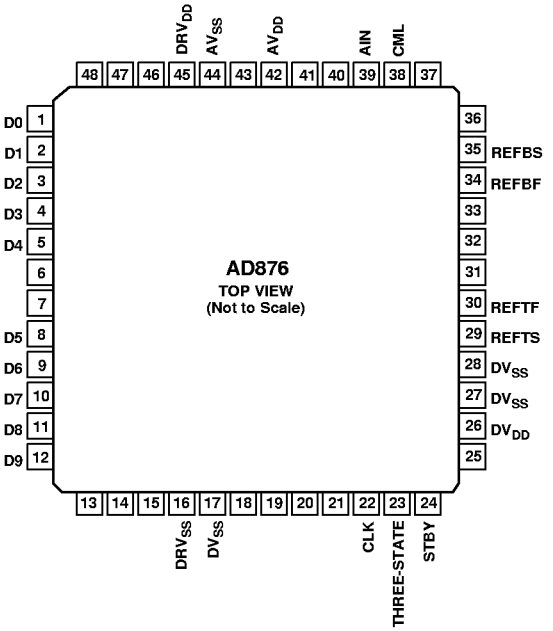
PIN CONFIGURATIONS

SOIC/SSOP



*PINS D0 AND D1 ARE LEFT OPEN FOR THE AD876JR-8
NC = NO CONNECT

TQFP



ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AV_{SS}	–0.5	+6.5	Volts
DV_{DD}, DRV_{DD}	DV_{SS}, DRV_{SS}	–0.5	+6.5	Volts
AV_{SS}	DV_{SS}, DRV_{SS}	–0.5	+0.5	Volts
AIN	AV_{SS}	–0.5	+6.5	Volts
REFTS, REFTF				
REFBS, REFBF	AV_{SS}	–0.5	+6.5	Volts
Digital Inputs, CLK	DV_{SS}, DRV_{SS}	–0.5	+6.5	Volts
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD876JR	0°C to +70°C	28-Lead SOIC	R-28
AD876JST-Reel	0°C to +70°C	48-Lead TQFP (Tape and Reel 13")	ST-48
AD876JR-8	0°C to +70°C	28-Lead SOIC	R-28
AD876AR	–40°C to +85°C	28-Lead SOIC	R-28
AD876ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD876JRS	0°C to +70°C	28-Lead SSOP	RS-28
AD876JRS-8	0°C to +70°C	28-Lead SSOP	RS-28

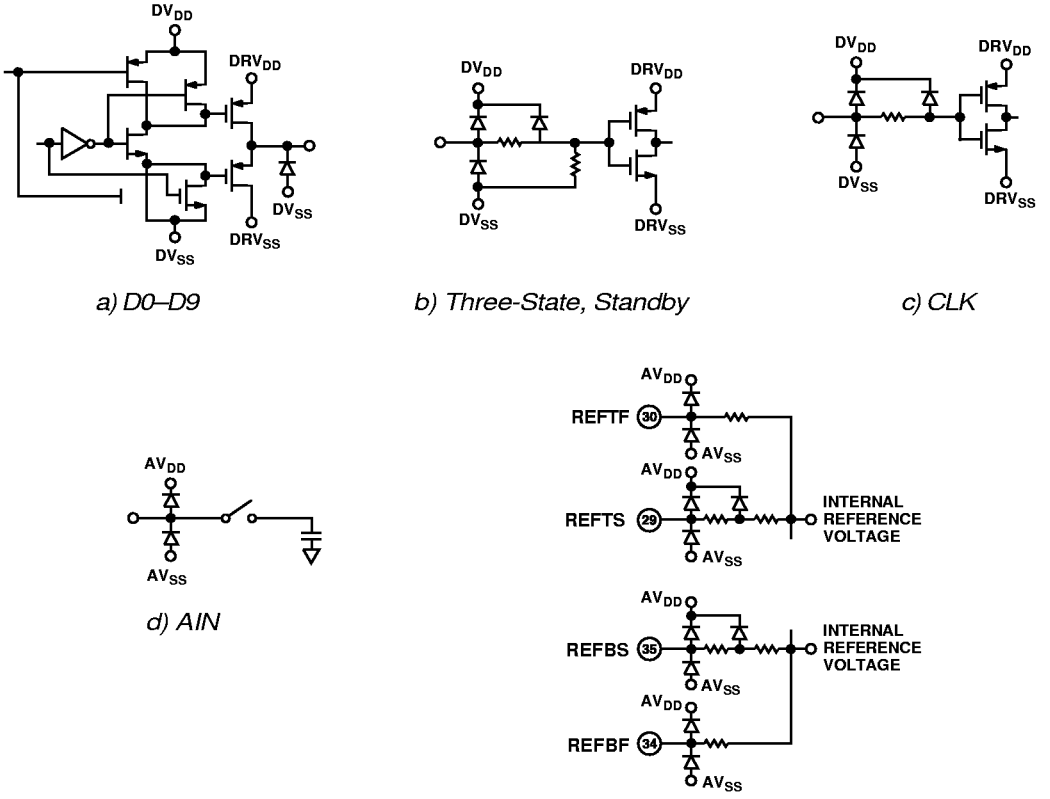


Figure 2. Equivalent Circuits

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD876 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD876–Typical Performance Characteristics

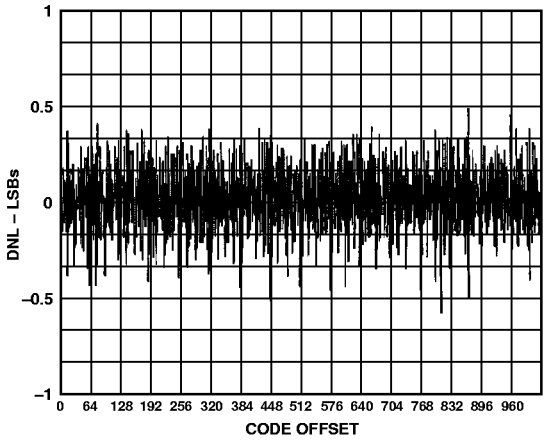


Figure 3. AD876 Typical DNL

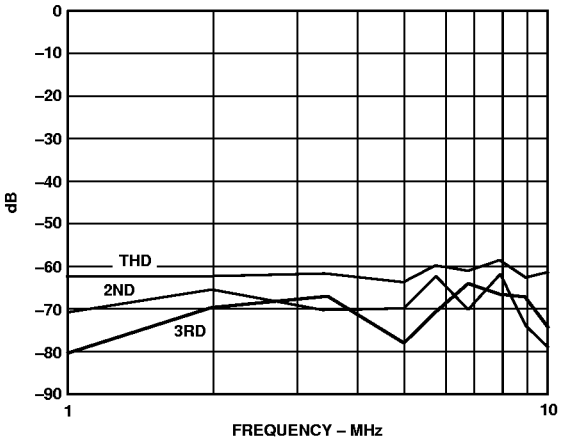


Figure 6. THD vs. Input Frequency 2nd, 3rd Harmonics

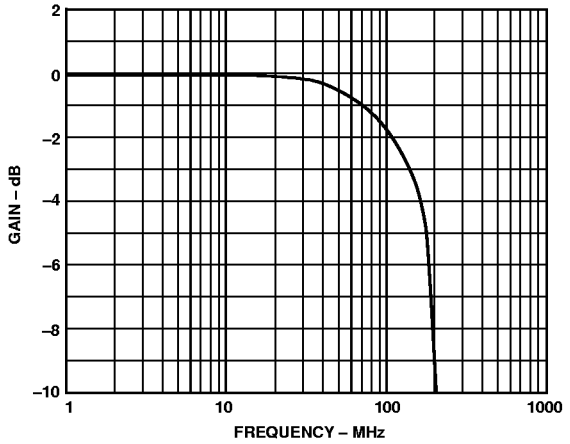


Figure 4. Full Power Bandwidth

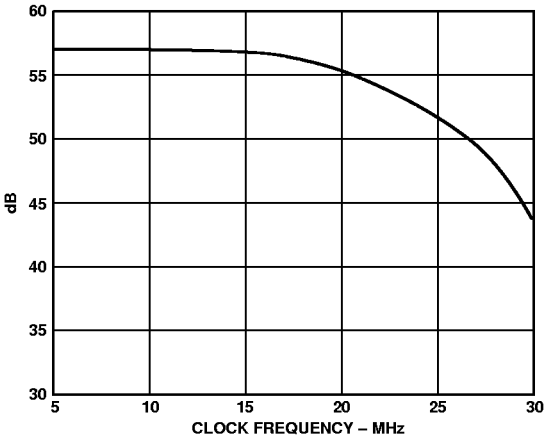


Figure 7. SINAD vs. CLK Frequency (AIN = –0.5 dB)

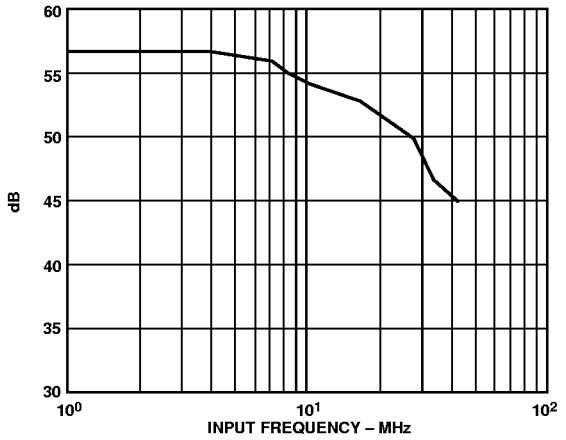


Figure 5. SINAD vs. Input Frequency (f_{CLK} = 20 MSPS, AIN = –0.5 dB)

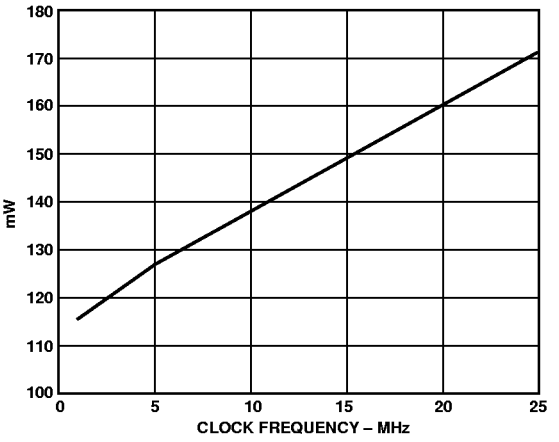


Figure 8. Power Consumption vs. Sample Rate

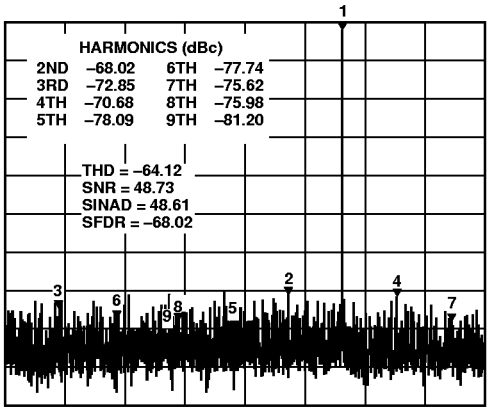


Figure 9. AD876JR-8 Typical FFT (f_{IN} = 3.58 MHz, AIN = –0.5 dB, f_{CLOCK} = 20 MSPS)

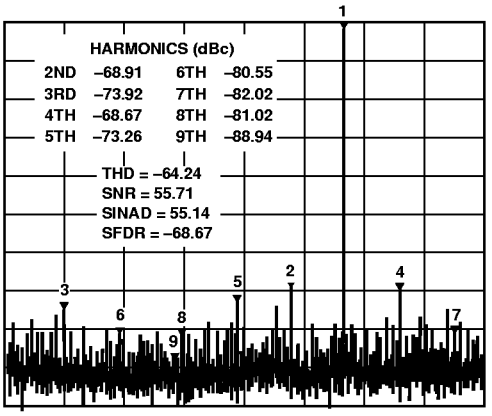


Figure 10. AD876 Typical FFT (f_{IN} = 3.58 MHz, AIN = –0.5 dB, f_{CLOCK} = 20 MSPS)

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) are guaranteed.

OFFSET ERROR

The first transition should occur at a level 1/2 LSB above "zero." Offset is defined as the deviation of the actual first code transition from that point.

GAIN ERROR

The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between the first and last code transitions.

PIPELINE DELAY (LATENCY)

The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

REFERENCE TOP/BOTTOM OFFSET

Resistance between the reference input and comparator input tap points causes offset errors. These errors can be nulled out by using the force-sense connection as shown in the Reference Input section.

THEORY OF OPERATION

The AD876 implements a pipelined multistage architecture to achieve high sample rate with low power. The AD876 distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the AD876 requires a small fraction of the 1023 comparators used in a traditional flash type A/D. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample while the second and third stages operate on the two preceding samples.

APPLYING THE AD876

DRIVING THE ANALOG INPUT

Figure 11 shows the equivalent analog input of the AD876, a sample-and-hold amplifier (SHA). Bringing CLK to a logic low level closes Switches 1 and 2 and opens Switch 3. The input source connected to AIN must charge capacitor C_H during this time. When CLK transitions from logic "low" to logic "high," Switch 1 opens first, placing the SHA in hold mode. Switch 2 opens subsequently. Switch 3 then closes, connects the feedback loop around the op amp, and forces the output of the op amp to equal the voltage stored on C_H. When CLK transitions from logic "high" to logic "low", Switch 3 opens first. Switch 2 closes and reconnects the input to C_H. Finally, Switch 1 closes and places the SHA in track mode.

The structure of the input SHA places certain requirements on the input drive source. The combination of the pin capacitance, C_P, and the hold capacitance, C_H, is typically less than 5 pF. The input source must be able to charge or discharge this capacitance to 10-bit accuracy in one half of a clock cycle. When the SHA goes into track mode, the input source must charge or discharge capacitor C_H from the voltage already stored on C_H (the previously captured sample) to the new voltage. In the worst case, a full-scale voltage step on the input, the input source must provide the charging current through the R_{ON} (50 Ω) of Switch 2 and quickly settle (within 1/2 CLK period). This situation corresponds to driving a low input impedance. On the other hand, when the source voltage equals the value previously stored on C_H, the hold capacitor requires no input current and the equivalent input impedance is extremely high.

Adding series resistance between the output of the source and the AIN pin reduces the drive requirements placed on the source. Figure 12 shows this configuration. The bandwidth of the particular application limits the size of this resistor. To maintain the performance outlined in the data sheet specifications, the resistor should be limited to 200 Ω or less. For applications with signal bandwidths less than 10 MHz, the user may increase the size of the series resistor proportionally. Alternatively, adding a shunt capacitance between the AIN pin and

analog ground can lower the ac source impedance. The value of this capacitance will depend on the source resistance and the required signal bandwidth.

The input span of the AD876 is a function of the reference voltages. For more information regarding the input range, see the DRIVING THE REFERENCE TERMINALS section of the data sheet.

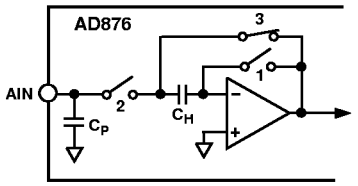


Figure 11. AD876 Equivalent Input Structure

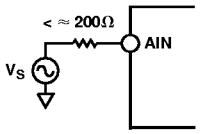


Figure 12. Simple AD876 Drive Requirements

In many cases, particularly in single-supply operation, ac-coupling offers a convenient way of biasing the analog input signal at the proper signal range. Figure 13 shows a typical configuration for ac-coupling the analog input signal to the AD876. Maintaining the specifications outlined in the data sheet requires careful selection of the component values. The most important concern is the $f_{-3\,dB}$ high-pass corner that is a function of R2, and the parallel combination of C1 and C2. The $f_{-3\,dB}$ point can be approximated by the equation

$$f_{-3\,dB} = \frac{1}{[2 \times \pi \times (R2)\,Ceq]}$$

where *Ceq* is the parallel combination of C1 and C2. Note that C1 is typically a large electrolytic or tantalum capacitor that becomes inductive at high frequencies. Adding a small ceramic or polystyrene capacitor on the order of 0.01 µF that does not become inductive until negligibly higher frequencies maintains a low impedance over a wide frequency range.

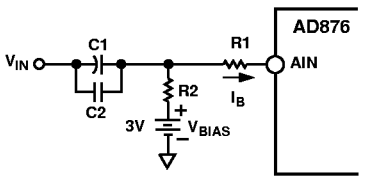


Figure 13. AC-Coupled Inputs

There are additional considerations when choosing the resistor values. The ac-coupling capacitors integrate the switching transients present at the input of the AD876 and cause a net dc bias current, I_B, to flow into the input. The magnitude of this bias current increases with increasing dc signal level and also increases with sample frequency. This bias current will result in an offset error of (R1 + R2) × I_B. If it is necessary to compensate this error, consider making R2 negligibly small or modifying V_{BIAS} to account for the resultant offset.

As an example, assume that the input to the AD876 must have a dc bias of 3 V and the minimum expected signal frequency is 20 kHz. At a sample clock frequency of 20 MHz, the dc bias current at 3 V dc is approximately 30 µA. If we choose R2 equal to 1 kΩ and R1 equal to 50 Ω, the parallel capacitance should be a minimum of 0.008 µF to avoid attenuating signals close to 20 kHz. Note that the bias current will cause a 31.5 mV offset from the 3 V bias.

In systems that must use dc-coupling, use an op amp to level-shift a ground-referenced signal to comply with the input requirements of the AD876. Figure 14 shows an AD817 configured in inverting mode with ac signal gain of –1. The dc voltage at the noninverting input of the op amp controls the amount of dc level shifting. A resistive voltage divider attenuates the REFBF signal. The op amp then multiplies the attenuated signal by 2. In the case where REFBF = 1.6 V, the dc output level will be 2.6 V. The AD817 is a low cost, fast settling, single supply op amp with a G = –1 bandwidth of 29 MHz. The AD818 is similar to the AD817 but has a 50 MHz bandwidth. Other appropriate op amps include the AD8011, AD812 (a dual), and the AD8001.

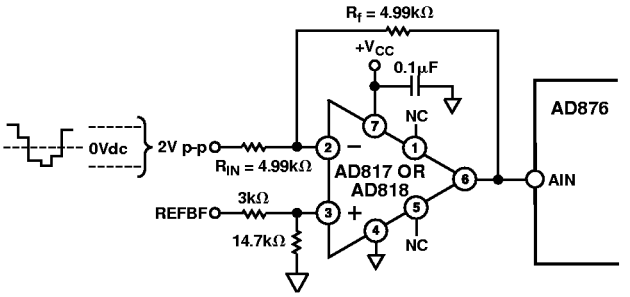


Figure 14. Bipolar Level Shift

An integrated difference amplifier such as the AD830 is an alternate means of providing dc level shifting. The AD830 provides a great deal of flexibility with control over offset and gain. Figure 15 shows the AD830 precisely level-shifting a unipolar, ground-referenced signal. The reference voltage, REFBS, determines the amount of level-shifting. The ac gain is 1. The AD830 offers the advantages of high CMRR, precise gain, offset, and high-impedance inputs when compared with a discrete implementation. For more information regarding the AD830, see the AD830 data sheet.

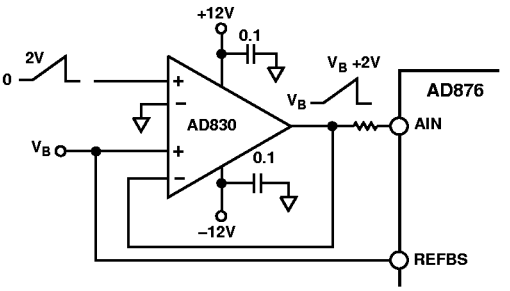


Figure 15. Level Shifting with the AD830

REFERENCE INPUT DRIVING THE REFERENCE TERMINALS

The AD876 requires an external reference on pins REFTF and REFBF. The AD876 provides reference sense pins, REFTS and REFBS, to minimize voltage drops caused by external and internal wiring resistance. A resistor ladder, nominally 250 Ω, connects pins REFTF and REFBF.

Figure 16 shows the equivalent input structure for the AD876 reference pins. There is approximately 5 Ω of resistance between both the REFTF and REFBT pins and the reference ladder. If the force-sense connections are not used, the voltage drop across the 5 Ω resistors will result in a reduced voltage appearing across the ladder resistance. This reduces the input span of the converter. Applying a slightly larger span between the REFTF and REFBF pins compensates this error. Note that the temperature coefficients of the 5 Ω resistors are 1350 ppm. The user should consider the effects of temperature when not using a force-sense reference configuration.

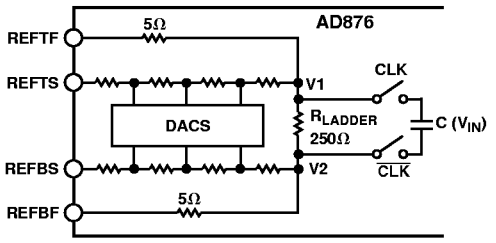


Figure 16. AD876 Equivalent Reference Structure

Do not connect the REFTS and REFBS pins in configurations that do not use a force-sense reference. Connecting the force and sense lines together allows current to flow in the sense lines. Any current allowed to flow through these lines must be negligibly small. Current flow causes voltage drops across the resistance in the sense lines. Because the internal D/As of the AD876 tap different points along the sense lines, each D/A would receive a slightly different reference voltage if current were flowing in these wires. To avoid this undesirable condition, leave the sense lines unconnected. Any current allowed to flow through these lines must be negligibly small (<100 μA).

The voltage drop across the internal resistor ladder determines the input span of the AD876. The driving voltages required at the V1 and V2 points are respectively +4 V and +2 V. Calculate the full-scale input span from the equation

$$Input\ Span\ (V) = REFTS - REFBS$$

This results in a full-scale input span of approximately +2 V when REFTS = +4 V and REFBS = +2 V In order to maintain the requisite 2 V drop across the internal ladder, the external reference must be capable of providing approximately 8.0 mA.

The user has flexibility in determining both the full-scale span of the analog input and where to center this voltage. Figure 17 shows the range over which the AD876 can operate without degrading the typical performance.

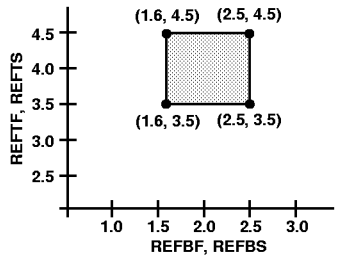


Figure 17. AD876 Reference Ranges

While the previous issues address the dc aspects of the AD876 reference, the user must also be aware of the dynamic impedance changes associated with the reference inputs. The simplified diagram of Figure 16 shows that the reference pins connect to a capacitor for one-half of the clock period. The size of the capacitor is a function of the analog input voltage.

The external reference must be able to maintain a low impedance over all *frequencies of interest* in order to provide the charge required by the capacitance. By supplying the requisite charge, the reference voltages will be relatively constant and performance will not degrade. For some reference configurations, voltage transients will be present on the reference lines; this is particularly true during the falling edge of CLK. It is important that the reference recovers from the transients and settles to the desired level of accuracy prior to the rising edges of CLK.

There are several reference configurations suitable for the AD876 depending on the application, desired level of accuracy, and cost trade-offs. The simplest configuration, shown in Figure 18, utilizes a resistor string to generate the reference voltages from the converter's analog power supply. The 0.1 μF bypass capacitors effectively reduce high-frequency transients. The 10 μF capacitors act to reduce the impedances at the REFTF and REFBF pins at lower frequencies. As input frequencies approach dc, the capacitors become ineffective, and small voltage deviations will appear across the biasing resistors. This application can maintain 10-bit accuracy for input frequencies above approximately 200 Hz. 8-bit applications can use this circuit for input frequencies above approximately 50 Hz.

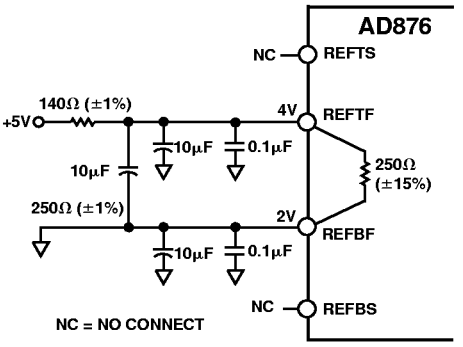


Figure 18. Low Cost Reference Circuit

This reference configuration provides the lowest cost but has several disadvantages. These disadvantages include poor dc power supply rejection and poor accuracy due to the variability of the internal and external resistors.

The AD876 offers force-sense reference connections to eliminate the voltage drops associated with the internal connections to the reference ladder. Figure 19 shows a suggested circuit using an AD826 dual, high speed op amp. This configuration uses 3.6 V and 1.6 V reference voltages for REFT and REFB, respectively. The connections shown in Figure 19 configure the op amps as voltage followers.

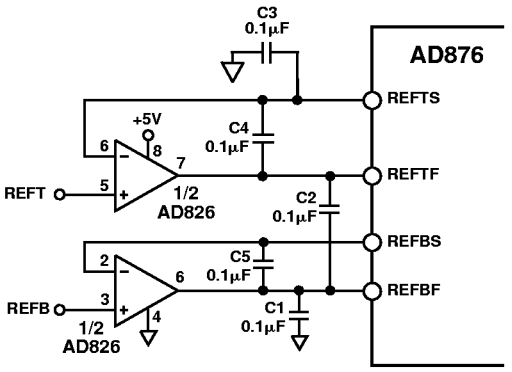


Figure 19. Kelvin Connected Reference Using the AD826

By connecting the op amp feedback through the sense connections of the AD876, the outputs of the op amps automatically adjust to compensate for the voltage drops that occur within the converter. The AD826 has the advantage of being able to maintain stability while driving unlimited capacitive loads. As a result, 0.1 µF capacitors C1, C2, and C3 can connect directly to the outputs of the op amps. These decoupling capacitors reduce high frequency transients. Capacitors C4 and C5 shunt across the internal resistors of the force sense connections and prevent instability.

This configuration provides excellent performance and a minimal number of components. The circuit also offers the advantage of operating from a single +5 V supply. While alternative op amps may also be suitable, consider the stability of these op amps while driving capacitive loads.

The circuit shown in Figure 20 allows a wider selection of op amps when compared with the previous configuration. An

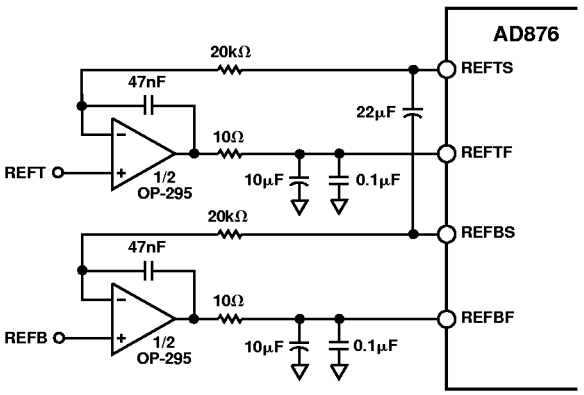


Figure 20. Kelvin Connected Reference Using the OP295

OP295 dual, single-supply op amp provides stable 3.6 V and 1.6 V reference voltages. The AD822 dual op amp is also suitable for single-supply applications. Each half of the OP295 is compensated to drive the 10 µF and 0.1 µF decoupling capacitors at the REFTF and REFBF pins and maintain stability.

Like any high resolution converter, the layout and decoupling of the reference is critical. The actual voltage digitized by the AD876 is relative to the reference voltages. In Figure 21, for example, the reference return and the bypass capacitors are connected to the shield of the incoming analog signal. Disturbances in the ground of the analog input, that will be common-mode to the REFT, REFB, and AIN pins because of the common ground, are effectively removed by the AD876's high common-mode rejection.

High frequency noise sources, V_{N1} and V_{N2}, are shunted to ground by decoupling capacitors. Any voltage drops between the analog input ground and the reference bypassing points will be treated as input signals by the converter via the reference inputs. Consequently, the reference decoupling capacitors should be connected to the same analog ground point used to define the analog input voltage. (For further suggestions, see the "Grounding and Layout Rules" section of the data sheet.)

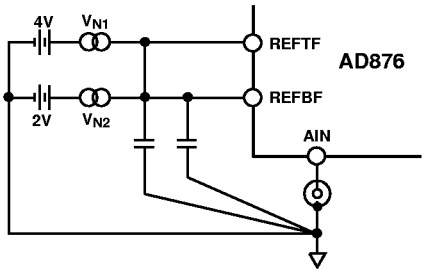


Figure 21. Recommended Bypassing for the Reference Inputs

CLOCK INPUT

The AD876 clock input is buffered internally with an inverter powered from the DRV_{DD} pin. This feature allows the AD876 to accommodate either +5 V or +3.3 V CMOS logic input signal swings with the input threshold for the CLK pin nominally at $DRV_{DD}/2$.

The AD876's pipelined architecture operates on both rising and falling edges of the input clock. To minimize duty cycle variations the recommended logic family to drive the clock input is high speed or advanced CMOS (HC/HCT, AC/ACT) logic. CMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 20 MSPS operation. The AD876 is designed to support a conversion rate of 20 MSPS; running the part at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD876 at slower clock rates.

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a reduction in power consumption. Figure 8 illustrates this trade-off.

DIGITAL INPUTS AND OUTPUTS

Each of the AD876 digital control inputs, THREE-STATE and STBY, has an input buffer powered from the DRV_{DD} supply pins. With DRV_{DD} set to +5 V, all digital inputs readily interface with +5 V CMOS logic. For interfacing with lower voltage CMOS logic, DRV_{DD} can be set to 3.3 V, effectively lowering the nominal input threshold of all digital inputs to 3.3 V/2 = 1.65 V.

The format of the digital output is straight binary. Table I shows the output format for the case where REFTS = 4 V and REFBS = 2 V.

Table I. Output Data Format

Approx. AIN (V)	THREE-STATE	DATA D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
>4	0	1	1	1	1	1	1	1	1	1	1
4	0	1	1	1	1	1	1	1	1	1	1
3	0	1	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
<2	0	0	0	0	0	0	0	0	0	0	0
X	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

A low power mode feature is provided such that for STBY = HIGH and the clock disabled, the static power of the AD876 will drop below 50 mW.

GROUNDING AND LAYOUT RULES

As is the case for any high performance device, proper grounding and layout techniques are essential in achieving optimal performance. The analog and digital grounds on the AD876 have been separated to optimize the management of return currents in a system. It is recommended that a printed circuit board (PCB) of at least 4 layers employing a ground plane and power planes be used with the AD876. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout which prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with the input signal traces and should be routed away from the input circuitry. Separate analog and digital grounds should be joined together directly under the AD876. A solid ground plane under the AD876 is also acceptable if the power and ground return currents are managed carefully. A general rule of thumb for mixed signal layouts dictates that the return currents from digital circuitry should not pass through critical analog circuitry. For further layout suggestions, see the *AD876 Evaluation Board data sheet.*

DIGITAL OUTPUTS

Each of the on-chip buffers for the AD876 output bits (D0–D9) is powered from the DRV_{DD} supply pins, separate from AV_{DD} or DV_{DD}. The output drivers are sized to handle a variety of logic families while minimizing the amount of glitch energy generated. In all cases, a fan-out of one is recommended to keep the capacitive load on the output data bits below the specified 20 pF level.

For DRV_{DD} = 5 V, the AD876 output signal swing is compatible with both high speed CMOS and TTL logic families. For TTL, the AD876 on-chip, output drivers were designed to support several of the high speed TTL families (F, AS, S). For applications where the clock rate is below 20 MSPS, other TTL families may be appropriate. For interfacing with lower voltage CMOS logic, the AD876 sustains 20 MSPS operation with DRV_{DD} = 3.3 V. In all cases, check your logic family data sheets for compatibility with the AD876 Digital Specification table.

THREE-STATE OUTPUTS

The digital outputs of the AD876 can be placed in a high impedance state by setting the THREE-STATE pin to HIGH. This feature is provided to facilitate in-circuit testing or evaluation. Note that this function is not intended for enabling/disabling the ADC outputs from a bus at 20 MSPS. Also, to avoid corruption of the sampled analog signal during conversion (3.5 clock cycles), it is highly recommended that the AD876 outputs be enabled on the bus prior to the first sampling. For the purpose of budgetary timing, the maximum access and float delay times (t_{DD}, t_{HL} shown in Figure 15) for the AD876 are 150 ns.

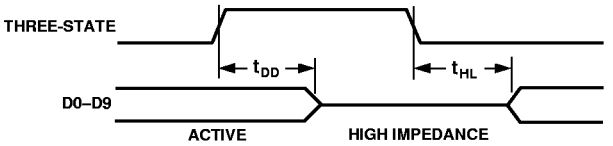


Figure 22. High-Impedance Output Timing Diagram

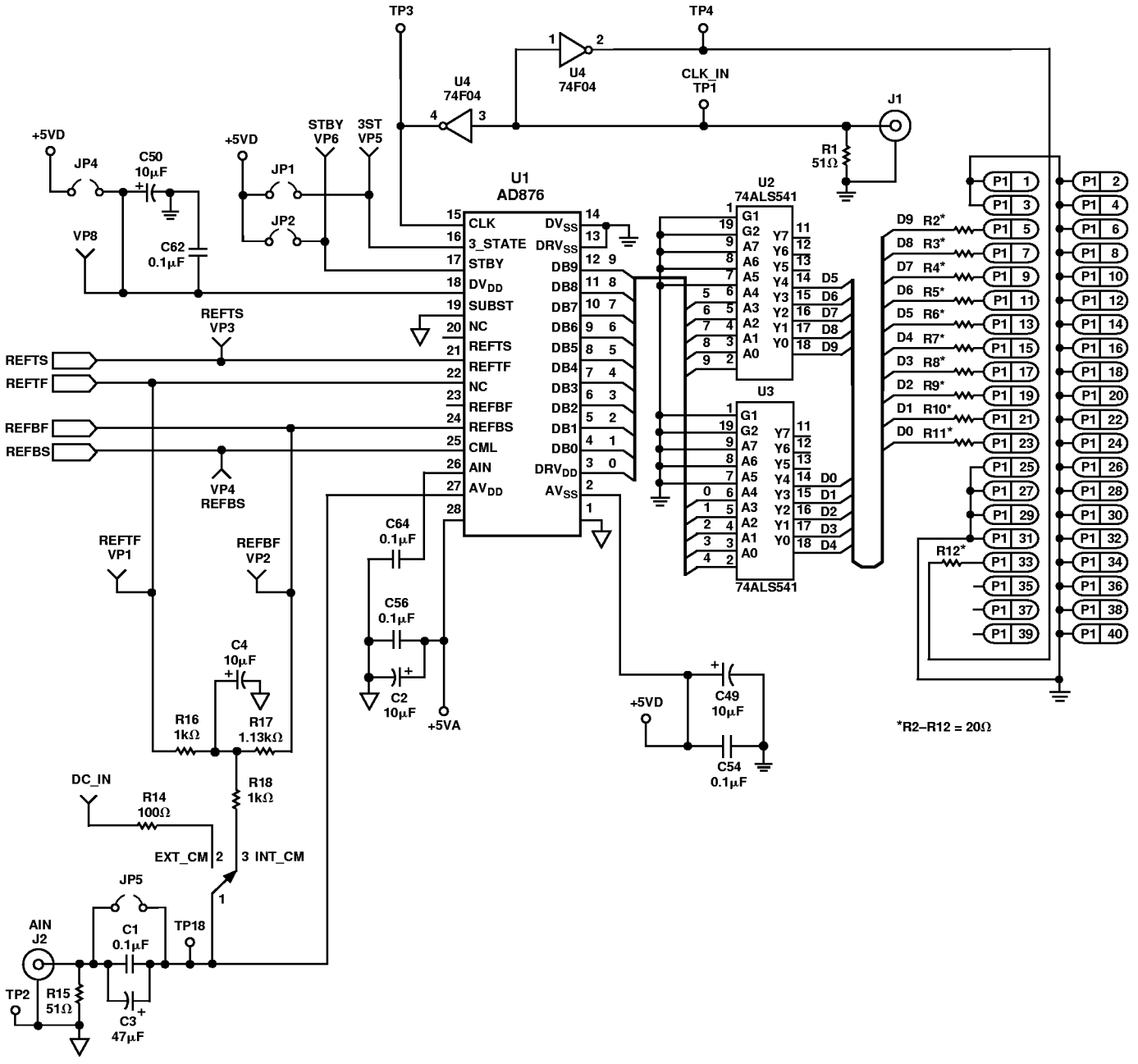


Figure 23. AD876 Evaluation Board Schematic

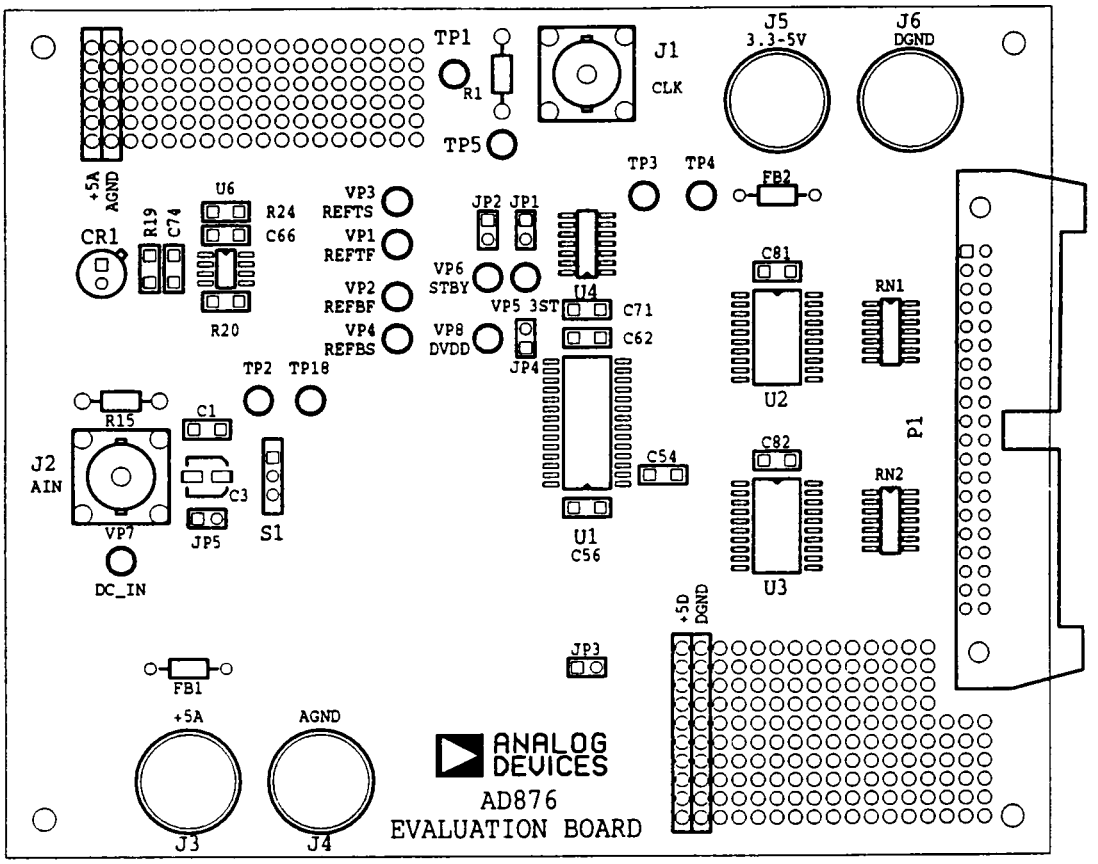


Figure 24. Silkscreen Layer, Component Side PCXB Layout

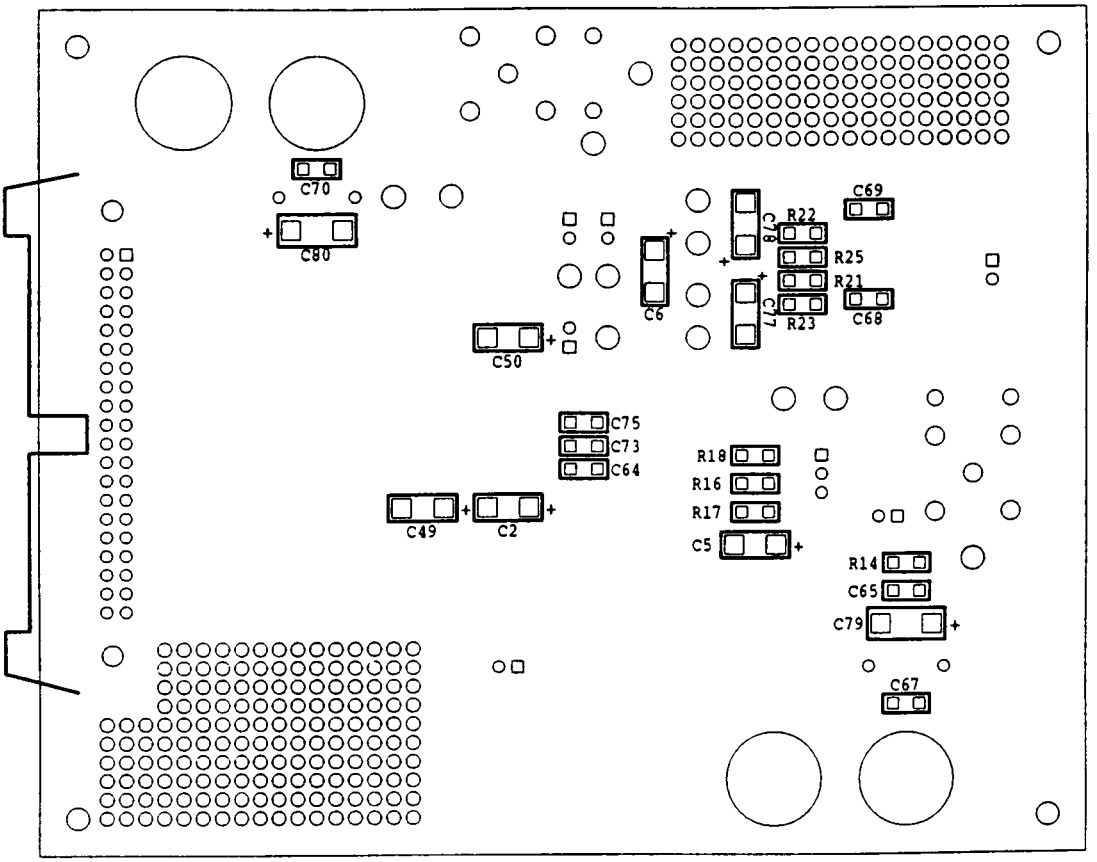


Figure 25. Silkscreen Layer, Circuit Side PCB Layout

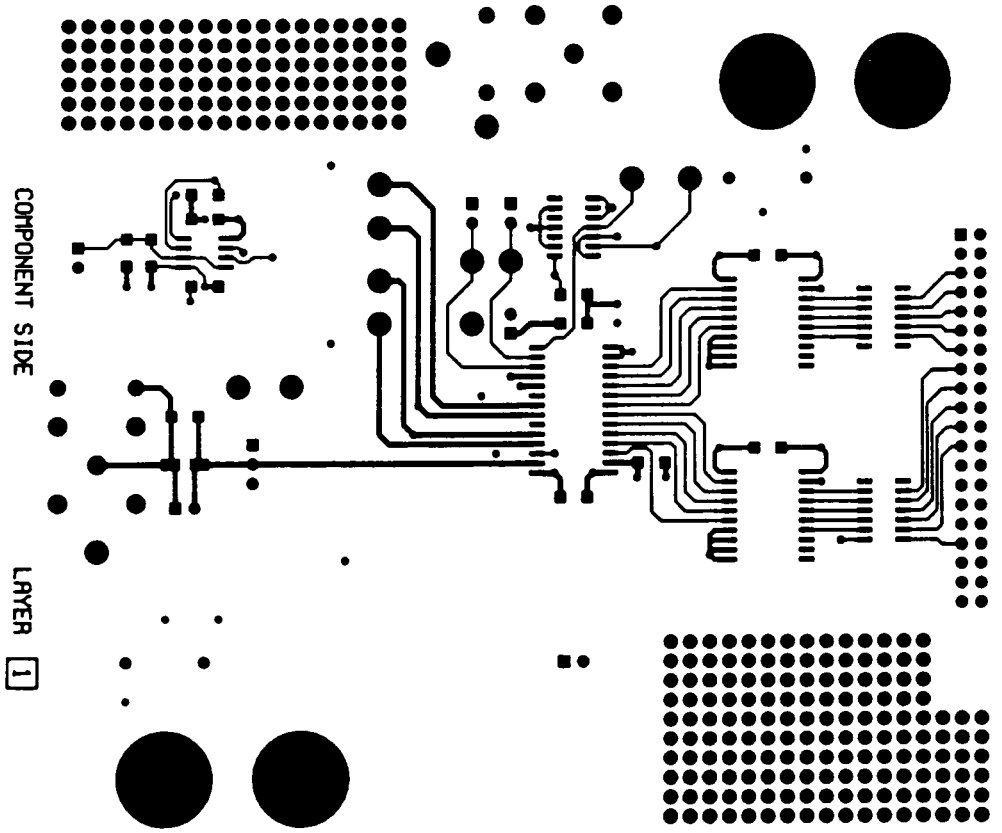


Figure 26. Component Side PCB Layout

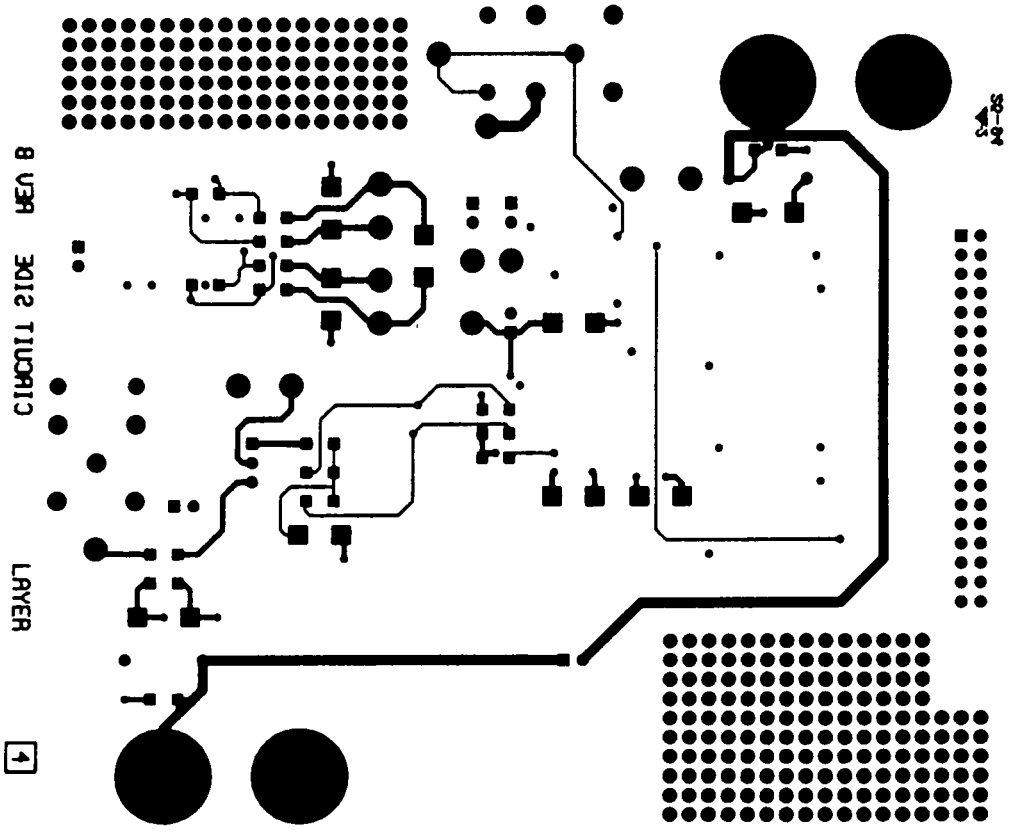


Figure 27. Circuit Side PCB Layout

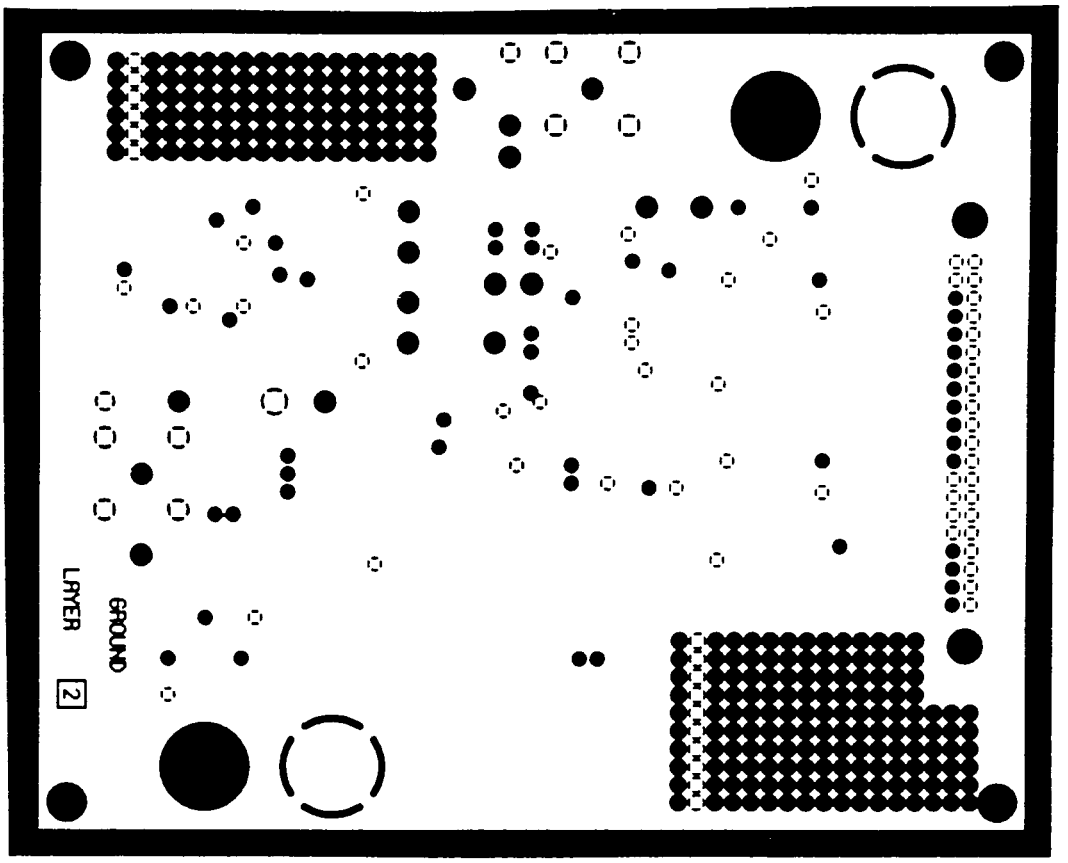


Figure 28. Ground Layer PCB Layout

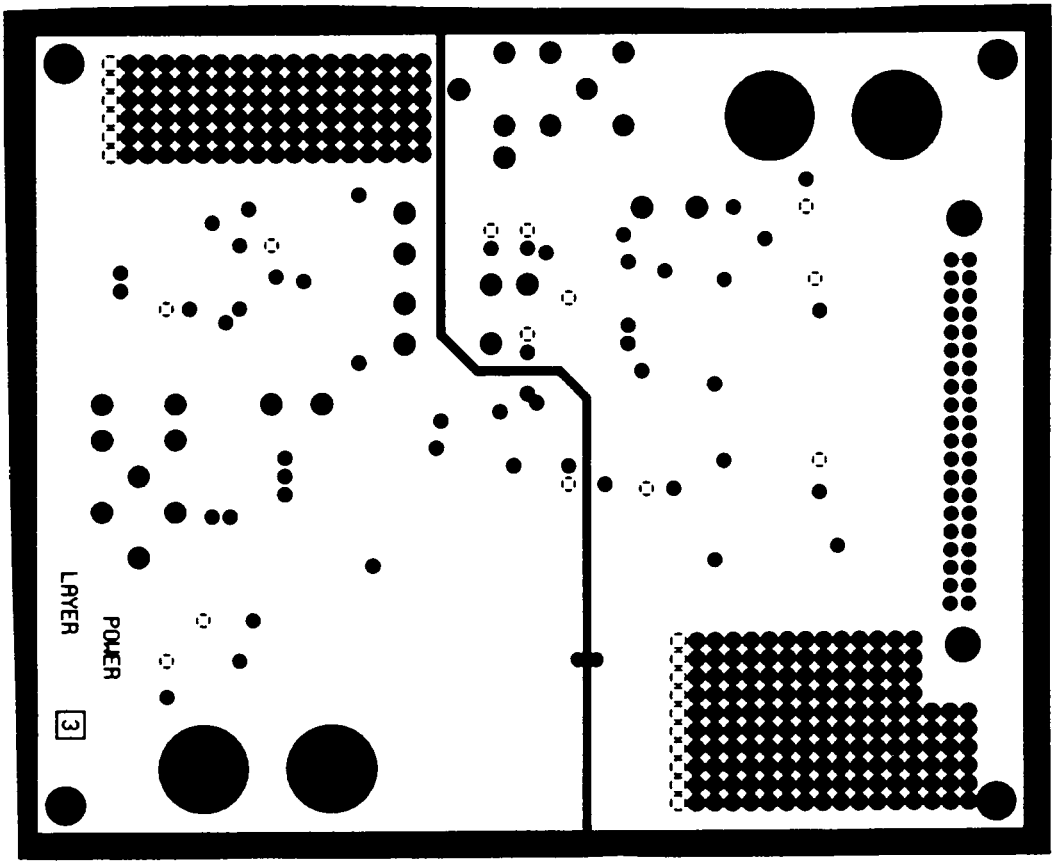
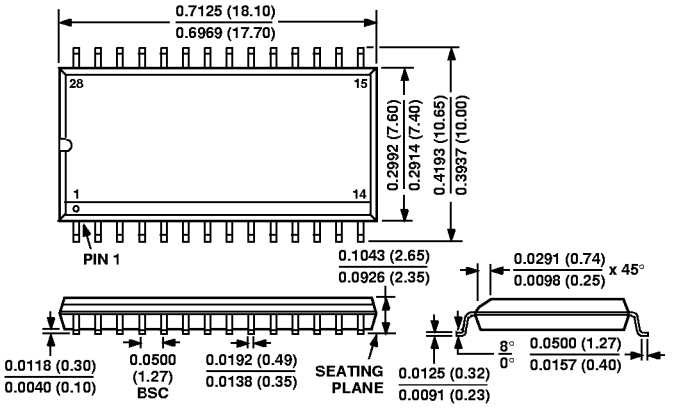


Figure 29. Power Layer PCB Layout

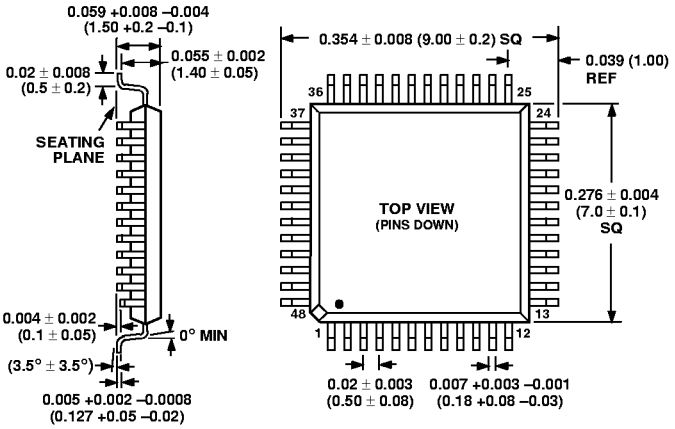
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

R-28
28-Lead Wide Body (SOIC)



ST-48
28-Lead Plastic Thin Quad Flatpack (TQFP)



RS-28
28-Lead Shrink Small Outline Package (SSOP)