



ANALOG DEVICES Fast, Complete Sampling 12-Bit A/D Converter with Microprocessor Interface

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AD678

1.1 Scope.

This specification covers the detail requirements for a 12-bit resolution A/D converter with complete microprocessor interface and an on-chip sample-hold amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD678S(X)/883B
-2	AD678T(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin DIP
J	J-44	44-Pin JLCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{CC} to AGND	+18 V to -0.3 V
V_{EE} to AGND	-18 V to +0.3 V
V_{DD} to DGND	0 V to +7 V
AGND to DGND	-1 V to +1 V
V_{CC} to V_{EE}	+26.4 V to -0.3 V
AIN, REF _{IN} to AGND	V_{EE} to V_{CC}
Digital Inputs to DGND	-0.5 V to +7 V
Digital Outputs to DGND	-0.5 V to $V_{DD} + 0.3$ V
Power Dissipation	1000 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 4^\circ\text{C}/\text{W}$ for J-44; $25^\circ\text{C}/\text{W}$ for D-28
 $\theta_{JA} = 80^\circ\text{C}/\text{W}$ for J-44; $60^\circ\text{C}/\text{W}$ for D-28

Tested in accordance with MIL-STD-750C in still air freely suspended under natural convection conditions.

AD678—SPECIFICATIONS

0816800 0040458 05T ANA

Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units	
Power Dissipation	P _D	-1, 2	745	745	745		Converting	mW max	
Internal Reference Output Voltage	V _{REF}	-1, 2	4.98	4.98	4.98		Bipolar 0.5 mA External Load	+V min	
			5.02	5.02	5.02			+V max	
Internal Reference Output Current	I _{REF}	-1, 2	1.5	1.5	1.5		Unipolar Mode	mA max	
			0.5	0.5	0.5		Bipolar Mode		
High Level Input Voltage	V _{IH}	-1, 2	2.0	2.0	2.0			+V min	
Low Level Input Voltage	V _{IL}	-1, 2	0.8	0.8	0.8			+V max	
Logic Input Current	I _{IH}	-1, 2	10	10	10		V _{IH} = 5.0 V V _{IL} = 0.0 V	±μA max	
High Level Output Voltage	V _{OH}	-1, 2	2.4	2.4	2.4		I _{OH} = -0.5 mA	+V min	
Low Level Output Voltage	V _{OL}	-1, 2	0.4	0.4	0.4		I _{OL} = 1.6 mA	+V max	
High Z Leakage Current	I _{OZ}	-1, 2	10	10	10		V _{IN} = 0, V _{DD}	±μA max	
Power Supply Current	I _{CC}	-1, 2	20	20	20		V _{CC} = 12.6 V, Converting	mA max	
			I _{EE}	-1, 2	-34	-34	-34		V _{EE} = -12.6 V, Converting
			I _{DD}	-1, 2	12	12	12		V _{DD} = +5.5 V, Converting
Integral Nonlinearity	INL	-1	1	2			Unipolar Mode	±LSB max	
			-2	1	2	1	1		
Differential Nonlinearity ²	DNL	-1, 2	12	12	12		All Codes Tested	Bits min	
Unipolar Zero Error	ZE _U	-1	3	10				±LSB max	
			-2	3	10		3		
Bipolar Zero Error	ZE _B	-1	5	10				±LSB max	
			-2	5	10		5		
Unipolar Zero Error Drift	ZE _U TC	-2			5		w/Internal Reference	±LSB max	
Bipolar Zero Error Drift	ZE _B TC	-2			5		w/Internal Reference	±LSB max	
Gain Error	GE	-1	6	20			Unipolar & Bipolar Modes	±LSB max	
			-2	6	20		6		
Gain Error Drift	GETC	-2			6		Unipolar Mode w/External Reference	±LSB max	
Gain Error Drift	GETC	-2			10		Unipolar & Bipolar Mode w/Internal Reference	±LSB max	
Power Supply Rejection Ratio	PSRR	-1, 2	2	2			Unipolar Mode ³	±LSB max	

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 4	Sub Group 5, 6	Test Condition ¹	Units
Signal-to-Noise and Distortion	S/(N+D)	-1	70	70	70	Bipolar, f _{IN} = 10.06 kHz	dB min
			-2	72	72	72	
Total Harmonic Distortion	THD	-1, 2	-80	-80	-80	Bipolar, f _{IN} = 10.06 kHz	dB max
Intermodulation Distortion Second-Order Products	IMD ₂	-1, 2	-80	-80	-80	Bipolar, f _A = 9.09 kHz; f _B = 9.58 kHz	dB max
Intermodulation Distortion Third-Order Products	IMD ₃	-1, 2	-80	-80	-80	Bipolar, f _A = 9.09 kHz; f _B = 9.58 kHz	dB max

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65E D

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
SC Delay	t _{SC}	-1, 2	50	50	50	See Figure 1	ns min
Conversion Rate	t _{CR}	-1, 2	5	5	5	See Figure 1	μs max
Convert Pulse Width	t _{CP}	-1, 2	97	97	97	See Figure 1	ns min
Conversion Time	t _C	-1, 2	4.4	4.4	4.4	See Figure 1	μs max
Status Delay	t _{SD}	-1, 2	0	0	0	See Figure 1	ns min
			400	400	400		ns max
Access Time	t _{BA}	-1, 2	100	100	100	See Figures 2, 3, 4	ns max
Float Delay	t _{FD}	-1, 2	10	10	10	See Figures 2, 3, 4	ns min
			80	80	80		ns max
Format Setup	t _{FS}	-1, 2	47	47	47	See Figure 3	ns min
OE Delay	t _{OE}	-1, 2	0	0	0	See Figures 3, 4	ns min
Read Pulse Width	t _{RP}	-1, 2	97	97	97	See Figures 3, 4	ns min
Conversion Delay	t _{CD}	-1, 2	150	150	150	See Figures 1, 3, 4	ns min
EOCEN Delay	t _{EO}	-1, 2	0	0	0	See Figure 2	ns min
Output Delay	t _{OD}	-1, 2	0	0	0	See Figure 1	ns max

NOTES

¹V_{CC} = +12 V ± 5%, V_{EE} = -12 V ± 5%, V_{DD} = 5 V ± 10%. See Figures 1, 2, 3, and 4 for timing information.

²Minimum resolution for which no missing codes are guaranteed.

³Test condition for PSRR, with limit shown as the change from nominal value to each extreme:

+11.4 V ≤ V_{CC} ≤ +12.6 V; V_{EE} = -12 V; V_{DD} = +5 V

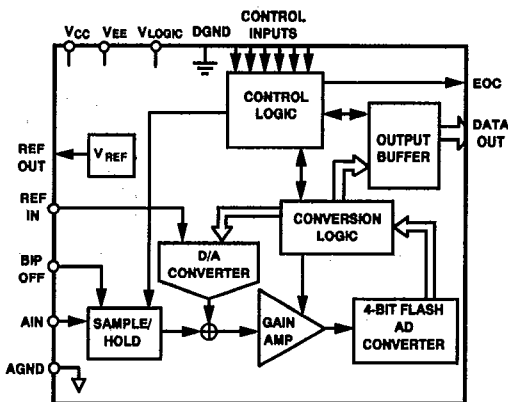
-12.6 V ≤ V_{EE} ≤ -11.4 V; V_{CC} = +12 V; V_{DD} = +5 V

+4.5 V ≤ V_{DD} ≤ +5.5 V; V_{CC} = +12 V; V_{EE} = -12 V

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3.2.1 Functional Block Diagram and Terminal Assignments

Description	D-28 Pin Description	J-44 Pin Description
EOCEN	1	1
OE	2	3
SC	3	5
CS	4	6
V _{EE}	5	8
AIN	6	10
AGND	7	11
REFOUT	8	12
REF _{IN}	9	14
BIPOFF	10	15
V _{CC}	11	17
12/8	12	19
SYNC	13	21
DGND	14	23
DB0 (HBE)	15	25
DB1 (R/L)	16	26
DB2	17	27
DB3	18	30
DB4	19	31
DB5	20	33
DB6	21	34
DB7	22	35
DB8	23	36
DB9	24	37
DB10	25	39
DB11	26	40
EOC	27	42
V _{DD}	28	43



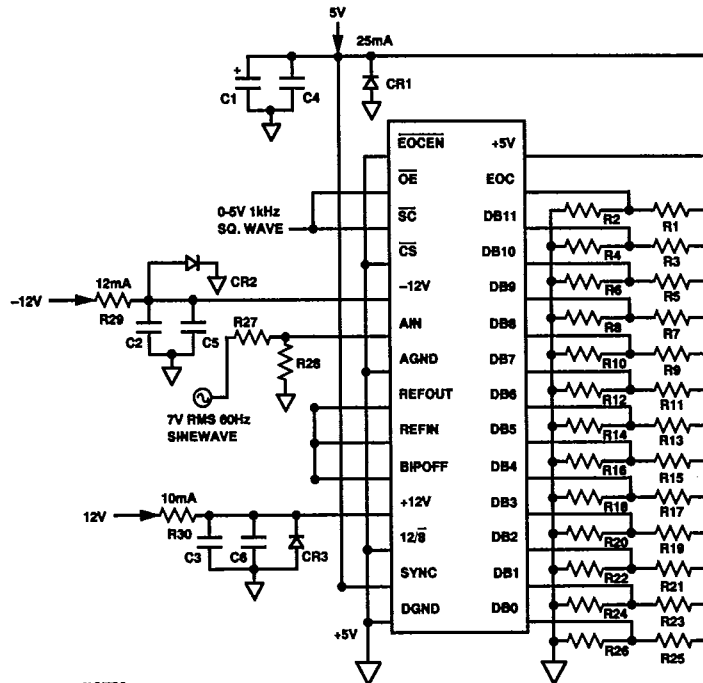
3.2.4 Microcircuit Technology Group

This circuit is covered by technology group (57).

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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



NOTES

1. C1, C2, C3 ARE 47 μ F CAPACITORS RATED AT 35V, 125°C.
2. C4, C5, C6 ARE 0.1 μ F CAPACITORS RATED AT 50V, 125°C.
3. CR1, CR2, CR3 ARE MRB20 DIODES.
4. R1-R26 ARE 3k Ω RESISTOR PACKS.
5. ALL CURRENTS SHOWN ARE MAXIMUM PER DEVICE.
6. R27, R28 ARE 10k Ω 1% 1/4 WATT METAL FILM RESISTORS.
7. R29 AND R30 ARE 1 Ω 2 WATT GLASS RESISTORS.

Burn-In Circuit

6 ANALOG-TO-DIGITAL CONVERTERS

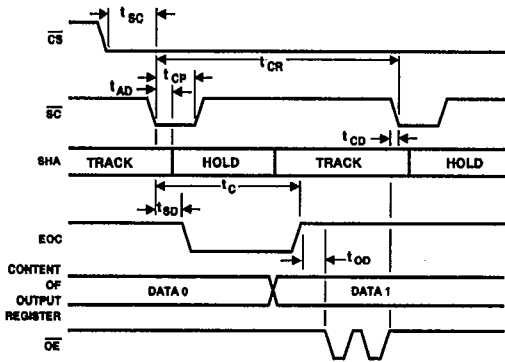


Figure 1. Conversion Timing

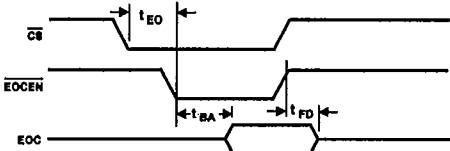


Figure 2. EOC Timing

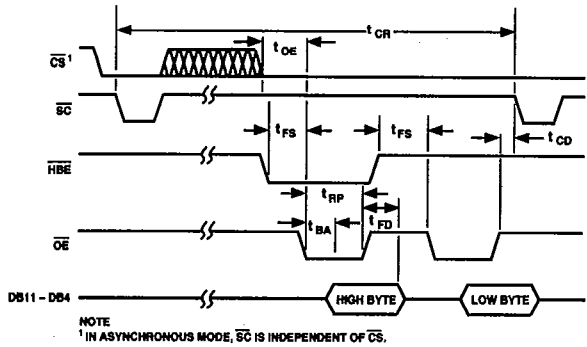


Figure 3. Output Timing, 8-Bit Read Mode

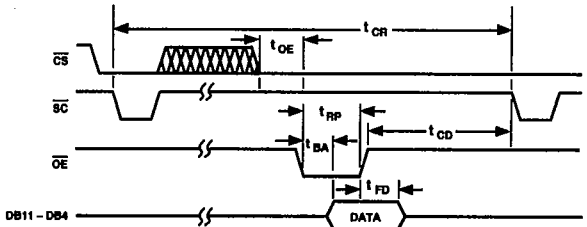


Figure 4. Output Timing, 12-Bit Read Mode

TEST	V _{CP}	C _{OUT}
ACCESS TIME HIGH Z TO LOGIC LOW	5V	100pF
FLOAT TIME LOGIC HIGH TO HIGH Z	0V	10pF
ACCESS TIME HIGH Z TO LOGIC HIGH	0V	100pF
FLOAT TIME LOGIC LOW TO HIGH Z	5V	10pF

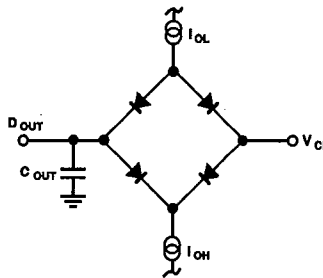


Figure 5. Load Circuit for Bus Timing Specifications