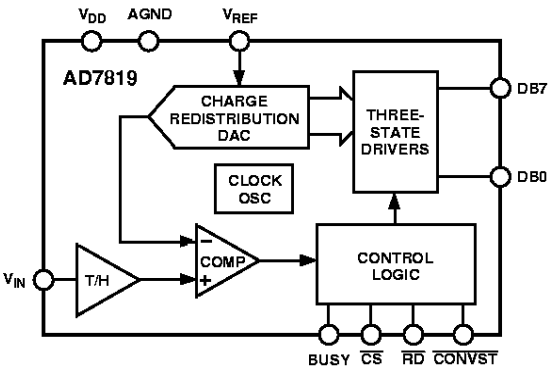
+2.7 V to +5.5 V, 200 kSPS 8-Bit Sampling ADC

AD7819

FEATURES

8-Bit ADC with 4.5 μs Conversion Time
On-Chip Track and Hold
Operating Supply Range: +2.7 V to +5.5 V
Specifications at +2.7 V – 3.6 V and 5 V ± 10%
8-Bit Parallel Interface
  8-Bit Read
Power Performance
  Normal Operation
    10.5 mW, V_{DD} = 3 V
  Automatic Power-Down
    57.75 μW @ 1 kSPS, V_{DD} = 3 V
Analog Input Range: 0 V to V_{REF}
Reference Input Range: 1.2 V to V_{DD}

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7819 is a high speed, microprocessor-compatible, 8-bit analog-to-digital converter with a maximum throughput of 200 kSPS. The converter operates off a single +2.7 V to +5.5 V supply and contains a 4.5 μs successive approximation A/D converter, track/hold circuitry, on-chip clock oscillator and 8-bit wide parallel interface. The parallel interface is designed to allow easy interfacing to microprocessors and DSPs. Using only address decoding logic the AD7819 is easily mapped into the microprocessor address space.

When used in its power-down mode, the AD7819 automatically powers down at the end of a conversion and powers up at the start of a new conversion. This feature significantly reduces the power consumption of the part at lower throughput rates. The AD7819 can also operate in a high speed mode where the part is not powered down between conversions. In this mode of operation the part is capable of providing 200 kSPS throughput.

The part is available in a small, 16-pin 0.3" wide, plastic dual-in-line package (DIP); in a 16-pin, 0.15" wide, narrow body small outline IC (SOIC) and in a 16-pin, narrow body, thin shrink small outline package (TSSOP).

PRODUCT HIGHLIGHTS

1. Low Power, Single Supply Operation
   The AD7819 operates from a single +2.7 V to +5.5 V supply and typically consumes only 10.5 mW of power. The power dissipation can be significantly reduced at lower throughput rates by using the automatic power-down mode.
2. Automatic Power-Down
   The automatic power-down mode, whereby the AD7819 goes into power-down mode at the end of a conversion and powers up before the next conversion, means the AD7819 is ideal for battery powered applications; e.g., 57.75 μW @ 1 kSPS. (See Power vs. Throughput Rate section.)
3. Parallel Interface
   An easy to use 8-bit wide parallel interface allows interfacing to most popular microprocessors and DSPs with minimal external circuitry.
4. Dynamic Specifications for DSP Users
   In addition to the traditional ADC specifications, the AD7819 is specified for ac parameters, including signal-to-noise ratio and distortion.

REV. 0

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AD7819–SPECIFICATIONS[1] (GND = 0 V, V_{REF} = +V_{DD} = 3 V ± 10% to 5 V ± 10%. All specifications –40°C to +125°C unless otherwise noted.)

Parameter	Y Version	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 30 kHz, f_{SAMPLE} = 136 kHz
Signal to (Noise + Distortion) Ratio[1]	48	dB min	
Total Harmonic Distortion (THD)[1]	–70	dB typ	
Peak Harmonic or Spurious Noise[1]	–70	dB typ	
Intermodulation Distortion[2]			fa = 29.1 kHz; fb = 29.8 kHz
2nd Order Terms	–77	dB typ	
3rd Order Terms	–77	dB typ	
DC ACCURACY			
Resolution	8	Bits	
Minimum Resolution for Which			
No Missing Codes Are Guaranteed	8	Bits	
Relative Accuracy[1]	±0.5	LSB max	
Differential Nonlinearity (DNL)[1]	±0.5	LSB max	
Total Unadjusted Error[1]	±1	LSB max	
Gain Error[1]	±0.5	LSB max	
Offset Error[1]	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0	V min	
	V_{REF}	V max	
Input Leakage Current[2]	±1	μA max	
Input Capacitance[2]	15	pF mx	
REFERENCE INPUTS[2]			
V_{REF} Input Voltage Range	1.2	V min	
	V_{DD}	V max	
Input Leakage Current	±1	μA max	
Input Capacitance	20	pF max	
LOGIC INPUTS[2]			
V_{INH}, Input High Voltage	2.0	V min	
V_{INL}, Input Low Voltage	0.4	V max	(0.8 V max, V_{DD} = 5 V)
Input Current, I_{IN}	±1	μA max	Typically 10 nA, V_{IN} = 0 V to V_{DD}
Input Capacitance, C_{IN}	8	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	2.4	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 μA
High Impedance Leakage Current	±1	μA max	
High Impedance Capacitance	15	pF max	
CONVERSION RATE			
Conversion Time	4.5	μs max	
Track/Hold Acquisition Time[1]	100	ns max	See DC Acquisition Section
POWER SUPPLY			
V_{DD}	2.7–5.5	Volts	For Specified Performance
I_{DD}			Digital Inputs = 0 V or V_{DD}
Normal Operation	3.5	mA max	
Power-Down	1	μA max	V_{DD} = 5 V
Power Dissipation			
Normal Operation	17.5	mW max	V_{DD} = 5 V
Power-Down	5	μW max	
Auto Power-Down (Mode 2)			V_{DD} = 3 V
1 kSPS Throughput	57.75	μW max	
10 kSPS Throughput	577.5	μW max	
50 kSPS Throughput	2.89	mW max	

NOTES

[1]See Terminology section.

[2]Sample tested during initial release and after any redesign or process change that may affect this parameter.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (–40°C to +125°C, unless otherwise noted)

Parameter	V_{DD} = 3 V ± 10%	V_{DD} = 5 V ± 10%	Units	Conditions/Comments
$t_{POWER-UP}$	1	1	µs (max)	Power-Up Time of AD7819 after Rising Edge of $\overline{CONVST}$.
t_1	4.5	4.5	µs (max)	Conversion Time.
t_2	30	30	ns (min)	$\overline{CONVST}$ Pulse Width.
t_3	30	30	ns (max)	$\overline{CONVST}$ Falling Edge to BUSY Rising Edge Delay.
t_4	0	0	ns (min)	$\overline{CS}$ to $\overline{RD}$ Setup Time.
t_5	0	0	ns (min)	$\overline{CS}$ Hold Time after $\overline{RD}$ High.
t_6[3]	10	10	ns (max)	Data Access Time after $\overline{RD}$ Low.
t_7[3, 4]	10	10	ns (max)	Bus Relinquish Time after $\overline{RD}$ High.
t_8[3]	50	50	ns (min)	Data Bus Relinquish to Falling Edge of $\overline{CONVST}$ Delay.

NOTES
[1]Sample tested to ensure compliance.
[2]See Figures 12, 13 and 14.
[3]These numbers are measured with the load circuit of Figure 1. They are defined as the time required for the o/p to cross 0.8 V or 2.4 V for V_{DD} = 5 V ± 10% and 0.4 V or 2 V for V_{DD} = 3 V ± 10%.
[4]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the Timing Characteristics is the true bus relinquish time of the part and as such is independent of external bus loading capacitances.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND ..... –0.3 V to +7 V
Digital Input Voltage to DGND
($\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$) ..... –0.3 V, V_{DD} + 0.3 V
Digital Output Voltage to DGND
(BUSY, DB0–DB7) ..... –0.3 V, V_{DD} + 0.3 V
REF_{IN} to AGND ..... –0.3 V, V_{DD} + 0.3 V
Analog Input ..... –0.3 V, V_{DD} + 0.3 V
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature .....+150°C
Plastic DIP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... +105°C/W
Lead Temperature, (Soldering 10 sec) .....+260°C
SOIC Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) .....+215°C
Infrared (15 sec) .....+220°C
SSOP Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 115°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) .....+215°C
Infrared (15 sec) .....+220°C
ESD ..... ≤4 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

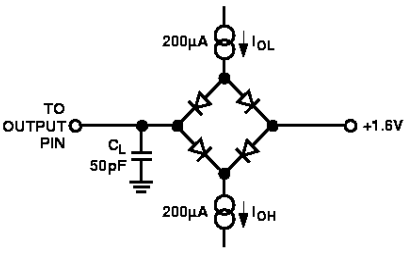


Figure 1. Load Circuit for Digital Output Timing Specifications

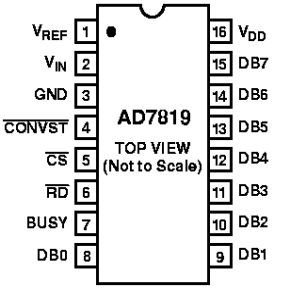
ORDERING GUIDE

Model	Linearity Error (LSB)	Package Description	Package Option
AD7819YN	±1 LSB	Plastic DIP	N-16
AD7819YR	±1 LSB	Small Outline IC	R-16A
AD7819YRU	±1 LSB	Thin Shrink Small Outline (TSSOP)	RU-16

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	V_{REF}	Reference Input, 1.2 V to V_{DD}.
2	V_{IN}	Analog Input, 0 V to V_{REF}.
3	GND	Analog and Digital Ground.
4	$\overline{CONVST}$	Convert Start. A low-to-high transition on this pin initiates a 1 μs pulse on an internally generated $\overline{CONVST}$ signal. A high-to-low transition on this line initiates the conversion process if the internal $\overline{CONVST}$ signal is low. Depending on the signal on this pin at the end of a conversion, the AD7819 automatically powers down.
5	$\overline{CS}$	Chip Select. This is a logic input. $\overline{CS}$ is used in conjunction with $\overline{RD}$ to enable outputs.
6	$\overline{RD}$	Read Pin. This is a logic input. When $\overline{CS}$ is low and $\overline{RD}$ goes low, the DB7–DB0 leave their high impedance state and data is driven onto the data bus.
7	BUSY	ADC Busy Signal. This is a logic output. This signal goes logic high during the conversion process.
8–15	DB0–DB7	Data Bit 0 to 7. These outputs are three-state TTL-compatible.
16	V_{DD}	Positive power supply voltage, +2.7 V to +5.5 V.

PIN CONFIGURATION
DIP/SOIC



TERMINOLOGY

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent upon the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02N + 1.76)\ dB$$

Thus for an 8-bit converter, this is 50 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7819 it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for parts where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7819 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second and third order terms are of different significance. The second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the fundamental expressed in dBs.

Relative Accuracy

Relative accuracy or endpoint nonlinearity is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (0000 . . . 000) to (0000 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Offset Error Match

This is the difference in Offset Error between any two channels.

Gain Error

This is the deviation of the last code transition (1111 . . . 110) to (1111 . . . 111) from the ideal, i.e., VREF – 1 LSB, after the offset error has been adjusted out.

Gain Error Match

This is the difference in Gain Error between any two channels.

Track/Hold Acquisition Time

Track/hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion (the point at which the track/hold returns to track mode). It also applies to situations where a change in the selected input channel takes place or where there is a step input change on the input voltage applied to the selected V_{IN} input of the AD7819. It means that the user must wait for the duration of the track/hold acquisition time after the end of conversion or after a step input change to V_{IN} before starting another conversion, to ensure that the part operates to specification.

CIRCUIT DESCRIPTION

Converter Operation

The AD7819 is a successive approximation analog-to-digital converter based around a charge redistribution DAC. The ADC can convert analog input signals in the range 0 V to V_{DD}. Figures 2 and 3 below show simplified schematics of the ADC. Figure 2 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN+}.

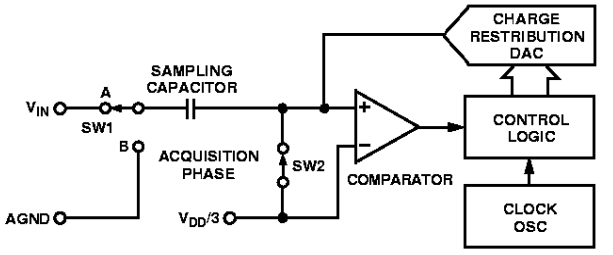


Figure 2. ADC Track Phase

When the ADC starts a conversion, see Figure 3, SW2 will open and SW1 will move to Position B causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced the conversion is complete. The Control Logic generates the ADC output code. Figure 7 shows the ADC transfer function.

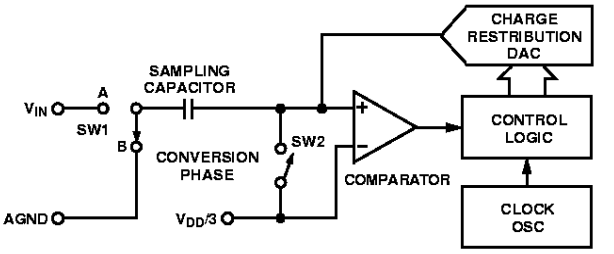


Figure 3. ADC Conversion Phase

TYPICAL CONNECTION DIAGRAM

Figure 4 shows a typical connection diagram for the AD7819. The parallel interface is implemented using an 8-bit data bus, the falling edge of $\overline{CONVST}$ brings the BUSY signal high and at the end of conversion, the falling edge of BUSY is used to initiate an ISR on a microprocessor. (See Parallel Interface section for more details.) V_{REF} is connected to a well decoupled V_{DD} pin to provide an analog input range of 0 V to V_{DD}. When V_{DD} is first connected the AD7819 powers up in a low current mode, i.e., power down. A rising edge on the $\overline{CONVST}$ input will cause the part to power up. (See Power-Up Times section.) If power consumption is of concern, the automatic power-down at the end of a conversion should be used to improve power performance. See Power vs. Throughput Rate section of the data sheet.

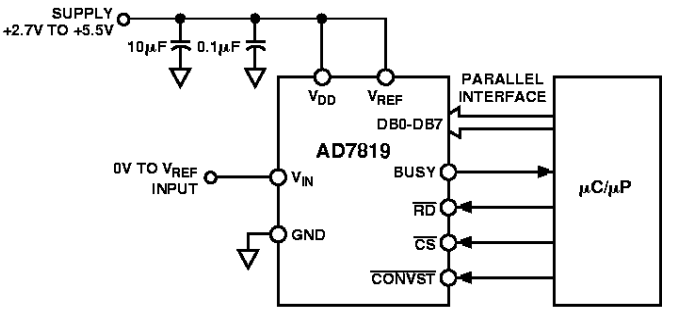


Figure 4. Typical Connection Diagram

Analog Input

Figure 5 shows an equivalent circuit of the analog input structure of the AD7819. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 20 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. The capacitor C2 is typically about 4 pF and can be primarily attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a multiplexer and a switch. This resistor is typically about 125 Ω. The capacitor C1 is the ADC sampling capacitor and has a capacitance of 3.5 pF.

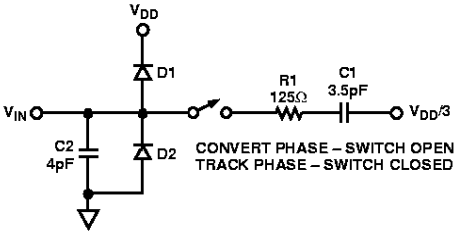


Figure 5. Equivalent Analog Input Circuit

DC Acquisition Time

The ADC starts a new acquisition phase at the end of a conversion and ends on the falling edge of the $\overline{CONVST}$ signal. At the end of a conversion there is a settling time associated with the sampling circuit. This settling time lasts approximately 100 ns. The analog signal on V_{IN} is also being acquired during this settling time. The minimum acquisition time needed is approximately 100 ns. Figure 6 shows the equivalent charging circuit for the sampling capacitor when the ADC is in its acquisition phase. R2 represents the source impedance of a buffer amplifier or resistive network, R1 is an internal multiplexer resistance and C1 is the sampling capacitor.

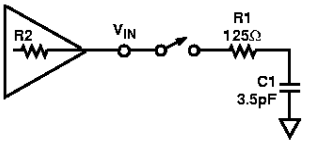


Figure 6. Equivalent Sampling Circuit

During the acquisition phase the sampling capacitor must be charged to within a 1/2 LSB of its final value. The time it takes to charge the sampling capacitor (T_{CHARGE}) is given by the following formula:

$$T_{CHARGE} = 6.2 \times (R2 + 125\ \Omega) \times 3.5\ pF$$

For small values of source impedance, the settling time associated with the sampling circuit (100 ns) is, in effect, the acquisition time of the ADC. For example, with a source impedance (R2) of 10 Ω, the charge time for the sampling capacitor is approximately 3 ns. The charge time becomes significant for source impedances of 2 kΩ and greater.

AC Acquisition Time

In ac applications it is recommended to always buffer analog input signals. The source impedance of the drive circuitry must be kept as low as possible to minimize the acquisition time of the ADC. Large values of source impedance will cause the THD to degrade at high throughput rates.

ADC TRANSFER FUNCTION

The output coding of the AD7819 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSBs, etc.). The LSB size is = $V_{REF}/256$. The ideal transfer characteristic for the AD7819 is shown in Figure 7 below.

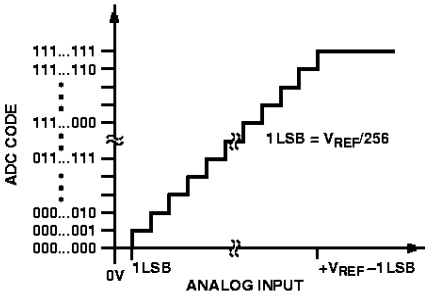


Figure 7. Transfer Characteristic

POWER-UP TIMES

The AD7819 has a 1 µs power-up time. When V_{DD} is first connected, the AD7819 is in a low current mode of operation. In order to carry out a conversion the AD7819 must first be powered up. The ADC is powered up by a rising edge on an internally generated $\overline{\text{CONVST}}$ signal, which occurs as a result of a rising edge on the external $\overline{\text{CONVST}}$ pin. The rising edge of the external $\overline{\text{CONVST}}$ signal initiates a 1 µs pulse on the internal $\overline{\text{CONVST}}$ signal. This pulse is present to ensure the part has enough time to power-up before a conversion is initiated, as a conversion is initiated on the falling edge of gated $\overline{\text{CONVST}}$. See Timing and Control section. Care must be taken to ensure that the $\overline{\text{CONVST}}$ pin of the AD7819 is logic low when V_{DD} is first applied.

When operating in Mode 2, the ADC is powered down at the end of each conversion and powered up again before the next conversion is initiated. (See Figure 8.)

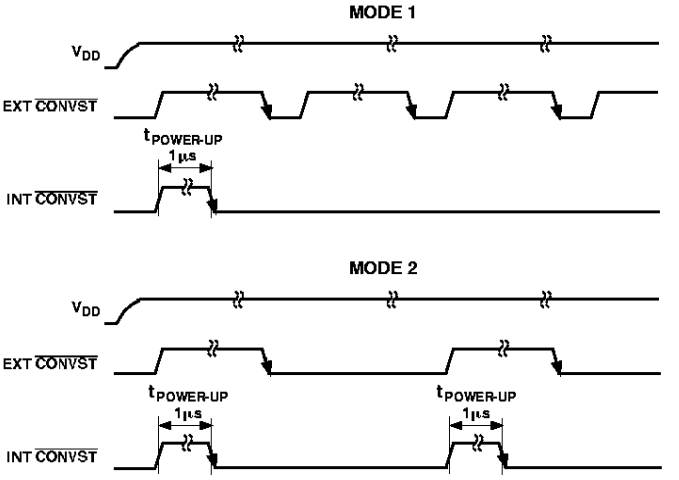


Figure 8. Power-Up Times

POWER VS. THROUGHPUT RATE

By operating the AD7819 in Mode 2, the average power consumption of the AD7819 decreases at lower throughput rates.

Figure 9 shows how the Automatic Power-Down is implemented using the external $\overline{\text{CONVST}}$ signal to achieve the optimum power performance for the AD7819. The AD7819 is operated in Mode 2 and the duration of the external $\overline{\text{CONVST}}$ pulse is set to be equal to or less than the power-up time of the device. As the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

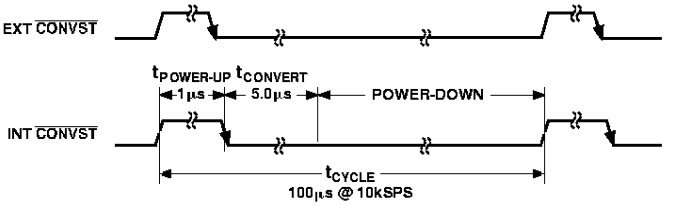


Figure 9. Automatic Power-Down

If, for example, the AD7819 is operated in a continuous sampling mode with a throughput rate of 10 kSPS, the power consumption is calculated as follows. The power dissipation during normal operation is 10.5 mW, V_{DD} = 3 V. If the power-up time is 1 µs and the conversion time is 4.5 µs, the AD7819 can be said to dissipate 10.5 mW for 5.5 µs (worst case) during each conversion cycle. If the throughput rate is 10 kSPS, the cycle time is then 100 µs and the average power dissipated during each cycle is (5.5/100) × (10.5 mW) = 577.5 µW.

Typical Performance Characteristics

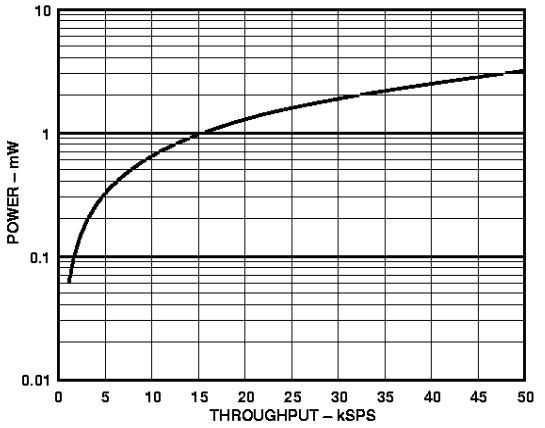


Figure 10. Power vs. Throughput

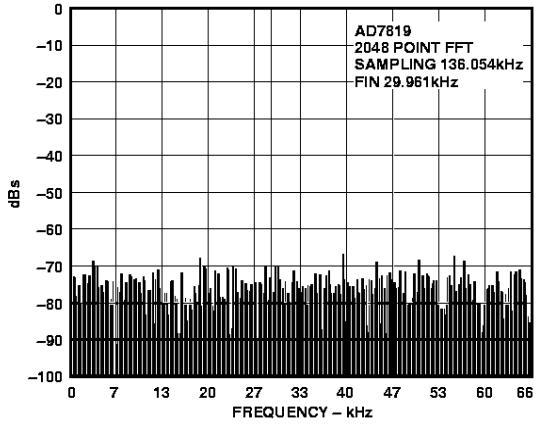


Figure 11. SNR

TIMING AND CONTROL

The AD7819 has only one input for timing and control, i.e., the $\overline{\text{CONVST}}$ (convert start signal). The rising edge of this $\overline{\text{CONVST}}$ signal initiates a 1 µs pulse on an internally generated $\overline{\text{CONVST}}$ signal. This pulse is present to ensure the part has enough time to power up before a conversion is initiated. If the external $\overline{\text{CONVST}}$ signal is low, the falling edge of the internal $\overline{\text{CONVST}}$ signal will cause the sampling circuit to go into hold mode and initiate a conversion. If, however, the external $\overline{\text{CONVST}}$ signal is high when the internal $\overline{\text{CONVST}}$ goes low, it is upon the falling edge of the external $\overline{\text{CONVST}}$ signal that the sampling circuitry will go into hold mode and initiate a conversion. The use of the internally generated 1 µs pulse as previously described can be likened to the configuration shown in Figure 12. The application of a $\overline{\text{CONVST}}$ signal at the $\overline{\text{CONVST}}$ pin triggers the generation of a 1 µs pulse. Both the external $\overline{\text{CONVST}}$ and this internal $\overline{\text{CONVST}}$ are input to an OR gate. The resultant signal has the duration of the longer of the two input signals. Once a conversion has been initiated, the BUSY signal goes high to indicate a conversion is in progress. At the end of conversion the sampling circuit returns to its tracking mode. The end of conversion is indicated by the BUSY signal going low. This signal may be used to initiate an ISR on a microprocessor. At this point the conversion result is latched into the output register where it may be read. The AD7819 has an 8-bit wide parallel interface. The state of the external $\overline{\text{CONVST}}$ signal at the end of conversion also establishes the mode of operation of the AD7819.

Mode 1 Operation (High Speed Sampling)

If the external $\overline{\text{CONVST}}$ is logic high when BUSY goes low, the part is said to be in Mode 1 operation. While operating in Mode 1 the AD7819 will not power down between conversions. The AD7819 should be operated in Mode 1 for high speed sampling applications, i.e., throughputs greater than 100 kSPS. Figure 13 shows the timing for Mode 1 operation. From this diagram one can see that a minimum delay of the sum of the conversion time and read time must be left between two successive falling edges of the external $\overline{\text{CONVST}}$. This is to ensure that a conversion is not initiated during a read.

Mode 2 Operation (Automatic Power-Down)

At slower throughput rates the AD7819 may be powered down between conversion to give a superior power performance. This is Mode 2 Operation and it is achieved by bringing the $\overline{\text{CONVST}}$ signal logic low before the falling edge of BUSY. Figure 14 shows the timing for Mode 2 Operation. The falling edge of the external $\overline{\text{CONVST}}$ signal may occur before or after the falling edge of the internal $\overline{\text{CONVST}}$ signal, but it is the later occurring falling edge of both that controls when the first conversion will take place. If the falling edge of the external $\overline{\text{CONVST}}$ occurs after that of the internal $\overline{\text{CONVST}}$, it means that the moment of the first conversion is controlled exactly, regardless of any jitter associated with the internal $\overline{\text{CONVST}}$ signal. The parallel interface is still fully operational while the AD7819 is powered down. The AD7819 is powered up again on the rising edge of the $\overline{\text{CONVST}}$ signal. The gated $\overline{\text{CONVST}}$ pulse will now remain high long enough for the AD7819 to fully power up, which takes about 1 µs. This is ensured by the internal $\overline{\text{CONVST}}$ signal, which will remain high for 1 µs.

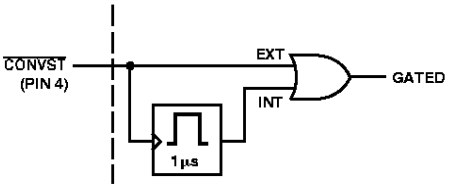


Figure 12.

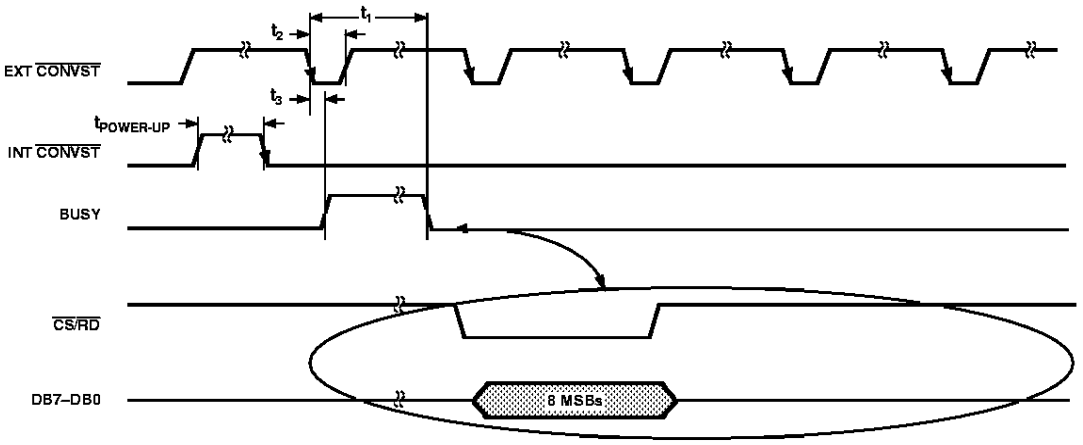


Figure 13. Mode 1 Operation

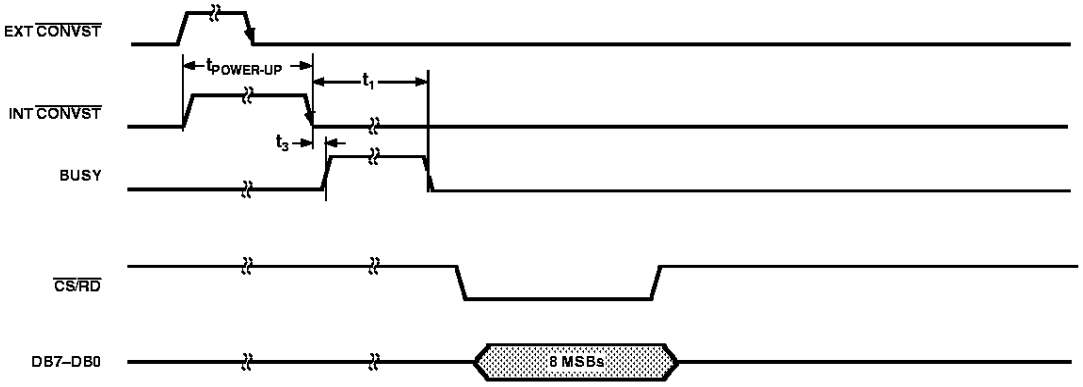


Figure 14. Mode 2 Operation

PARALLEL INTERFACE

The parallel interface of the AD7819 is eight bits wide. The output data buffers are activated when both $\overline{CS}$ and $\overline{RD}$ are logic low. At this point the contents of the data register are placed on the 8-bit data bus. Figure 15 shows the timing diagram for the parallel port. The Parallel Interface of the AD7819 is reset when BUSY goes logic high. Care must be taken to ensure that a read operation does not occur while BUSY is high. Data read from the AD7819 while BUSY is high will be invalid. For optimum performance the read operation should end at least 100 ns (t_{10}) prior to the falling edge of the next $\overline{CONVST}$.

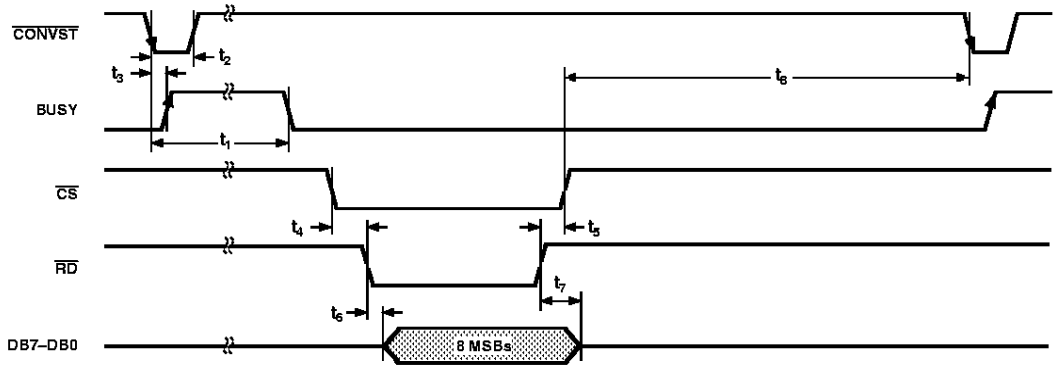


Figure 15. Parallel Port Timing

MICROPROCESSOR INTERFACING

The parallel port on the AD7819 allows the device to be interfaced to a range of many different microcontrollers. This section explains how to interface the AD7819 with some of the more common microcontroller parallel interface protocols.

AD7819 to 8051

Figure 16 shows a parallel interface between the AD7819 and the 8051 microcontroller. The BUSY signal on the AD7819 provides an interrupt request to the 8051 when a conversion begins. Port 0 of the 8051 may serve as an input or output port, or as in this case when used together, may be used as a bidirectional low-order address and data bus. The address latch enable output of the 8051 is used to latch the low byte of the address during accesses to the device, while the high-order address byte is supplied from Port 2. Port 2 latches remain stable when the AD7819 is addressed, as they do not have to be turned around (set to 1) for data input as is the case for Port 0.

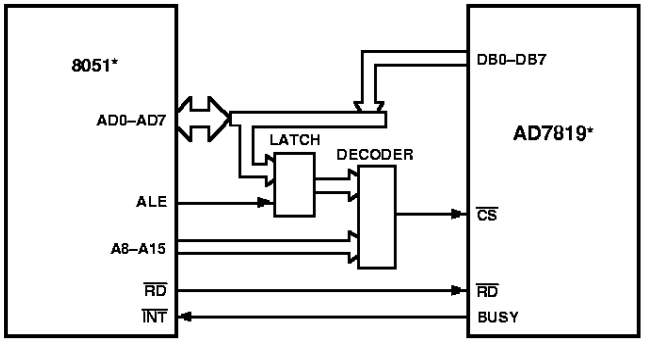


Figure 16. Interfacing to the 8051

AD7819 to PIC16C6x/7x

Figure 17 shows a parallel interface between the AD7819 and the PIC16C64/65/74. The BUSY signal on the AD7819 provides an interrupt request to the microcontroller when a conversion begins. Of the PIC16C6x/7x range of microcontrollers, only the PIC16C64/65/74 can provide the option of a parallel slave port. Port D of the microcontroller will operate as an 8-bit wide parallel slave port when control bit PSPMODE in the TRISE register is set. Setting PSPMODE enables the port pin RE0 to be the $\overline{RD}$ output and RE2 to be the $\overline{CS}$ output. For this functionality, the corresponding data direction bits of the TRISE register must be configured as outputs (reset to 0). See user PIC16/17 Microcontroller User Manual.

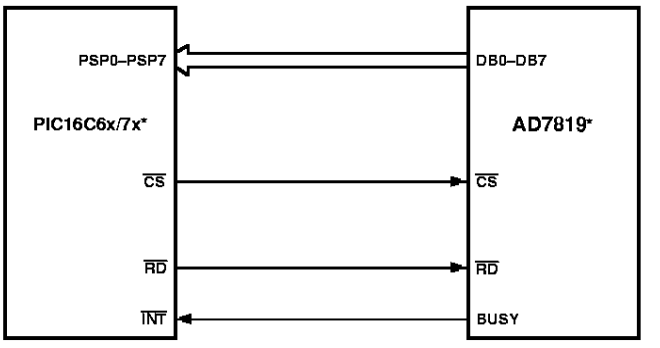


Figure 17. Interfacing to the PIC16C6x/7x

AD7819 to ADSP-21xx

Figure 18 shows a parallel interface between the AD7819 and the ADSP-21xx series of DSPs. As before, the BUSY signal on the AD7819 provides an interrupt request to the DSP when a conversion begins.

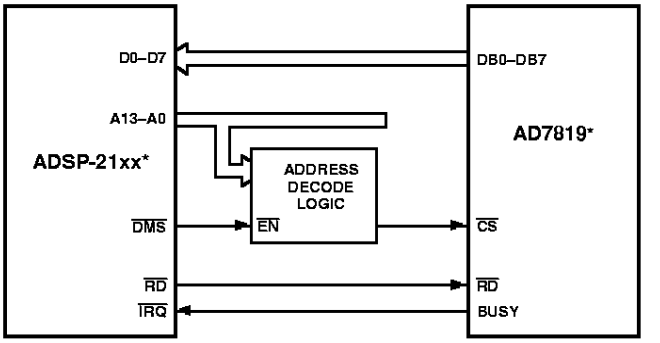
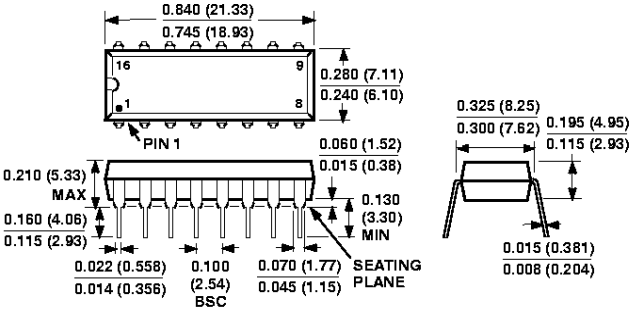


Figure 18. Interfacing to the ADSP-21xx

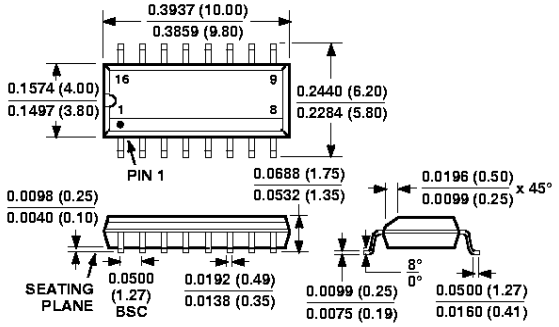
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

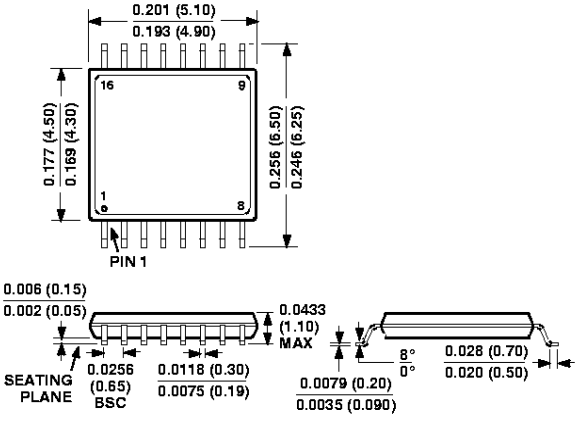
16-Lead Plastic DIP
(N-16)



16-Lead Small Outline Package
(R-16A)



16-Lead Thin Shrink Small Outline Package
(RU-16)



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