AK5522

Differential Input Stereo 32-bit ΔΣ ADC with Excellent PSRR

1. General Description

The AK5522 is a 32-bit, from 8kHz to 192kHz sampling A/D converter for line and microphone inputs of digital audio systems. It achieves 108dB dynamic range and 98dB S/(N+D) while keeping low power consumption performance. Four types of digital filters are integrated and selectable according to the sound quality preference.

The AK5522 has great power supply rejection ratio, (PSRR), and common mode rejection ratio, (CMRR), enabling to maintain sufficient characteristics when connecting USB bus power or DCDC converter output as a power supply. It is suitable for applications with noisy power supply such as USB audio interface, wireless speakers and car audio equipment.

In addition, the AK5522 integrates a regulator with high PSRR for DAC power supply. Using the AK5522 with a DAC such as the AK4432 or the AK4452, it is enable to bring maximum DAC performance even in a poor power supply condition. Moreover, the AK5522 integrates low-jitter PLL circuit that generates a master clock for DAC from LRCK or BICK. It provides a low-EMI solution by avoiding unnecessary drawing of the master clock that has high frequency, on the board.

The AK5522 helps reducing components and a mounting space with these features for environmental noise.

2. Features

- ☐ **Sampling Rate:** 8kHz - 192kHz
- ☐ **Input:** Full Differntial, Pseudo Differential, Single-Ended
- ☐ **S/(N+D):** 98dB typ.
- ☐ **DR, S/N:** 108dB typ.
- ☐ **PSRR:** 80dB typ.
- ☐ **CMRR:** 80dB typ.
- ☐ **Internal Filter:** Four types of LPF, Digital HPF
- ☐ **Short Group Delay:** 4.4/fs (Short Delay Slow roll-off)
- ☐ **Output Format:** 32-bit MSB justified, I^2S or TDM (Cascade Connection available)
- ☐ **Operation Mode:** Master or Slave Modes
- ☐ **Programmable Gain Amp:** –3dB - +12dB/1dB (Fixed at 0dB in Parallel Control mode)
- ☐ **Integrated PLL:** Generates the master clock from BICK or LRCK
- ☐ **Master Clock Output:** Output master clock generated by the PLL
- ☐ **Voltage Regulator for External DAC Power:** Generates 3.3V from 5V applied to AVDD pin.
- ☐ **Power Supply:** Analog 4.5 - 5.5V or 3.0 - 3.6V, Digital 3.0 - 3.6V or 1.7 - 1.98V
- ☐ **Control Mode:** Parallel Control mode (Pin setting)
  Serial Control mode (I^2C Bus setting)
- ☐ **Power Consumption:** 76 mW (@AVDD=5.0V, DVDD=3.3V, fs=48kHz)
- ☐ **Operation Temperature:** –40 - 105°C
- ☐ **Package:** 24-pin QFN 4mmx4mm, 0.5mm pitch

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4. Block Diagram

■ Block Diagram

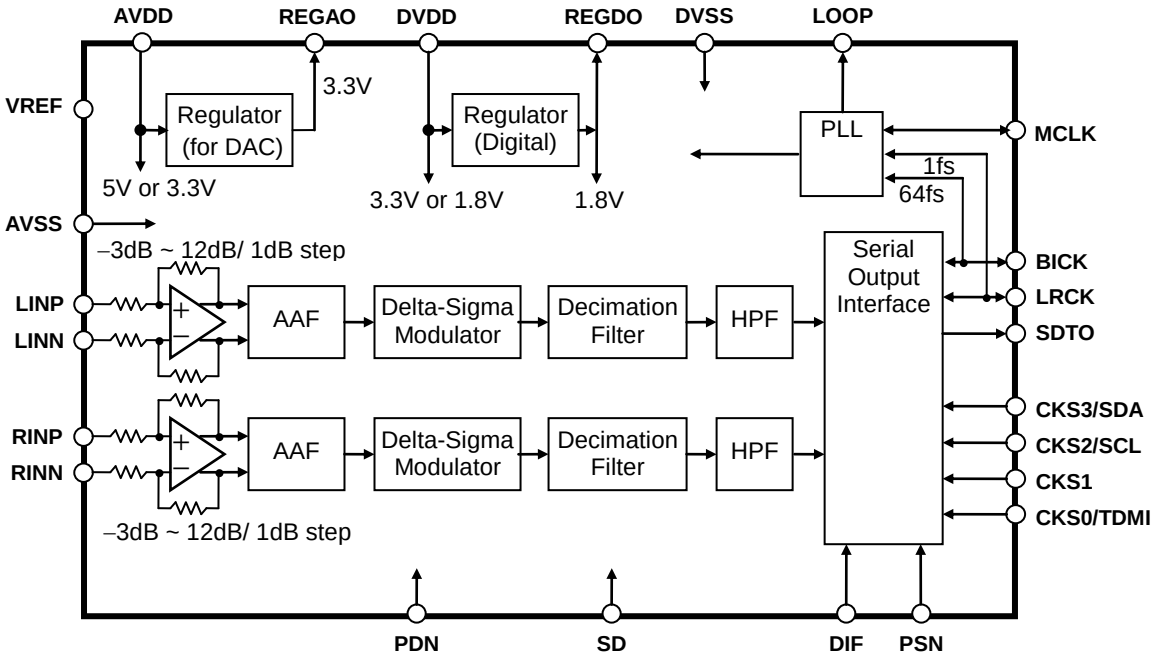


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations

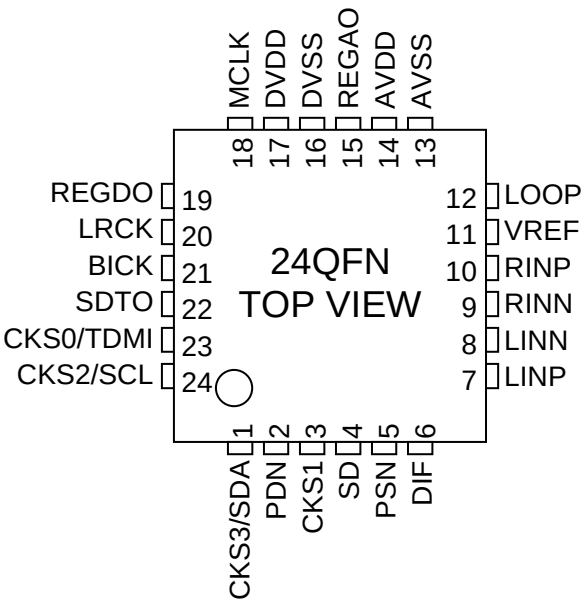


Figure 2. Pin Configurations

■ Pin Functions

No.	Pin Name	I/O	Function	Power Down Status
1	CKS3	I	Clock Mode Select Pin in Parallel Control mode	Hi-Z
	SDA	IO	Control Data I/O Pin for I^2C Bus in Serial Control mode	Hi-Z
2	PDN	I	Reset and Power Down Pin	Hi-Z
3	CKS1	I	Clock Mode Select Pin	Hi-Z
4	SD	I	Digital Filter Select Pin in Parallel Control mode "L": Sharp Roll-Off, "H": Short Delay Sharp Roll-Off	Hi-Z
5	PSN	I	Control Mode Select Pin "L": Serial Control mode, "H": Parallel Control mode	Hi-Z
6	DIF	I	Data Format Select Pin in Parallel Control mode "L": MSB Justified, "H": I^2S Compatible	Hi-Z
7	LINP	I	L Channel Positive Signal Input Pin	Hi-Z
8	LINN	I	L Channel Negative Signal Input Pin	Hi-Z
9	RINN	I	R Channel Negative Signal Input Pin	Hi-Z
10	RINP	I	R Channel Positive Signal Input Pin	Hi-Z
11	VREF	O	Internal Reference Voltage Decoupling Pin Decouple this pin to AVSS with a 1μF±50% capacitor.	Hi-Z, Pulled-down with 0.7kΩ
12	LOOP	O	PLL Loop Filter Connect Pin Connect this pin to AVSS with a 0.01μF±50% capacitor.	Hi-Z
13	AVSS	P	Analog Ground Pin	-
14	AVDD	P	Analog Power Supply Pin. 3.0 - 3.6V or 4.5 - 5.5V	-
15	REGAO	O	Regulator for External DAC Output Pin AVDD=4.5V - 5.5V: 3.3V typ. AVDD=3.0V - 3.6V: Low (External capacitor is not necessary) Connect to AVSS with a 10μF±50% capacitor. Additionally, this pin must be decoupled to the power supply pin of an external DAC with a 10μF±50% and a 0.1μF±50% capacitors in parallel. (Figure 81, Figure 82)	Hi-Z, Pulled-down with 0.5kΩ
16	DVSS	P	Digital Ground Pin	-
17	DVDD	P	Digital Power Supply Pin. 3.0 - 3.6V	-
18	MCLK	I	Master Clock Input Pin in EXT Master / EXT Slave / PLL Master mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	Hi-Z (Input mode)
		O	Master Clock Output Pin in PLL Slave mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	
19	REGDO	O	Regulator Stabilization Capacitor Connect Pin DVDD=3.0V - 3.6V: Output 1.8V typ. Connect to DVSS with a 1μF±50% capacitor.	Hi-Z
		I	DVDD=1.7V - 1.98V: Connect to DVDD	-
20	LRCK	I	Channel Clock Input Pin in Slave mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	Hi-Z (Input mode)
		O	Channel Clock Output Pin in Master mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	
21	BICK	I	Audio Serial Data Clock Input Pin in Slave mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	Hi-Z (Input mode)
		O	Audio Serial Data Clock Output Pin in Master mode This pin is pulled-down to DVSS internally with a 100kΩ resister.	
22	SDTO	O	Audio Serial Data Output Pin	L
23	CKS0	I	Clock Mode Select Pin in Parallel Control mode	Hi-Z
	TDMI	I	TDM Data Input Pin in TDM mode	Hi-Z
24	CKS2	I	Clock Mode Select Pin in Parallel Control mode	Hi-Z
	SCL	I	Control Clock Input Pin for I^2C Bus in Serial Control mode	Hi-Z

I/O I: Input, O: Output, IO: Input and Output, P: Power Supply

Note 1. All digital input pins must not be allowed to float.

■ Handling of Unused Pin

The unused I/O pins should be connected appropriately.

Classification	Pin Name	Setting
Analog	LINP, LINN, RINP, RINN	Open
	REGAO (AVDD = 4.5V - 5.5V, Regulator for DAC = Enable)	Decouple with a 10 μF capacitor to AVSS
	REGAO (AVDD = 4.5V - 5.5V, Regulator for DAC = Disable)	Open
	REGAO (AVDD = 3.0V - 3.6V)	Open
	LOOP	Open
Digital	CKS1, CKS0, SD, DIF (Serial Control mode)	Connect to DVSS
	TDMI (TDM mode)	Connect to DVSS
	MCLK (PLL Slave mode)	Open

6. Absolute Maximum Ratings

(AVSS=DVSS=0V; Note 2)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Analog (AVDD pin) Digital (DVDD pin) Digital (REGDO pin)	VA VD VRD	−0.3 −0.3 −0.3	6.0 6.0 2.5	V V V
Input Current (Any Pin Except Supplies)		IIN	-	±10	mA
Analog Input Voltage (LINP/N, RINP/N pins) (Note 3)		VINA	VDM−0.3	VDP+0.3 or 6.0 (Note 4)	V
Digital Input Voltage (Note 5)		VIND	−0.3	VD+0.3 or 6.0 (Note 6)	V
Ambient Temperature (Power applied)		Ta	−40	105	°C
Storage Temperature		Tstg	−65	150	°C

Note 2. All voltages with respect to ground.
Note 3. VDM and VDP are the voltages generated internally.
Note 4. The maximum value of input voltage is lower value between (VDP+0.3) V or 6.0 V.
Note 5. PDN, SD, LRCK, BICK, MCLK, PSN, CKS0/TDMI, CKS1, CKS2/SCL, CKS3/SDA and DIF pins
Note 6. The maximum value of input voltage is lower value between (VD+0.3) V or 6.0 V.

Mode	AVDD	VDM	VDP
Power-down	3.0 - 3.6V, 4.5 - 5.5V	AVSS	AVDD
Normal operation	4.5 - 5.5V	−0.75V	5.25V
	3.0 - 3.6V	−1.50V	4.50V

Table 1. VDM, VDP Voltage

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(AVSS=DVSS=0V; Note 2)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Analog (AVDD)	VA	4.5	5.0	5.5	V
	Analog (AVDD)	VA	3.0	3.3	3.6	V
	Using internal regulator Digital (DVDD)	VD	3.0	3.3	3.6	V
	Not using internal regulator Digital (DVDD) Digital (REGDO)	VD VRD	1.7	1.8	1.98	V

Note 2. All voltages with respect to ground.
Note 7. The power up sequence between AVDD and DVDD is not critical. If DVDD is 1.7V to 1.98V then the DVDD pin should be connect to the REGDO pin.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

■ Analog Power Supply=5.0V

(Ta=25°C; AVDD=5.0V; DVDD=3.3V, fs=48kHz, 96kHz; 192kHz, BICK=64fs; Signal Frequency=1kHz; 32-bit Data; Measurement frequency=20Hz - 20kHz at fs=48kHz, 40Hz - 40kHz at fs=96kHz and 192kHz, Gain=0dB, unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Analog Input Characteristics:						
Resolution (Note 8)			-	-	32	Bit
Input Voltage			2.0	2.1	2.2	Vrms
S/(N+D)	fs=48kHz BW=20kHz	–1dBFS	92	98	-	dB
		–20dBFS	-	86	-	dB
		–60dBFS	-	46	-	dB
	fs=96kHz BW=40kHz	–1dBFS	-	97	-	dB
		–20dBFS	-	83	-	dB
		–60dBFS	-	43	-	dB
	fs=192kHz BW=40kHz	–1dBFS	-	97	-	dB
		–20dBFS	-	83	-	dB
		–60dBFS	-	43	-	dB
Dynamic Range (–60dBFS with A-weighted)	fs=48kHz, BW=20kHz		103	108	-	dB
Dynamic Range (–60dBFS)	fs=96kHz, 192kHz, BW=40kHz		98	103	-	dB
S/N (A-weighted)	fs=48kHz, BW=20kHz		103	108	-	dB
S/N	fs=96kHz, 192kHz, BW=40kHz		98	103	-	dB
Input Resistance	Full Differential	Gain= +12dB	5	8.5	-	kΩ
		0dB	10	20.7	-	kΩ
		–3dB	10	23.8	-	kΩ
	Pseudo Differential Single End	Gain= +12dB	5	14.0	-	kΩ
		0dB	10	27.3	-	kΩ
		–3dB	10	30.3	-	kΩ
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch			-	0	0.5	dB
Power Supply Rejection Ratio (PSRR) (Note 9)			-	80	-	dB
Common Mode Rejection Ratio (CMRR)			55	80	-	dB
VREF pin Output Voltage			3.72	3.92	4.12	V
Regulator for External DAC						
Output Voltage			3.0	3.3	3.6	V
Output Current			-	-	15	mA
Power Supply Rejection Ratio (Note 9)			-	80	-	dB
Output Noise (Flat)			-	–101	-	dBV
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = “H”) (Note 10)						
AVDD			-	12	18	mA
DVDD	(fs=48kHz)		-	4.7	8	mA
DVDD	(fs=96kHz)		-	8.1	13	mA
DVDD	(fs=192kHz)		-	7.6	12	mA
Power down mode (PDN pin = “L”) (Note 11)						
AVDD+DVDD			-	0	10	μA

Note 8. ADC full-scale input voltage at Gain=0dB. The signal input amplitude can’t exceed 2.1Vrms (typ.) even if the gain is from –3dB to –1dB.

Note 9. PSRR is applied to AVDD, DVDD with 20Hz - 20kHz sine wave.

Note 10. PLL Master mode. PLL3-0 bits = “0101b”

Note 11. All digital inputs are fixed to DVDD or DVSS.

■ Analog Power Supply=3.3V

(Ta=25°C; VA=3.3V; VD=3.3V, fs=48kHz, 96kHz, 192kHz, BICK=64fs; Signal Frequency=1kHz; 32-bit Data; Measurement frequency=20Hz - 20kHz at fs=48kHz, 40Hz - 40kHz at fs=96kHz and 192kHz, Gain=0dB, unless otherwise specified.)

Parameter			Min.	Typ.	Max.	Unit
Analog Input Characteristics:						
Resolution			-	-	32	Bit
Input Voltage		(Note 8)	2.0	2.1	2.2	Vrms
S/(N+D)	fs=48kHz BW=20kHz	−1dBFS	87	93	-	dB
		−20dBFS	-	83	-	dB
		−60dBFS	-	43	-	dB
	fs=96kHz BW=40kHz	−1dBFS	-	92	-	dB
		−20dBFS	-	80	-	dB
		−60dBFS	-	40	-	dB
	fs=192kHz BW=40kHz	−1dBFS	-	92	-	dB
		−20dBFS	-	80	-	dB
		−60dBFS	-	40	-	dB
Dynamic Range (−60dBFS with A-weighted)	fs=48kHz, BW=20kHz		99	104	-	dB
Dynamic Range (−60dBFS)	fs=96kHz, 192kHz, BW=40kHz		94	99	-	dB
S/N (A-weighted)	fs=48kHz, BW=20kHz		99	104	-	dB
S/N	fs=96kHz, 192kHz, BW=40kHz		94	99	-	dB
Input Resistance	Full Differential	Gain= +12dB	5	12.0	-	kΩ
		0dB	10	25.2	-	kΩ
		−3dB	10	29.4	-	kΩ
	Pseudo Differential Single End	Gain= +12dB	5	18.4	-	kΩ
		0dB	10	30.9	-	kΩ
		−3dB	10	32.4	-	kΩ
Interchannel Isolation			110	120		dB
Interchannel Gain Mismatch			-	0	0.5	dB
Power Supply Rejection Ratio		(Note 9)	-	80	-	dB
Common Mode Rejection Ratio (CMRR)			55	80	-	dB
VREF pin Output Voltage			2.34	2.47	2.60	V
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = “H”)		(Note 10)				
AVDD			-	11	16	mA
DVDD	(fs=48kHz)		-	4.7	8	mA
DVDD	(fs=96kHz)		-	8.1	13	mA
DVDD	(fs=192kHz)		-	7.6	12	mA
Power down mode (PDN pin = “L”)		(Note 11)				
AVDD+DVDD			-	0	10	μA

Note 8. ADC full-scale input voltage at Gain=0dB. The signal input amplitude can’t exceed 2.1Vrms (typ.) even if the gain is from −3dB to −1dB.
Note 9. PSRR is applied to AVDD, DVDD with 20Hz - 20kHz sine wave.
Note 10. PLL Master mode. PLL3-0 bits = “0101b”
Note 11. All digital inputs are fixed to DVDD or DVSS.

9. Filter Characteristics

■ ADC Filter Characteristics (fs= 48kHz)

(Ta= –40 - +105°C, AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 3) (Parallel Control mode: SD pin="L", Serial Control mode: SD bit="0", SLOW bit="0")						
Passband (Note 12)	+0.001/–0.06dB –6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 12)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 4) (Parallel Control mode: Not Available, Serial Control mode: SD bit="0", SLOW bit="1")						
Passband (Note 12)	+0.001/–0.076dB –6.0dB	PB	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 12)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	6.7	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 5) (Parallel Control mode: SD pin="H", Serial Control mode: SD bit="1", SLOW bit="0")						
Passband (Note 12)	+0.001/–0.06dB –6.0dB	PB	0 -	- 24.4	22.0 -	kHz kHz
Stopband (Note 12)		SB	27.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 13)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 6) (Parallel Control mode: Not Available, Serial Control mode: SD bit="1", SLOW bit="1")						
Passband (Note 12)	+0.001/–0.076dB –6.0dB	PB -	0 -	- 21.9	12.5 -	kHz kHz
Stopband (Note 12)		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 20.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 13)		GD	-	4.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 12)	–3.0dB –0.5dB –0.1dB	FR	- - -	1.0 2.5 6.5	- - -	Hz Hz Hz

Note 12. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.06dB) =0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.076dB) =0.26 × fs (SLOW ROLL-OFF).

Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces. The signal frequency is 1kHz.

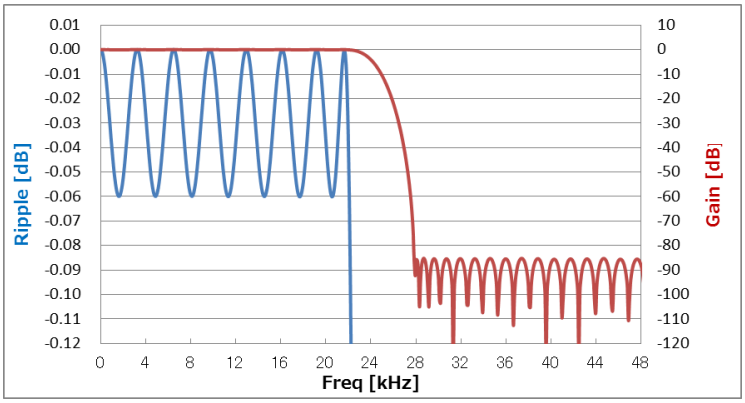


Figure 3. SHARP ROLL-OFF (fs=48kHz)

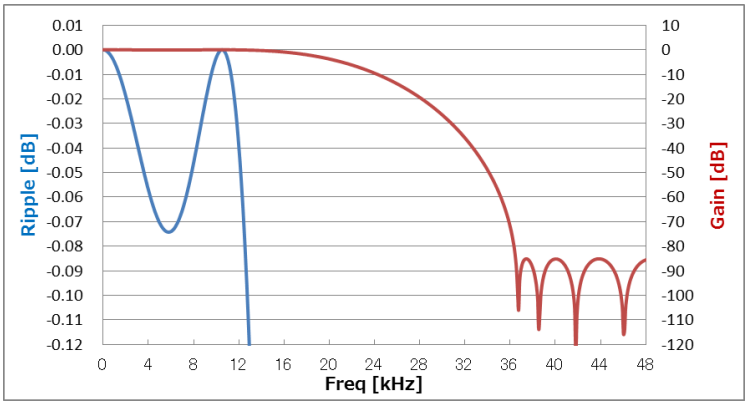


Figure 4. SLOW ROLL-OFF (fs=48kHz)

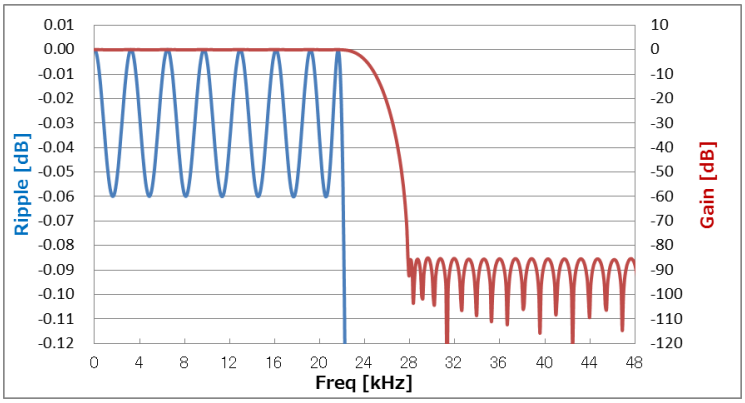


Figure 5. SHORT DELAY SHARP ROLL-OFF (fs=48kHz)

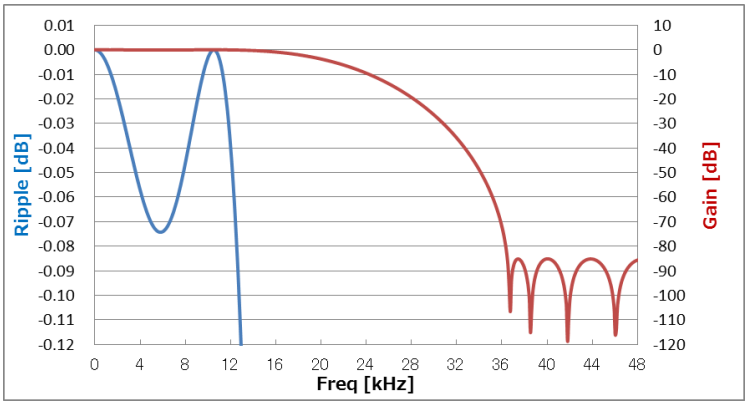


Figure 6. SHORT DELAY SLOW ROLL-OFF (fs=48kHz)

■ **ADC Filter Characteristics (fs= 96kHz)**

(Ta= –40 - +105°C, AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 7) (Parallel Control mode: SD pin="L", Serial Control mode: SD bit="0", SLOW bit="0")						
Passband (Note 12)	+0.001/–0.06dB –6.0dB	PB	0	- 48.8	44.1	kHz kHz
Stopband (Note 12)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	18.8	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 8) (Parallel Control mode: Not Available, Serial Control mode: SD bit="0", SLOW bit="1")						
Passband (Note 12)	+0.001/–0.076dB –6.0dB	PB	0 -	- 43.8	25	kHz kHz
Stopband (Note 12)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	6.7	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF (Figure 9) (Parallel Control mode: SD pin="H", Serial Control mode: SD bit="1", SLOW bit="0")						
Passband (Note 12)	+0.001/–0.06dB –6.0dB	PB	0 -	- 48.8	44.1 -	kHz kHz
Stopband (Note 12)		SB	55.7	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	2.8	1/fs
Group Delay (Note 13)		GD	-	4.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF (Figure 10) (Parallel Control mode: Not Available, Serial Control mode: SD bit="1", SLOW bit="1")						
Passband (Note 12)	+0.001/–0.076dB –6.0dB	PB	0 -	- 43.8	25 -	kHz kHz
Stopband (Note 12)		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	1.2	1/fs
Group Delay (Note 13)		GD	-	4.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 12)	–3.0dB –0.5dB –0.1dB	FR	- - -	1.0 2.5 6.5	- - -	Hz Hz Hz

Note 12. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/–0.06dB) = 0.46 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/–0.076dB) = 0.26 × fs (SLOW ROLL-OFF).

Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces. The signal frequency is 1kHz.

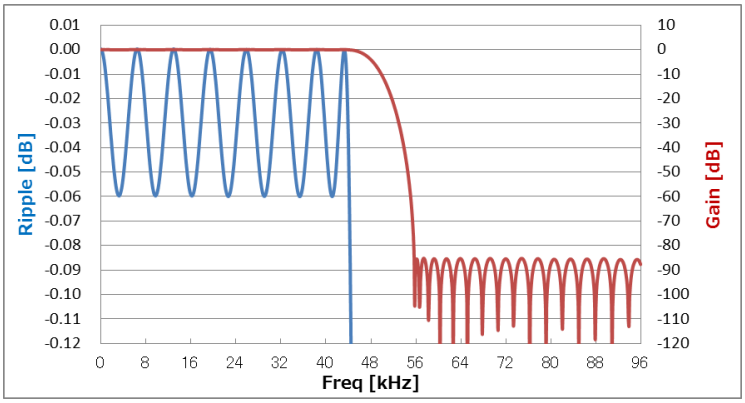


Figure 7. SHARP ROLL-OFF (fs=96kHz)

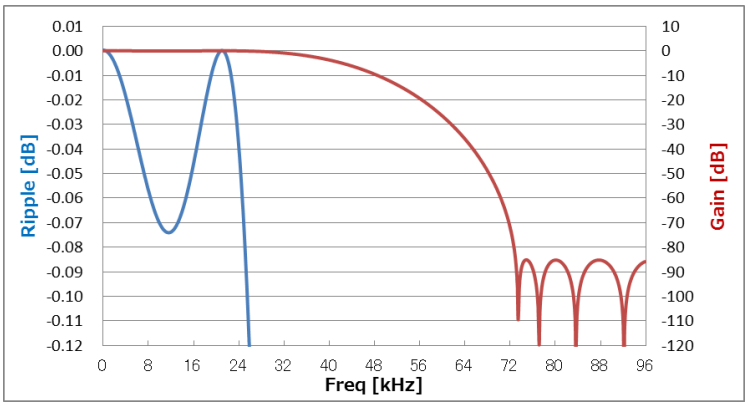


Figure 8. SLOW ROLL-OFF (fs=96kHz)

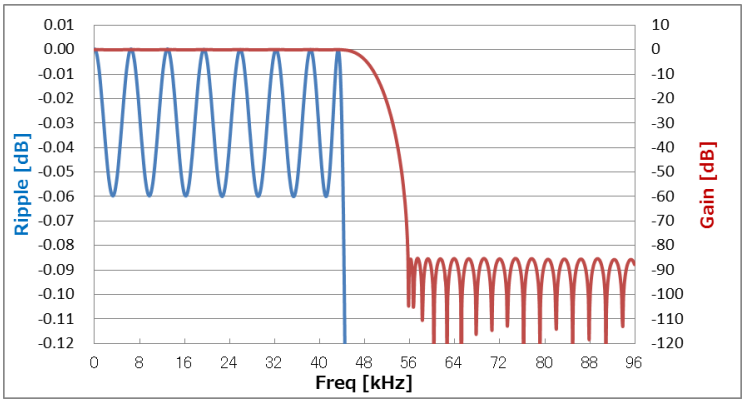


Figure 9. SHORT DELAY SHARP ROLL-OFF (fs=96kHz)

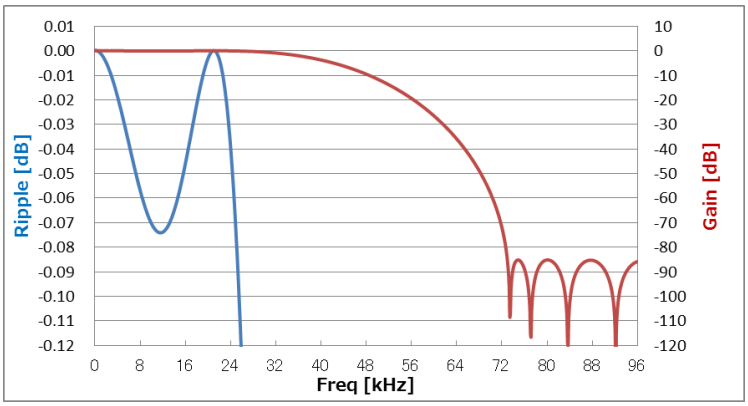


Figure 10. SHORT DELAY SLOW ROLL-OFF (fs=96kHz)

■ **ADC Filter Characteristics (fs= 192kHz)**

(Ta= −40 - +105°C, AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Digital Filter (Decimation LPF): SHARP ROLL-OFF (Figure 11) (Parallel Control mode: SD pin="L", Serial Control mode: SD bit="0", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.037dB −6.0dB	PB	0	- 100.2	83.7	kHz kHz
Stopband (Note 12)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	14.9	-	1/fs
Digital Filter (Decimation LPF): SLOW ROLL-OFF (Figure 12) (Parallel Control mode: Not Available, Serial Control mode: SD bit="0", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.1dB −6.0dB	PB	0	- 75.2	31.5	kHz kHz
Stopband (Note 12)		SB	146	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	0	-	1/fs
Group Delay (Note 13)		GD	-	7.9	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SHARP ROLL-OFF FILTER (Figure 13) (Parallel Control mode: SD pin="H", Serial Control mode: SD bit="1", SLOW bit="0")						
Passband (Note 12)	+0.001/−0.037dB −6.0dB	PB	0 -	- 100.2	83.7 -	kHz kHz
Stopband (Note 12)		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	0.3	1/fs
Group Delay (Note 13)		GD	-	6.4	-	1/fs
Digital Filter (Decimation LPF): SHORT DELAY SLOW ROLL-OFF FILTER (Figure 14) (Parallel Control mode: Not Available, Serial Control mode: SD bit="1", SLOW bit="1")						
Passband (Note 12)	+0.001/−0.1dB −6.0dB	PB	0 -	- 75.2	31.5 -	kHz kHz
Stopband (Note 12)		SB	146	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion 0 - 40.0kHz		ΔGD	-	-	0.4	1/fs
Group Delay (Note 13)		GD	-	6.4	-	1/fs
Digital Filter (HPF):						
Frequency Response (Note 12)	−3.0dB −0.5dB −0.1dB	FR	- - -	1.0 2.5 6.5	- - -	Hz Hz Hz

Note 12. The passband and stopband frequencies scale with fs.
For example, PB (+0.001dB/−0.037dB) =0.436 × fs (SHARP ROLL-OFF).
For example, PB (+0.001dB/−0.1dB) =0.164 × fs (SLOW ROLL-OFF).

Note 13. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the L channel MSB output timing of the SDTO. It may have an error of +1[1/fs] at maximum when outputting data via audio interfaces. The signal frequency is 1kHz.

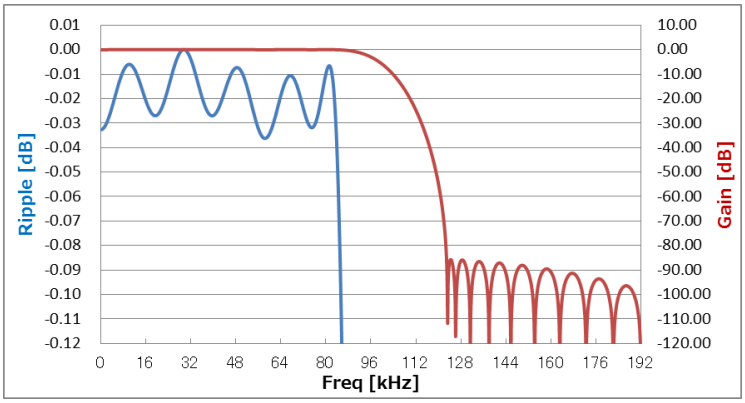


Figure 11. SHARP ROLL-OFF (fs=192kHz)

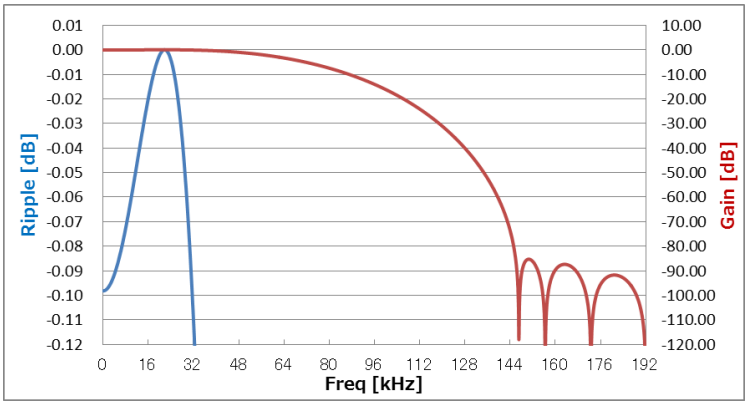


Figure 12. SLOW ROLL-OFF (fs=192kHz)

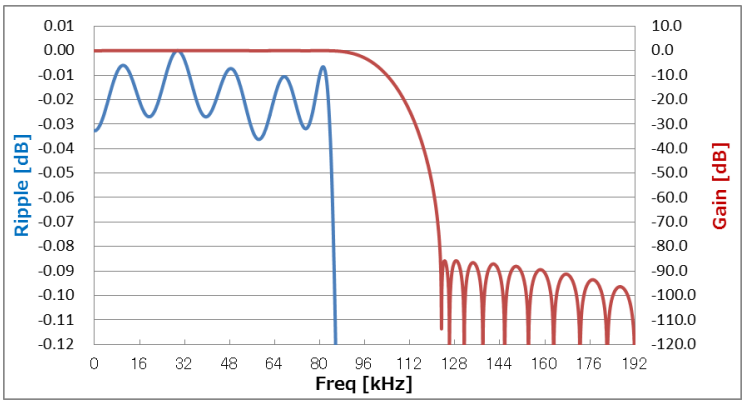


Figure 13. SHORT DELAY SHARP ROLL-OFF (fs=192kHz)

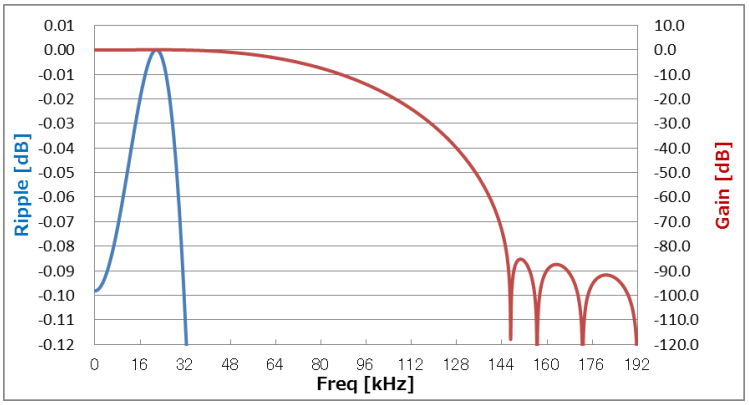


Figure 14. SHORT DELAY SLOW ROLL-OFF (fs=192kHz)

10. DC Characteristics

(Ta=−40 - 105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DVDD=1.7V - 1.98V					
High-Level Input Voltage (Note 14)	VIH	80%DVDD	-	-	V
Low-Level Input Voltage (Note 14)	VIL	-	-	20% DVDD	V
DVDD=3.0V - 3.6V					
High-Level Input Voltage (Note 14)	VIH	70% DVDD	-	-	V
Low-Level Input Voltage (Note 14)	VIL	-	-	30% DVDD	V
High-Level Output Voltage (Note 15) (Iout=−100μA)	VOH	DVDD −0.5	-	-	V
Low-Level Output Voltage (Note 15) (Iout= 100μA)	VOL	-	-	0.5	V
Low-Level Output Voltage (Note 16)	VOL				
(DVDD=1.7V - 1.98V: Iout=3mA)		-	-	20% DVDD	V
(DVDD=3.0V - 3.6V: Iout=3mA)		-	-	0.4	V
Input Leakage Current (Note 14)	Iin	-	-	±10	μA

Note 14. PDN, SD, LRCK (Slave mode), BICK (Slave mode), MCLK (Input), PSN, CKS0/TDMI, CKS1, CKS2/SCL, CKS3/SDA (Input), DIF

Note 15. SDTO, LRCK (Master mode), BICK (Master mode), MCLK (Output)

Note 16. SDA (Output)

11. Switching Characteristics (Parallel Control Mode)

■ System Clocks

□ External Master Mode (Parallel Control Mode)

(Ta=–40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
MCLK=256fsn					
Frequency	fMCLK	2.048	-	13.824	MHz
Pulse Width Low	tMCLKL	32	-	-	ns
Pulse Width High	tMCLKH	32	-	-	ns
MCLK=512fsn, 256fsd, 128fsq					
Frequency	fMCLK	4.096	-	27.648	MHz
Pulse Width Low	tMCLKL	16	-	-	ns
Pulse Width High	tMCLKH	16	-	-	ns
LRCK Output Timing					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		8	-	54	kHz
Double Speed	fsd				
MCLK 256fs		54	-	108	kHz
Quad Speed	fsq				
MCLK 128fs		108	-	216	kHz
Duty Cycle	dLRCK	-	50	-	%
BICK Output Timing					
Stereo Mode					
Period	tBICK	-	1/(64fs)	-	s
Duty Cycle	dBICK	-	50	-	%

□ **External Slave Mode (Parallel Control Mode)**

(Ta=–40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
MCLK=256fsn					
Frequency	fMCLK	2.048	-	13.824	MHz
Pulse Width Low	fMCLKL	29	-	-	ns
Pulse Width High	fMCLKH	29	-	-	ns
MCLK=384fsn					
Frequency	fMCLK	3.072	-	18.432	MHz
Pulse Width Low	fMCLKL	22	-	-	ns
Pulse Width High	fMCLKH	22	-	-	ns
MCLK=512fsn, 256fsd, 128fsq					
Frequency	fMCLK	4.096	-	27.648	MHz
Pulse Width Low	fMCLKL	15	-	-	ns
Pulse Width High	fMCLKH	15	-	-	ns
MCLK=768fsn, 384fsd, 192fsq					
Frequency	fMCLK	6.144	-	36.864	MHz
Pulse Width Low	fMCLKL	11	-	-	ns
Pulse Width High	fMCLKH	11	-	-	ns
LRCK Input Timing					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		8	-	54	kHz
MCLK 384fs, 768fs		8	-	48	kHz
MCLK 1024fs		8	-	32	kHz
Double Speed	fsd				
MCLK 256fs		54	-	108	kHz
MCLK 384fs		48	-	96	kHz
Quad Speed	fsq				
MCLK 128fs		108	-	216	kHz
MCLK 192fs		96	-	192	kHz
Duty Cycle	dLRCK	45	-	55	%
TDM256 Mode					
Frequency	fs				Hz
Normal Speed	fsn	8	-	48	kHz
Pulse Width Low	tLRCKL	1/(256fs)	-	-	s
Pulse Width High	tLRCKH	1/(256fs)	-	-	s
BICK Input Timing					
Stereo Mode					
Period	tBICK				
Normal Speed		1/(256fsn)	-	-	s
Double Speed		1/(128fsd)	-	-	s
Quad Speed		1/(64fsq)	-	-	s
Pulse Width Low	tBICKL	32	-	-	ns
Pulse Width High	tBICKH	32	-	-	ns
TDM256 Mode					
Period	tBICK	-	1/(256fs)	-	s
Pulse Width Low	tBICKL	14	-	-	ns
Pulse Width High	tBICKH	14	-	-	ns

□ PLL Slave Mode (PLL Reference Clock = BICK pin) (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Output Timing					
Stereo Mode					
Frequency					
512fs	fMCLK	-	512fs	-	Hz
256fs		-	256fs	-	Hz
128fs		--	128fs	--	Hz
Duty Cycle	dMCLK	45	50	55	%
Pulse Width Low (@24.576MHz)	tMCLK20	16	-	-	ns
Pulse Width High (@24.576MHz)	tMCLK80	16	-	-	ns
LRCK Input Timing (Note 17)					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		-	44.1	-	kHz
		-	48	-	kHz
Double Speed	fsd				
MCLK 256fs		-	88.2	-	kHz
		-	96	-	kHz
Quad Speed	fsq				
MCLK 128fs		-	176.4	-	kHz
		-	192	-	kHz
Duty Cycle	dLRCK	45	-	55	%
BICK Input Timing					
Stereo Mode					
Period	tBICK	-	1/(64fs)	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s

Note 17. The PLL mode does not support variable pitch mode.

□ **PLL Slave Mode (PLL Reference Clock = LRCK pin) (Parallel Control Mode)**

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Output Timing					
Stereo Mode					
Frequency					
512fs	fMCLK	-	512fs	-	Hz
256fs		-	256fs	-	Hz
128fs		-	128fs	-	Hz
Duty Cycle	dMCLK	45	50	55	%
Pulse Width Low (@24.576MHz)	tMCLK20	16	-	-	ns
Pulse Width High (@24.576MHz)	tMCLK80	16	-	-	ns
LRCK Input Timing (Note 17)					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		-	44.1	-	kHz
		-	48	-	kHz
Double Speed	fsd				
MCLK 256fs		-	88.2	-	kHz
		-	96	-	kHz
Quad Speed	fsq				
MCLK 128fs		-	176.4	-	kHz
		-	192	-	kHz
Duty Cycle	dLRCK	45	-	55	%
BICK Input Timing					
Stereo Mode					
Period	tBICK				
Normal Speed		1/(256fsn)	-	-	s
Double Speed		1/(128fsd)	-	-	s
Quad Speed		1/(64fsq)	-	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s

Note 17. The PLL mode does not support variable pitch mode.

■ Audio Interface

□ External Master Mode (Parallel Control Mode)

(Ta=–40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed , Double Speed, Quad Speed Mode					
DVDD=1.7V - 1.98V					
BICK "↓" to LRCK	tMBLR	–14	-	14	ns
LRCK to SDTO (MSB justified)	tLRS	–24	-	24	ns
BICK "↓" to SDTO	tBSD	–24	-	24	ns
DVDD=3.0V - 3.6V					
BICK "↓" to LRCK	tMBLR	–7	-	7	ns
LRCK to SDTO (MSB justified)	tLRS	–20	-	20	ns
BICK "↓" to SDTO	tBSD	–20	-	20	ns

□ PLL Slave Mode, External Slave Mode (Parallel Control Mode)

(Ta=–40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode					
Normal Speed , Double Speed, Quad Speed Mode					
DVDD=1.7V - 1.98V					
LRCK to BICK "↑" (Note 18)	tLRB	58	-	-	ns
BICK "↑" to LRCK (Note 18)	tBLR	58	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	48	ns
BICK "↓" to SDTO	tSLR	-	-	48	ns
DVDD=3.0V - 3.6V					
LRCK to BICK "↑" (Note 18)	tLRB	33	-	-	ns
BICK "↑" to LRCK (Note 18)	tBLR	33	-	-	ns
LRCK to SDTO (MSB Justified)	tLRS	-	-	28	ns
BICK "↓" to SDTO	tSLR	-	-	28	ns
TDM256 Mode					
Normal Speed Mode					
LRCK to BICK "↑" (Note 18)	tLRB	23	-	-	ns
BICK "↑" to LRCK (Note 18)	tBLR	23	-	-	ns
BICK "↑" to SDTO	tBSDD	5	-	36	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns

Note 18. BICK rising edge must not occur at the same time as LRCK edge.

■ Power-down, Reset (Parallel Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 19)	tPD	150	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns

Note 19. The AK5522 can be reset by setting the PDN pin to “L” upon power-up. The PDN pin must held “L” for more than 150ns for a certain reset. The AK5522 is not reset by the “L” pulse less than 30ns.

■ Timing Diagram (Parallel Control Mode)

Clock Timings (Parallel Control Mode)

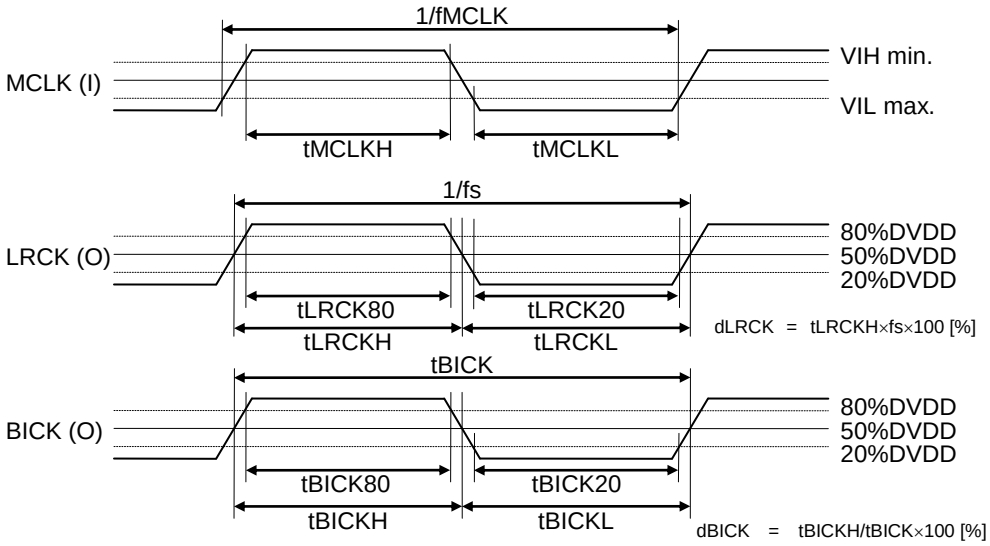


Figure 15. Clock Timing (External Master Mode)

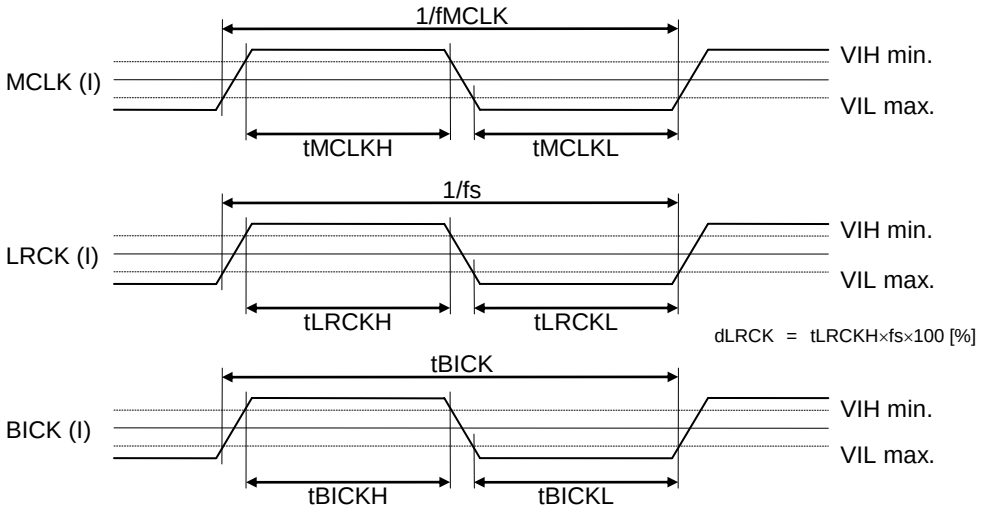


Figure 16. Clock Timing (External Slave Mode)

Clock Timings (Parallel Control Mode) (continued)

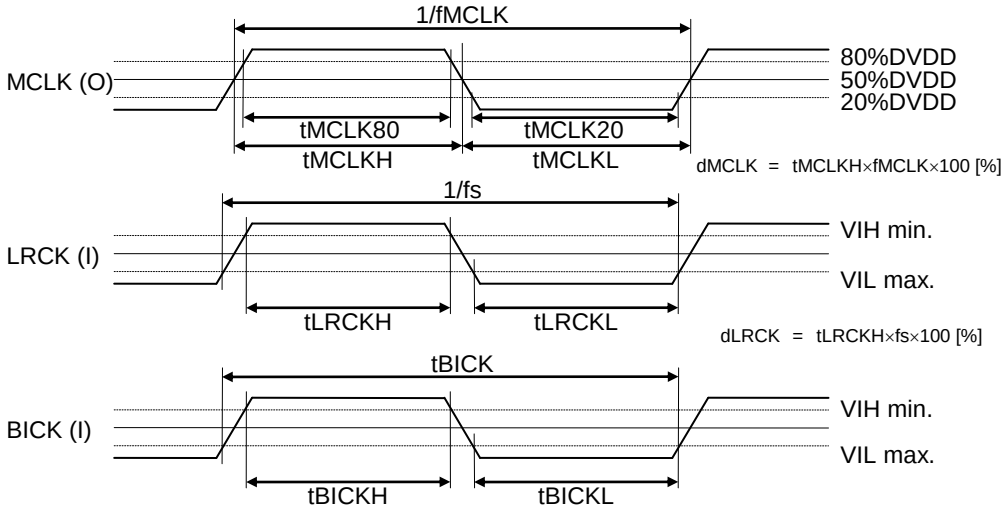


Figure 17. Clock Timing (PLL Slave Mode)

Audio Interface Timings (Parallel Control Mode)

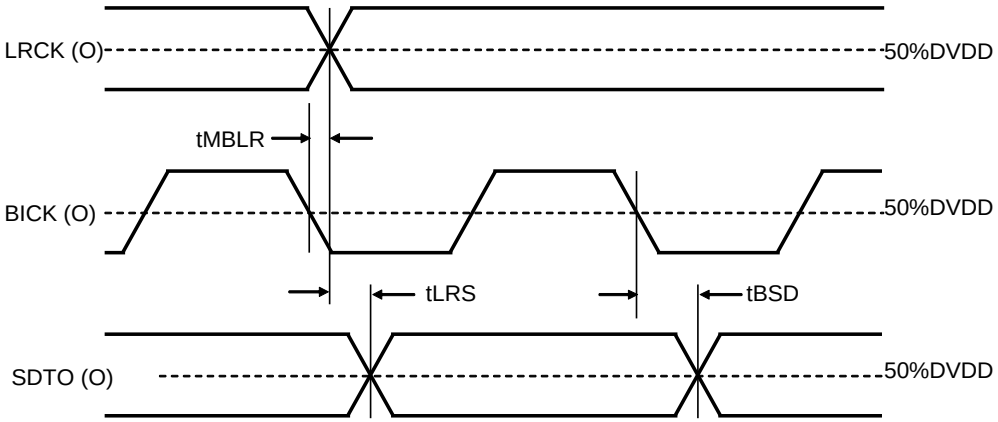


Figure 18. Audio Interface Timing (External Master Mode)

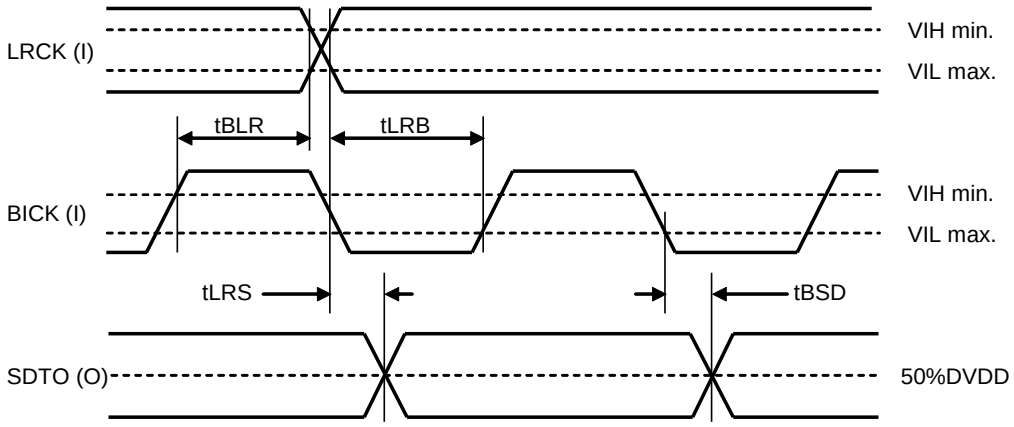


Figure 19. Audio Interface Timing (PLL Slave Mode, External Slave Mode)

Audio Interface Timings (Parallel Control Mode) (continued)

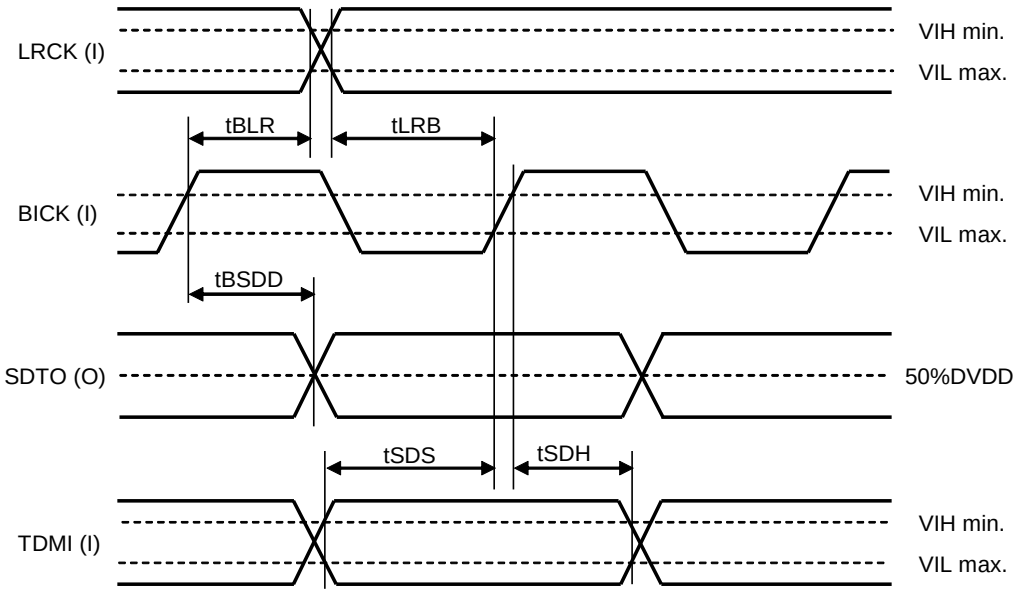


Figure 20. Audio Interface Timing (TDM mode & Slave Mode)

Power-down Timing

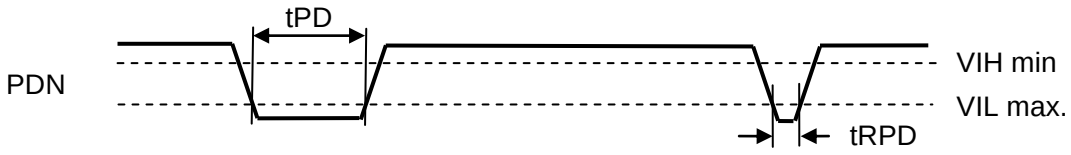


Figure 21. Power-down & Reset Timing

12. Switching Characteristics (Serial Control Mode)

■ System Clocks

□ External Master Mode (Serial Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
MCLK=256fsn					
Frequency	fMCLK	2.048	-	13.824	MHz
Pulse Width Low	tMCLKL	32	-	-	ns
Pulse Width High	tMCLKH	32	-	-	ns
MCLK=512fsn, 256fsd, 128fsq					
Frequency	fMCLK	4.096	-	27.648	MHz
Pulse Width Low	tMCLKL	16	-	-	ns
Pulse Width High	tMCLKH	16	-	-	ns
LRCK Output Timing					
Stereo Mode					
Frequency (fs)					
Normal Speed					
MCLK 256fs, 512fs	fsn	8	-	54	kHz
Double Speed					
MCLK 256fs	fsd	54	-	108	kHz
Quad Speed					
MCLK 128fs	fsq	108	-	216	kHz
Duty Cycle	dLRCK	-	50	-	%
TDM256 Mode					
Frequency (fs)					
Normal Speed	fsn	8	-	48	kHz
Double Speed	fsd	48	-	96	kHz
Pulse Width Low	tLRCKL	-	1/(8fs)	-	s
Pulse Width High	tLRCKH	-	1/(8fs)	-	s
TDM128 Mode					
Frequency (fs)					
Quad Speed	fsq	96	-	192	kHz
Pulse Width Low	tLRCKL	-	1/(4fs)	-	s
Pulse Width High	tLRCKH	-	1/(4fs)	-	s

□ **External Master Mode (Serial Control Mode) (Continued)**

BICK Output Timing						
Stereo Mode						
	Period (Table 18)	tBICK	-		-	
	BCKO1-0 bit = “00”		-	1/(32fs)	-	s
	BCKO1-0 bit = “01”		-	1/(64fs)	-	s
	BCKO1-0 bit = “10”		-	1/(128fs)	-	s
	BCKO1-0 bit = “11”		-	1/(256fs)	-	s
	Duty Cycle	dBICK	-	50	-	%
TDM256 Mode						
	Period (Table 18)	tBICK		1/(256fs)		s
	Duty Cycle	dBICK	-	50	-	%
TDM128 Mode						
	Period (Table 18)	tBICK		1/(128fs)		s
	Duty Cycle (Note 20)	dBICK	-	50	-	%

Note 20. MCLK duty cycle is 50%.

□ **External Slave Mode (Serial Control Mode)**

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
MCLK Input Timing					
MCLK=256fsn					
Frequency	fMCLK	2.048	-	13.824	MHz
Pulse Width Low	tMCLKL	32	-	-	ns
Pulse Width High	tMCLKH	32	-	-	ns
MCLK=384fsn					
Frequency	fMCLK	3.072	-	18.432	MHz
Pulse Width Low	tMCLKL	22	-	-	ns
Pulse Width High	tMCLKH	22	-	-	ns
MCLK=512fsn, 256fsd, 128fsq					
Frequency	fMCLK	4.096	-	27.648	MHz
Pulse Width Low	tMCLKL	16	-	-	ns
Pulse Width High	tMCLKH	16	-	-	ns
MCLK=768fsn, 384fsd, 192fsq					
Frequency	fMCLK	6.144	-	36.864	MHz
Pulse Width Low	tMCLKL	11	-	-	ns
Pulse Width High	tMCLKH	11	-	-	ns

□ **External Slave Mode (Serial Control Mode) (Continued)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
LRCK Input Timing					
Stereo Mode					
Frequency (fs)					
Normal Speed	fsn				
MCLK 256fs, 512fs		8	-	54	kHz
MCLK 384fs, 768fs		8	-	48	kHz
Double Speed	fsd				
MCLK 256fs		54	-	108	kHz
MCLK 384fs		48	-	96	kHz
Quad Speed	fsq				
MCLK 128fs		108	-	216	kHz
MCLK 192fs		96	-	192	kHz
Duty Cycle	dLRCK	45	-	55	%
TDM256 Mode					
Frequency (fs)					
Normal Speed	fsn	8	-	48	kHz
Double Speed	fsd	48	-	96	kHz
Pulse Width Low	tLRCKL	1/(256fs)	-	-	s
Pulse Width High	tLRCKH	1/(256fs)	-	-	s
TDM128 Mode					
Frequency (fs)					
Quad Speed	fsq	96	-	192	kHz
Pulse Width Low	tLRCKL	1/(128fs)	-	-	s
Pulse Width High	tLRCKH	1/(128fs)	-	-	s
BICK Input Timing					
Stereo Mode					
Period	tBICK	-		-	
Normal Speed		1/(256fsn)	-	-	s
Double Speed		1/(128fsd)		-	s
Quad Speed		1/(64fsq)		-	s
Duty Cycle	dBICK	45	-	55	%
TDM256 Mode					
Period	tBICK	-	1/(256fs)	-	s
Pulse Width Low	tBICKL				
Normal Speed		33	-	-	ns
Double Speed		14	-	-	ns
Pulse Width High	tBICKH				
Normal Speed		33	-	-	ns
Double Speed		14	-	-	ns
TDM128 Mode					
Period	tBICK	-	1/(128fs)	-	s
Pulse Width Low	tBICKL				
Quad Speed		14	-	-	ns
Pulse Width High	tBICKH				
Quad Speed		14	-	-	ns

□ PLL Master Mode (PLL Reference Clock = MCLK pin) (Serial Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Input Timing					
Frequency	fMCLK	11.2896	-	27	MHz
Pulse Width Low	tMCLKL	0.4/fMCLK	-	-	s
Pulse Width High	tMCLKH	0.4/fMCLK	-	-	s
LRCK Output Timing (Note 17)					
Stereo mode					
Frequency (f)			See Table 22		
Normal Speed	fsn	-	Mode 0-8	-	Hz
Double Speed	fsd	-	Mode 9-11	-	Hz
Quad Speed	fsq	-	Mode 12-14	-	Hz
Duty Cycle	dLRCK	-	50	-	%
TDM256 mode					
Frequency (fs)			See Table 22		
Normal Speed	fsn	-	Mode 0-8	-	Hz
Double Speed	fsd	-	Mode 9-11	-	Hz
Pulse Width Low	tLRCKL				
I2S compatible		-	1/(8fs)	-	s
MSB justified		-	7/(8fs)	-	s
Pulse Width High	tLRCKH				
I2S compatible		-	7/(8fs)	-	s
MSB justified		-	1/(8fs)	-	s
TDM128 mode					
Frequency (fs)			See Table 22		
Quad Speed	fsq	-	Mode 12-14	-	Hz
Pulse Width Low	tLRCKL				
I2S compatible		-	1/(4fs)	-	s
MSB justified		-	3/(4fs)	-	s
Pulse Width High	tLRCKH				
I2S compatible		-	3/(4fs)	-	s
MSB justified		-	1/(4fs)	-	s

Note 17. The PLL mode does not support variable pitch mode.

□ **PLL Master Mode (PLL Reference Clock = MCLK pin) (Serial Control Mode) (Continued)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
BICK Output Timing					
Stereo Mode					
Period (Table 18)	tBICK	-		-	
BCKO1-0 bit = "00"		-	1/(32fs)	-	s
BCKO1-0 bit = "01"		-	1/(64fs)	-	s
BCKO1-0 bit = "10"		-	1/(128fs)	-	s
BCKO1-0 bit = "11"		-	1/(256fs)	-	s
Duty Cycle	dBICK	-	50	-	%
TDM256 Mode (Normal Speed)					
Period (Table 18)	tBICK		1/(256fs)		s
Duty Cycle	dBICK	-	50	-	%
TDM256 Mode (Double Speed)					
Period (Table 18)	tBICK		1/(256fs)		s
Duty Cycle	dBICK	-	50	-	%
TDM128 Mode (Quad Speed)					
Period (Table 18)	tBICK		1/(128fs)		s
Duty Cycle	dBICK	-	50	-	%

□ PLL Slave Mode (PLL Reference Clock = BICK pin) (Serial Control Mode)

(Ta=–40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Output Timing					
Stereo Mode, TDM128 Mode, TDM256 Mode					
Frequency					
512fs	fMCLK	-	512fs	-	Hz
256fs		-	256fs	-	Hz
128fs		-	128fs	-	Hz
Duty Cycle	dMCLK	45	50	55	%
Pulse Width Low (@24.576MHz)	tMCLK20	16	-	-	ns
Pulse Width High (@24.576MHz)	tMCLK80	16	-	-	ns
Duty Cycle (@16.384MHz)	dMCLK	-	60	-	%
LRCK Input Timing (Note 17)					
Stereo Mode					
Frequency (fs)		-	See Table 22	-	
Normal Speed	fsn	-	Mode 0-8	-	Hz
MCLK 256fs, 512fs					
Double Speed	fsd	-	Mode 9-11	-	Hz
MCLK 256fs					
Quad Speed	fsq	-	Mode 12-14	-	Hz
MCLK 128fs					
Duty Cycle	dLRCK	45		55	%
TDM256 Mode					
Frequency (fs)		-	See Table 22	-	
Normal Speed	fsn	-	Mode 0-8	-	Hz
Double Speed	fsd	-	Mode 9-11	-	Hz
Pulse Width Low	tLRCKL	1/(256fs)	-	255/(256fs)	s
Pulse Width High	tLRCKH	1/(256fs)	-	255/(256fs)	s
TDM128 Mode					
Frequency (fs)		-	See Table 22	-	
Quad Speed	fsq	-	Mode 12-14	-	Hz
Pulse Width Low	tLRCKL	1/(128fs)	-	127/(128fs)	s
Pulse Width High	tLRCKH	1/(128fs)	-	127/(128fs)	s
BICK Input Timing					
Stereo Mode					
Period	tBICK	-	1/(64fs)	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s

Note 17. The PLL mode does not support variable pitch mode.

□ **PLL Slave Mode (PLL Reference Clock = LRCK pin) (Serial Control Mode)**

(Ta=–40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK Output Timing					
Stereo mode, TDM128 mode, TDM256 mode					
Frequency					
512fs	fMCLK	-	512fs	-	Hz
256fs		-	256fs	-	Hz
128fs		-	128fs	-	Hz
Duty Cycle	dMCLK	45	50	55	%
Pulse Width Low (@24.576MHz)	tMCLK20	16	-	-	ns
Pulse Width High (@24.576MHz)	tMCLK80	16	-	-	ns
Duty Cycle (@16.384MHz)	dMCLK	-	60	-	%
LRCK Input Timing (Note 17)					
Stereo mode					
Frequency (fs)			See Table 22		
Normal Speed MCLK 256fs, 512fs	fsn	-	Mode 0-8	-	Hz
Double Speed MCLK 256fs	fsd	-	Mode 9-11	-	Hz
Quad Speed MCLK 128fs	fsq	-	Mode 12-14	-	Hz
Duty Cycle	Duty	45	-	55	%
TDM256 mode					
Frequency (fs)			See Table 22		
Normal Speed	fsn	-	Mode 0-8	-	Hz
Double Speed	fsd	-	Mode 9-11	-	Hz
Pulse Width Low	tLRCKL	1/(256fs)	-	255/(256fs)	s
Pulse Width High	tLRCKH	1/(256fs)	-	255/(256fs)	s
TDM128 mode					
Frequency (fs)			See Table 22		
Quad Speed	fsq	-	Mode 12-14	-	Hz
Pulse Width Low	tLRCKL	1/(128fs)	-	127/(128fs)	s
Pulse Width High	tLRCKH	1/(128fs)	-	127/(128fs)	s
BICK Input Timing					
Stereo mode					
Period	tBICK				
Normal Speed		1/(256fsn)	-	-	s
Double Speed		1/(128fsd)	-	-	s
Quad Speed		1/(64fsn)	-	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s
TDM256 mode					
Period	tBICK	-	1/(256fs)	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s
TDM128 mode					
Period	tBICK	-	1/(128fs)	-	s
Pulse Width Low	tBICKL	0.4 x tBICK	-	-	s
Pulse Width High	tBICKH	0.4 x tBICK	-	-	s

Note 17. The PLL mode does not support variable pitch mode.

■ Audio Interface

□ External Master Mode, PLL Master Mode (Serial Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Stereo Mode (Normal Speed , Double Speed, Quad Speed)					
DVDD=1.7V - 1.98V					
BICK "↓" to LRCK	tMBLR	−14	-	14	ns
LRCK to SDTO (MSB justified)	tLRS	−24	-	24	ns
BICK "↓" to SDTO	tBSD	−24	-	24	ns
DVDD=3.0V - 3.6V					
BICK "↓" to LRCK	tMBLR	−7	-	7	ns
LRCK to SDTO (MSB justified)	tLRS	−20	-	20	ns
BICK "↓" to SDTO	tBSD	−20	-	20	ns
TDM256 Mode (Normal Speed , Double Speed)					
BICK "↓" to LRCK	tMBLR	−10	-	10	ns
BICK "↑" to SDTO	tBSDD	5	-	36	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns
TDM128 Mode (Quad Speed)					
BICK "↓" to LRCK	tMBLR	−10	-	10	ns
BICK "↑" to SDTO	tBSDD	5	-	36	ns
TDMI Setup time to BICK "↑"	tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"	tSDH	5	-	-	ns

□ **External Slave Mode, PLL Slave Mode (Serial Control Mode)**

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Stereo Mode (Normal Speed , Double Speed, Quad Speed)						
DVDD=1.7V - 1.98V						
LRCK to BICK "↑"	(Note 18)	tLRB	58	-	-	ns
BICK "↑" to LRCK	(Note 18)	tBLR	58	-	-	ns
LRCK to SDTO (MSB Justified)		tLRS	-	-	48	ns
BICK "↓" to SDTO		tSLR	-	-	48	ns
DVDD=3.0V - 3.6V						
LRCK to BICK "↑"	(Note 18)	tLRB	33	-	-	ns
BICK "↑" to LRCK	(Note 18)	tBLR	33	-	-	ns
LRCK to SDTO (MSB Justified)		tLRS	-	-	28	ns
BICK "↓" to SDTO		tSLR	-	-	28	ns
TDM256 Mode (Normal Speed)						
LRCK to BICK "↑"	(Note 18)	tLRB	23	-	-	ns
BICK "↑" to LRCK	(Note 18)	tBLR	23	-	-	ns
BICK "↑" to SDTO		tBSDD	5	-	36	ns
TDMI Setup time to BICK "↑"		tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"		tSDH	5	-	-	ns
TDM256 Mode (Double Speed)						
LRCK to BICK "↑"	(Note 18)	tLRB	14	-	-	ns
BICK "↑" to LRCK	(Note 18)	tBLR	14	-	-	ns
BICK "↑" to SDTO		tBSDD	5	-	36	ns
TDMI Setup time to BICK "↑"		tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"		tSDH	5	-	-	ns
TDM128 (Quad Speed)						
LRCK to BICK "↑"	(Note 18)	tLRB	14	-	-	ns
BICK "↑" to LRCK	(Note 18)	tBLR	14	-	-	ns
BICK "↑" to SDTO		tBSDD	5	-	36	ns
TDMI Setup time to BICK "↑"		tSDS	5	-	-	ns
TDMI Hold time to BICK "↑"		tSDH	5	-	-	ns

Note 18. BICK rising edge must not occur at the same time as LRCK edge.

■ I²C Bus, Power-down, Reset (Serial Control Mode)

(Ta=−40 - +105°C; AVDD=3.0 - 3.6V or 4.5 - 5.5V, DVDD=3.0 - 3.6V or 1.7 - 1.98V, C_L=20pF, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Control Interface Timing (I²C Bus):					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 21)	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	1.0	μs
Fall Time of Both SDA and SCL Lines	tF	0.6	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0	-	-	μs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	-	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF
Power-down & Reset Timing					
PDN Accept Pulse Width (Note 19)	tAPD	150	-	-	ns
PDN Reject Pulse Width	tRPD	-	-	30	ns

Note 19. The AK5522 can be reset by setting the PDN pin to “L” upon power-up. The PDN pin must held “L” for more than 150ns for a certain reset. The AK5522 is not reset by the “L” pulse less than 30ns.

Note 21. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

■ Timing Diagram (Serial Control Mode)

Clock Timings (Serial Control Mode)

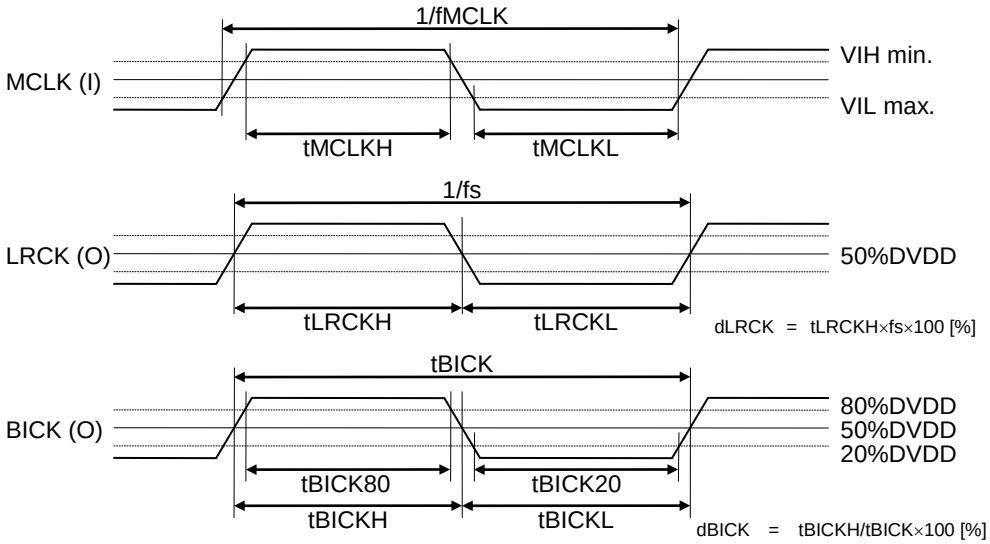


Figure 22. Clock Timing (External Master Mode)

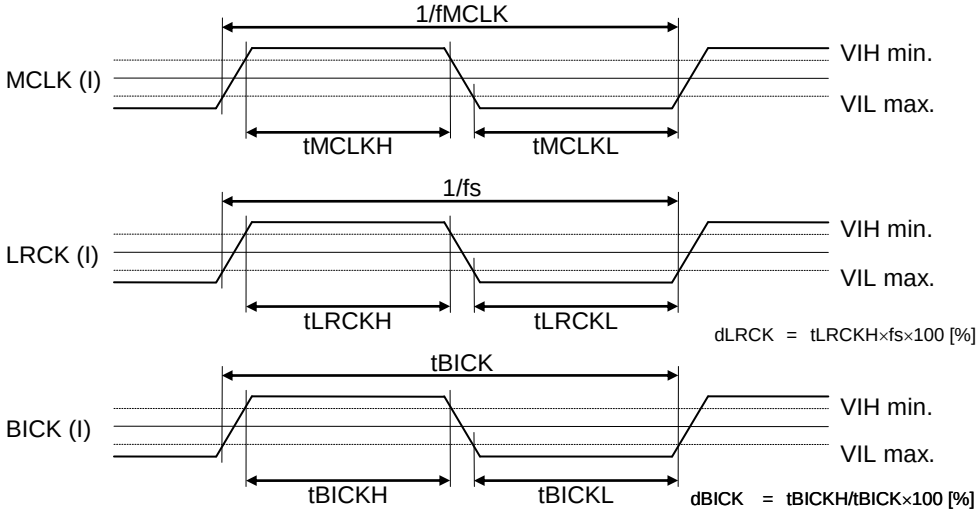


Figure 23. Clock Timing (External Slave Mode)

Clock Timings (Serial Control Mode) (continued)

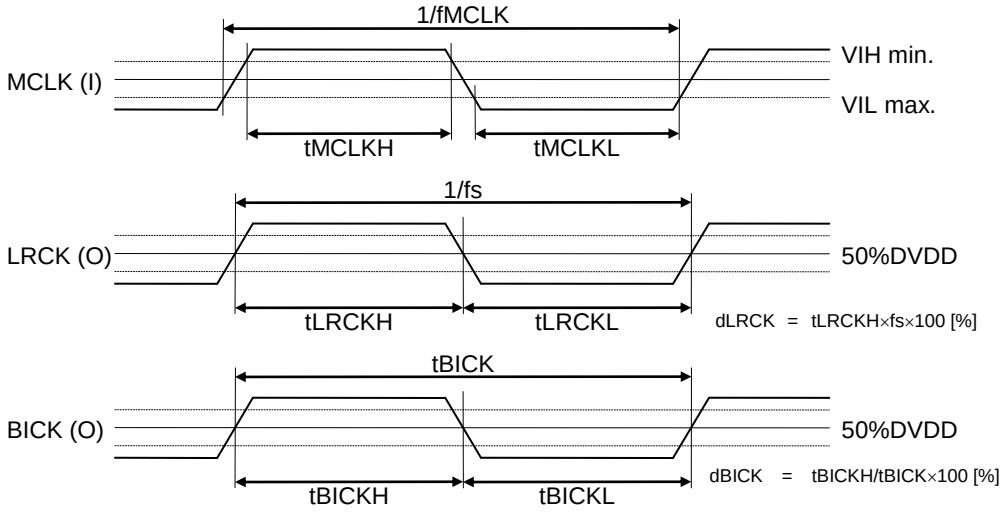


Figure 24. Clock Timing (PLL Master Mode)

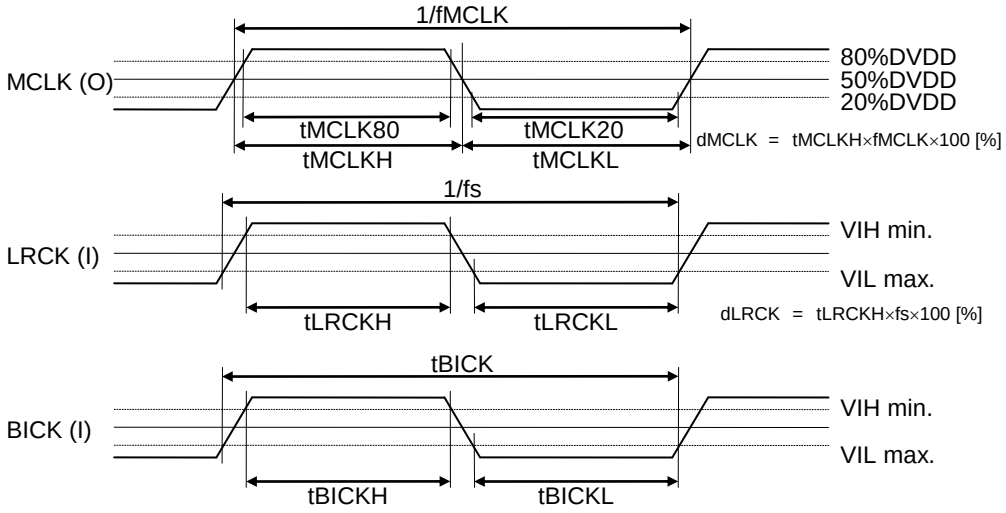


Figure 25. Clock Timing (PLL Slave Mode)

Audio Interface Timings (Serial Control Mode)

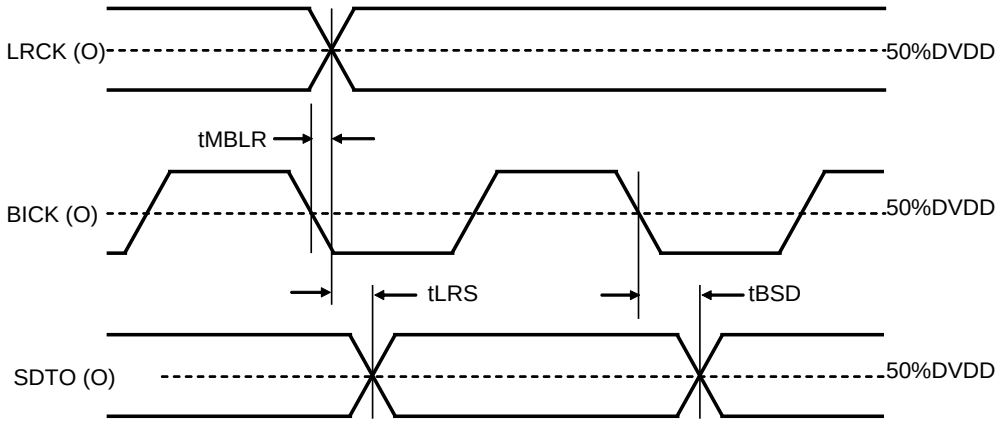


Figure 26. Audio Interface Timing (PLL Master mode, External Master Mode)

Audio Interface Timings (Serial Control Mode) (continued)

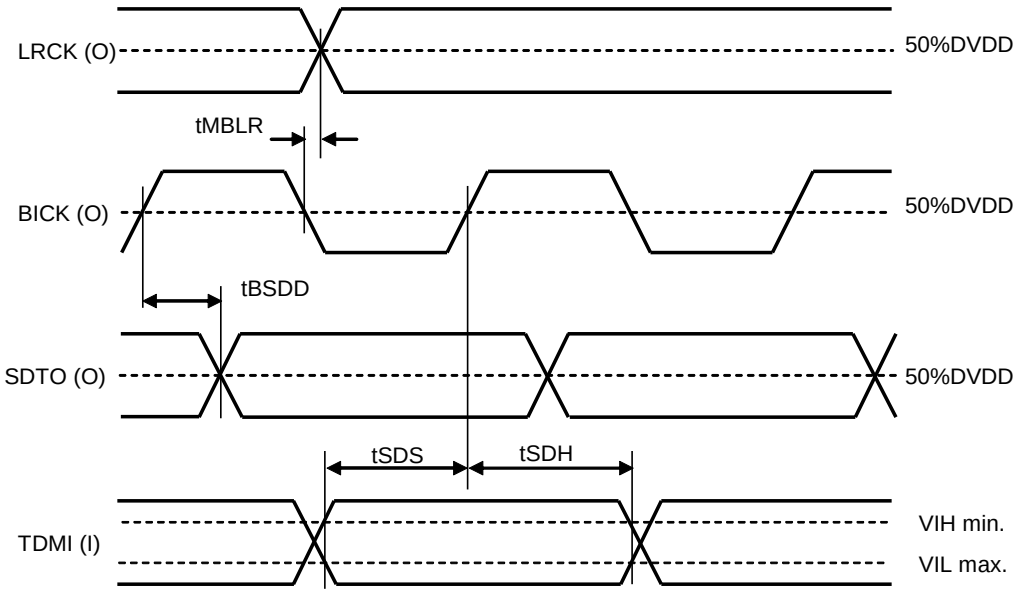


Figure 27. Audio Interface Timing (TDM mode & Master Mode)

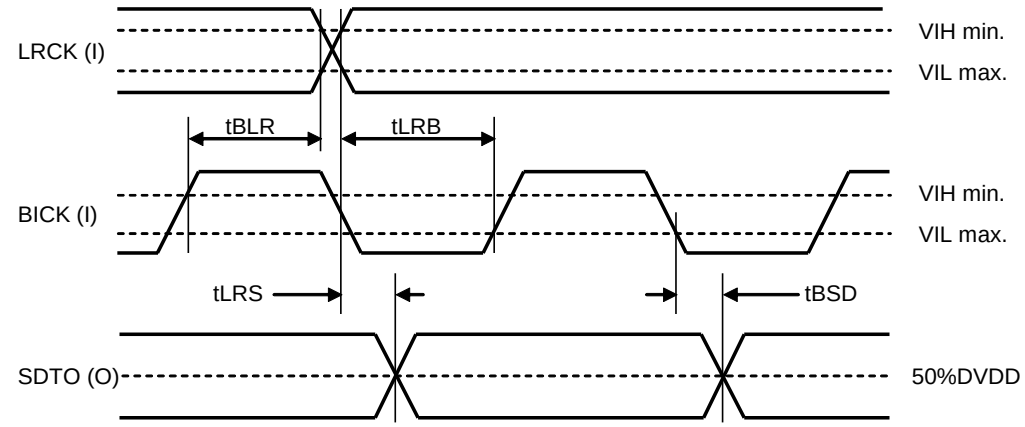


Figure 28. Audio Interface Timing (PLL Slave mode, External Slave Mode)

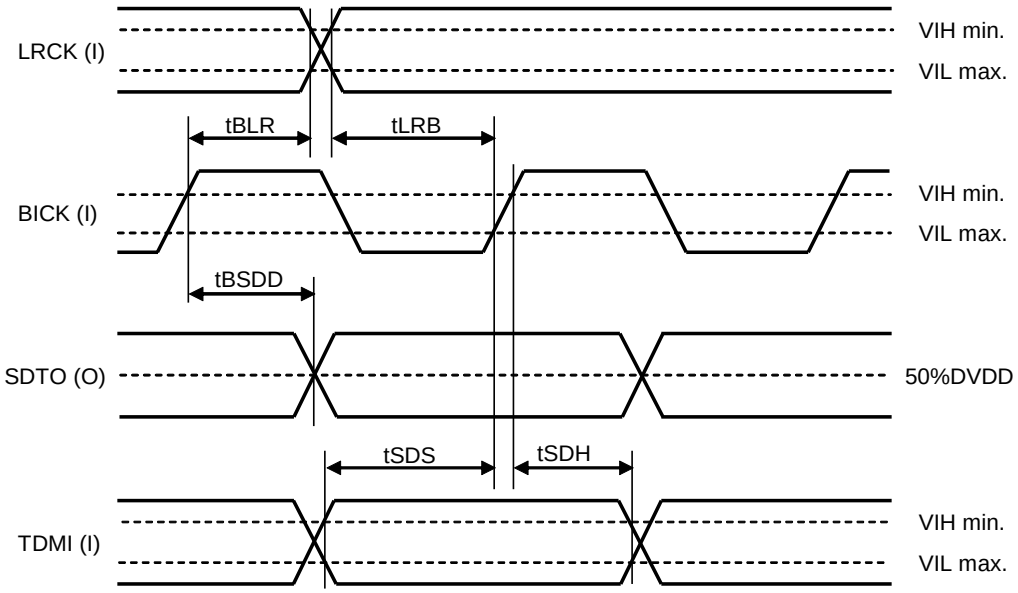


Figure 29. Audio Interface Timing (TDM mode & Slave Mode)

Audio Interface Timings (Serial Control Mode) (continued)

I²C Bus Timing

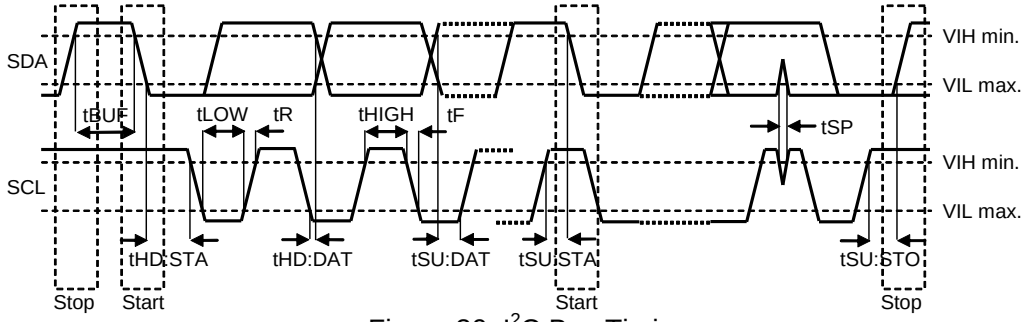


Figure 30. I²C Bus Timing

Power-down Timing

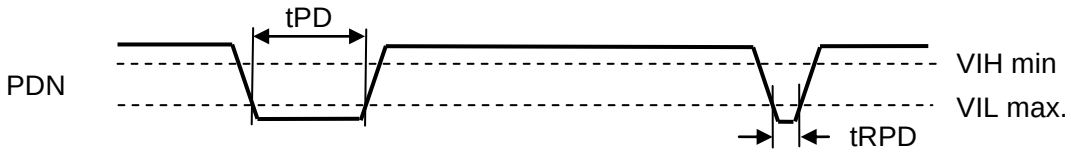


Figure 31. Power-down & Reset Timing

13. Functional Descriptions (Parallel Control Mode)

■ Digital Power Supply

DVDD is the power for the digital core and the digital I/O buffer. The digital core operates with 1.8V power supply. This 1.8V is generated from DVDD (3.3V) by the internal voltage regulator. It is possible to supply 1.8V for DVDD. In this case, connect the REGDO pin with the DVDD pin in order to supply power to the digital core.

■ Analog Power Supply

AVDD is the power for the analog block and the regulator for external DAC power supply.

■ Regulator for External DAC Power Supply

The AK5522 has a regulator for an external DAC power supply. The regulator generates 3.3V from 5V of AVDD. When AVDD is 3.3V the regulator is disabled automatically.

■ Parallel / Serial Control Mode

There are two control modes for operation setting.
The AK5522 is in parallel control mode by setting the PSN pin = “H”. Operation in parallel control mode is set by the CKS3-0 pins, the SD pin and the DIF pin. The AK5522 is in serial control mode by setting the PSN pin = “L”. Operation in serial control mode is selected by control registers. The control registers are set by I^2C bus. When the AK5522 is in operation, the state of the PSN pin cannot be changed.

■ System Clocks (Parallel Control Mode)

The AK5522 requires a master clock (MCLK), an audio serial data clock (BICK) and a channel clock (LRCK).

There are three clock modes to connect the clocks with external devices in parallel control mode (Table 2). The clock mode is selected by CKS3-0 pins (Table 3).

Clock Mode	Clock Pin Status			Connection Diagram
	MCLK	BICK	LRCK	
EXT Master	In	Out	Out	Figure 32
EXT Slave	In	In	In	Figure 33
PLL Slave	Out	In (Ref.)	In (Ref.)	Figure 34

Table 2. Clock Mode (Parallel Control)

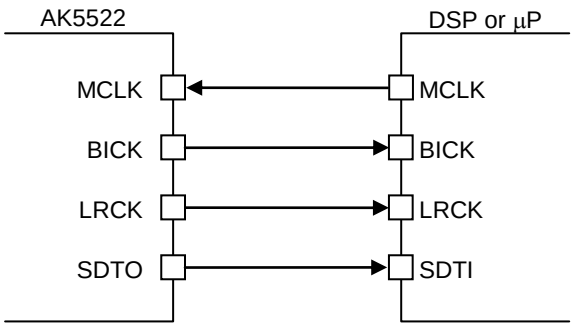


Figure 32. EXT Master Mode

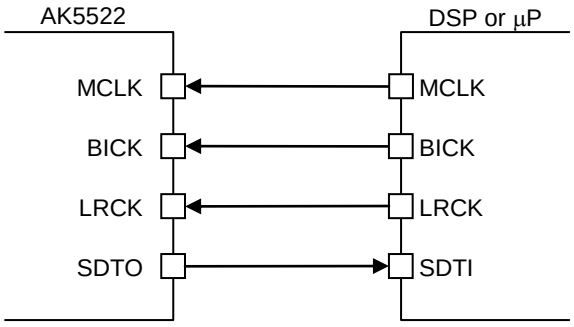
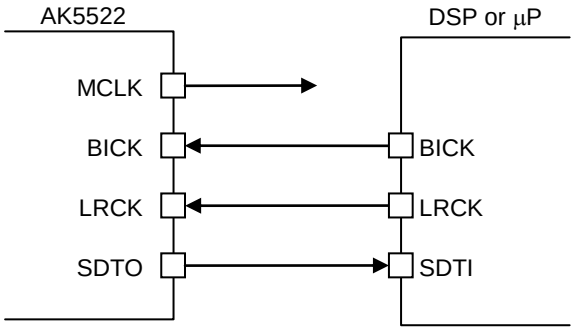


Figure 33. EXT Slave Mode



The reference clock for PLL is selected from BICK and LRCK.

Figure 34. PLL Slave Mode

The AK5522 integrates a phase detection circuit for LRCK. If the internal timing becomes out of synchronization in slave mode, the AK5522 is reset automatically and the phase is re-synchronized. The frequency of operation clocks and clock mode should be changed while the PDN pin= “L”. A stable clock must be supplied after releasing the reset. When synchronizing more than two devices, stop the system clock and reset all AK5522’s once by the PDN pin. Then, input the same system clock to all AK5522’s after making pin or register settings.

■ Operation Mode (Parallel Control Mode)

The operation modes are shown in Table 3.

Mode	CKS3 /SDA pin	CKS2 /SCL pin	CKS1 pin	CKS0 /TDMI pin	Master /Slave	Stereo /TDM	MCLK	I/O	LRCK (fs) [kHz]	I/O	BICK	I/O	PLL Clock
0	L	L	L	L	Master	Stereo	512fs	I	8 - 54	O	64fs	O	OFF
1	L	L	L	H	Master	Stereo	256fs	I	54 - 108	O	64fs	O	OFF
2	L	L	H	L	Master	Stereo	256fs	I	8 - 54	O	64fs	O	OFF
3	L	L	H	H	Master	Stereo	128fs	I	108 - 216	O	64fs	O	OFF
4	L	H	L	L	Slave	Stereo	1024fs	I	8 - 32	I	32fs, 64fs, 128fs, 256fs	I	OFF
							768fs	I	8 - 48	I			OFF
							512fs	I	8 - 54	I			OFF
							384fs	I	48 - 96	I	32fs, 64fs, 128fs	I	OFF
							256fs	I	54 - 108	I			OFF
							192fs,	I	96 - 192	I	32fs, 64fs	I	OFF
							128fs	I	108 - 216	I			OFF
5	L	H	L	H	Slave	Stereo	384fs,	I	8 - 48	I	32fs, 64fs, 128fs, 256fs	I	OFF
							256fs	I	8 - 54	I			OFF
6	L	H	H	L	Slave	Stereo	512fs	O	44.1, 48	I	64fs	I	BICK
7	L	H	H	H	Slave	Stereo	256fs	O	44.1, 48	I	64fs	I	BICK
8	H	L	L	L	Slave	Stereo	256fs	O	88.2, 96	I	64fs	I	BICK
9	H	L	L	H	Slave	Stereo	128fs	O	176.4, 192	I	64fs	I	BICK
10	H	L	H	L	Slave	Stereo	512fs	O	44.1, 48	I	32fs, 64fs, 128fs, 256fs	I	LRCK
11	H	L	H	H	Slave	Stereo	256fs	O	44.1, 48	I			LRCK
12	H	H	L	L	Slave	Stereo	256fs	O	88.2, 96	I	32fs, 64fs, 128fs	I	LRCK
13	H	H	L	H	Slave	Stereo	128fs	O	176.4, 192	I	32fs, 64fs	I	LRCK
14	H	H	H	TDMI	Slave	TDM	256fs	I	8 - 54	I	256fs	I	OFF

Table 3. Operation Mode Setting (Parallel Control Mode)

EXT Master Mode (Parallel Control Mode)
The operation mode 0-3 in Table 3 are external master mode.

Mode	CKS3 /SDA pin	CKS2 /SCL pin	CKS1 pin	CKS0 /TDMI pin	Stereo /TDM	MCLK	I/O	LRCK (fs) [kHz]	I/O	BICK	I/O	PLL
0	L	L	L	L	Stereo	512fs	I	8 - 54	O	64fs	O	OFF
1	L	L	L	H	Stereo	256fs	I	54 - 108	O	64fs	O	OFF
2	L	L	H	L	Stereo	256fs	I	8 - 54	O	64fs	O	OFF
3	L	L	H	H	Stereo	128fs	I	108 - 216	O	64fs	O	OFF

Table 4. EXT Master Mode Setting (Parallel Control Mode)

	MCLK [MHz]		
fs [kHz]	128fs	256fs	512fs
8	N/A	2.048	4.096
16	N/A	4.096	8.192
32	N/A	8.192	16.384
48	N/A	12.288	24.576
96	N/A	24.576	N/A
192	24.576	N/A	N/A

(N/A: Not available)

Table 5. System Clock Example (EXT Master Mode)

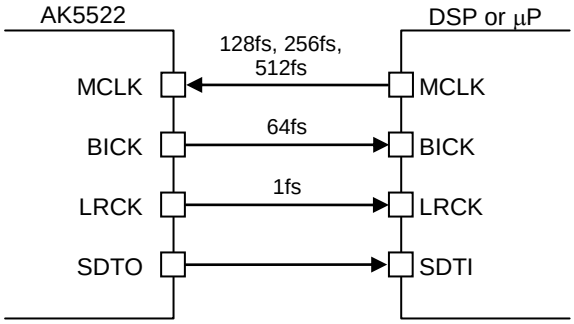


Figure 35. EXT Master Mode

EXT Slave Mode (Parallel Control Mode)
The operation mode 4-5 and mode 14 in Table 3 are external slave mode.
MCLK should be synchronized with LRCK but the phase is not critical.

Mode	CKS3 /SDA pin	CKS2 /SCL pin	CKS1 pin	CKS0 /TDMI pin	Stereo /TDM	MCLK	I/O	LRCK (fs) [kHz]	I/O	BICK	I/O	PLL
4	L	H	L	L	Stereo	1024fs	I	8 - 32	I	32fs, 64fs, 128fs, 256fs	I	OFF
						768fs	I	8 - 48	I			OFF
						512fs	I	8 - 54	I			OFF
						384fs	I	48 - 96	I	32fs, 64fs, 128fs	I	OFF
						256fs	I	54 - 108	I			OFF
						192fs	I	96 - 192	I	32fs, 64fs	I	OFF
						128fs	I	108 - 216	I			OFF
5	L	H	L	H	Stereo	384fs	I	8 - 48	I	32fs, 64fs, 128fs, 256fs	I	OFF
						256fs	I	8 - 54	I			OFF
14	H	H	H	TDMI	TDM	256fs	I	8 - 54	I	256fs	I	OFF

Table 6. EXT Slave mode Setting (Parallel Control Mode)

	MCLK [MHz]						
fs [kHz]	128fs	192fs	256fs	384fs	512fs	768fs	1024fs
8	N/A	N/A	2.048	3.072	4.096	6.144	8.192
16	N/A	N/A	4.096	6.144	8.192	12.288	16.384
32	N/A	N/A	8.192	12.288	16.384	24.576	32.768
48	N/A	N/A	12.288	18.432	24.576	36.864	N/A
96	N/A	18.432	24.576	36.864	N/A	N/A	N/A
192	24.576	36.864	N/A	N/A	N/A	N/A	N/A

(N/A: Not Available)

Table 7. System Clock Example (EXT Slave Mode)

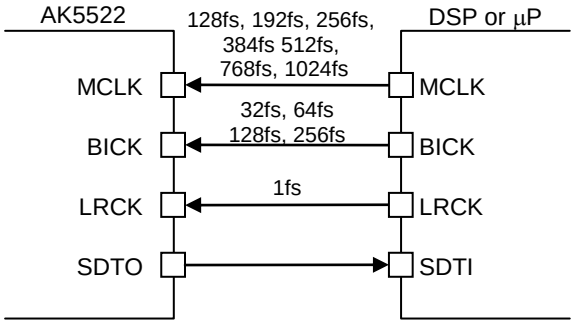


Figure 36. EXT Slave Mode (Stereo Output)

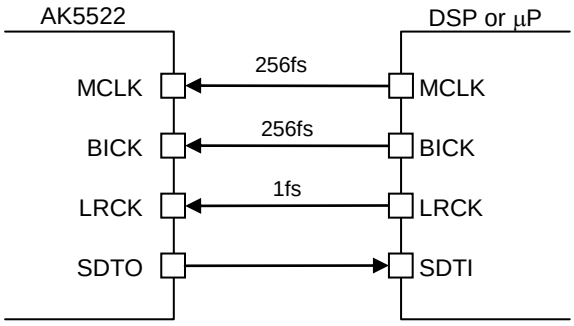


Figure 37. EXT Slave Mode (TDM Output)

PLL Slave Mode (Parallel Control Mode)
The operation mode 6-13 in Table 3 are PLL slave mode. The PLL generates an internal master clock from BICK (64fs) or LRCK (fs). And the master clock is output from the MCLK pin.

Mode	CKS3 /SDA pin	CKS2 /SCL pin	CKS1 pin	CKS0 /TDMI pin	Stereo /TDM	MCLK Freq.	I/O	LRCK Freq. (fs) [kHz]	I/O	BICK Freq.	I/O	PLL Clock
6	L	H	H	L	Stereo	512fs	O	44.1, 48	I	64fs	I	BICK
7	L	H	H	H	Stereo	256fs	O	44.1, 48	I	64fs	I	BICK
8	H	L	L	L	Stereo	256fs	O	88.2, 96	I	64fs	I	BICK
9	H	L	L	H	Stereo	128fs	O	176.4, 192	I	64fs	I	BICK
10	H	L	H	L	Stereo	512fs	O	44.1, 48	I	32fs, 64fs, 128fs, 256fs	I	LRCK
11	H	L	H	H	Stereo	256fs	O	44.1, 48	I			LRCK
12	H	H	L	L	Stereo	256fs	O	88.2, 96	I	32fs, 64fs, 128fs	I	LRCK
13	H	H	L	H	Stereo	128fs	O	176.4, 192	I	32fs, 64fs	I	LRCK

Table 8. PLL Slave Mode Setting (Parallel Control Mode)

	MCLK [MHz]		
fs [kHz]	128fs	256fs	512fs
44.1	N/A	11.2896	22.5792
48	N/A	12.288	24.576
88.2	N/A	22.5792	N/A
96	N/A	24.576	N/A
176.4	22.5792	N/A	N/A
192	24.576	N/A	N/A

(N/A: Not available)

Table 9. System Clock Example (PLL Slave Mode)

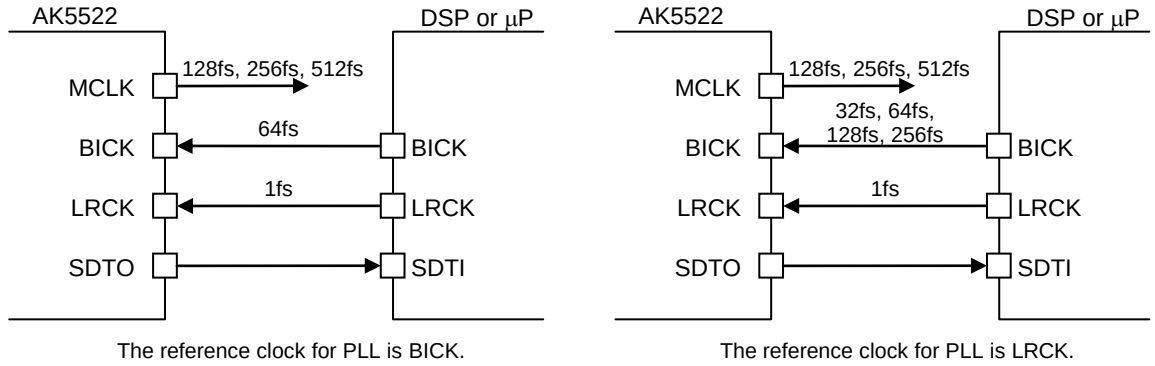


Figure 38. PLL Slave Mode

■ Audio Interface Format (Parallel Control Mode)

The audio interface format is selected with the DIF pin.

DIF pin	Data Format
L	32bit MSB Justified
H	32bit I^2S Compatible

Table 10. Audio Interface Format

■ Cascade Connection in TDM Mode (Parallel Control Mode)

The AK5522 supports cascade connection of four devices in TDM256 mode. Figure 39 shows a connection example. All A/D converted data of connected AK5522's are output from the SDTO pin of the last AK5522 by cascade connection.

When using multiple devices on cascade connection, internal operation timing of each device may differ for one MCLK cycle depending on MCLK and BICK input timings. To prevent this timing difference, BICK "↓" should be more than ± 10ns from MCLK "↑" as shown in Table 11.

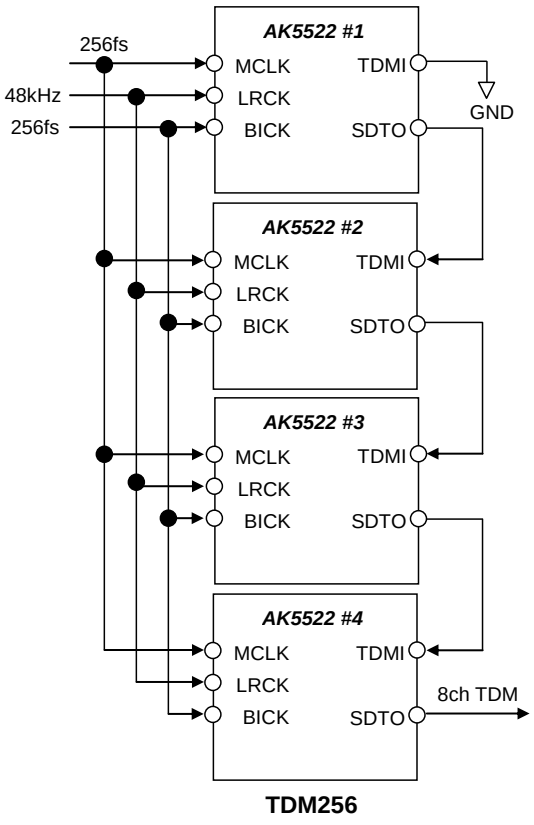


Figure 39. Cascade Connection

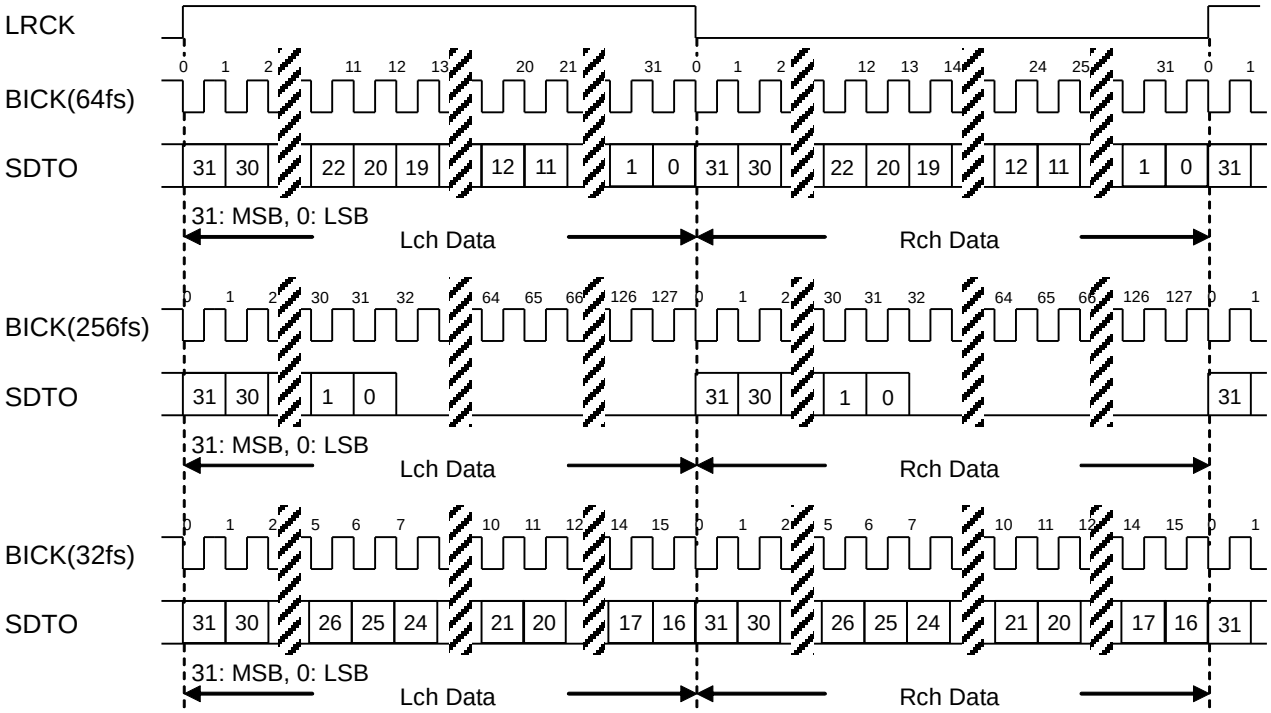


Figure 40. Stereo Output Timing (MSB Justified)

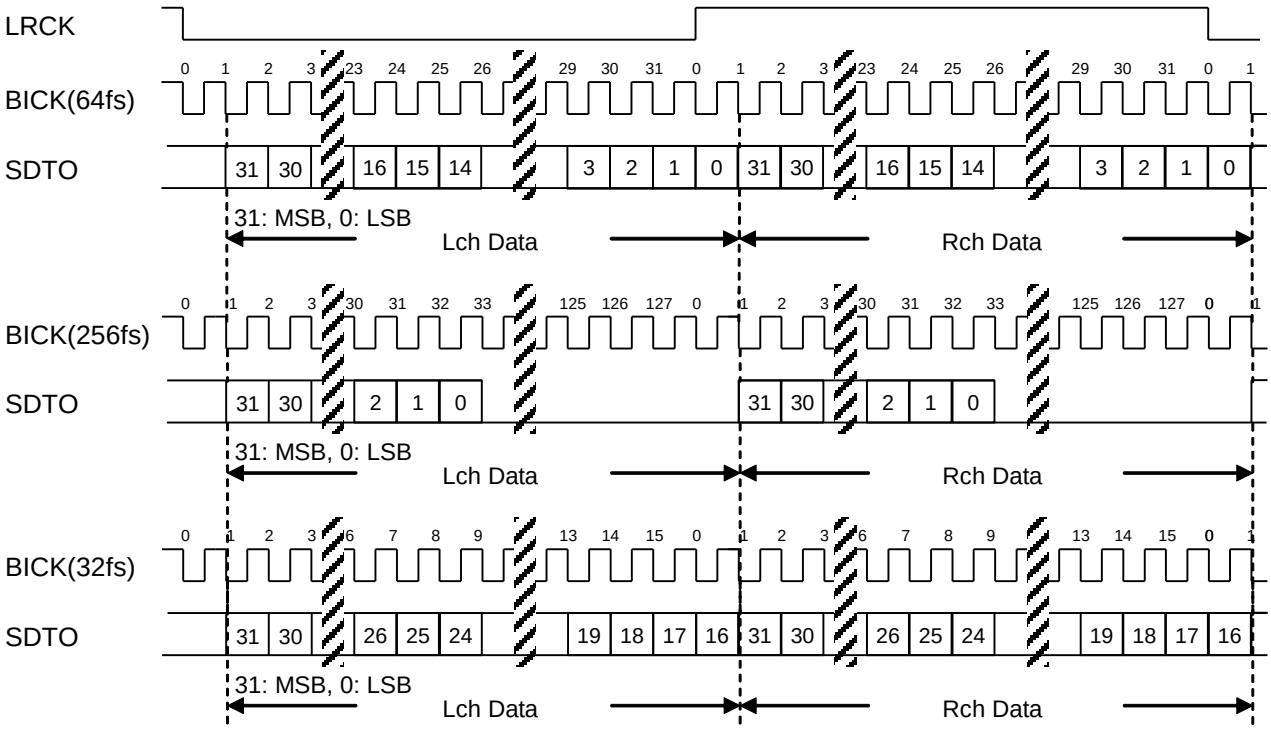


Figure 41. Stereo Output Timing (I^2S Compatible)

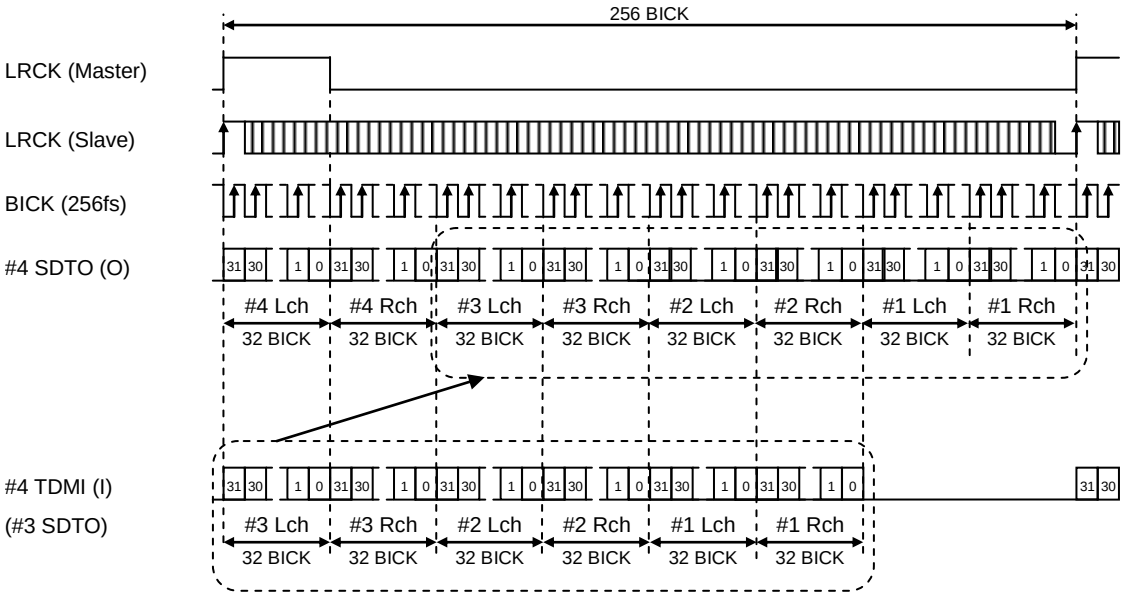


Figure 42. TDM256 Output Timing (MSB Justified)

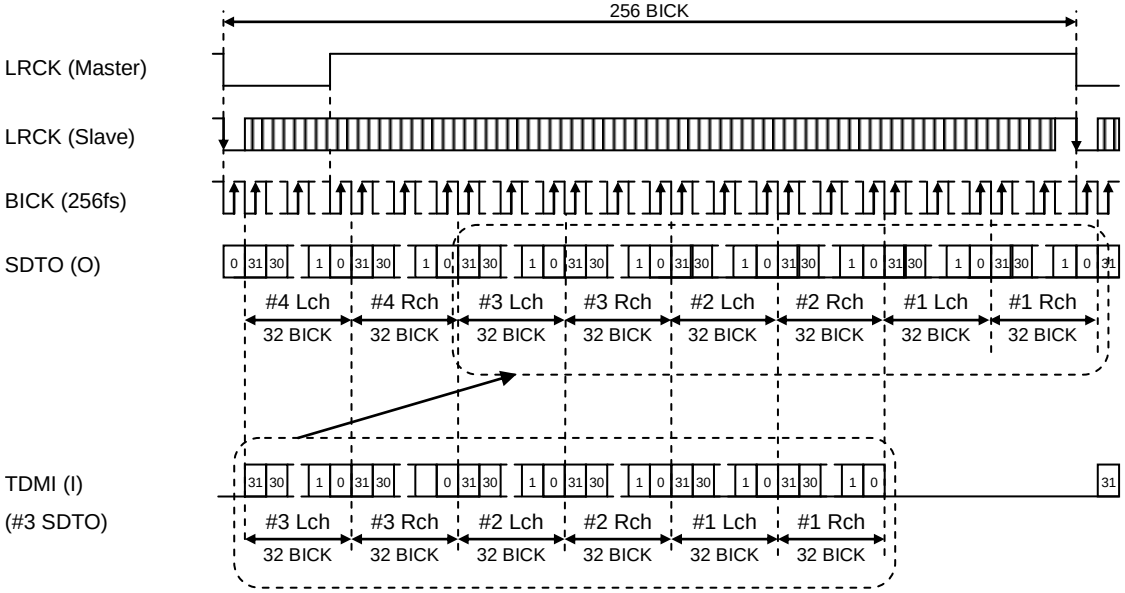


Figure 43. TDM256 Output Timing (I^2S Compatible)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MCLK "↑" to BICK "↓"	tMCB	10	-	-	ns
BICK "↓" to MCLK"↑"	tBIM	10	-	-	ns

Table 11. TDM mode Clock Timing

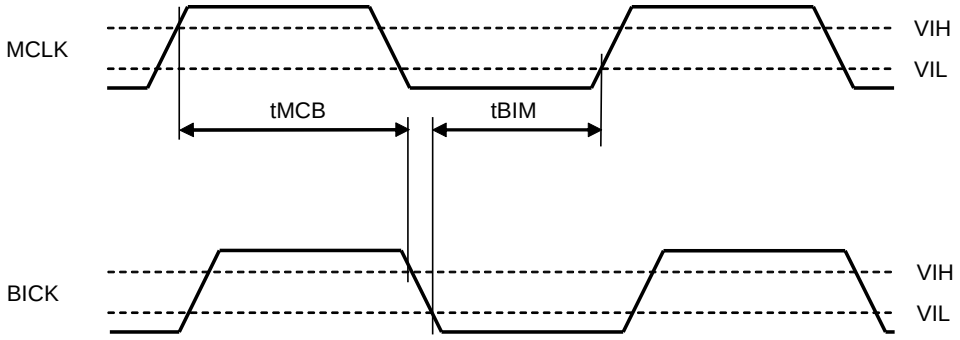


Figure 44. Audio Interface Timing (Slave Mode, TDM mode MCLK=BICK)

■ Digital HPF (Parallel Control Mode)

The AK5522 has a digital high-pass filter for DC offset cancellation. The cut-off frequency of the high-pass filter is fixed to 1.0Hz when fs=48kHz (Normal Speed mode), 96kHz (Double Speed mode) or 192kHz (Quad Speed mode). In parallel control mode, the HPF is always enabled.

■ Digital Filter Setting (Parallel Control Mode)

In parallel control mode, two types of digital filters can be selected by the SD pin.

SD pin	Filter
0	Sharp Roll-off Filter
1	Short Delay Sharp Roll-off Filter

Table 12. Digital Filter Setting (Parallel Control Mode)

■ Input Gain (Parallel Control Mode)

In parallel control mode, input gain is fixed to 0dB. The input gain is selectable only in serial control mode.

■ Power-up Function/ Sequence (Parallel Control Mode)

An initialization sequence begins when the PDN pin is changed from "H" to "L". The initialization sequence operates with the following clock according to the clock mode.

Clock Mode	Initializing Clock
EXT Mater	MCLK
EXT Slave	MCLK
PLL Slave	BICK, LRCK

Table 13. Initialization Clock (Parallel Control Mode)

When power up the AK5522, the PDN pin should be changed to "H" from "L" after AVDD, DVDD and REGDO reach 95% of their typical voltages. The clock frequency or clock mode (EXT/PLL, Master/Slave) should be changed while the PDN pin is "L".

External Master Mode (Parallel Control Mode)

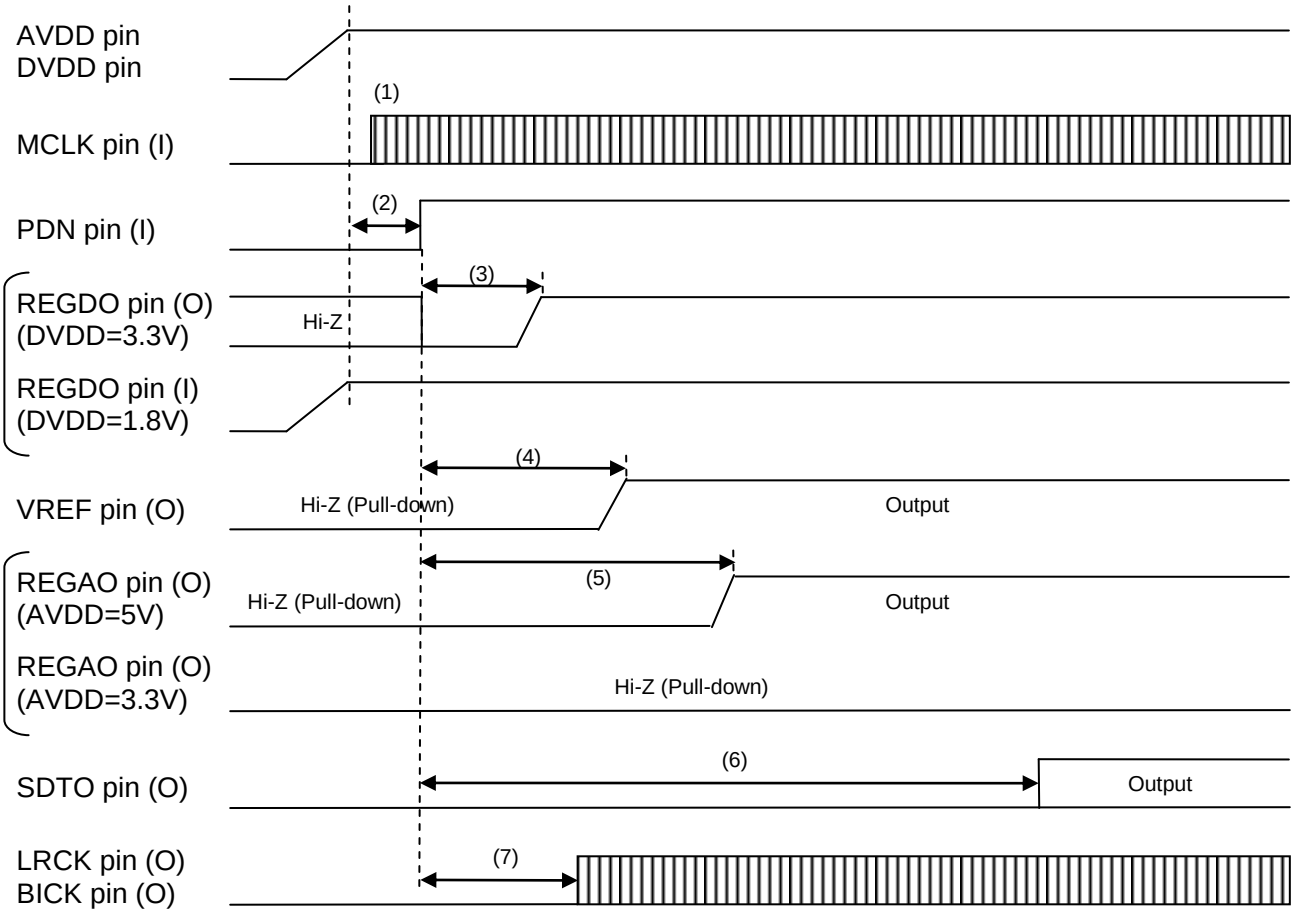


Figure 45. Power-up Sequence (Parallel Control mode, EXT Master Mode)

(1) Input MCLK after power on the power supplies.
(2) Raise the PDN pin from “L” to “H”. The PDN pin should be held to “L” for more than 150 ns after power on the power supplies.
(3) The internal regulator for digital core powers up after 17.8ms (max.) from a rising edge of the PDN pin. This timing is counted by the internal oscillator.
(4) The VREF pin outputs reference voltage after 35.7ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(5) The REGAO pin outputs 3.3V after 42.7ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(6) The SDTO pin starts outputting A/D data after 102.9ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(7) The LRCK and BICK pins start outputting clocks after 17.8ms (max.) from the rising edge of the PDN pin.

Wait time (4), (5) and (6) depend on the sampling frequency as shown in the expressions below.
(4): 27.8ms+378×n/fs (max.)
(5): 22.8ms+953×n/fs (max.)
(6): 17.8ms+4086×n/fs (max.)
Normal speed: n=1, Double speed: n=2, Quad speed: n=4

External Slave Mode (Parallel Control Mode)

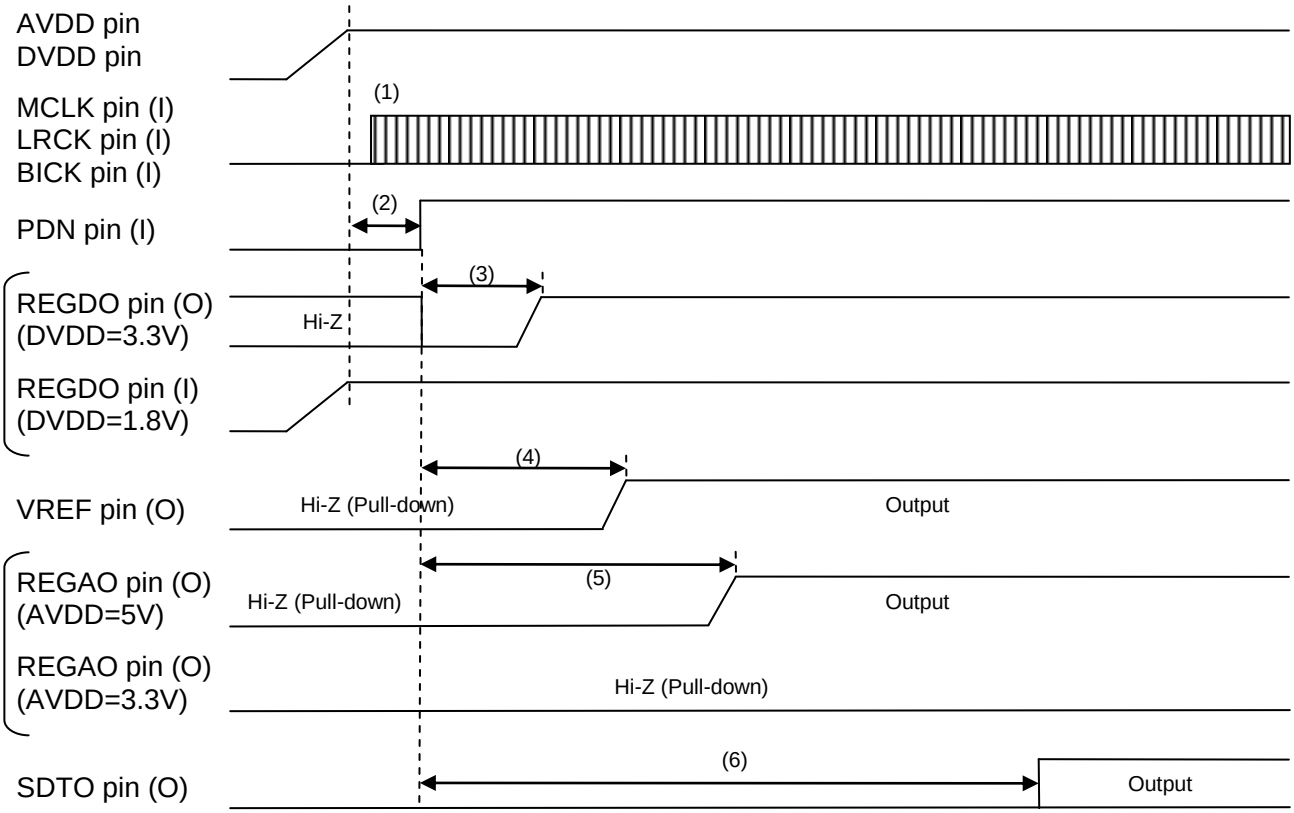


Figure 46. Power-up Sequence (Parallel Control mode, EXT Slave Mode)

(1) Input MCLK, LRCK and BICK after power on the power supplies.
(2) Raise the PDN pin from “L” to “H”. The PDN pin should be held to “L” for more than 150 ns after power on the power supplies.
(3) The Internal regulator for digital core powers up after 17.8ms (max.) from a rising edge of the PDN pin. This timing is counted by the internal oscillator.
(4) The VREF pin outputs reference voltage after 35.7ms (max.@fs=48kHz) from the rising edge of the PDN.
(5) The REGAO pin outputs 3.3V after 42.7ms (max.@fs=48kHz) from the rising edge of the PDN.
(6) The SDTO pin starts outputting A/D data after 102.9ms (max.@fs=48kHz) from the rising edge of the PDN.

Wait time (4), (5) and (6) depend on the sampling frequency as shown in the expressions below.
(4): 27.8ms+378×n/fs (max.)
(5): 22.8ms+953×n/fs (max.)
(6): 17.8ms+4086×n/fs (max.)
Normal speed: n=1, Double speed: n=2, Quad speed: n=4

PLL Slave Mode (Parallel Control Mode)

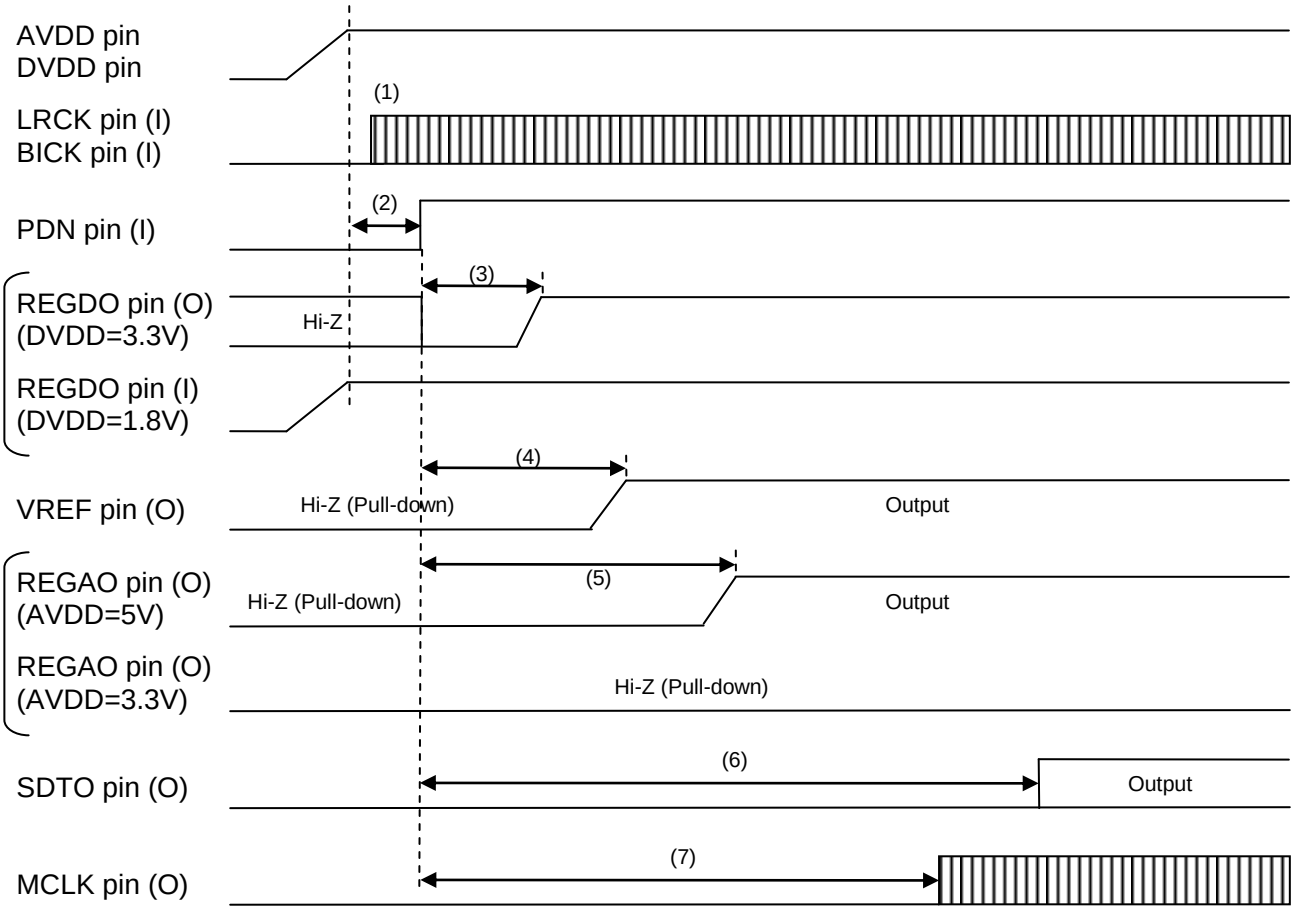


Figure 47. Power-up Sequence (Parallel Control mode, PLL Slave Mode)

(1) Input LRCK and BICK after power on the power supplies.
(2) Raise the PDN pin from “L” to “H”. The PDN pin should be held to “L” for more than 150 ns after power on the power supplies.
(3) The internal regulator for digital core powers up after 17.8ms (max.) from a rising edge of the PDN pin. This timing is counted by the internal oscillator.
(4) The VREF pin outputs reference voltage after 35.7ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(5) The REGAO pin outputs 3.3V after 42.7ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(6) The SDTO pin starts outputting A/D data after 102.9ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(7) The MCLK pin starts outputting clocks after 77.7ms (max.@fs=48kHz) from the rising edge of the PDN pin. (Reference is LRCK)

Wait time (4), (5) and (6) depend on the sampling frequency as shown in the expressions below.
(4): 27.8ms+378×n/fs (max.)
(5): 22.8ms+953×n/fs (max.)
(6): 17.8ms+4086×n/fs (max.)
(7): 57.8ms+953×n/fs (max.) (Reference = LRCK)
(7): 19.8ms+953×n/fs (max.) (Reference = BICK)
Normal speed: n=1, Double speed: n=2, Quad speed: n=4

■ Power Down Function/ Sequence

The AK5522 enters power-down mode by setting the PDN pin to “L”. Digital filters are reset at the same time.

14. Functional Descriptions (Serial Control Mode)

■ Digital Power Supply

DVDD is the power for the digital core and the digital I/O buffer. The digital core is operates off of a 1.8V power supply. This 1.8V is generated from DVDD (3.3V) by the internal voltage regulator. DVDD is also able to supply a 1.8V. In this case, the voltage regulator is disabled automatically. Connect the REGDO pin with the DVDD pin to supply a 1.8V power for the digital core.

■ Analog Power Supply

AVDD is the power for the analog block and the regulator for external DAC power supply.

■ Regulator for External DAC Power Supply

The AK5522 has a regulator for an external DAC power supply. The regulator generates 3.3V from 5V of AVDD. When AVDD is 3.3V the regulator is disabled automatically.

■ Parallel / Serial Control Mode

There are two control modes for operation mode setting.
The AK5522 is in parallel control mode by setting the PSN pin = “H”. Operation mode in parallel control mode is selected by the CKS3-0 pins. The AK5522 is in serial control mode by setting the PSN pin = “L”. Operation mode in serial control mode is selected by control registers. The control registers are set by I^2C bus. When the AK5522 is in operation, the state of PSN pin cannot be changed.

■ System Clocks (Serial Control Mode)

The AK5522 requires a master clock (MCLK), an audio serial data clock (BICK) and a channel clock (LRCK).

There are four clock modes to connect with external devices in serial control mode (Table 14). The clock mode is selected by control registers.

Clock Mode	Clock Pin Status			Connection Diagram
	MCLK	BICK	LRCK	
EXT Master	In	Out	Out	Figure 48
EXT Slave	In	In	In	Figure 49
PLL Master	In (Ref.)	Out	Out	Figure 50
PLL Slave	Out	In (Ref.)	In (Ref.)	Figure 51

Table 14. Clock Mode (Serial Control)

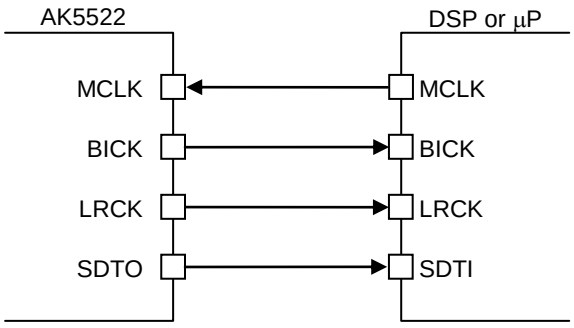


Figure 48. EXT Master Mode

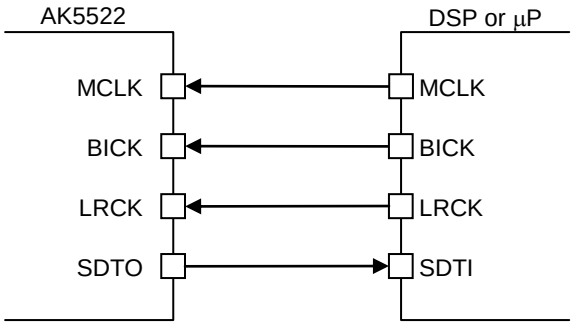


Figure 49. EXT Slave Mode

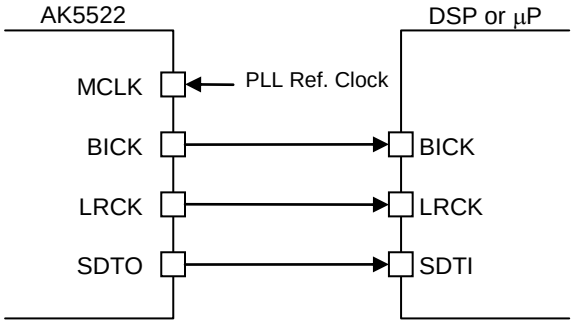


Figure 50. PLL Master Mode

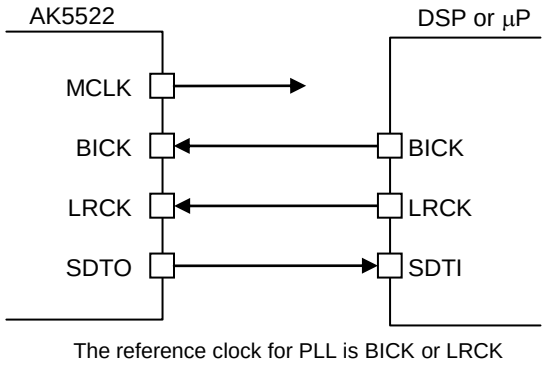


Figure 51. PLL Slave Mode

The AK5522 integrates a phase detection circuit for LRCK. If the internal timing becomes out of synchronization in slave mode, the AK5522 is reset automatically and the phase is re-synchronized. The frequency of operation clock and clock mode should be changed while the PDN pin="L" or RSTN bit="0". A stable clock must be supplied after releasing the reset. When synchronizing more than two devices, stop the system clock and reset all AK5522's once by the PDN pin. Then, input the same system clock to all AK5522's after making pin or register settings.

■ Operation Mode (Serial Control Mode)

In Serial Control Mode, operation mode is selected by PDPLLN, CM3-0 and PLL3-0 bits.

When PDPLLN bit= “0”, the clock mode is EXT Master Mode or EXT Slave Mode. In these mode, the operation mode is selected by CM3-0 bits.

EXT Master Mode (Serial Control Mode)

Mode	CM3 bit	CM2 bit	CM1 bit	CM0 bit	Stereo /TDM Table 17	MCLK Freq.	I/O	LRCK Freq. (fs) [kHz]	I/O	BICK Freq.	I/O	PLL
0	0	0	0	0	Stereo TDM256	512fs	I	8 - 54	O	Table 18	O	OFF
1	0	0	0	1	Stereo TDM256	256fs	I	54 - 108	O	Table 18	O	OFF
2	0	0	1	0	Stereo TDM256	256fs	I	8 - 54	O	Table 18	O	OFF
3	0	0	1	1	Stereo TDM128	128fs	I	108 - 216	O	Table 18	O	OFF

Table 15. EXT Master Mode Setting (Serial Control Mode)

	MCLK [MHz]		
fs [kHz]	128fs	256fs	512fs
8	N/A	2.048	4.096
16	N/A	4.096	8.192
32	N/A	8.192	16.384
48	N/A	12.288	24.576
96	N/A	24.576	N/A
192	24.576	N/A	N/A

(N/A: Not available)

Table 16. System Clock Example (EXT Master Mode)

The data output mode is selected by TDM1-0 bits.

TDM1 bit	TDM0 bit	Output Mode	
0	0	Normal (Stereo)	(default)
0	1	TDM128	
1	0	TDM256	
1	1	Not Available	

Table 17. Output Mode Setting (Serial Control Mode)

The BICK frequency is selected by BCKO1-0 bits.

BCKO1 bit	BCKO0 bit	BICK Frequency Stereo Mode	BICK Frequency TDM mode	
0	0	32fsn,32fsd,32fsq	N/A	
0	1	64fsn,64fsd,64fsq	N/A	(default)
1	0	128fsn, 128fsd	N/A	
1	1	256fsn	256fsn,256fsd,128fsq	

(N/A: Not available)

Table 18. BICK Output Frequency (Serial Control Mode)

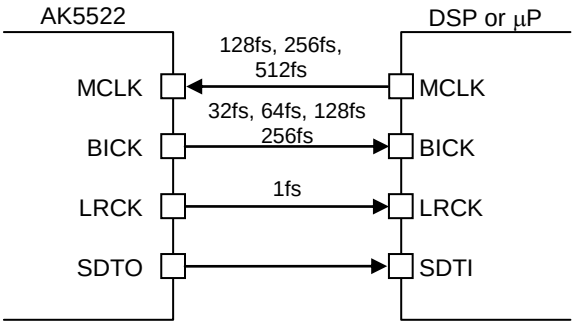


Figure 52. EXT Master Mode (Stereo Output)

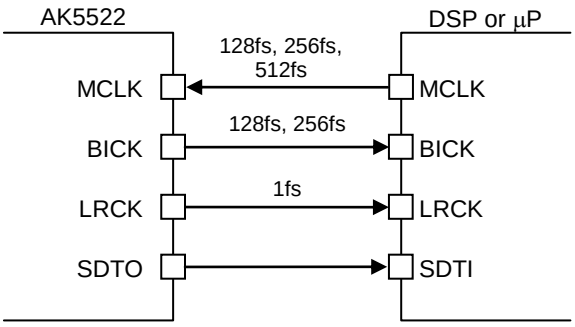


Figure 53. EXT Master Mode (TDM128, TDM256 Output)

EXT Slave Mode (Serial Control Mode)

Mode	CM3 bit	CM2 bit	CM1 bit	CM0 bit	Stereo /TDM Table 17	MCLK Freq.	I/O	LRCK Freq. (fs) [kHz]	I/O	BICK Freq. (Stereo)	BICK Freq. (TDM)	I/O	PLL
4	0	1	0	0	Stereo TDM256	1024fs	I	8 - 32	I	32fs, 64fs, 128fs, 256fs	256fs	I	OFF
						768fs	I	8 - 48	I				OFF
						512fs	I	8 - 54	I				OFF
						384fs	I	48 - 96	I	32fs, 64fs, 128fs	256fs	I	OFF
						256fs	I	54 - 108	I				OFF
					Stereo TDM128	192fs	I	96 - 192	I	32fs, 64fs	128fs	I	OFF
						128fs	I	108 - 216	I				OFF
5	0	1	0	1	Stereo TDM256	384fs	I	8 - 48	I	32fs, 64fs, 128fs, 256fs	256fs	I	OFF
						256fs	I	8 - 54	I				OFF

Table 19. EXT Slave Mode Setting (Serial Control Mode)

	MCLK [MHz]						
fs [kHz]	128fs	192fs	256fs	384fs	512fs	768fs	1024fs
8	N/A	N/A	2.048	3.072	4.096	6.144	8.192
16	N/A	N/A	4.096	6.144	8.192	12.288	16.384
32	N/A	N/A	8.192	12.288	16.384	24.576	32.768
48	N/A	N/A	12.288	18.432	24.576	36.864	N/A
96	N/A	18.432	24.576	36.864	N/A	N/A	N/A
192	24.576	36.864	N/A	N/A	N/A	N/A	N/A

(N/A: Not Available)

Table 20. System Clock Example (EXT Slave Mode)

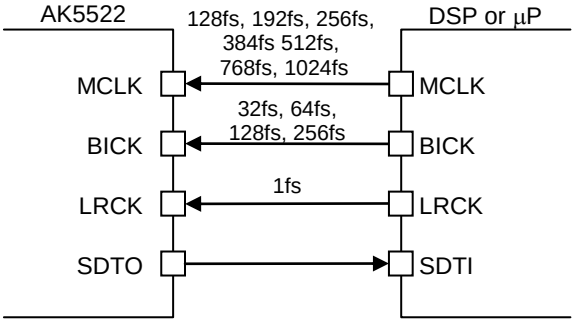


Figure 54. EXT Slave Mode

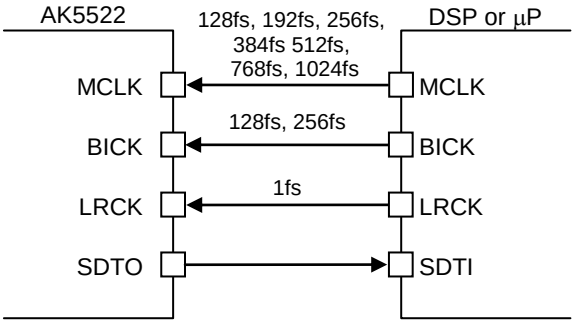


Figure 55. EXT Slave Mode (TDM128, TDM256 Output)

If PDPLLN bit="1" then the clock mode is PLL Master Mode or PLL Slave Mode. In these modes, the operation mode is selected by PLL3-0 bits.

PLL Master Mode (Serial Control Mode)

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	Stereo /TDM Table 17	Ref. Clock	MCLK Freq.	I/O	BICK Freq.	I/O	LRCK Freq. (fs)	I/O	PLL Lock Time (max.)
4	0	1	0	0	Stereo TDM256 TDM128	MCLK	11.2896MHz	I	Table 18	O	Table 22	O	10ms
5	0	1	0	1			12.288MHz	I		O		O	
6	0	1	1	0			12MHz	I		O		O	
7	0	1	1	1			16MHz	I		O		O	
8	1	0	0	0			24MHz	I		O		O	
9	1	0	0	1			19.2MHz	I		O		O	
10	1	0	1	0			13MHz	I		O		O	
11	1	0	1	1			26MHz	I		O		O	
12	1	1	0	0			13.5MHz	I		O		O	
13	1	1	0	1			27MHz	I		O		O	

Table 21. PLL Master Mode Setting (Serial Control Mode)

In PLL Master Mode, the sampling clock (LRCK) frequency is selected by FS3-0 bits. The bit clock (BICK) frequency is selected by BCKO1-0 bits.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Symbol	Sampling Frequency Mode (Note 22)	
0	0	0	0	0	fsn	8 kHz	
1	0	0	0	1		11.025 kHz	
2	0	0	1	0		12 kHz	
3	0	0	1	1		16 kHz	
4	0	1	0	0		22.05 kHz	
5	0	1	0	1		24 kHz	
6	0	1	1	0		32 kHz	
7	0	1	1	1		44.1 kHz	
8	1	0	0	0		48 kHz	(default)
9	1	0	0	1	fsd	64 kHz	
10	1	0	1	0		88.2 kHz	
11	1	0	1	1		96 kHz	
12	1	1	0	0	fsq	128 kHz	
13	1	1	0	1		176.4 kHz	
14	1	1	1	0		192 kHz	
15	1	1	1	1		192 kHz	

Table 22. Setting of Sampling Frequency at PDPLLN bit = "1" (N/A: Not Available)

Note 22. In PLL master mode, the sampling frequency generated by PLL differs slightly from the sampling frequency of mode name in some combinations of MCLK frequency (PLL3-0 bits) and sampling frequency (FS3-0 bits). (Table 23, Table 24)

Unit [kHz]

Sampling Freq. Mode Name	MCLK Frequency				
	11.2896MHz	12.288MHz	12MHz	16MHz	24MHz
8 kHz mode	8.000000	8.000000	8.000000	8.000000	8.000000
11.025 kHz mode	11.025000	11.025000	**11.024877**	**11.025117**	**11.024877**
12 kHz mode	12.000000	12.000000	12.000000	12.000000	12.000000
16 kHz mode	16.000000	16.000000	16.000000	16.000000	16.000000
22.05 kHz mode	22.050000	22.050000	**22.049753**	**22.050234**	**22.049753**
24 kHz mode	24.000000	24.000000	24.000000	24.000000	24.000000
32 kHz mode	32.000000	32.000000	32.000000	32.000000	32.000000
44.1 kHz mode	44.100000	44.100000	**44.099507**	**44.100467**	**44.099507**
48 kHz mode	48.000000	48.000000	48.000000	48.000000	48.000000
64 kHz mode	64.000000	64.000000	64.000000	64.000000	64.000000
88.2 kHz mode	88.200000	88.200000	**88.199013**	**88.200935**	**88.199013**
96 kHz mode	96.000000	96.000000	96.000000	96.000000	96.000000
128 kHz mode	128.000000	128.000000	128.000000	128.000000	128.000000
176.4 kHz mode	176.400000	176.400000	**176.398026**	**176.401869**	**176.398026**
192 kHz mode	192.000000	192.000000	192.000000	192.000000	192.000000

Table 23. Actual Sampling Frequency (1)

Unit [kHz]

Sampling Freq. Mode Name	MCLK Frequency				
	19.2MHz	13MHz	26MHz	13.5MHz	27MHz
8 kHz mode	8.000000	**7.999786**	**7.999786**	**8.000300**	**8.000300**
11.025 kHz mode	11.025000	**11.024877**	**11.024877**	**11.025218**	**11.025218**
12 kHz mode	12.000000	**11.999679**	**11.999679**	**12.000451**	**12.000451**
16 kHz mode	16.000000	**15.999572**	**15.999572**	**16.000601**	**16.000601**
22.05 kHz mode	22.050000	**22.049753**	**22.049753**	**22.050436**	**22.050436**
24 kHz mode	24.000000	**23.999358**	**23.999358**	**24.000901**	**24.000901**
32 kHz mode	32.000000	**31.999144**	**31.999144**	**32.001202**	**32.001202**
44.1 kHz mode	44.100000	**44.099507**	**44.099507**	**44.100871**	**44.100871**
48 kHz mode	48.000000	**47.998716**	**47.998716**	**48.001803**	**48.001803**
64 kHz mode	64.000000	**63.998288**	**63.998288**	**64.002404**	**64.002404**
88.2 kHz mode	88.200000	**88.199013**	**88.199013**	**88.201742**	**88.201742**
96 kHz mode	96.000000	**95.997432**	**95.997432**	**96.003606**	**96.003606**
128 kHz mode	128.000000	**127.996575**	**127.996575**	**128.004808**	**128.004808**
176.4 kHz mode	176.400000	**176.398026**	**176.398026**	**176.403485**	**176.403485**
192 kHz mode	192.000000	**191.994863**	**191.994863**	**192.007212**	**192.007212**

Table 24. Actual Sampling Frequency (2)

Note 23. Point 7 digits or less is rounded.

INVMCLK bit selects MCLK edge for PLL.

INVMCLK bit	Reference Edge	
0	Falling Edge	(default)
1	Rising Edge	

Table 25. MCLK Edge for PLL

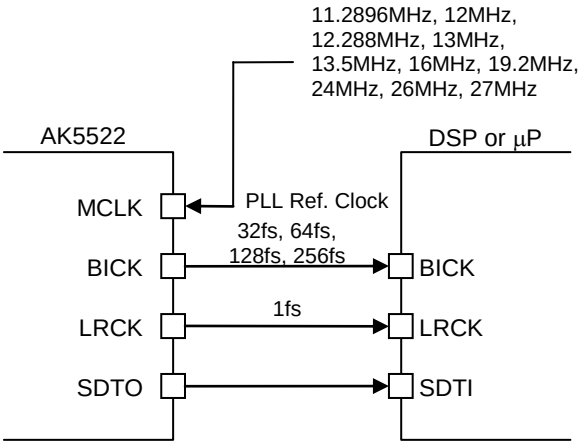


Figure 56. PLL Master Mode (Stereo Output)

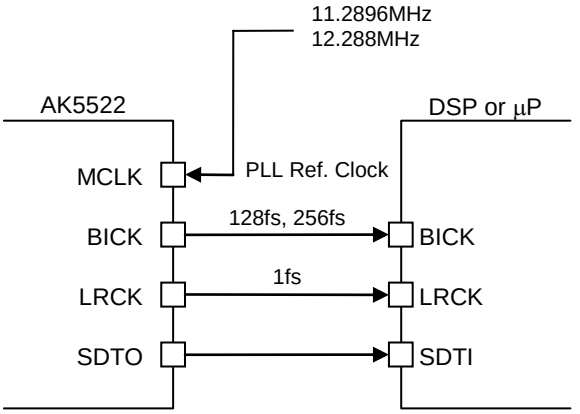


Figure 57. PLL Master Mode (TDM128, TDM256 Output)

PLL Slave Mode (Serial Control Mode)

Mode	PLL3 bit	PLL2 bit	PLL1 bit	PLL0 bit	Stereo /TDM	Ref. Clock	MCLK Freq.	I/O	BICK Freq. (Stereo)	BICK Freq. (TDM)	I/O	LRCK (fs) Freq. Table 22	I/O	PLL Lock Time (max.)
0	0	0	0	0	Stereo	BICK	512fs	O	64fs	N/A	I	Mode 0 - 8	I	2ms
1	0	0	0	1	Stereo	BICK	256fs	O	64fs	N/A	I	Mode 0 - 11	I	2ms
2	0	0	1	0	Stereo	BICK	128fs	O	64fs	N/A	I	Mode 12 - 14	I	2ms
3	0	0	1	1	Stereo TDM256	LRCK	512fs	O	32fs, 64fs, 128fs, 256fs	256fs	I	Mode 0 - 8	I	40ms
14	1	1	1	0	Stereo TDM256	LRCK	256fs	O	32fs, 64fs, 128fs	256fs	I	Mode 0 - 11	I	40ms
15	1	1	1	1	Stereo TDM128	LRCK	128fs	O	32fs, 64fs	128fs	I	Mode 12 - 14	I	40ms

(N/A: Not Available)

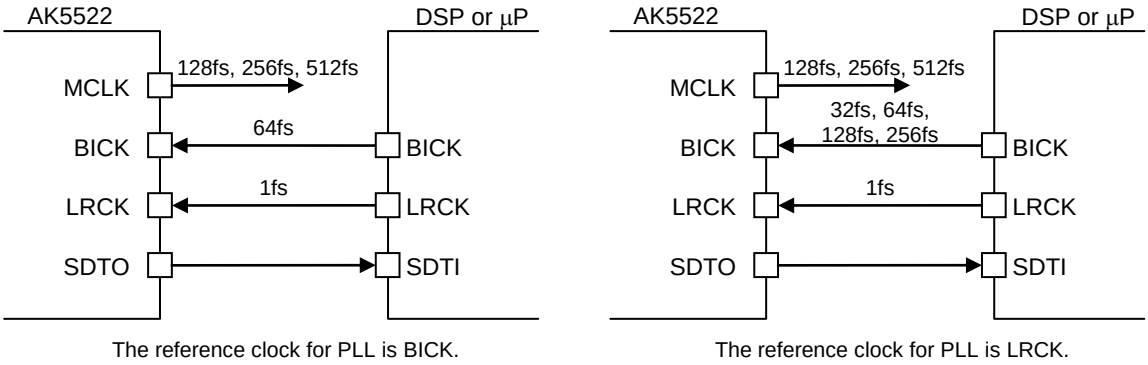
Table 26. PLL Slave Mode Setting (Serial Control Mode)

In PLL slave mode, FS3-0 bits have to be set according to the sampling clock (LRCK) frequency. (Table 22)

	MCLK [MHz]		
fs [kHz]	128fs	256fs	512fs
8	N/A	2.048	4.096
16	N/A	4.096	8.192
32	N/A	8.192	16.384
48	N/A	12.288	24.576
96	N/A	24.576	N/A
192	24.576	N/A	N/A

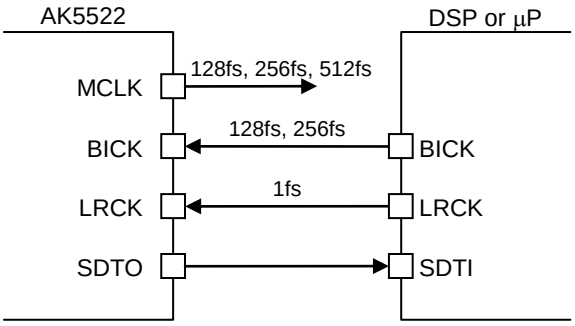
(N/A: Not Available)

Table 27. System Clock Example (PLL Slave Mode)



The reference clock for PLL is BICK. The reference clock for PLL is LRCK.

Figure 58. PLL Slave Mode



The reference clock for PLL is LRCK.

Figure 59. PLL Slave Mode (TDM128, TDM256 Output)

■ Audio Interface Format (Serial Control Mode)

The audio interface format is selected with the DIF bit.

DIF bit	Data Format	
0	32bit MSB Justified	(default)
1	32bit I^2S Compatible	

Table 28. Audio Interface Format

■ Cascade Connection in TDM Mode (Serial Control Mode)

The AK5522 supports cascade connection of four devices in TDM256 and TDM128 modes. Figure 60 shows a connection example. All A/D converted data of connected AK5522's are output from the SDTO pin of the last AK5522 by cascade connection.

TDM1 bit	TDM0 bit	Output Mode	
0	0	Normal (Stereo)	(default)
0	1	TDM128	
1	0	TDM256	
1	1	Not Available	

Table 29. Output Mode Setting (Serial Control Mode)

When using multiple devices in slave mode on cascade connection, internal operation timing of each device may differ for one MCLK cycle depending on MCLK and BICK input timings. To prevent this timing difference, BICK "↓" should be more than ± 10ns from MCLK "↑" as shown in Table 30.

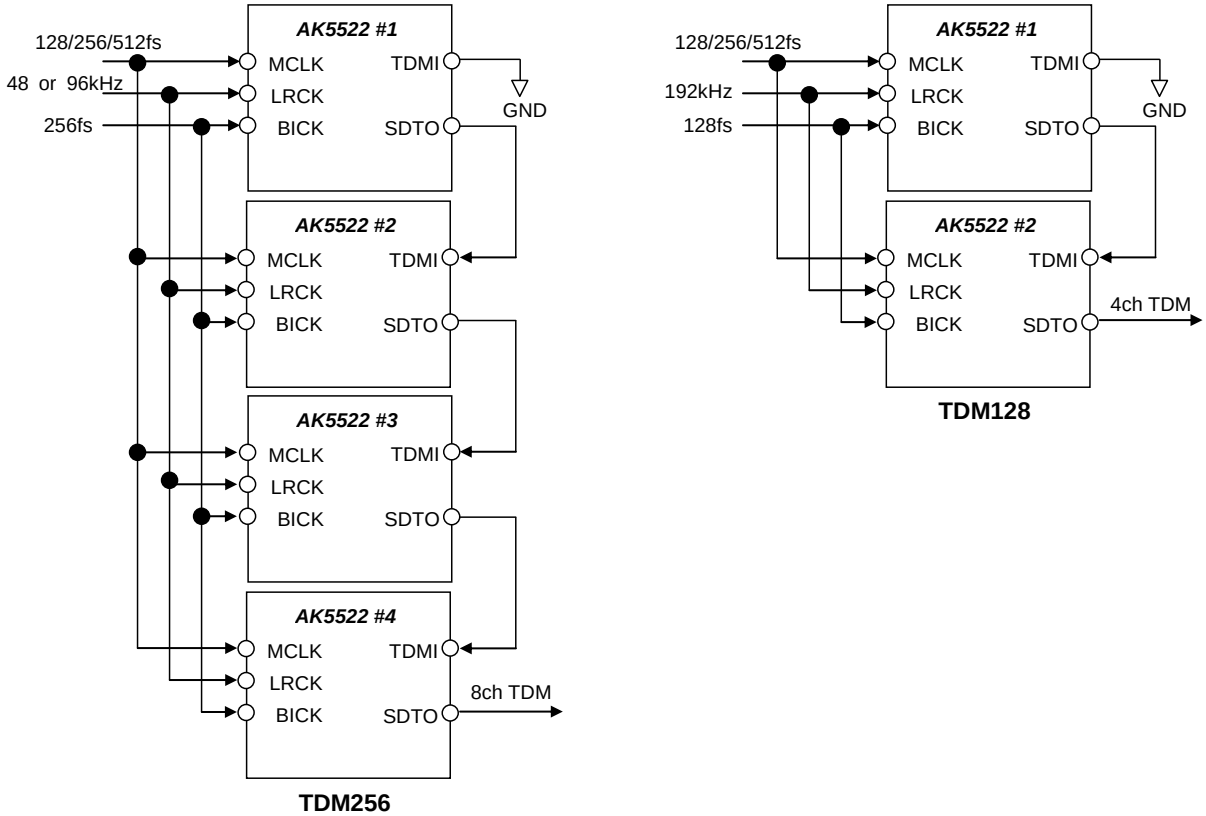


Figure 60. Cascade Connection

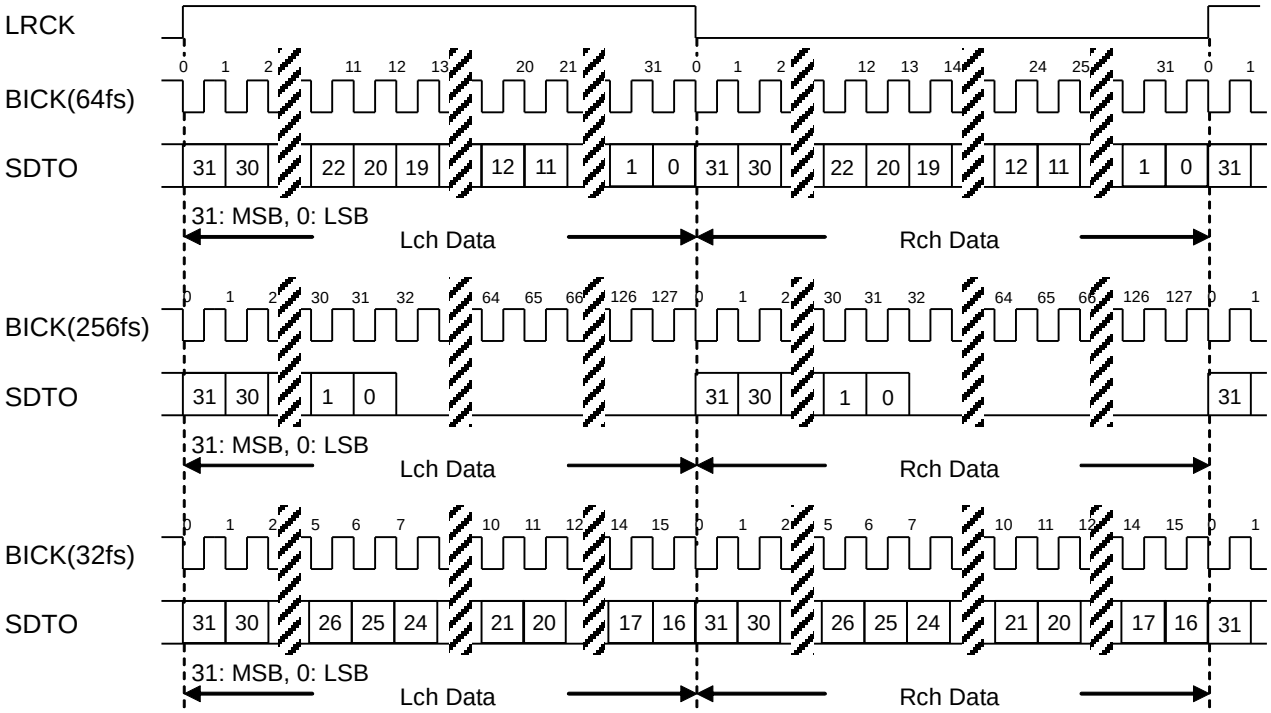


Figure 61. Stereo Output Timing (MSB Justified)

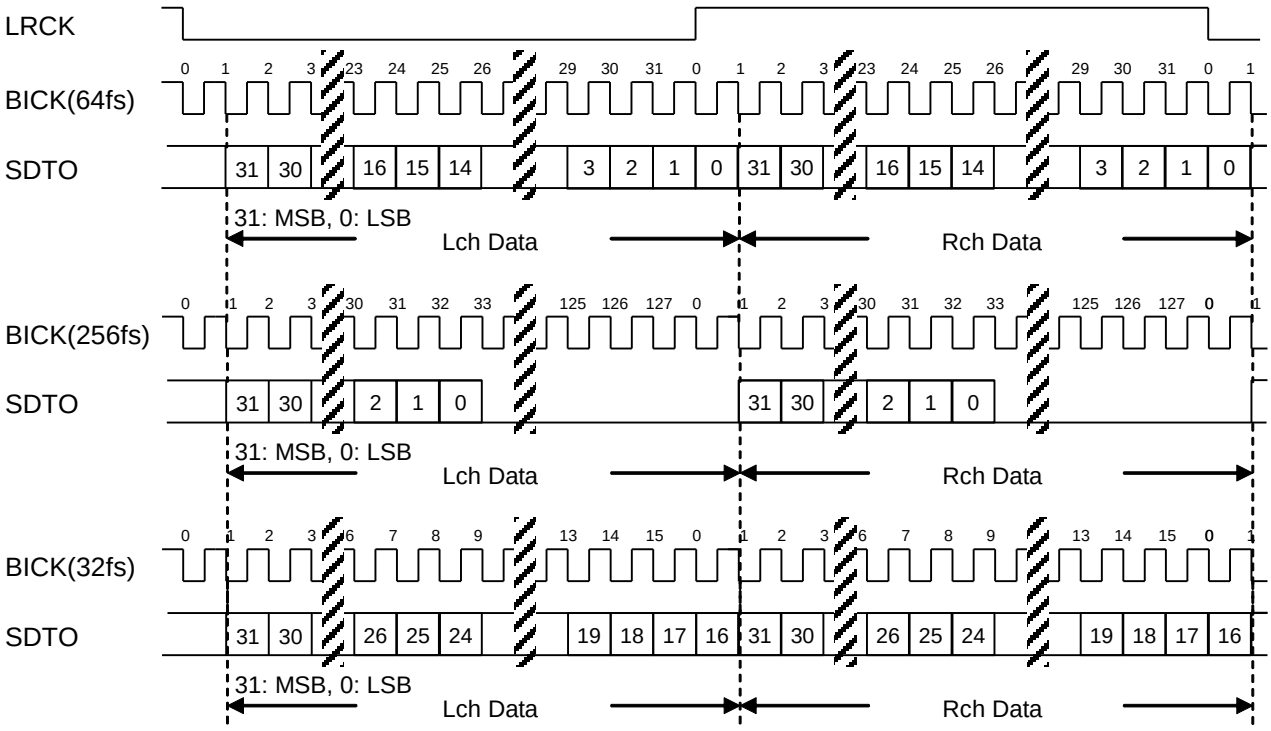


Figure 62. Stereo Output Timing (I^2S Compatible)

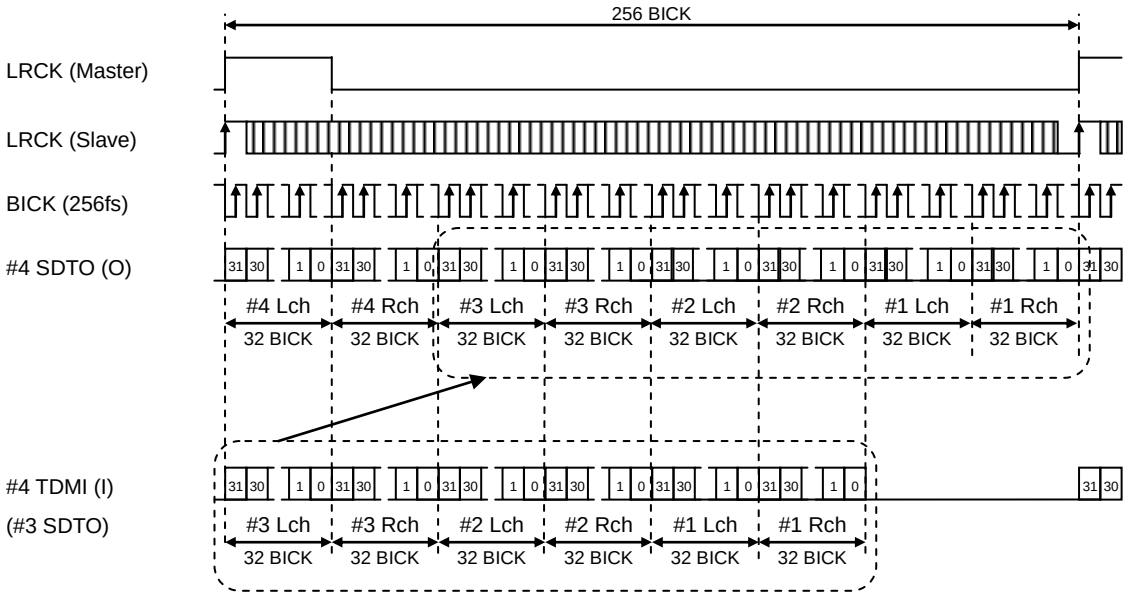


Figure 63. TDM256 Output Timing (MSB Justified)

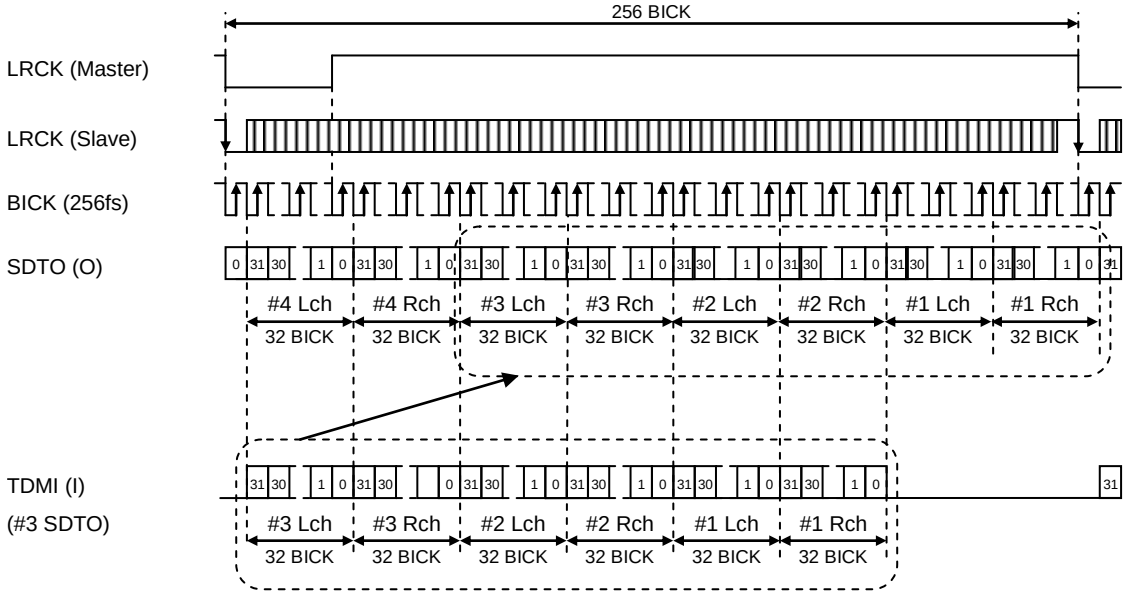


Figure 64. TDM256 Output Timing (I^2S Compatible)

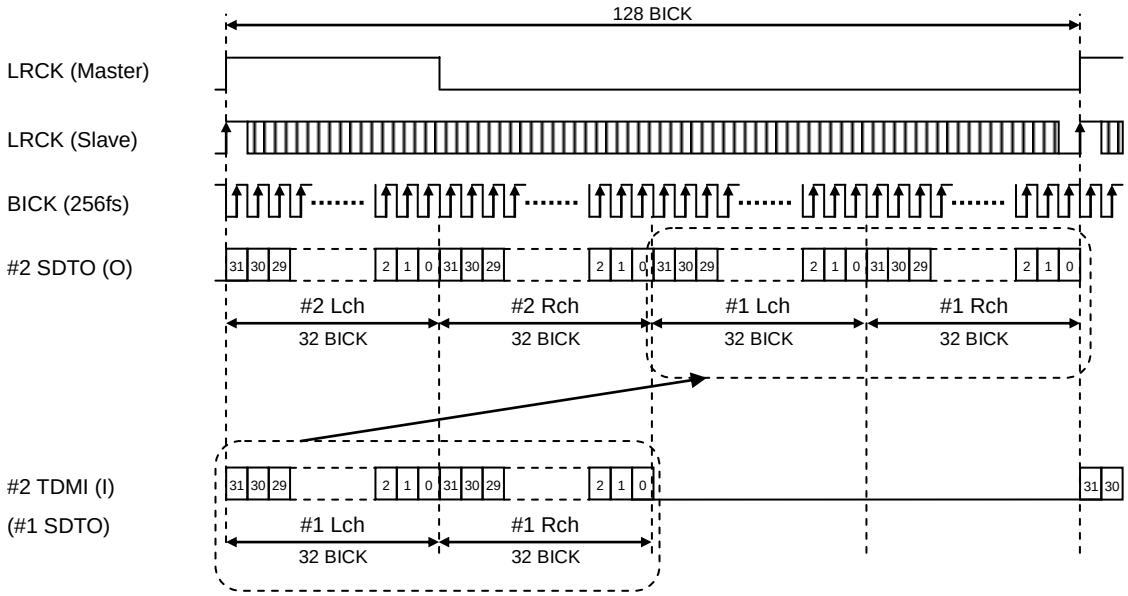


Figure 65. TDM128 Output Timing (MSB Justified)

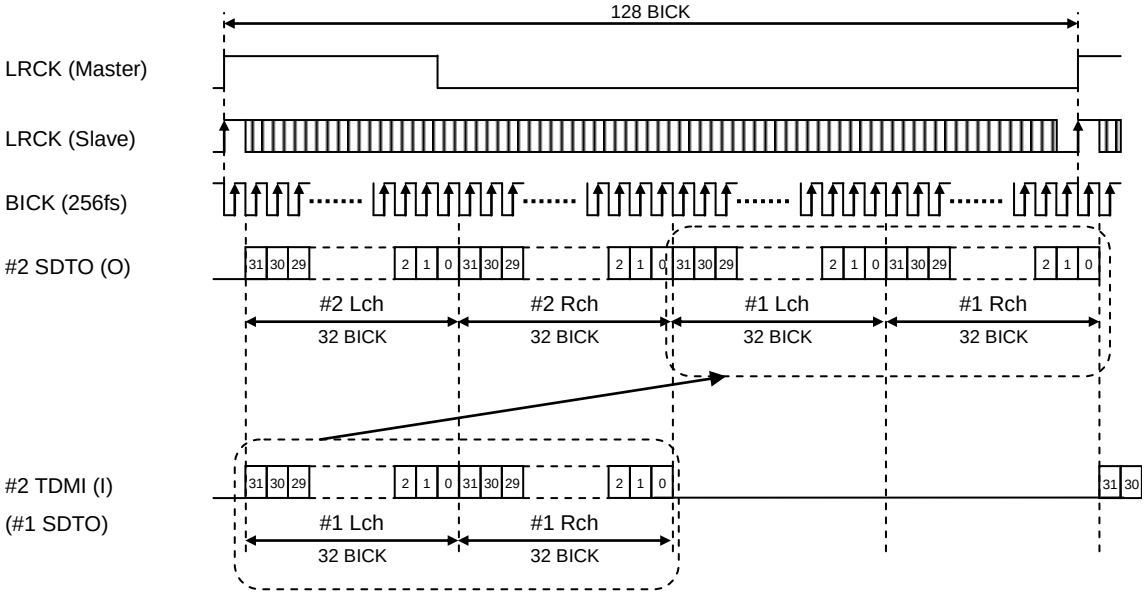


Figure 66. TDM128 Output Timing (I^2S Compatible)

Parameter	Symbol	Min.	Typ.	Max	Unit
MCLK "↑" to BICK "↓"	tMCB	10	-	-	ns
BICK "↓" to MCLK"↑"	tBIM	10	-	-	ns

Table 30. TDM mode Clock Timing

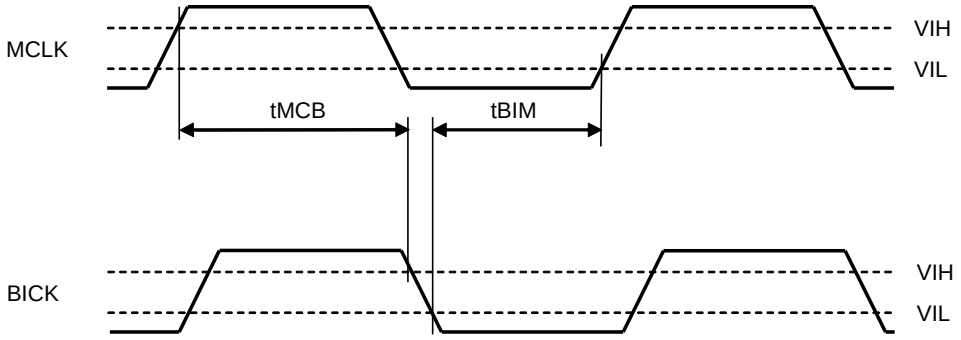


Figure 67. Audio Interface Timing (Slave Mode, TDM mode MCLK=BICK)

■ Digital HPF (Serial Control Mode)

The AK5522 has a digital high-pass filter for DC offset cancellation. The cut-off frequency of the high-pass filter is fixed to 1.0Hz when fs=48kHz (Normal Speed mode), 96kHz (Double Speed mode) or 192kHz (Quad Speed mode). In serial control mode, the HPF is enabled if HPFE bit= "1".

■ Digital Filter Setting (Serial Control Mode)

The AK5522 has four types of digital filters and they can be selected by SD and SLOW bits.

SD bit	SLOW bit	Filter
0	0	Sharp Roll-off Filter
0	1	Slow Roll-off Filter
1	0	Short Delay Sharp Roll-off Filter
1	1	Short Delay Slow Roll-off Filter

Table 31. Digital Filter Setting (Serial Control Mode)

■ **Input Gain (Serial Control Mode)**

It is able to select input gain in serial control mode. The input gain is set by GR3-0 bits and GL3-0 bits.

GR3 bit GL3 bit	GR2 bit GL2 bit	GR1 bit GL1 bit	GR0 bit GL0 bit	Input Gain	
0	0	0	0	+12dB	
0	0	0	1	+11dB	
0	0	1	0	+10dB	
0	0	1	1	+9dB	
0	1	0	0	+8dB	
0	1	0	1	+7dB	
0	1	1	0	+6dB	
0	1	1	1	+5dB	
1	0	0	0	+4dB	
1	0	0	1	+3dB	
1	0	1	0	+2dB	
1	0	1	1	+1dB	
1	1	0	0	0dB	(default)
1	1	0	1	-1dB	
1	1	1	0	-2dB	
1	1	1	1	-3dB	

Table 32. Input Gain Setting

■ **Device Reset (Serial Control Mode)**

When RSTN bit is set to “0”, analog blocks become power down state. At the same time, digital filters and timing circuits are reset. In this case, control registers are not reset.

■ **Block Power Control (Serial Control Mode)**

Power management bits are available for each block. (regulator for DAC, PLL, right-channel of ADC and left-channel of ADC). It is able to power down unused block to save power consumption.

■ **Power up Function/ Sequence (Serial Control Mode)**

An initialization sequence begins when the PDN pin status is changed from “H” to “L”. The initialization sequence operates with the following clock according to the clock mode.

Clock Mode	Initializing Clock
EXT Mater	MCLK
EXT Slave	MCLK
PLL Master	MCLK
PLL Slave	BICK, LRCK

Table 33. Initialization Clock (Serial Control Mode)

When power up the AK5522, the PDN pin should be changed to “H” from “L” after AVDD, DVDD and REGDO reach 95% of their typical voltages. The clock frequency or clock mode (EXT/PLL, Master/Slave) should be changed while the PDN pin is “L”.

External Master Mode (Serial Control Mode)

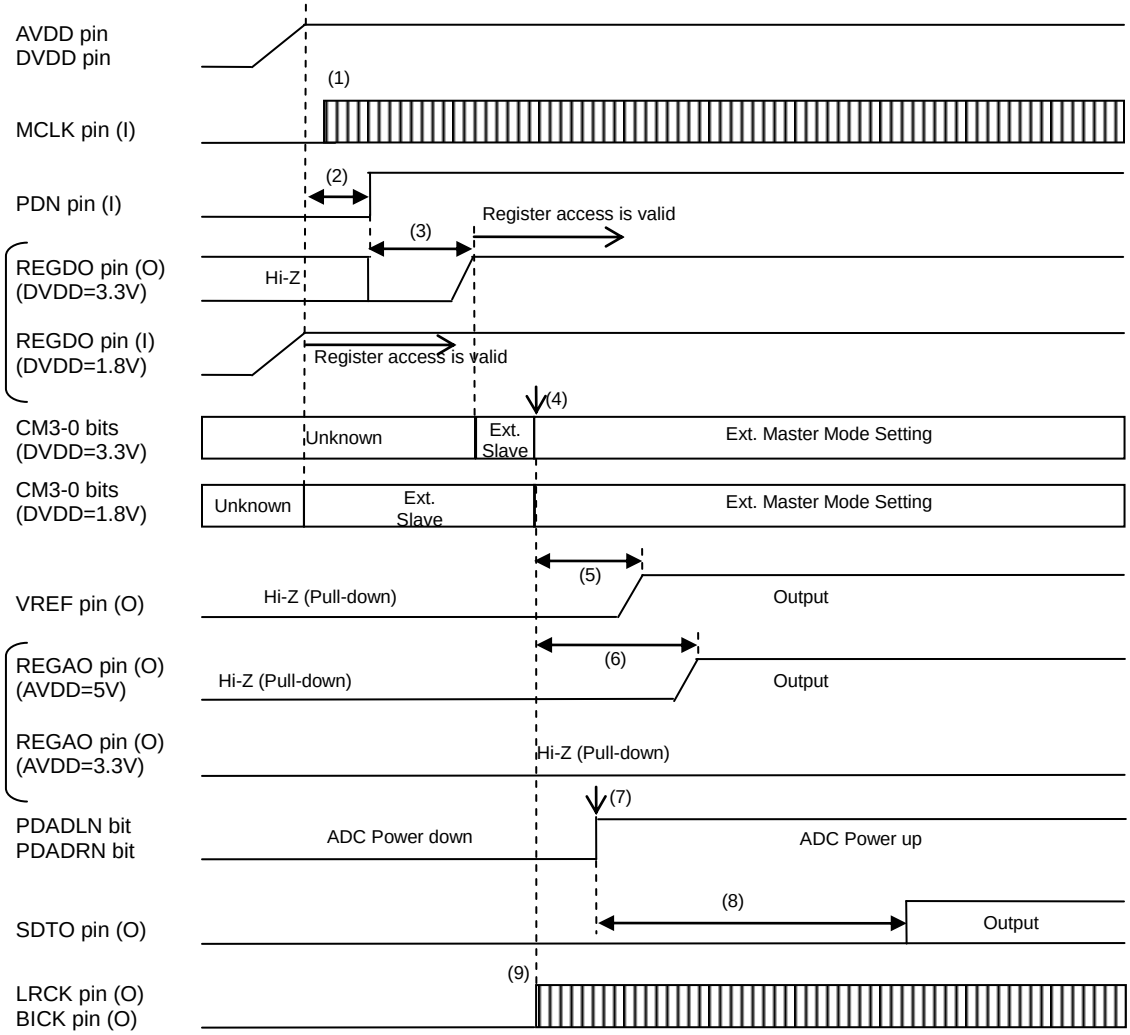


Figure 68. Power-up Sequence (Serial Control Mode, EXT Master Mode)

(1) Input MCLK after power on the power supplies.
(2) Raise the PDN pin from “L” to “H”. The PDN pin should be held to “L” for more than 150 ns after power on the power supplies.
(3) The internal regulator for digital core powers up after 17.8ms (max.) from a rising edge of the PDN pin. This timing is counted by the internal oscillator.
(4) Set the CM3-0 bits to External Master mode.
(5) The VREF pin outputs reference voltage after 17.9ms (max.@fs=48kHz) from the setting CM3-0 bits.
(6) The REGAO pin outputs 3.3V after 24.9ms (max.@fs=48kHz) from the setting CM3-0 bits.
(7) Set “1” into PDALN/PDARN bits after setting other registers.
(8) The SDTO pin starts outputting A/D data after 64.6ms (max.@fs=48kHz) from PDADLN/PDADRN bit = “1”.
(9) The LRCK and BICK pins start outputting clocks after the setting CM3-0 bits.

Wait time (5), (6) and (8) depend on the sampling frequency as shown in the expressions below.
(5): 10ms+378×n/fs (max.)
(6): 5ms+953×n/fs (max.)
(8): 3100×n/fs (max.)
Normal speed: n=1, Double speed: n=2, Quad speed: n=4

External Slave Mode (Serial Control Mode)

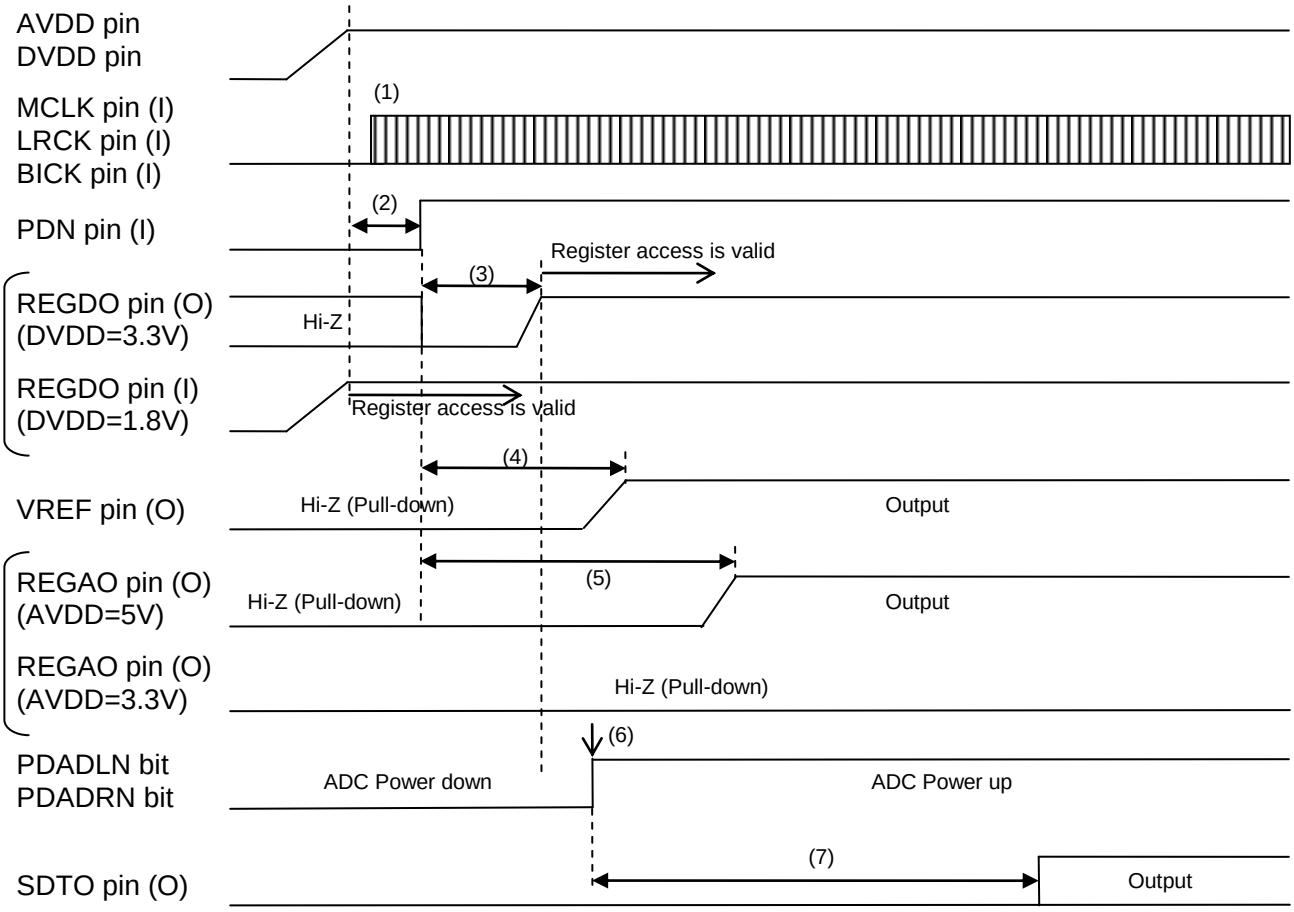


Figure 69. Power-up Sequence (Serial Control mode, EXT Slave Mode)

(1) Input MCLK, LRCK and BICK after power on the power supplies.
(2) Raise the PDN pin from “L” to “H”. The PDN pin should be held to “L” for more than 150 ns after power on the power supplies.
(3) The Internal regulator for digital core powers up after 17.8ms (max.) from a rising edge of the PDN pin. This timing is counted by the internal oscillator. Register accesses will be valid after REGDO voltage is raised up.
(4) The VREF pin outputs reference voltage after 35.7ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(5) The REGAO pin outputs 3.3V after 42.7ms (max.@fs=48kHz) from the rising edge of the PDN pin.
(6) Set “1” into PDALN/PDARN bits after setting other registers.
(7) The SDTO pin starts outputting A/D data after 64.6ms (max.@fs=48kHz) from PDALN/PDARN bit = “1”.

Wait time (4), (5) and (6) depend on the sampling frequency as shown in the expressions below.
(4): 27.8ms+378×n/fs (max.)
(5): 22.8ms+953×n/fs (max.)
(7): 3100×n/fs (max.)
Normal speed: n=1, Double speed: n=2, Quad speed: n=4

PLL Master Mode (Serial Control Mode)

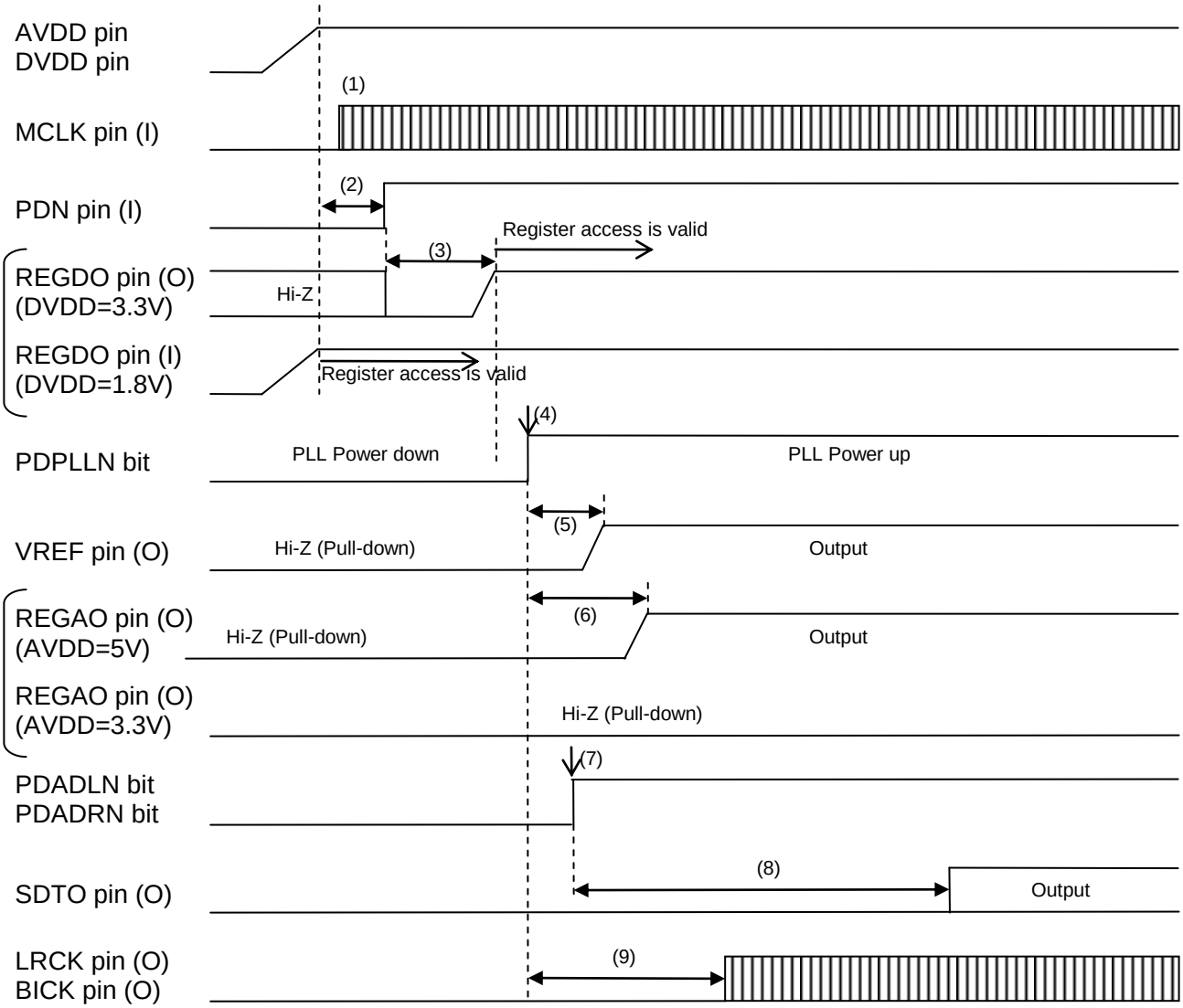


Figure 70. Power up Sequence (Serial Control mode, PLL Master Mode)

(1) Input MCLK after power on the power supplies.
(2) Raise the PDN pin from “L” to “H”. The PDN pin should be held to “L” for more than 150 ns after power on the power supplies.
(3) The Internal regulator for digital core powers up after 17.8ms (max.) from a rising edge of the PDN pin. This timing is counted by the internal oscillator. Register accesses will be valid after REGDO voltage is raised up.
(4) Set “1” into PDPLLN bit after settling the REGDO pin and setting PLL master mode.
(5) The VREF pin outputs reference voltage after 17ms (max.) from PDPLLN bit = “1”.
(6) The REGAO pin outputs 3.3V after 22.6ms (max.) from PDPLLN bit = “1”.
(7) Set “1” into PDALN/PDARN bit after setting other registers.
(8) The SDTO pin starts outputting A/D data after 64.6ms (max.@fs=48kHz) from PDADLN/PDADRN bit = “1”.
(9) The LRCK and BICK pins start outputting clocks after 27.6ms (max.) from PDPLLN bit = “1”.

Wait time (8) depend on the sampling frequency as shown in the expressions below.
(8): 3100×n/fs (max.)
Normal speed: n=1, Double speed: n=2, Quad speed: n=4

PLL Slave Mode (Serial Control Mode)

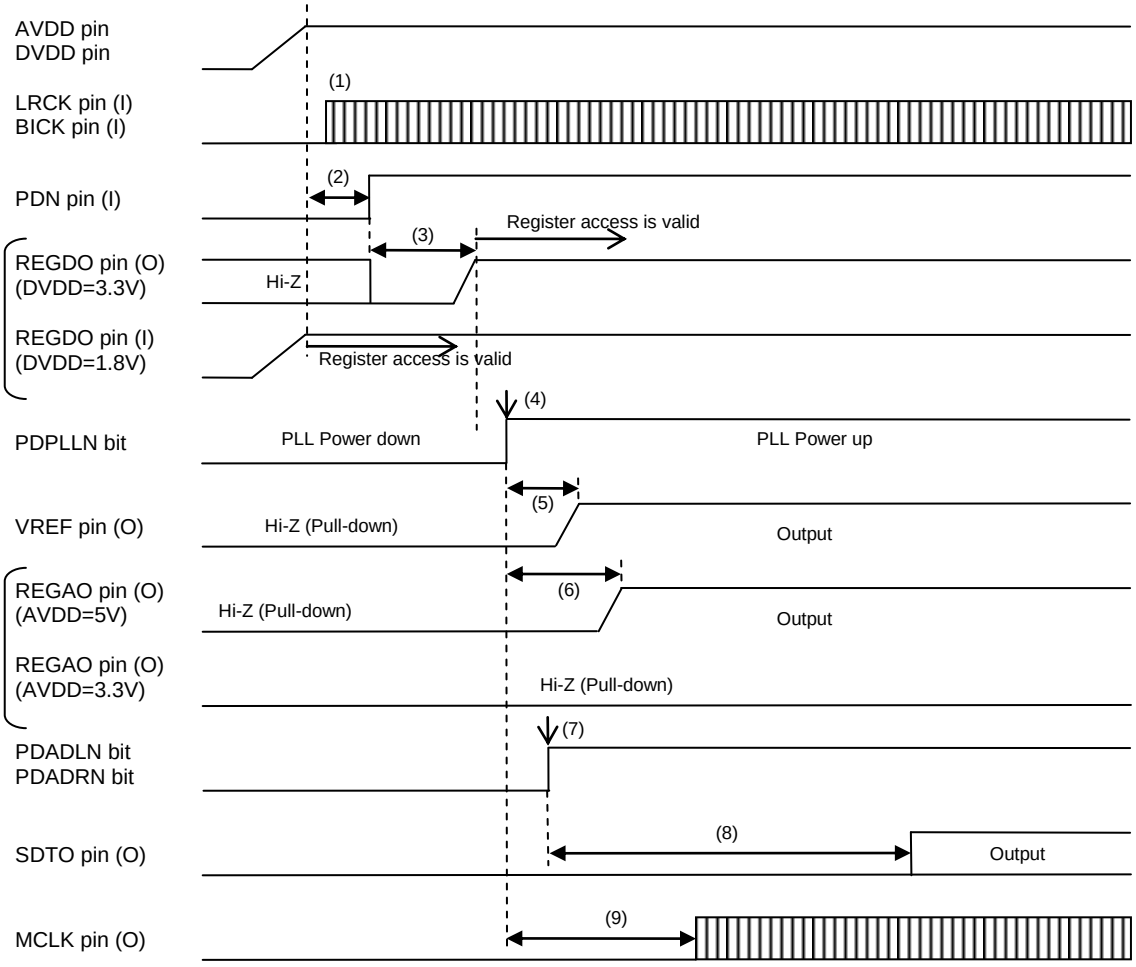


Figure 71. Power up Sequence (Serial Control mode, PLL Slave Mode)

(1) Input LRCK and BICK after power on the power supplies.
(2) Raise the PDN pin from “L” to “H”. The PDN pin should be held to “L” for more than 150 ns after power on the power supplies.
(3) The Internal regulator for digital core powers up after 17.8ms (max.) from a rising edge of the PDN pin. This timing is counted by the internal oscillator. Register accesses will be valid after REGDO voltage is raised up.
(4) Set “1” into PDPLLN bit after settling the REGDO pin and setting PLL slave mode.
(5) The VREF pin outputs reference voltage after 17.9ms (max.@fs=48kHz) from PDPLLN bit = “1”.
(6) The REGAO pin outputs 3.3V after 24.9ms (max.@fs=48kHz) from PDPLLN bit = “1”.
(7) Set “1” into PDALN/PDARN bit after setting other registers.
(8) The SDTO pin starts outputting A/D data after 64.6ms (max.@fs=48kHz) from PDADLN/PDADRN bit = “1”.
(9) The MCLK pin starts outputting clock after 59.9ms (max.@fs=48kHz, Ref=LRCK) from PDPLLN bit = “1”.

Wait time (5), (6), (8) and (9) depend on the sampling frequency as shown in the expressions below.
(5): 10ms+378×n/fs (max.)
(6): 5ms+953×n/fs (max.)
(8): 3100×n/fs (max.)
(9): 40ms+953×n/fs (max.) (Reference = LRCK)
(9): 2ms+953×n/fs (max.) (Reference = BICK)
Normal speed: n=1, Double speed: n=2, Quad speed: n=4

■ Power Down Function/ Sequence

The AK5522 enters power-down mode by setting the PDN pin to “L”. Digital filters are reset at the same time. The PDN pin has to be “L” when changing the input clock frequency.

In slave mode, system reset is released by inputting BICK and LRCK after setting the PDN pin to “H”. The AK5522 detects a rising edge of MCLK first, and then exits power-down mode by a rising edge of LRCK.
In master mode, system reset is released by inputting MCLK after setting the PDN pin to “H”. The AK5522 exits power-down mode by a rising edge of MCLK. Initialization cycle starts when power-down mode is released. During initialization, the ADC digital outputs of both channels are in 2’s complement format and forced to “0”. The ADC outputs settle to data correspondent to the input signals after the end of initialization (This settling takes approximately the group delay time).

■ Register Control Interface

The AK5522 supports the fast-mode I^{2}C-bus (max: 400kHz, Ver1.0).

WRITE Operations
Figure 72 shows the data transfer sequence of the I^{2}C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 78). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The seven bits of the slave address are fixed as “0010001”. If the slave address matches that of the AK5522, the AK5522 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 79). R/W bit = “1” indicates that the read operation is to be executed. “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK5522. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 74). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 75). The AK5522 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 78).

The AK5522 can perform more than one byte write operation per sequence. After receipt of the third byte the AK5522 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “04H” prior to generating a stop condition, the address counter will “roll over” to “00H” and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 80) except for the START and STOP conditions.

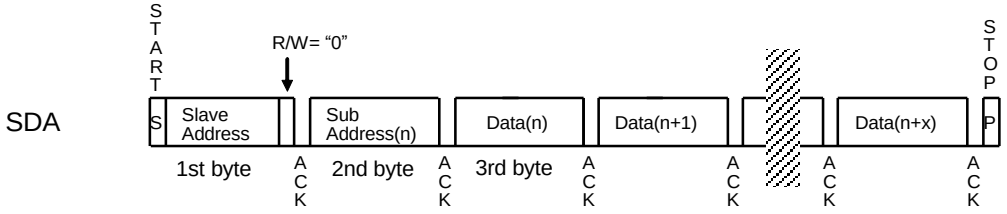


Figure 72. Data Transfer Sequence at the I^{2}C-Bus Mode

0	0	1	0	0	0	1	R/W

Figure 73. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 74. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 75. Byte Structure After The Second Byte

READ Operations
Set the R/W bit = “1” for the READ operation of the AK5522. After transmission of data, the master can read the next address’s data by generating acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “04H” prior to generating stop condition, the address counter will “roll over” to “00H” and the data of “00H” will be read out.

The AK5522 supports two basic read operations: Current Address Read and Random Address Read.

(1) Current Address Read
The AK5522 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address “n”, the next CURRENT READ operation would access data from the address “n+1”. After receipt of the slave address with R/W bit “1”, the AK5522 generates acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate acknowledge but generates a stop condition instead, the AK5522 ceases transmission.

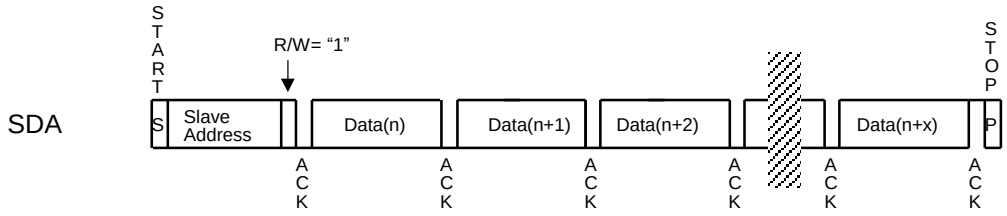


Figure 76. Current Address Read

(2) Random Address Read
The random read operation allows the master to access any memory location at random. Prior to issuing a slave address with the R/W bit =“1”, the master must execute a “dummy” write operation first. The master issues a start request, a slave address (R/W bit = “0”) and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit =“1”. The AK5522 then generates acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate acknowledge but generates a stop condition instead, the AK5522 ceases transmission.

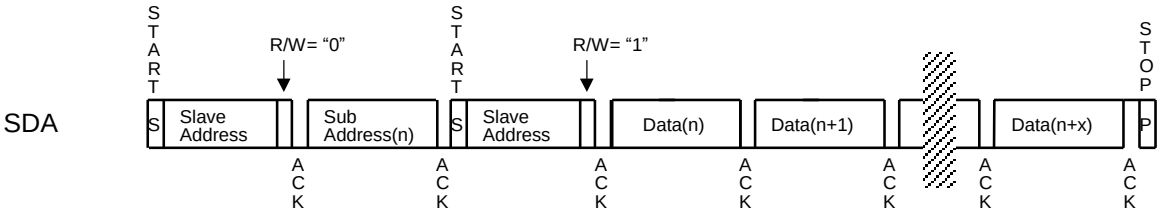


Figure 77. Random Address Read

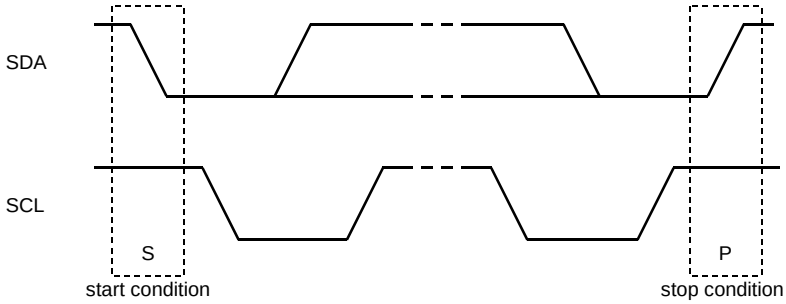


Figure 78. START and STOP Conditions

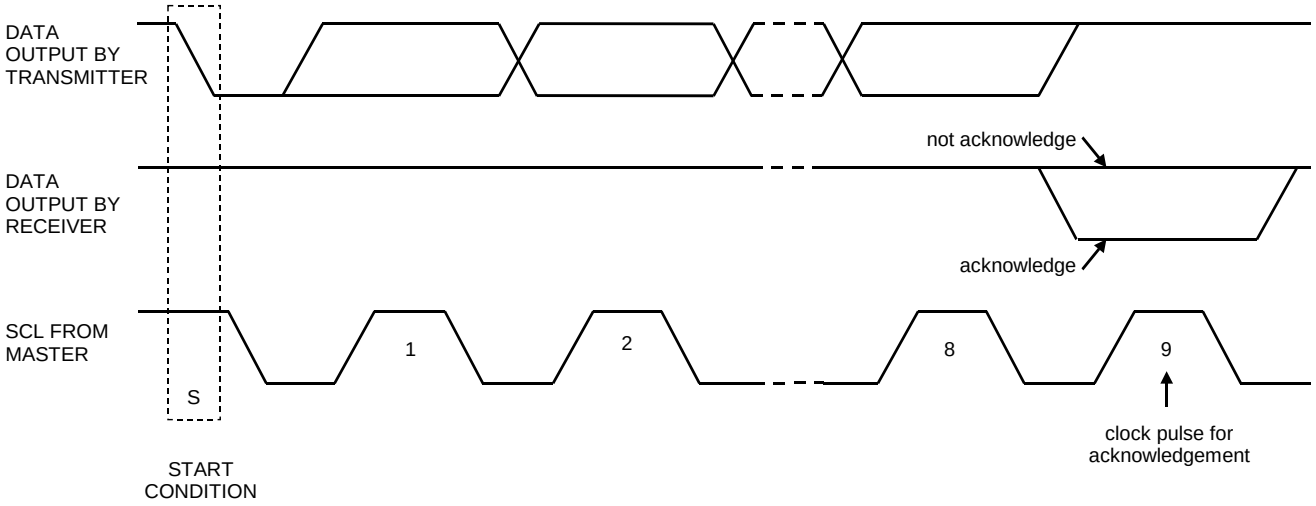


Figure 79. Acknowledge on the I^2C-Bus

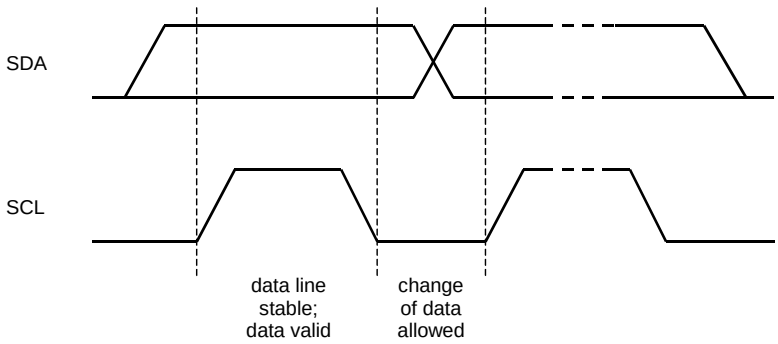


Figure 80. Bit Transfer on the I^2C-Bus

■ **Register Map**

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	PDLDOAN	PDPLLN	PDADLN	PDADRN	RSTN
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
02H	Control 1	CM3	CM2	CM1	CM0	TDM1	TDM0	DIF	HPFE
03H	Control 2	0	0	0	INVMCLK	BCKO1	BCKO0	SD	SLOW
04H	Input Gain	GR3	GR2	GR1	GR0	GL3	GL2	GL1	GL0

Note 24. Data must not be written into addresses from “05H” to “1FH”.
Note 25. The bits indicated as “0” or “1” must contain a “0” or “1” value. When RSTN bit is set to “0”, the internal digital filter and the control block are reset but the register values are not initialized.
Note 26. When the PDN pin is set to “L”, all registers are initialized to their default values.

■ **Register Definitions**

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	0	PDLDOAN	PDPLLN	PDADLN	PDADRN	RSTN
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	1	0	0	0	1

RSTN: Internal Reset
0: Reset
1: Normal Operation (default)

PDADRN: R-Channel Power Management
0: Power Down (default)
1: Normal Operation

PDADLN: L-Channel Power Management
0: Power Down (default)
1: Normal Operation

PDPLLN: PLL Power Management
0: Power Down (default)
1: Normal Operation

PDLDOAN: REGAO (Regulator for DAC) Power Management
0: Power Down
1: Normal Operation (default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	PLL Control	FS3	FS2	FS1	FS0	PLL3	PLL2	PLL1	PLL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	0	0	0	0

PLL3-0: PLL Reference Clock Frequency Select (Table 21, Table 26)

FS3-0: Sampling Clock Frequency Select (Table 22)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 1	CM3	CM2	CM1	CM0	TDM1	TDM0	DIF	HPFE
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	0	0	1

HPFE: HPF Enable
0: Disable
1: Enable (default)

DIF: Data Format Select
0: 32bit MSB Justified (default)
1: 32bit I^2S Compatible

TDM1-0: TDM Output Select
00: Normal (default)
01: TDM128
10: TDM256
11: Not Available

CM3-CM0: External Clock Mode Select (Table 15, Table 19)
Default 0100b (EXT Slave: Mode 4)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Control 2	0	0	0	INVMCLK	BCKO1	BCKO0	SD	SLOW
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	1	0	0

SLOW: Slow Roll-Off Filter Select
0: Sharp Roll Off (default)
1: Slow Roll Off

SD: Short Delay Filter Select
0: Normal (default)
1: Short Delay

BCKO1-0: BICK Frequency Select in Master Mode
00: 32fsn, 32fsd, 32fsq
01: 64fsn, 64fsd, 64fsq (default)
10: 128fsn, 128fsd
11: 256fsn (TDM mode: 256fsn, 256fsd, 128fsq)

INVMCLK: PLL Input MCLK polarity inverse
0: PLL uses MCLK falling edge (default)
1: PLL uses MCLK rising edge
RSTN bit must be set to “0” when changing INVMCLK bit.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Input Gain	GR3	GR2	GR1	GR0	GL3	GL2	GL1	GL0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	0	0	1	1	0	0

GL3-0: L-channel Input Gain Select (Table 32)
GR3-0: R-channel Input Gain Select (Table 32)

15. Recommended External Circuits

Figure 81 - Figure 84 show recommended external connection. An evaluation board (AKD5522) is available for fast evaluation as well as suggestions for peripheral circuitry.

AVDD=5.0V, DVDD=3.3V

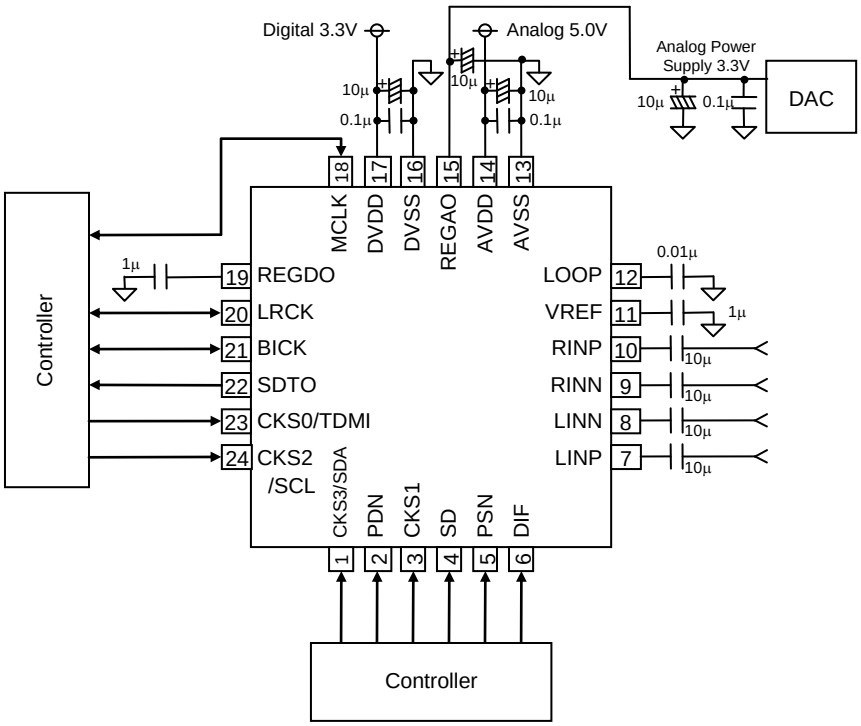


Figure 81. Typical Connection Diagram (Analog 5V, Digital I/O 3.3V)

AVDD=5.0V, DVDD=1.8V

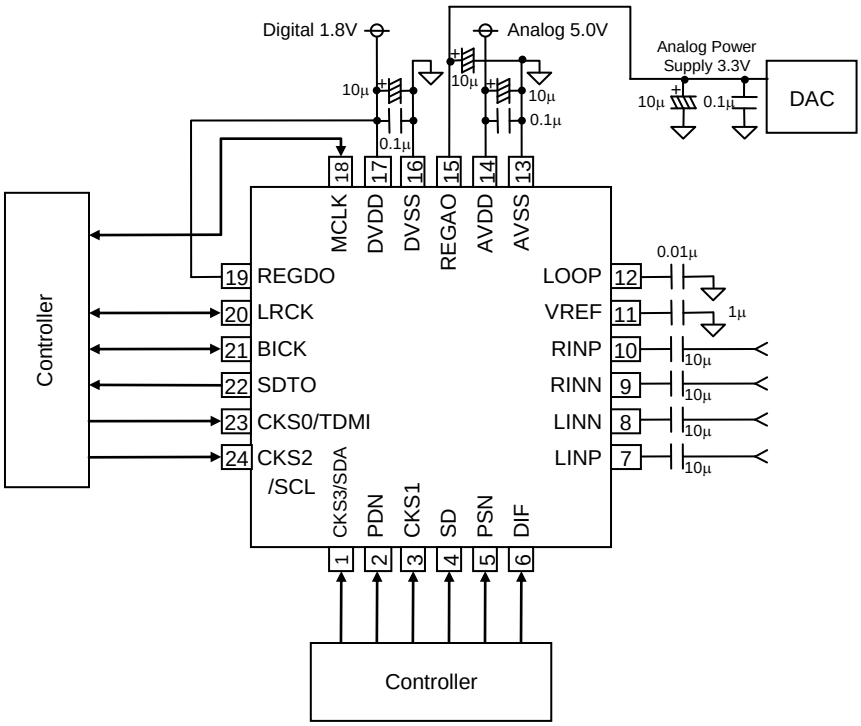


Figure 82. Typical Connection Diagram (Analog 5V, Digital I/O 1.8V)

AVDD=3.3V, DVDD=3.3V

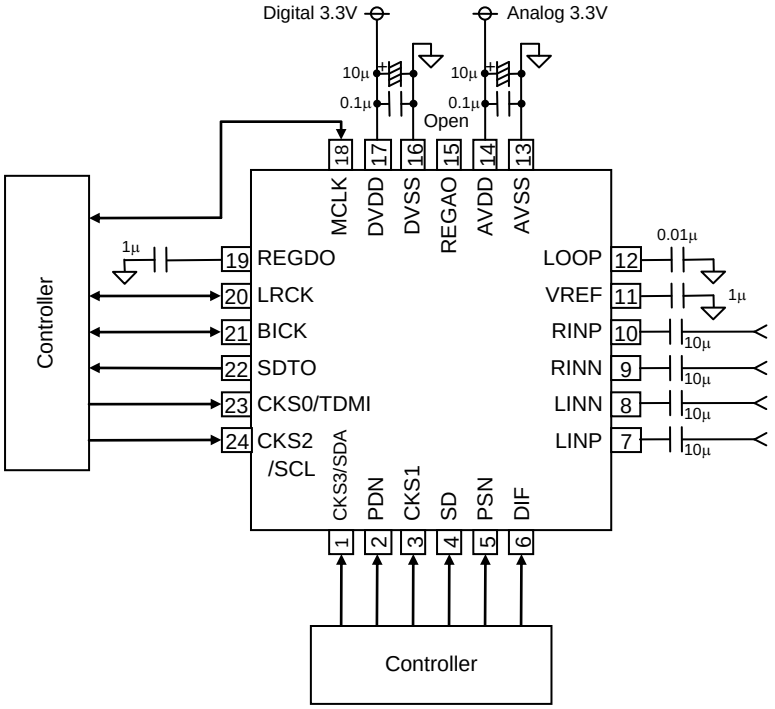


Figure 83. Typical Connection Diagram (Analog 3.3V, Digital I/O 3.3V)

AVDD=3.3V, DVDD=1.8V

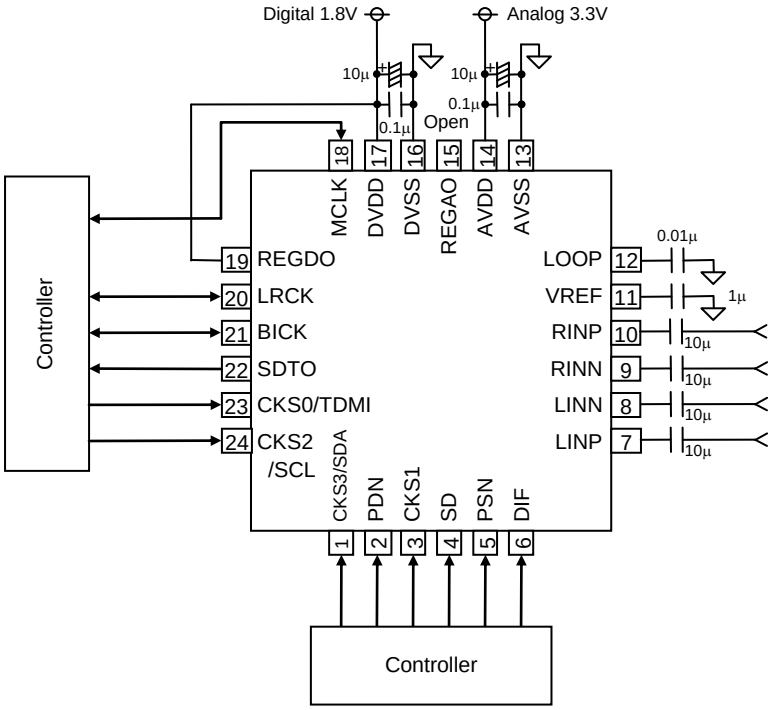


Figure 84. Typical Connection Diagram (Analog 3.3V, Digital I/O 1.8V)

Note 27. All digital input pins must not be allowed to float.

1. Grounding and Power Supply Decoupling

The AK5522 requires careful attention to power supply and grounding arrangements. Normally AVDD and DVDD are supplied from analog supply of the system. If AVDD and DVDD are supplied separately, the power up sequence is not critical. **DVSS and AVSS must be connected to the same analog ground plane.** System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

2. Reference Voltage

The VREF should be bypassed with a 1 μF ceramic capacitor to VSS. No load current may be drawn from the VREF pin. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling noise.

3. Analog Inputs

The Analog input signal is differentially supplied into the modulator via the LINP and the LINN pins or the RINP and the RINN pins. The input voltage is the difference between the LINP and LINN pins or the RINP and RINN pins. The full scale signal on ADC is 2.1Vrms (typ). Input signal is pulled up to internal reference voltage. The internal reference voltage is 2.22V±5% when AVDD= 4.5 to 5.5 V or 1.50V±5% when AVDD = 3.0 to 3.6V. The output code format is two's complement. The internal HPF removes DC offset (including DC offset by the ADC itself).

Any voltage which exceeds the upper limit of VDP+0.3V and lower limit of VDM−0.3V and any current beyond 10mA for the analog input pins should be avoided. Excessive voltages or currents to the input pins may damage the device. Hence input pins must be protected from signals at or beyond these limits. Use caution especially when using ±15V for other analog circuits in the system.

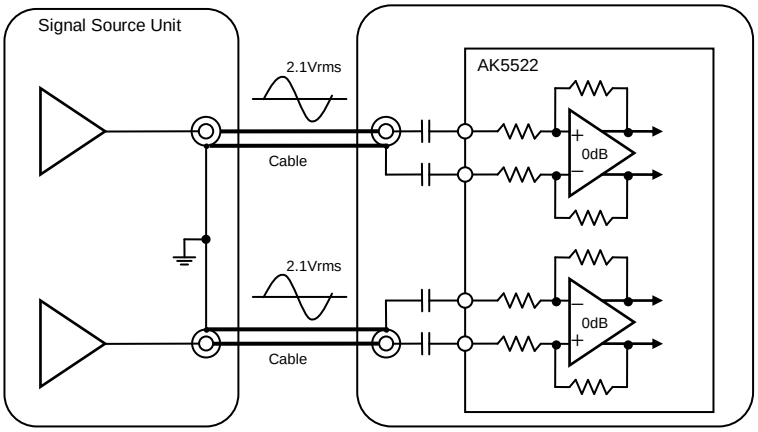


Figure 85. Analog Signal Connection (Pseudo Differential Input)

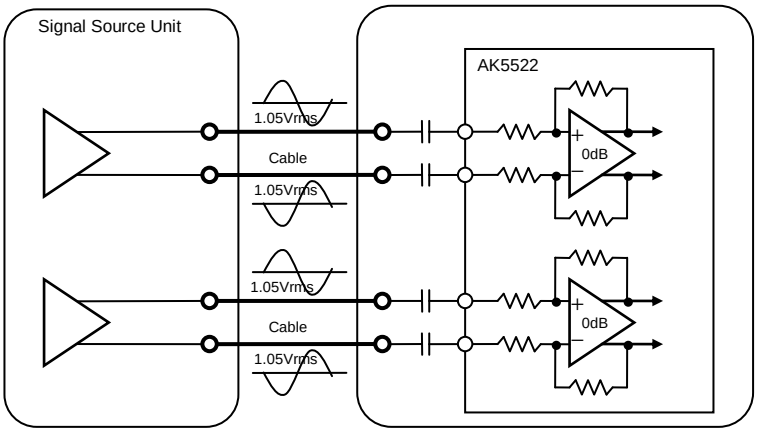


Figure 86. Analog Signal Connection (Full Differential Input)

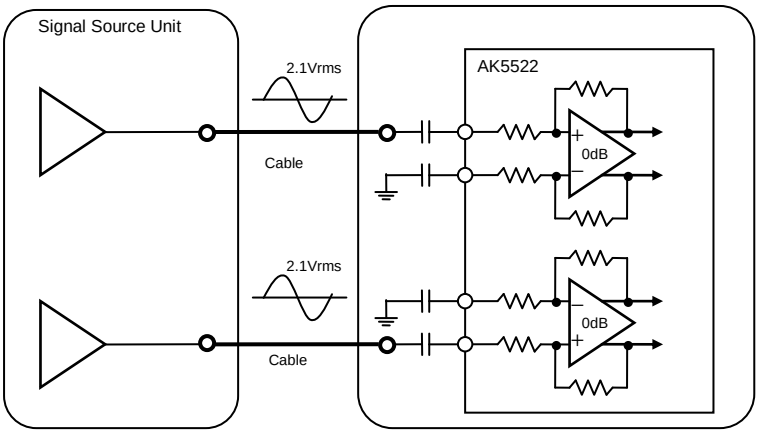
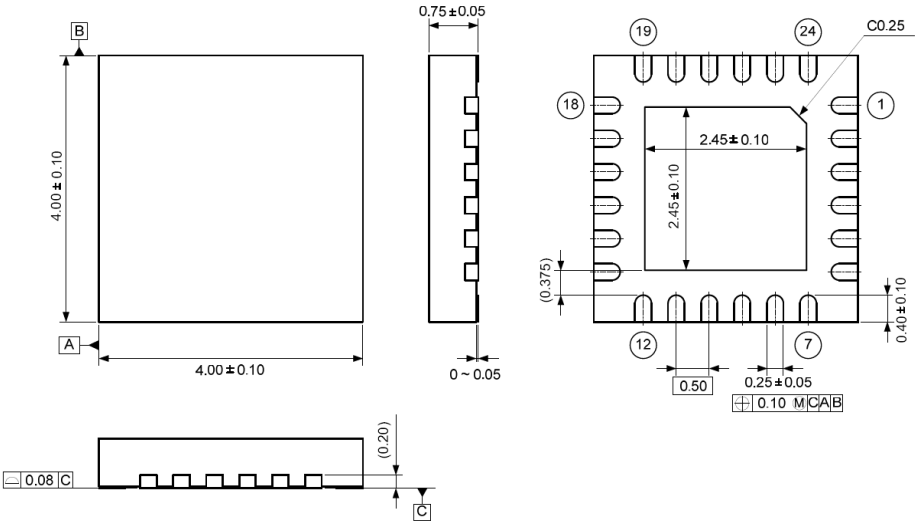


Figure 87. Analog Signal Connection (Single Ended Input)

16. Package

■ Outline Dimensions

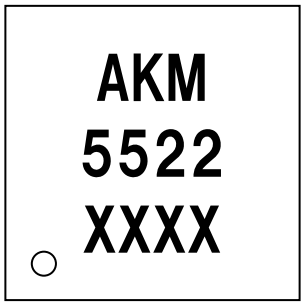
24-pin QFN (Unit mm)



■ Material & Lead Finish

Package molding compound: Epoxy Resin
Lead frame material: Cu
Pin surface treatment: Solder (Pb free) Plate

■ Marking



1

1) Pin #1 indication
2) Date Code : XXXX (4 digits)
3) Marketing Code : 5522
4) AKM Logo: AKM

17. Ordering Guide

■ **Ordering Guide**

AK5522VN	-40 - 105ºC	24-pin QFN
AKD5522	Evaluation Board for the AK5522	

18. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
17/03/28	00	First Edition		

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