

MOSFET – N-Channel, SUPERFET® II, FRFET® 650 V, 20.6 A, 190 mΩ

FCH190N65F-F085

Description

SUPERFET II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently SUPERFET II is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC-DC, Interleaved Boost PFC, Boost PFC for HEV-EV automotive.

SUPERFET II, FRFET MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

Features

- Typ. $R_{DS(on)}$ = 148 mΩ at V_{GS} = 10 V, I_D = 10 A
- Typ. $Q_{g(tot)}$ = 63 nC at V_{GS} = 10 V, I_D = 10 A
- UIS Capability
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV



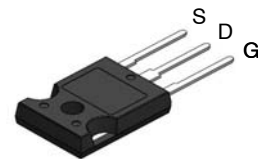
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V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
650 V	190 mΩ @ 10 V	20.6 A

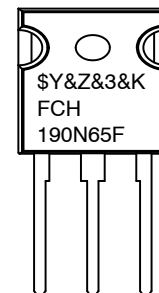


N-CHANNEL MOSFET



TO-247-3LD
CASE 340CK

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCH190N65F-F085	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH190N65F–F085

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	±20	V
I _D	Drain Current – Continuous (V _{GS} = 10) (Note 1)	20.6	A
	Pulsed Drain Current	See Fig. 4	A
E _{AS}	Single Pulsed Avalanche Rating (Note 2)	400	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P _D	Power Dissipation	208	W
	Derate Above 25°C	1.67	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25 °C, L = 50 mH, I_{AS} = 4 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. I_{SD} ≤ 10 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 380 V, Starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH190N65F	FCH190N65F–F085	TO–247–3	–	–	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.6	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

4. R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

FCH190N65F–F085

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	650	–	–	V
I _{DSS}	Drain to Source Leakage Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	10	μA
		T _J = 25 °C			1	mA
		T _J = 150 °C (Note 5)	–	–	1	mA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	3	–	5	V
R _{DS(on)}	Drain to Source On Resistance	I _D = 27 A V _{GS} = 10 V	–	148	190	mΩ
		T _J = 25 °C		346	401	mΩ
		T _J = 150 °C (Note 5)	–	346	401	mΩ

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	2447	3181	pF
C _{oss}	Output Capacitance		–	2345	3048	pF
C _{rss}	Reverse Transfer Capacitance		–	131	–	pF
R _g	Gate Resistance	f = 1 MHz	–	0.5	–	Ω
Q _{g(tot)}	Total Gate Charge	V _{DD} = 380 V, I _D = 10 A, V _{GS} = 10 V	–	63	82	nC
Q _{g(th)}	Threshold Gate Charge		–	4.3	5.6	nC
Q _{gs}	Gate to Source Gate Charge		–	12.6	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	28	–	nC

SWITCHING CHARACTERISTICS

t _{on}	Turn-On Time	V _{DD} = 380 V, I _D = 10 A, V _{GS} = 10 V, R _G = 4.7 Ω	–	40	100	ns
t _{d(on)}	Turn-On Delay Time		–	25	–	ns
t _r	Rise Time		–	14.5	–	ns
t _{d(off)}	Turn-Off Delay Time		–	64	–	ns
t _f	Fall Time		–	5	–	ns
t _{off}	Turn-Off Time		–	69	158	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Voltage	V _{GS} = 0 V, I _{SD} = 10 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 520 V, I _F = 10 A, dI _{SD} /dt = 100 A/μs	–	141	–	ns
Q _{rr}	Reverse Recovery Charge		–	889	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

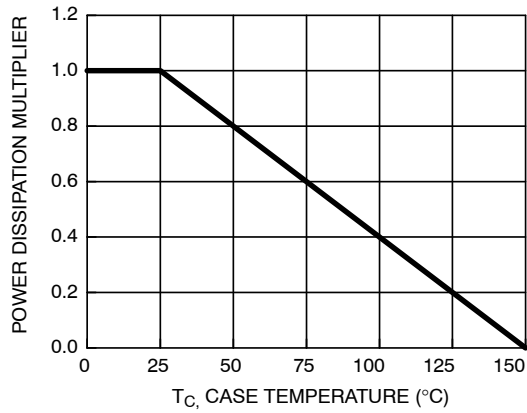


Figure 1. Normalized Power Dissipation vs. Case Temperature

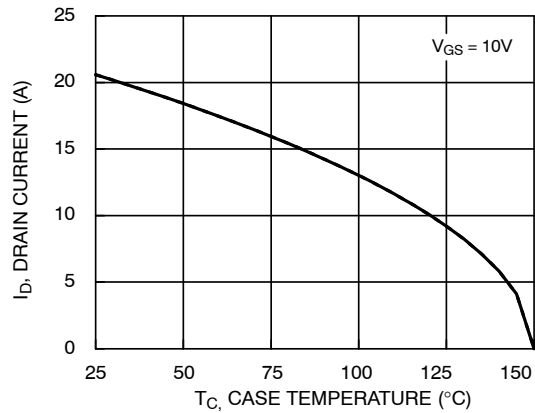


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

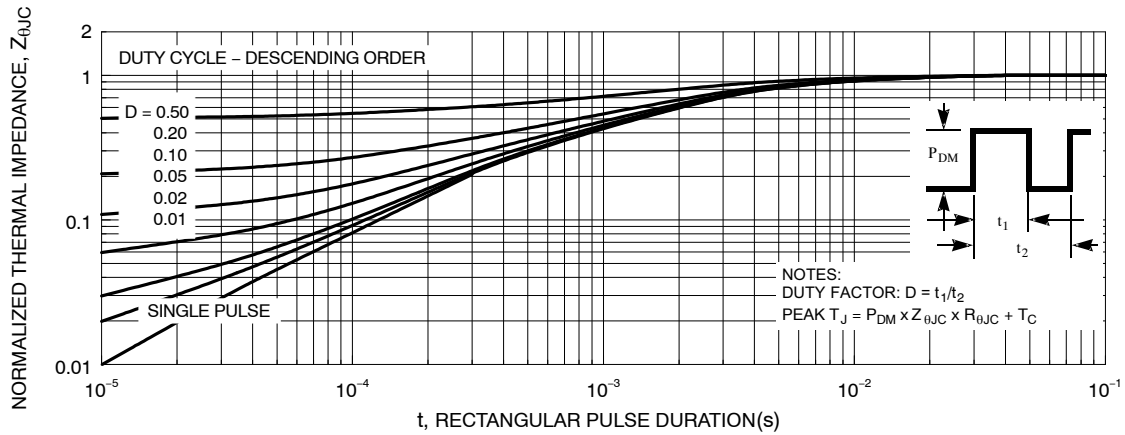


Figure 3. Normalized Maximum Transient Thermal Impedance

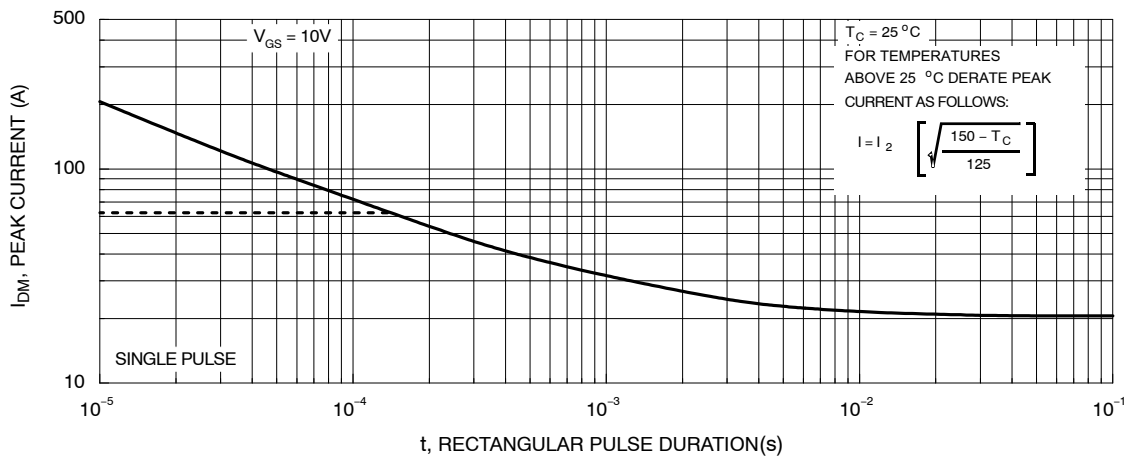


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

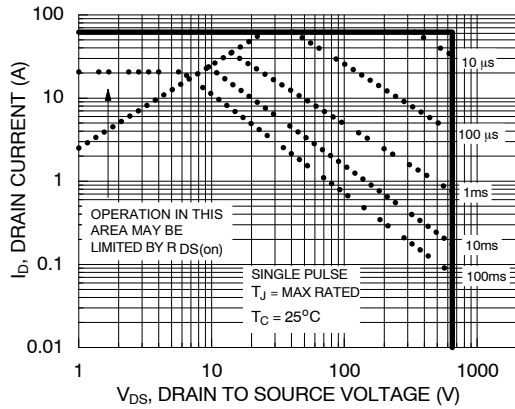


Figure 5. Forward Bias Safe Operating Area

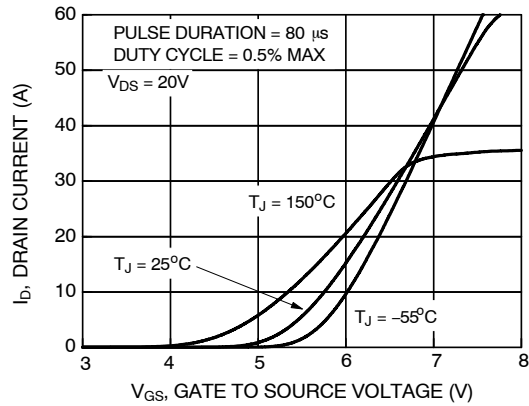


Figure 6. Transfer Characteristics

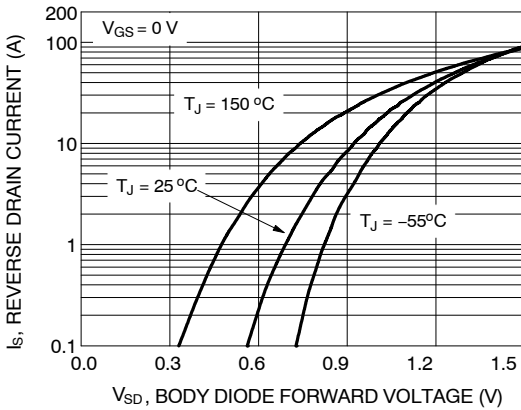


Figure 7. Forward Diode Characteristics

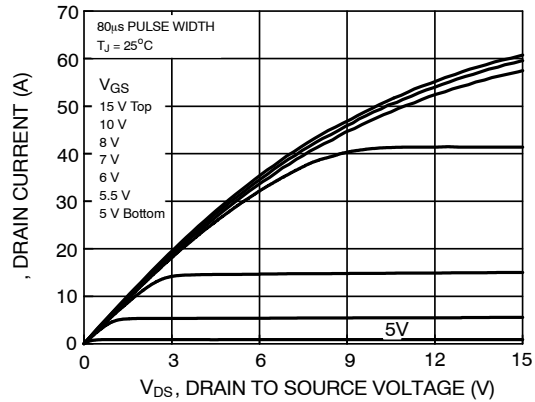


Figure 8. Saturation Characteristics

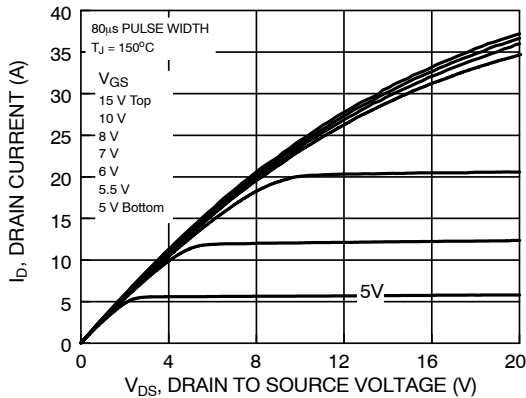
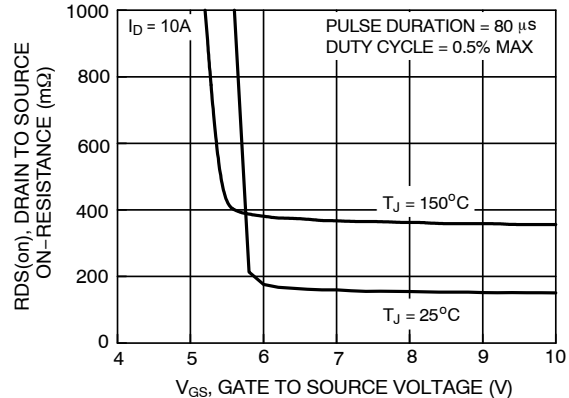


Figure 9. Saturation Characteristics

Figure 10. $R_{DS(on)}$ vs. Gate Voltage

TYPICAL CHARACTERISTICS

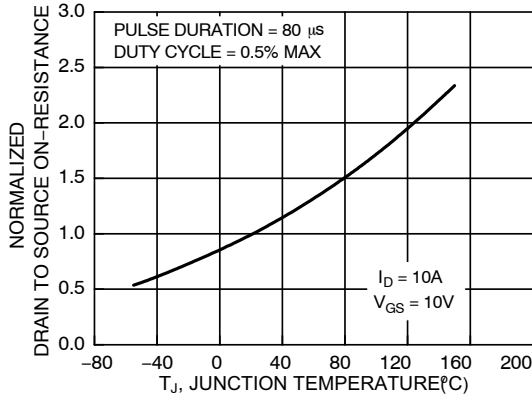


Figure 11. Normalized $R_{DS(on)}$ vs. Junction Temperature

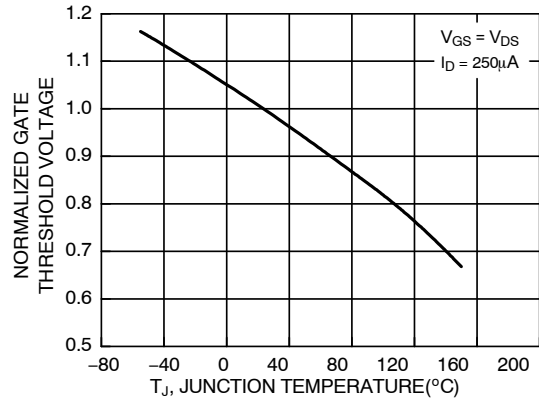


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

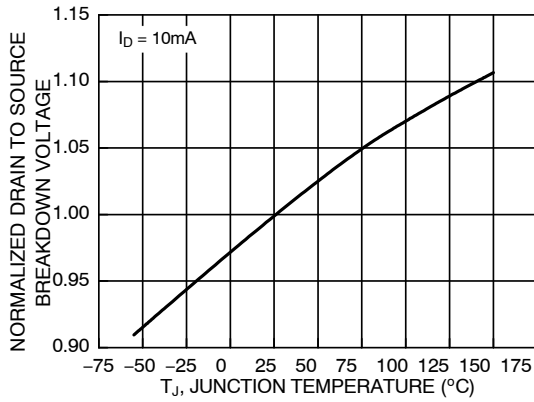


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

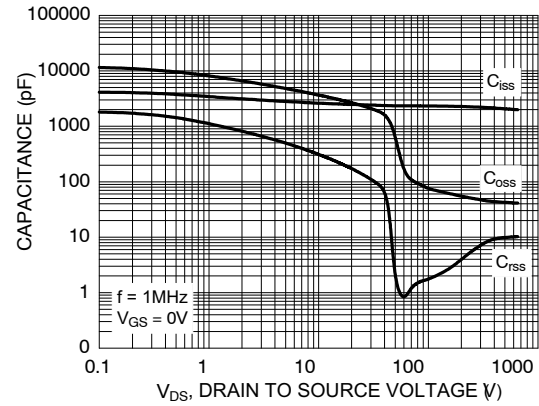


Figure 14. Capacitance vs. Drain to Source Voltage

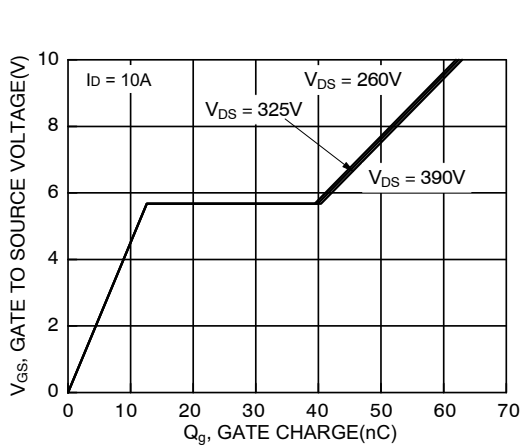


Figure 15. Gate Charge vs. Gate to Source Voltage

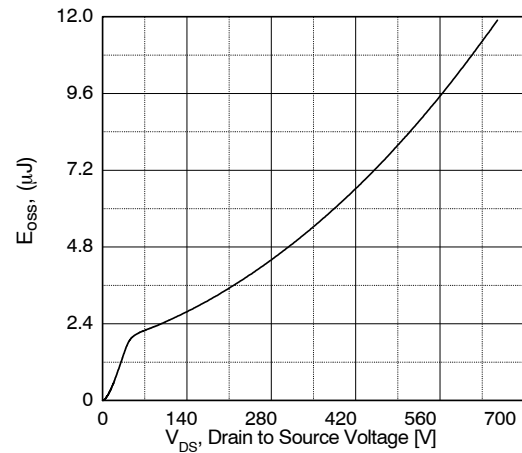


Figure 16. E_{oss} vs. Drain to Source Voltage



Figure 17. Gate Charge Test Circuit & Waveform



Figure 18. Resistive Switching Test Circuit & Waveforms



Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

FCH190N65F-F085

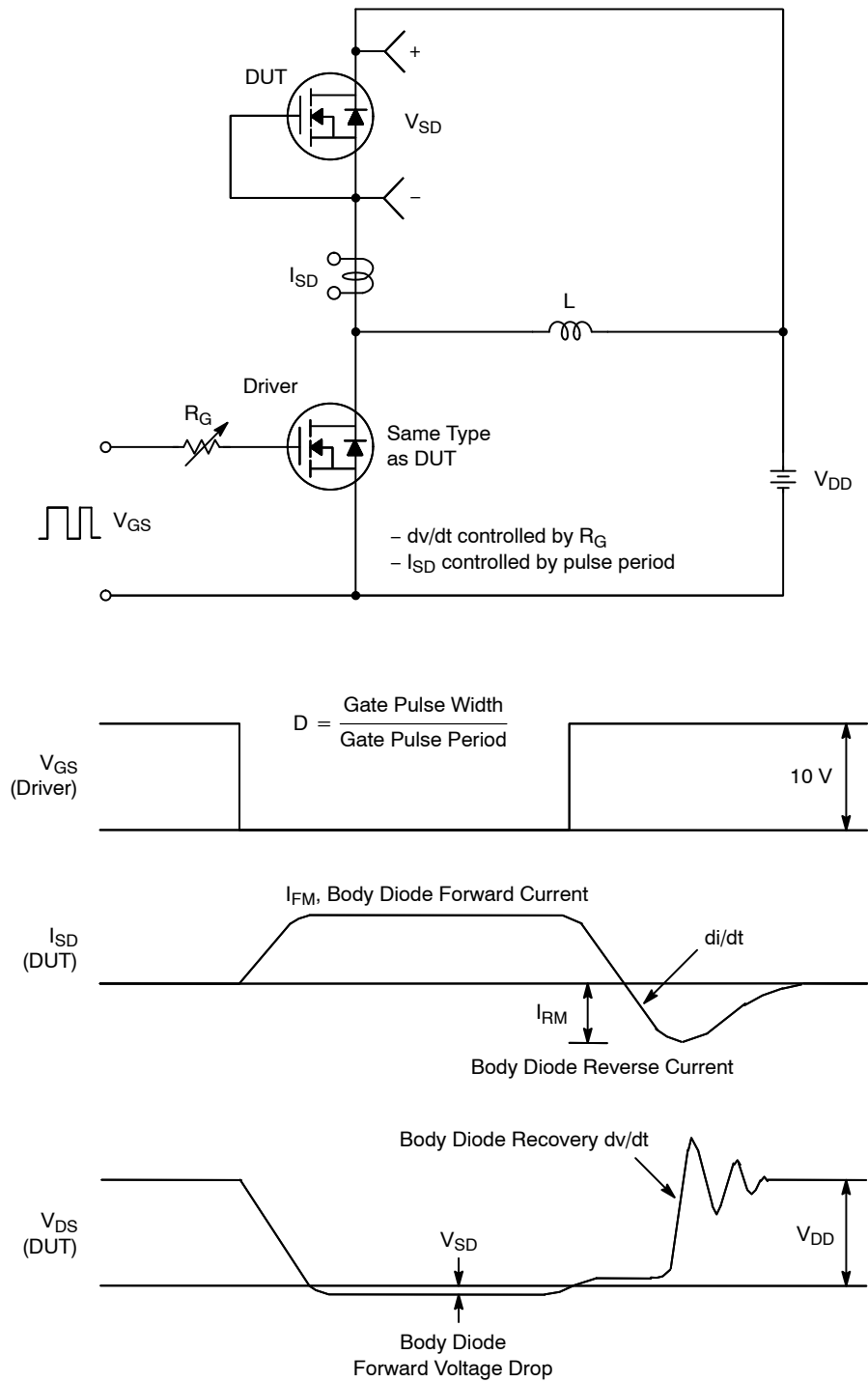


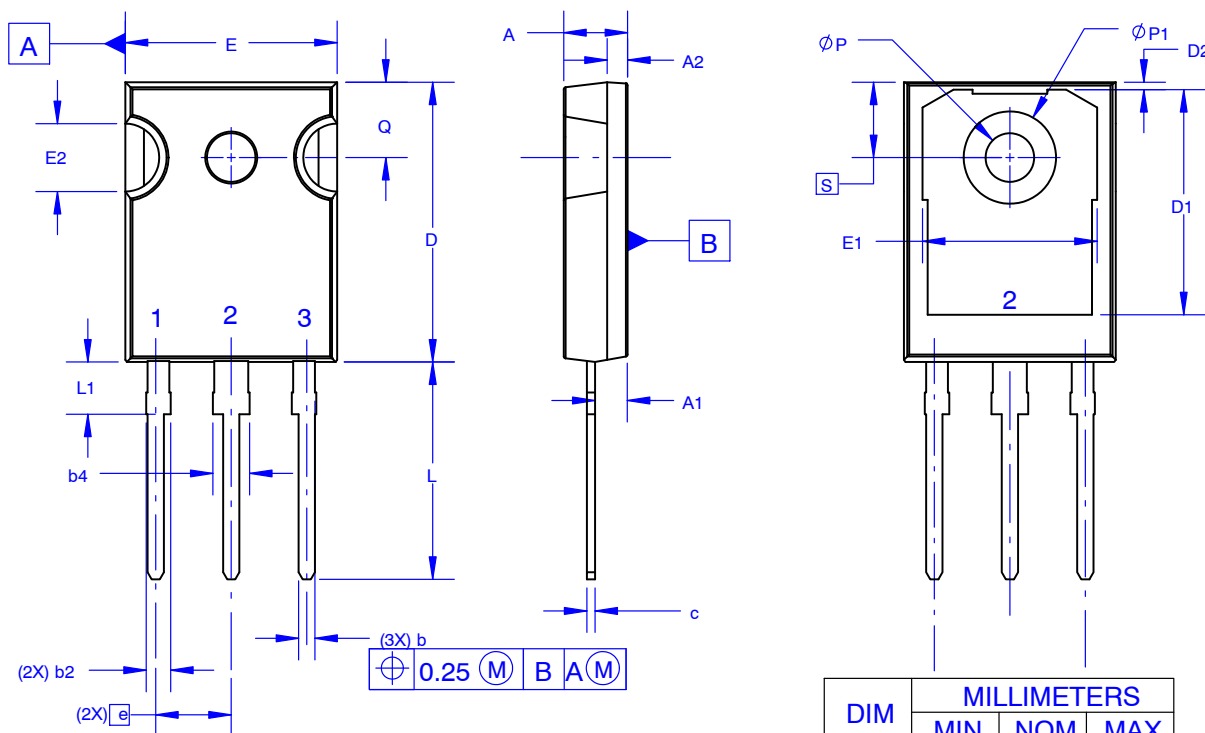
Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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TO-247-3LD SHORT LEAD CASE 340CK ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ϕP	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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