

MOSFET - Power, Single N-Channel

40 V, 1.1 mΩ, 240 A

FDBL9406L-F085

Features

- Small Footprint (TOLL) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	40	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	240	A
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^{\circ}\text{C}$	P_D	300	W
		$T_C = 100^{\circ}\text{C}$		150	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	43	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 100^{\circ}\text{C}$		31	
		$T_A = 25^{\circ}\text{C}$	P_D	3.5	W
		$T_A = 100^{\circ}\text{C}$		1.7	
Pulsed Drain Current	$T_C = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		I_{DM}	2755	A
Operating Junction and Storage Temperature Range			T_J , T_{stg}	-55 to +175	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	100	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 85\text{ A}$; $L = 60\text{ }\mu\text{H}$)			E_{AS}	217	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	43	

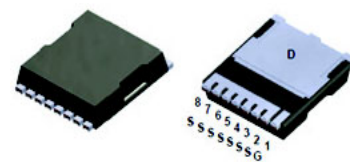
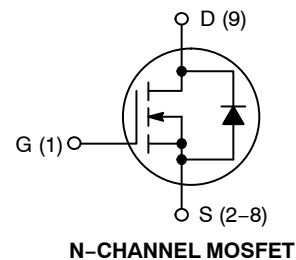
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Current is limited by bondwire configuration.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



ON Semiconductor®

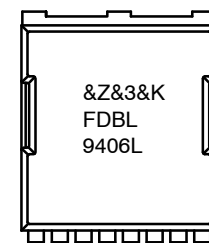
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	1.1 mΩ @ 10 V	80 A
	1.78 mΩ @ 4.5 V	



MO-299A
CASE 100CU

MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 FDBL9406L = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

FDBL9406L–F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J		–	19.3	–	mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V, T _J = 25°C	–	–	1	μA
		V _{GS} = 0 V, V _{DS} = 40 V, T _J = 175°C	–	–	1	mA
Zero Gate Voltage Drain Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V	–	–	±100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = 250 μA	1	1.9	3	V
Threshold Temperature Coefficient	V _{GS(th)} /T _J		–	–6.5	–	mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 80 A	–	0.9	1.1	mΩ
		V _{GS} = 4.5 V, I _D = 40 A	–	1.25	1.78	

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 20 V	–	8600	–	pF
Output Capacitance	C _{oss}		–	2380	–	pF
Reverse Transfer Capacitance	C _{rss}		–	106	–	pF
Gate Resistance	R _g	V _{GS} = 0.5 V, f = 1 MHz	–	2	–	Ω
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 32 V, I _D = 80 A	–	58	–	nC
		V _{GS} = 10 V, V _{DS} = 32 V, I _D = 80 A	–	121	–	
Threshold Gate Charge	Q _{g(th)}	V _{GS} = 0 to 1 V	–	7	–	
Gate-to-Source Gate Charge	Q _{gs}	V _{DD} = 32 V, I _D = 80 A	–	26	–	
Gate-to-Drain “Miller” Charge	Q _{gd}		–	19	–	
Plateau Voltage	V _{GP}		–	3.2	–	V

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, I _D = 80 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	22	–	ns
Turn-On Rise Time	t _r		–	22	–	ns
Turn-Off Delay Time	t _{d(off)}		–	134	–	ns
Turn-Off Fall Time	t _f		–	44	–	ns

DRAIN–SOURCE DIODE CHARACTERISTICS

Source-to-Drain Diode Voltage	V _{SD}	I _{SD} = 80 A, V _{GS} = 0 V	–	0.81	1.25	V
		I _{SD} = 40 A, V _{GS} = 0 V	–	0.77	1.2	V
Reverse Recovery Time	T _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs I _S = 80 A	–	77	–	ns
Charge Time	t _a		–	38	–	
Discharge Time	t _b		–	39	–	
Reverse Recovery Charge	Q _{RR}		–	95	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

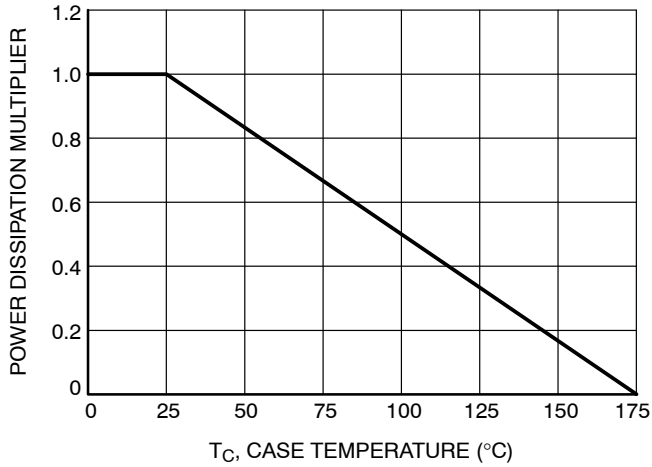


Figure 1. Normalized Power Dissipation vs. Case Temperature

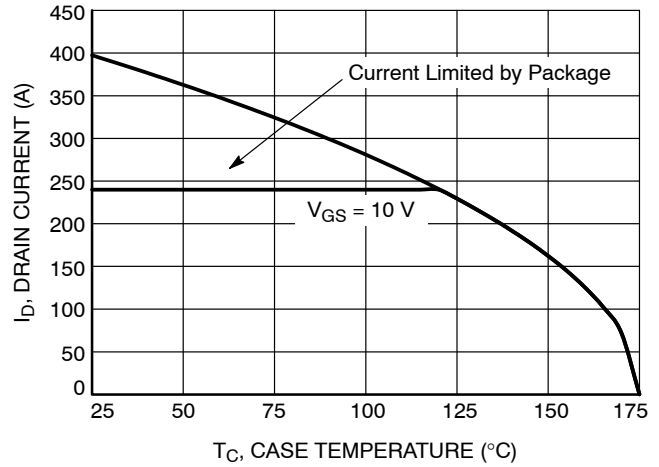


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

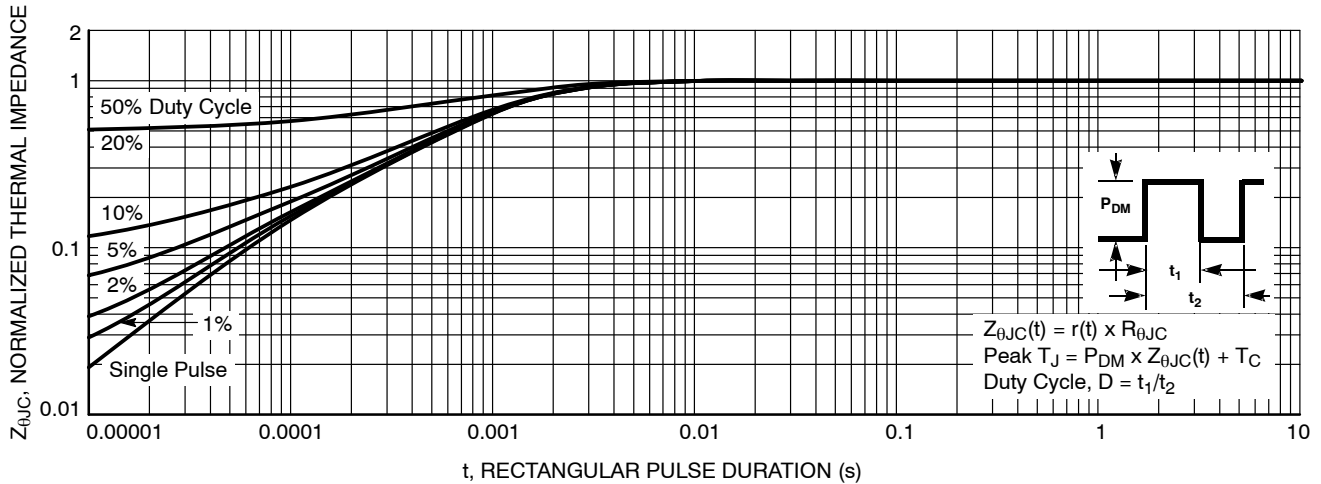


Figure 3. Normalized Maximum Transient Thermal Impedance

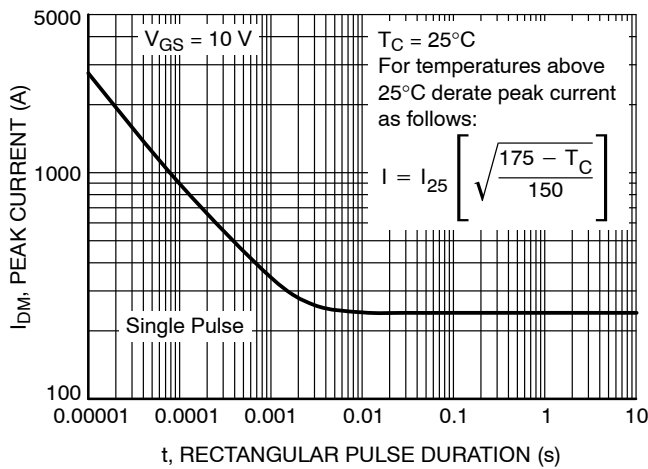


Figure 4. Peak Current Capability

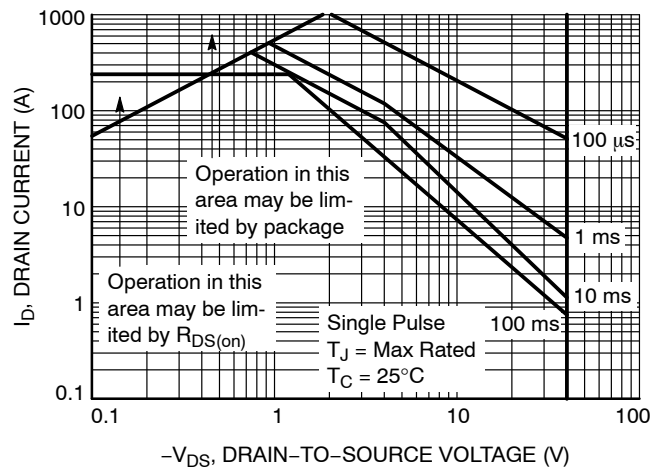


Figure 5. Forward Bias Safe Operating Area

TYPICAL CHARACTERISTICS

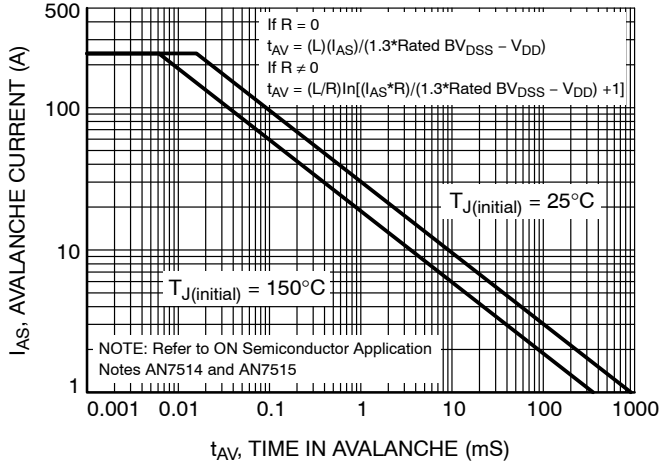


Figure 6. Unclamped Inductive Switching Capability

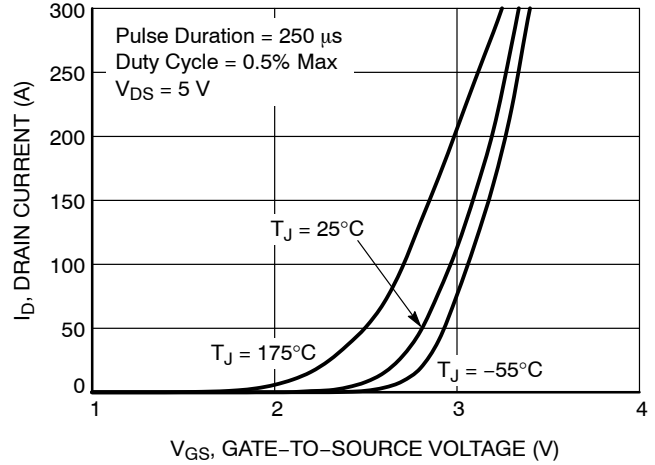


Figure 7. Transfer Characteristics

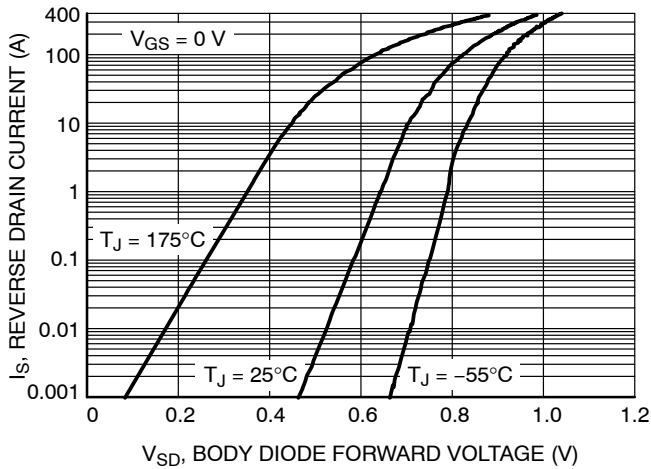


Figure 8. Forward Diode Characteristics

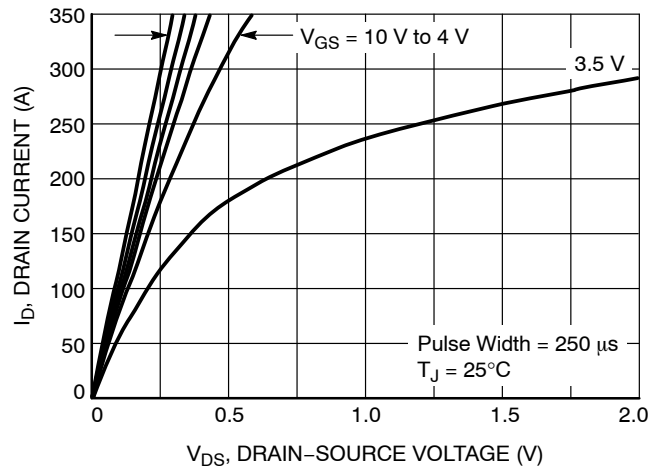


Figure 9. Saturation Characteristics

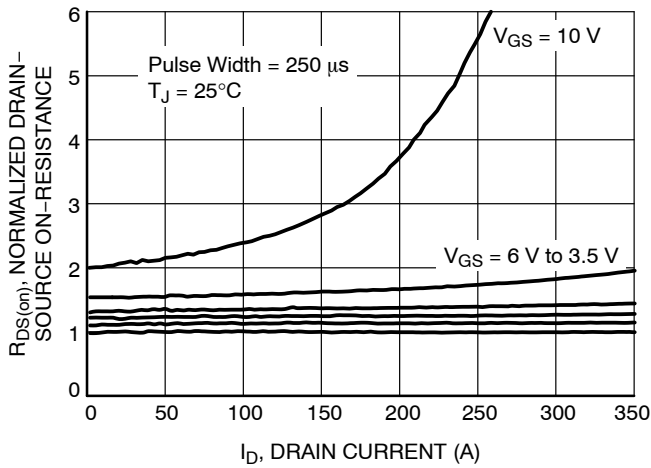


Figure 10. Normalized $R_{DS(on)}$ vs. Drain Current

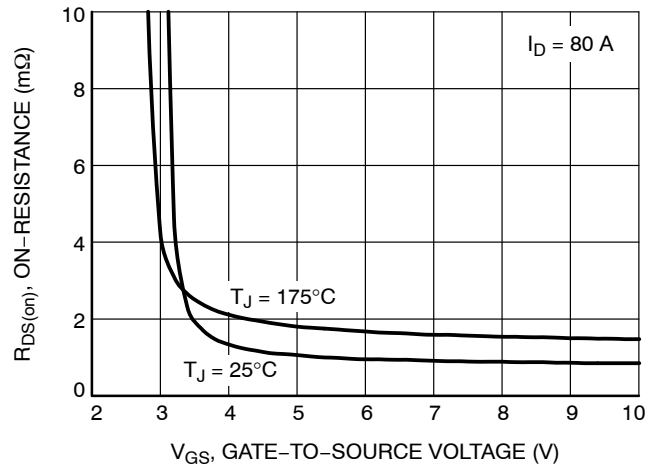


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

TYPICAL CHARACTERISTICS

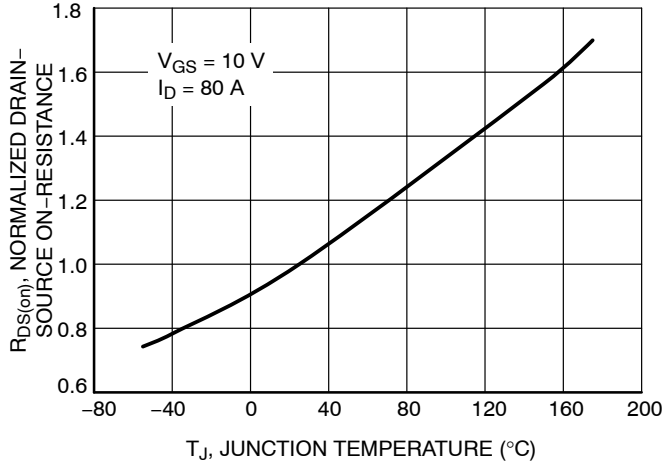


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

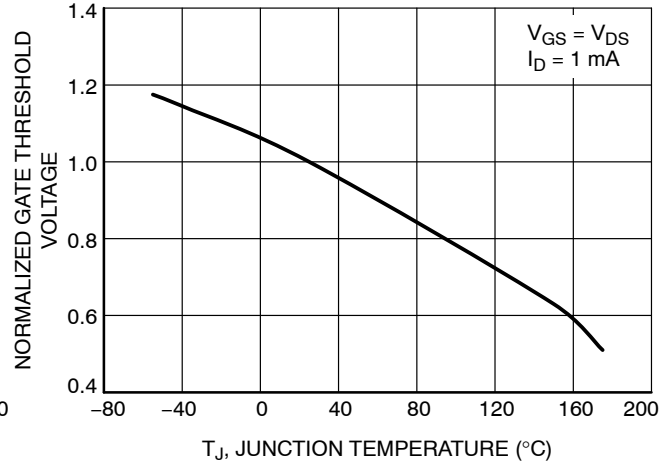


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

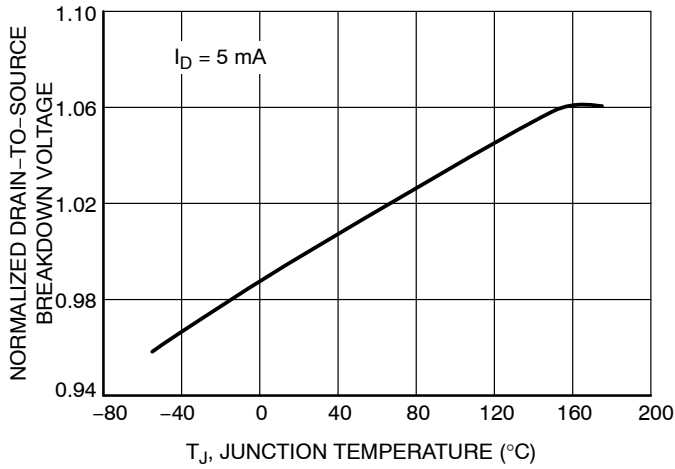


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

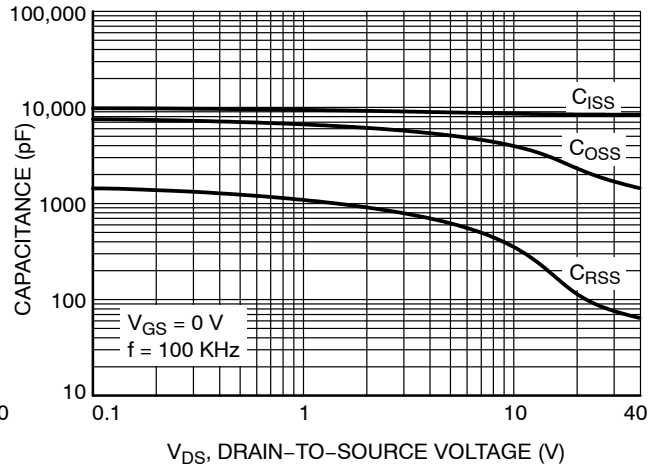


Figure 15. Capacitance vs. Drain-to-Source Voltage

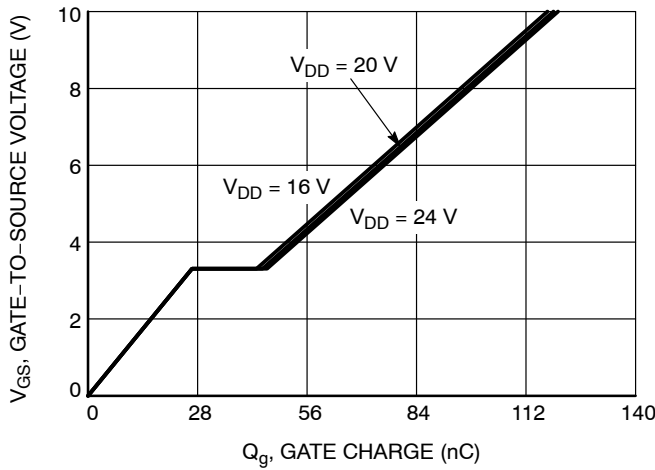


Figure 16. Gate Charge vs. Gate-to-Source Voltage

FDBL9406L–F085

PACKAGE MARKING AND ORDERING INFORMATION

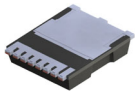
Part Number	Top Marking	Package	Reel Size	Tape Width	Quantity
FDBL9406L–F085	FDBL9406L	H-PSOF8L (Pb-Free / Halogen Free)	13"	24 mm	2000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

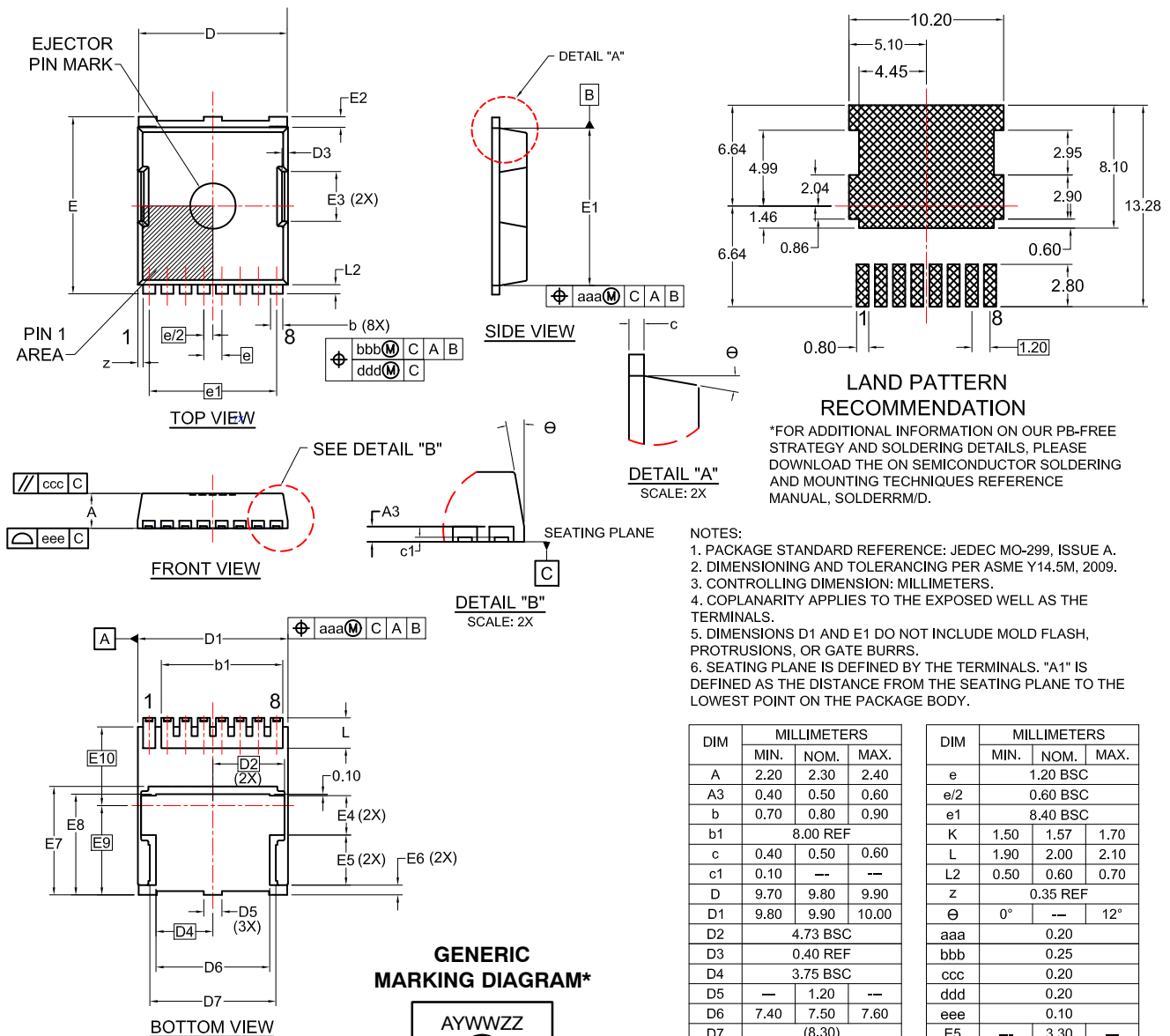
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H-PSOF8L 11.68x9.80 CASE 100CU ISSUE A

DATE 06 JAN 2020



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A3	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	---	1.20	---
D6	7.40	7.50	7.60
D7	(8.30)		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	---	2.60	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	1.50	1.57	1.70
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		
E5	---	3.30	---
E6	---	0.65	---
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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