

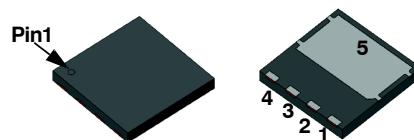
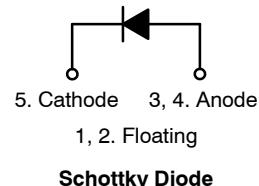
Silicon Carbide Schottky Diode

650 V, 4 A



ON Semiconductor®

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**PQFN 8x8, 2P
CASE 483AP**

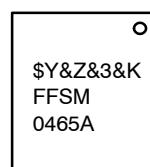
Features

- Max Junction Temperature 175°C
- Avalanche Rated 23 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FFSM0465A = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FFSM0465A

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{RRM}	Peak Repetitive Reverse Voltage		650	V
E _{AS}	Single Pulse Avalanche Energy (Note 1)		23	mJ
I _F	Continuous Rectified Forward Current @ T _C < 152°C		4	A
	Continuous Rectified Forward Current @ T _C < 135°C		5.7	
I _{F, Max}	Non-Repetitive Peak Forward Surge Current	T _C = 25°C, 10 µs	320	A
		T _C = 150°C, 10 µs	310	A
I _{F,SM}	Non-Repetitive Forward Surge Current		21	A
I _{F,RM}	Repetitive Forward Surge Current		15	A
P _{tot}	Power Dissipation	T _C = 25°C	43	W
		T _C = 150°C	7.2	W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. E_{AS} of 23 mJ is based on starting T_J = 25°C, L = 1 mH, I_{AS} = 6.8 A, V = 50 V.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max	3.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V _F	Forward Voltage	I _F = 4 A, T _C = 25°C	–	1.50	1.75	V
		I _F = 4 A, T _C = 125°C	–	1.6	2.0	
		I _F = 4 A, T _C = 175°C	–	1.72	2.4	
I _R	Reverse Current	V _R = 650 V, T _C = 25°C	–	–	200	µA
		V _R = 650 V, T _C = 125°C	–	–	400	
		V _R = 650 V, T _C = 175°C	–	–	600	
Q _C	Total Capacitive Charge	V = 400 V	–	15	–	nC
C	Total Capacitance	V _R = 1 V, f = 100 kHz	–	247	–	pF
		V _R = 200 V, f = 100 kHz	–	29	–	
		V _R = 400 V, f = 100 kHz	–	22	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping [†]
FFSM0465A	FFSM0465A	PQFN 8x8, 2P (Pb-Free/Halogen Free)	3000Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

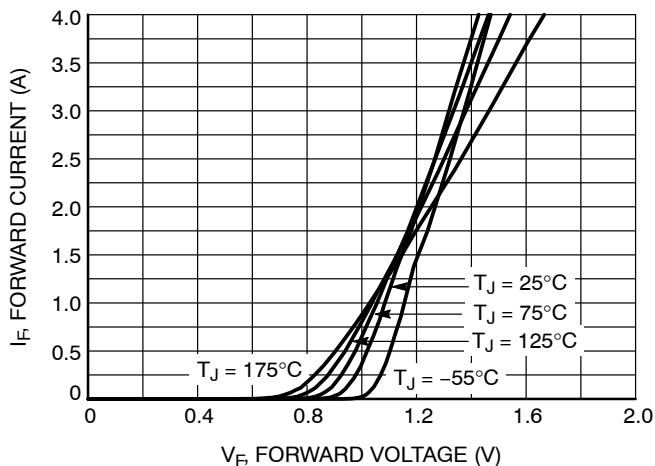


Figure 1. Forward Characteristics

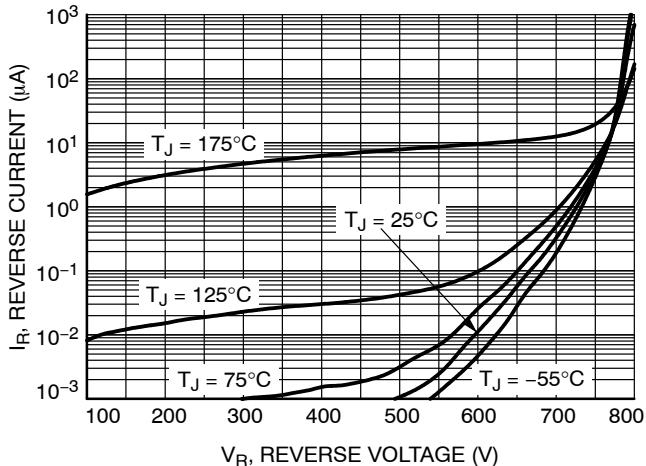


Figure 2. Reverse Characteristics

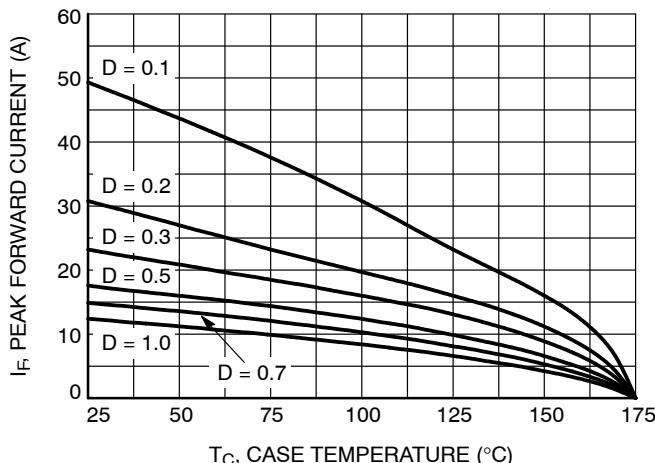


Figure 3. Current Derating

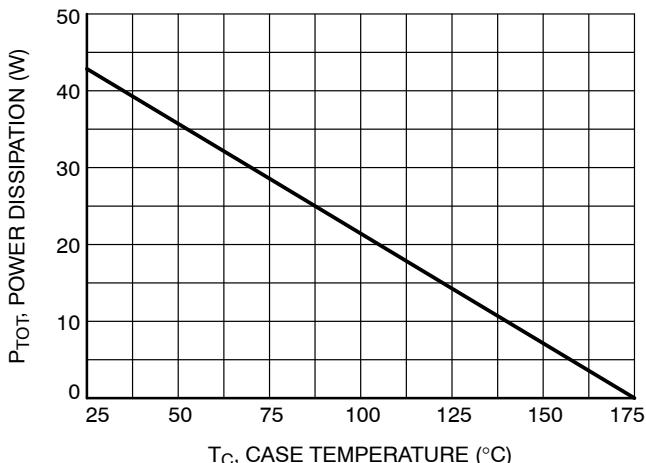


Figure 4. Power Derating

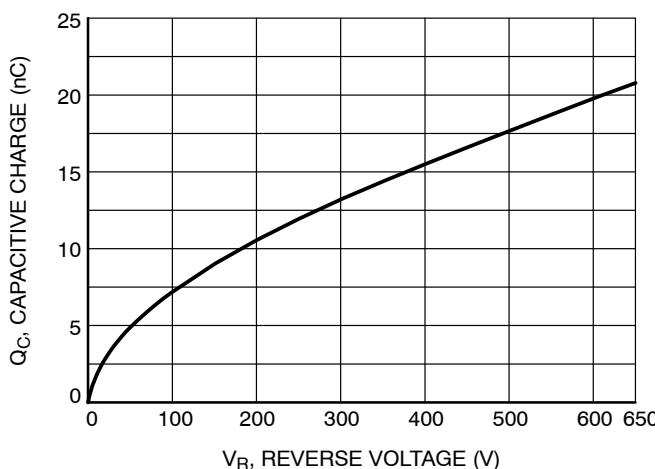


Figure 5. Capacitive Charge vs. Reverse Voltage

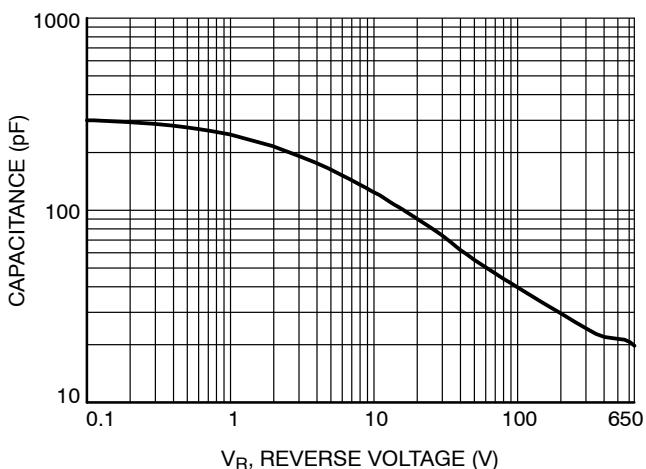


Figure 6. Capacitance vs. Reverse Voltage

FFSM0465A

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

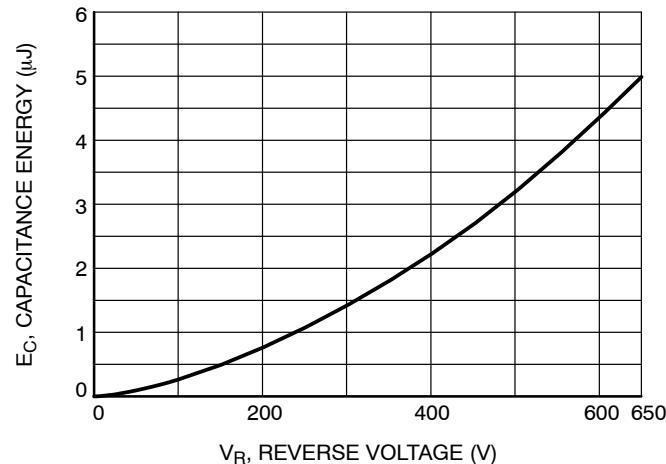


Figure 7. Capacitance Stored Energy

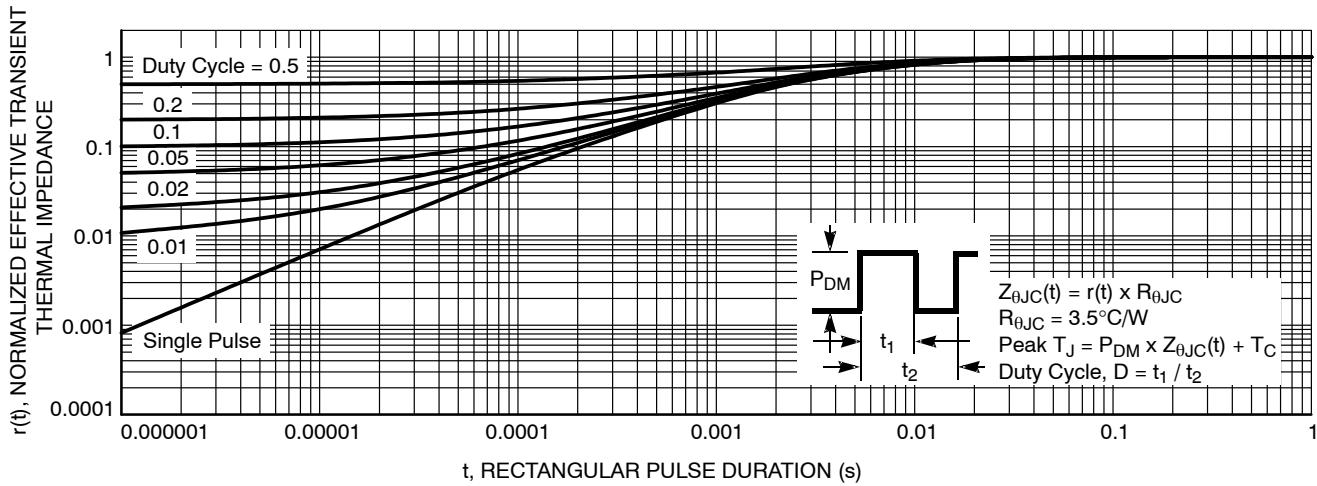


Figure 8. Junction-to-Case Transient Thermal Response Curve

TEST CIRCUIT AND WAVEFORMS

$L = 1 \text{ mH}$
 $R < 0.1 \Omega$
 $V_{DD} = 50 \text{ V}$
 $\text{EAVL} = 1/2LI^2 [V_{R(\text{AVL})} / (V_{R(\text{AVL})} - V_{DD})]$
 $Q1 = \text{IGBT (}BV_{CES} > \text{DUT } V_{R(\text{AVL})}\text{)}$

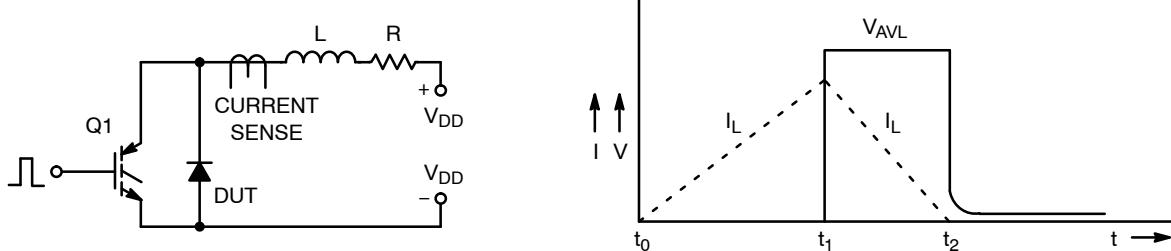
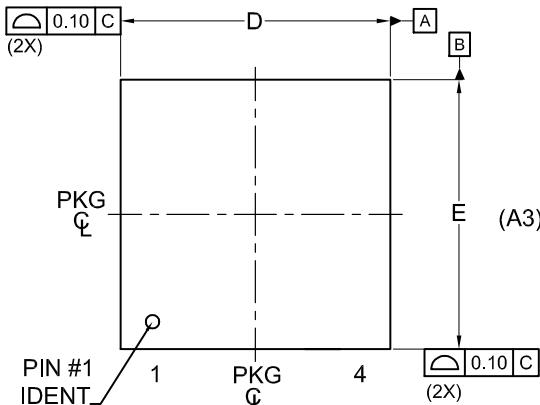


Figure 9. Unclamped Inductive Switching Test Circuit & Waveform



PQFN4 8X8, 2P
CASE 483AP
ISSUE A

DATE 06 JUL 2021



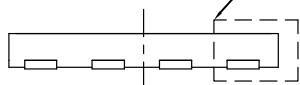
DETAIL A
SCALE: 2X

NOTES:

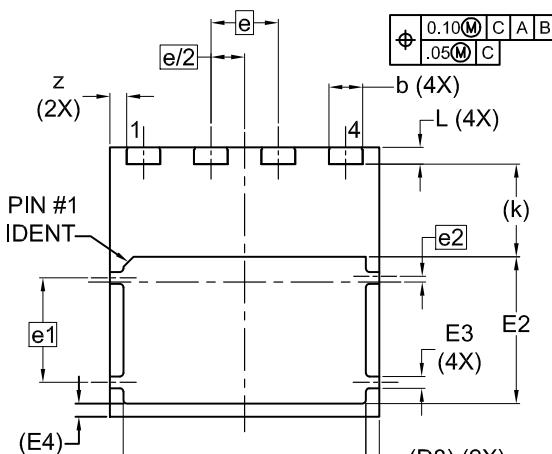
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

TOP VIEW

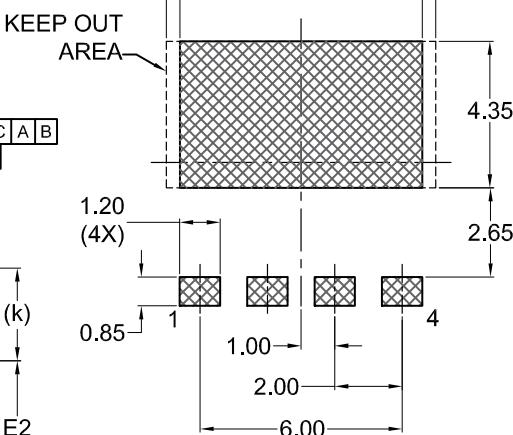
SEE DETAIL A



FRONT VIEW



BOTTOM VIEW



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20	REF	
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D2	7.10	7.20	7.30
D3	0.40	REF	
E	7.90	8.00	8.10
E2	4.25	4.35	4.45
E3	0.25	0.35	0.45
E4	0.40	REF	
e	2.00	BSC	
e/2	1.00	BSC	
e1	3.10	BSC	
e2	0.17	BSC	
k	2.75	REF	
L	0.40	0.50	0.60

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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