TEXAS INSTRUMENTS

TPS62050, TPS62051, TPS62052, TPS62054, TPS62056

SLVS432F – SEPTEMBER 2002 – REVISED JUNE 2015

TPS6205x 800-mA Synchronous Step-Down Converter

1 Features

- High-Efficiency Synchronous Step-Down Converter With up to 95% Efficiency
- 12-µA Quiescent Current (Typical)
- 2.7-V to 10-V Operating Input Voltage Range
- Adjustable Output Voltage Range: 0.7 V to 6 V
- Fixed Output Voltage Options Available With 1.5 V, 1.8 V, and 3.3 V
- Synchronizable to External Clock: Up to 1.2 MHz
- High-Efficiency Over a Wide Load Current Range in Power-Save Mode
- 100% Maximum Duty Cycle for Lowest Dropout
- Low-Noise Operation in Forced Fixed-Frequency PWM Operation Mode
- Internal Softstart
- Overtemperature and Overcurrent Protected
- Available in 10-Pin Micro-Small Outline Package MSOP

2 Applications

- Cellular Phones
- Organizers, PDAs, and Handheld PCs
- Low-Power DSP Supplies
- Digital Cameras and Hard Disks

3 Description

The TPS6205x devices are a family of high-efficiency synchronous step-down DC-DC converters that are ideally suited for systems powered from a 1- or 2-cell Li-Ion battery or from a 3- to 5-cell NiCd, NiMH, or alkaline battery.

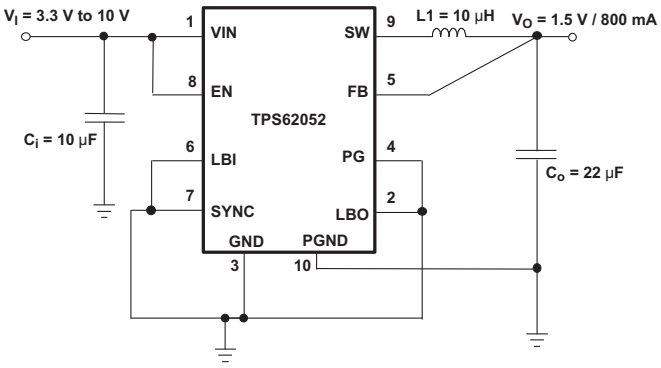
The TPS6205x devices are synchronous pulse width modulation (PWM) converters with integrated N- and P-channel power MOSFET switches. Synchronous rectification increases efficiency and reduces external component count. To achieve highest efficiency over a wide load current range, the converter enters a power-saving pulse frequency modulation (PFM) mode at light load currents. Operating frequency is typically 850 kHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 600 kHz to 1.2 MHz. For low noise operation, the converter can be programmed into forced-fixed frequency in PWM mode. In shutdown mode, the current consumption is reduced to less than 2 µA. The TPS6205x devices are available in the 10-pin (DGS) micro-small outline package (MSOP) and operates over a free air temperature range of –40°C to 85°C.

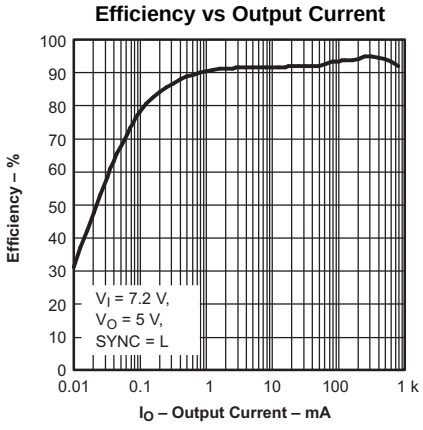
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62050	VSSOP (10)	3.00 mm × 3.00 mm
TPS62051		
TPS62052		
TPS62054		
TPS62056		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application Schematic





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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2011) to Revision F **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision D (October 2003) to Revision E **Page**

- Changed to Revision E, June 2011 ... 1
- Changed formatting. ... 1
- Changed "goes active high" to "floats" in Terminal Functions table, row PG, description. ... 3
- Changed "becomes active" to "floats" in last paragraph of Power Good Comparator section. ... 10

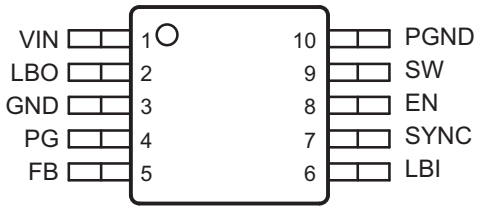
6 Device Comparison Table

PACKAGED DEVICES PLASTIC MSOP(1) (DGS)	OUTPUT VOLTAGE	LBI/LBO FUNCTIONALITY
TPS62050DGS	Adjustable 0.7 V to 6 V	Standard
TPS62051DGS	Adjustable 0.7 V to 6 V	Enhanced
TPS62052DGS	1.5 V	Standard
TPS62054DGS	1.8 V	Standard
TPS62056DGS	3.3 V	Standard

(1) The DGS packages are available taped and reeled. Add an R suffix to the device type (that is, TPS62050DGSR) to order quantities of 2500 devices per reel.

7 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	Enable. A logic high enables the converter, logic low forces the device into shutdown mode, reducing the supply current to less than 2 µA.
FB	5	I	Feedback pin for the fixed output voltage option. For the adjustable version, an external resistive divider is connected to this pin. The internal voltage divider is disabled for the adjustable version.
GND	3	I	Ground
LBI	6	I	Low battery input.
LBO	2	O	Open-drain low battery output. Logic low signal indicates a low battery voltage.
PG	4	O	Power good comparator output. This is an open-drain output. A pullup resistor must be connected between PG and VOUT. The output floats when the output voltage is greater than 95% of the nominal value.
PGND	10	I	Power ground. Connect all power grounds to this pin.
SW	9	O	Connect the inductor to this pin. This pin is the switch pin and connected to the drain of the internal power MOSFETS.
SYNC	7	I	Input for synchronization to the external clock signal. This input can be connected to an external clock or pulled to GND or V_I. When an external clock signal is applied, the device synchronizes to this external clock and the device operates in fixed PWM mode. When the pin is pulled to either GND or V_I, the internal oscillator is used and the logic level determines if the device operates in fixed PWM or PWM/PFM mode.
			SYNC = HIGH: Low-noise mode enabled, fixed-frequency PWM operation is forced.
			SYNC = LOW (GND): Power save mode enabled, PFM/PWM mode enabled.
VIN	1	I	Supply voltage input.

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
V_I	Supply voltage	–0.3	11	V
	Voltage at EN, SYNC	–0.3	V_I	V
	Voltage at LBI, FB, LBO, PG	–0.3	7	V
	Voltage at SW	–0.3	11(2)	V
I_O	Output current		850	mA
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	85	°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage at the SW pin is sampled in PFM mode 15 µs after the PMOS has switched off. During this time the voltage at SW is limited to 7 V maximum. Therefore, the output voltage of the converter is limited to 7 V maximum.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage at V_I	2.7		10	V
Voltage at PG, LBO			6	V
Maximum output current			800(1)	mA
Operating junction temperature	–40		125	°C

(1) Assuming no thermal limitation

8.4 Thermal Information

THERMAL METRIC(1)		TPS6205x DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

V_I = 7.2 V, V_O = 3.3 V, I_O = 300 mA, EN = V_I, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage			2.7		10	V
$I_{(Q)}$	Operating quiescent current		I_O = 0 mA, SYNC = GND, V_I = 7.2 V		12	20	µA
$I_{(SD)}$	Shutdown current		EN = GND		1.5	5	µA
			EN = GND, T_A = 25°C		1.5	3	
$I_{Q(LBI)}$	Quiescent current with enhanced LBI comparator version.		EN = V_I, LBI = GND, TPS62051 only		5		µA
ENABLE							
V_{IH}	EN high level input voltage			1.3			V
V_{IL}	EN low level input voltage					0.3	V
	EN trip point hysteresis				100		mV
I_{lkg}	EN input leakage current		EN = GND or VIN, V_I = 7.2 V		0.01	0.2	µA
$I_{(EN)}$	EN input current		0.6 V ≤ $V_{(EN)}$ ≤ 4 V		2		µA
$V_{(UVLO)}$	Undervoltage lockout threshold				1.6		V
POWER SWITCH							
$R_{DS(ON)}$	P-channel MOSFET ON-resistance		V_I ≥ 5.4 V; I_O = 300 mA		400	650	mΩ
			V_I = 2.7 V; I_O = 300 mA		600	850	
	P-channel MOSFET leakage current		V_{DS} = 10 V			1	µA
	P-channel MOSFET current limit		V_I = 7.2V, V_O = 3.3 V	1000	1200	1400	mA
$R_{DS(ON)}$	N-channel MOSFET ON-resistance		V_I ≥ 5.4 V; I_O = 300 mA		300	450	mΩ
			V_I = 2.7 V; I_O = 300 mA		450	550	
	N-channel MOSFET leakage current		V_{DS} = 6 V			1	µA
POWER GOOD OUTPUT, LBI, LBO							
$V_{(PG)}$	Power good trip voltage				Vml –2%		V
	Power good delay time		V_O ramping positive		50		µs
			V_O ramping negative		200		
V_{OL}	PG, LBO output low voltage		$V_{(FB)}$ = 0.8 × V_O nominal, $I_{(sink)}$ = 1 mA			0.3	V
	PG, LBO output leakage current		$V_{(FB)}$ = V_O nominal, $V_{(LBI)}$ = V_I		0.01	0.25	µA
	Minimum supply voltage for valid power good, LBO signal				2.3		V
$V_{(LBI)}$	Low-battery input trip voltage		Input voltage falling		1.21		V
	Low-battery input trip point accuracy					1.5%	
$V_{(LBI,HYS)}$	Low-battery input hysteresis				15		mV
$I_{lkg(LBI)}$	LBI leakage current				0.01	0.1	µA
OSCILLATOR							
f_S	Oscillator frequency			600	850	1000	kHz
$f_{(SYNC)}$	Synchronization range			600		1200	kHz
V_{IH}	SYNC high-level input voltage			1.5			V
V_{IL}	SYNC low-level input voltage					0.3	V
I_{lkg}	SYNC input leakage current		SYNC = GND or VIN		0.01	0.1	µA
	SYNC trip point hysteresis				100		mV
	Duty cycle of external clock signal			20%		90%	
OUTPUT							
V_O	Adjustable output voltage	TPS62050, TPS62051		0.7		6	V
$V_{(FB)}$	Feedback voltage	TPS62050, TPS62051			0.5		V
	FB leakage current	TPS62050, TPS62051			0.02	0.1	µA
	Feedback voltage tolerance	TPS62050, TPS62051	V_I = 2.7 V to 10 V, 0 mA < I_O < 600 mA	–3%		3%	

Electrical Characteristics (continued)

V_I = 7.2 V, V_O = 3.3 V, I_O = 300 mA, EN = V_I, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Fixed output voltage tolerance(1)	TPS62052	V_I = 2.7 V to 10 V, 0 mA < I_O < 600 mA	–3%		3%	
		TPS62054	V_I = 2.7 V to 10 V, 0 mA < I_O < 600 mA	–3%		3%	
		TPS62056	V_I = 3.75 V to 10 V, 0 mA < I_O < 600 mA	–3%		3%	
	Resistance of internal voltage divider for fixed-voltage versions			700	1000	1300	kΩ
	Line regulation		V_O = 3.3 V, V_I = 5 V to 10 V, I_O = 600 mA		5.2		mV/V
	Load regulation		V_I = 7.2 V; I_O = 10 mA to 600 mA		0.0045		%/mA
η	Efficiency		V_I = 5 V; V_O = 3.3 V; I_O = 300 mA		93%		
			V_I = 3.6 V; V_O = 2.5 V; I_O = 200 mA		93%		
	Duty cycle range for main switches					100%	
	Minimum t_{on} time for main switch				100		ns
	Shutdown temperature				145		°C
	Start-up time		I_O = 200 mA, V_I = 5 V, V_o = 3.3 V, C_o = 22 µF, L = 10 µH		1		ms

(1) The worst case $R_{DS(ON)}$ of the PMOS in 100% mode for an input voltage of 3.3 V is 0.75 Ω. This value can be used to determine the minimum input voltage if the output current is less than 600 mA with the TPS62056.

8.6 Typical Characteristics

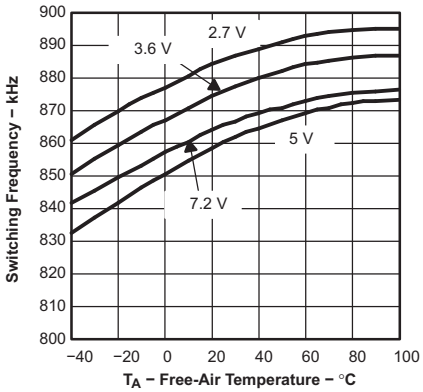


Figure 1. Switching Frequency vs Free-Air Temperature

9 Detailed Description

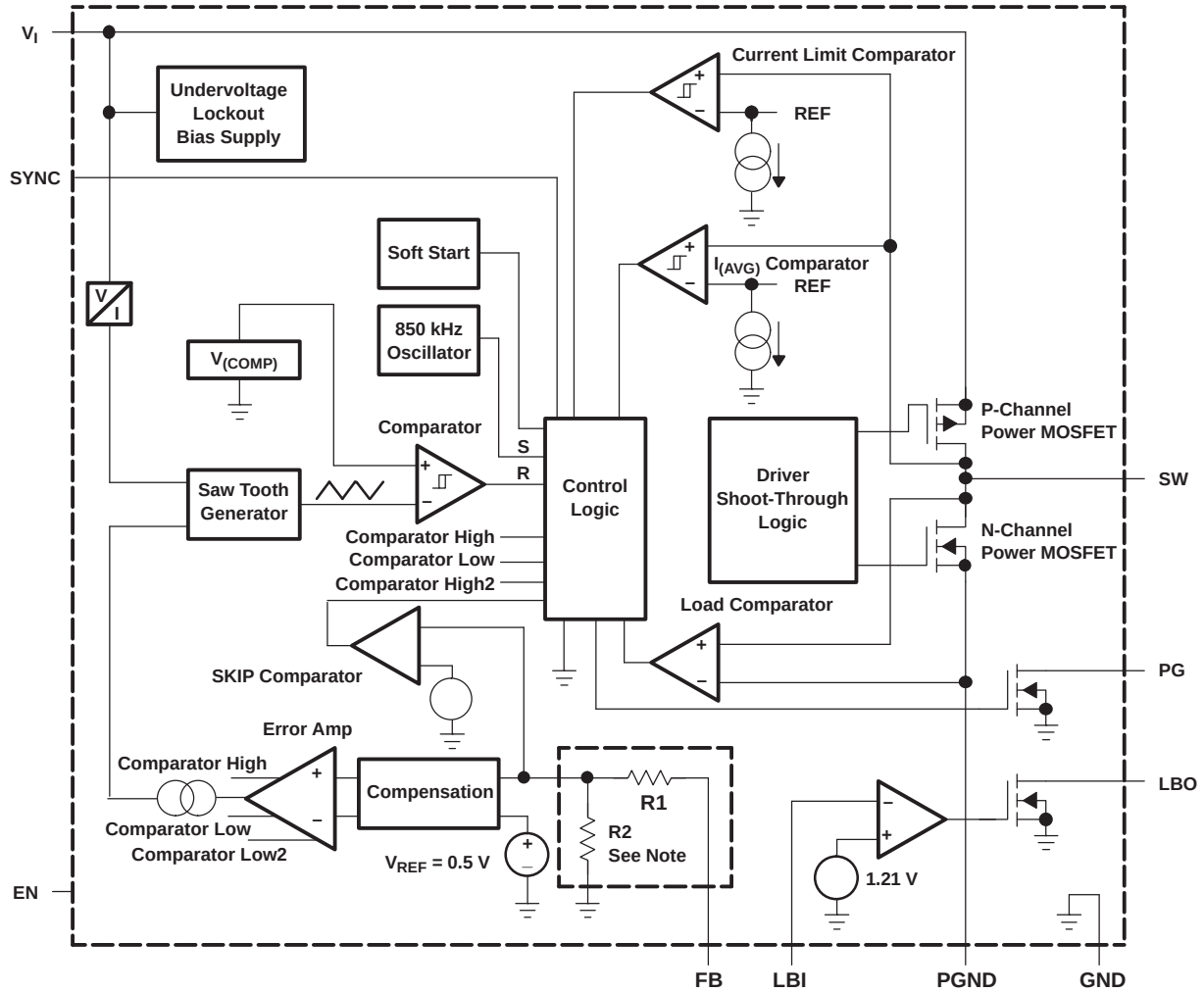
9.1 Overview

The TPS6205x family of devices are synchronous step-down converters that operate with a 850-kHz fixed-frequency pulse width modulation (PWM) at moderate to heavy load currents and enters the power save mode at light load current.

During PWM operation, the converter uses a unique fast response voltage mode control scheme with input voltage feed forward to achieve good line and load regulation with the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal (S), the P-channel MOSFET switch is turned on and the inductor current ramps up until the voltage comparator trips and the control logic turns the switch off. Also the switch is turned off by the current limit comparator if the current limit of the P-channel switch is exceeded. After the dead time preventing current shoot through, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again, turning off the N-channel rectifier and turning on the P-channel switch.

The error amplifier as well as the input voltage determines the rise time of the saw tooth generator; therefore, any change in input voltage or output voltage directly controls the duty cycle of the converter giving a very good line and load transient regulation.

9.2 Functional Block Diagram



NOTE: For the adjustable versions (TPS62050, TPS62051 devices), the internal feedback driver is disabled and the FB pin is directly connected to the GM amplifier.

9.3 Feature Description

9.3.1 Enable and Overtemperature Protection

A logic low on EN forces the TPS6205x devices into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 2 µA in the shutdown mode. When the device is in thermal shutdown, the bandgap is forced to stay on even if the device is set into shutdown by pulling EN to GND. As soon as the temperature drops below the threshold, the device automatically starts again.

If an output voltage is present when the device is disabled, which could be an external voltage source or super cap, the reverse leakage current is specified under *Electrical Characteristics*. Pulling the enable pin high starts up the TPS6205x devices with the soft-start as described in *Soft-Start*. If the EN pin is connected to any voltage other than V_I or GND, an increased leakage current of typically 10 µA and up to 20 µA can occur.

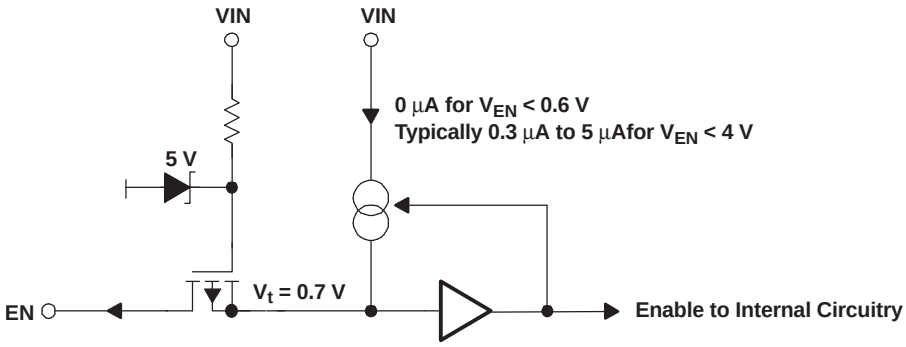


Figure 2. Internal Circuit of the ENABLE Pin

The EN pin can be used in a pushbutton configuration as shown in Figure 3. The external resistor to GND must be capable of sinking 0.3 µA with a minimum voltage drop of 1.3 V to keep the system enabled when both switches are open. When the ON-button is pressed, the device is enabled and the current through the external resistor keeps the voltage level high to ensure that the device stays on when the ON-button is released. When the OFF-button is pressed, the device is switched off and the current through the external resistor is zero. The device therefore stays off even when the OFF-button is released.

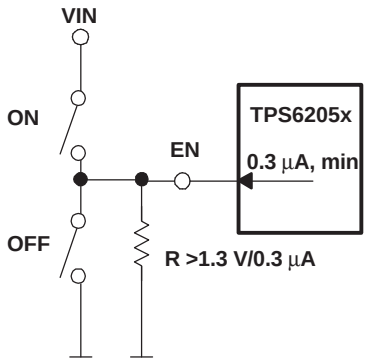


Figure 3. Pushbutton Configuration for the EN-Pin

9.3.2 Low-Battery Detector (Standard Version)

The low-battery output (LBO) is an open-drain type which goes low when the voltage at the low battery input (LBI) falls below the trip point of 1.21 V ±1.5%. The voltage at which the low-battery warning is issued is adjusted with a resistive divider as shown in Figure 5. TI recommends the sum of the resistors R1 and R2 to be in the 100-kΩ to 1-MΩ range for high-efficiency at low output current. An external pullup resistor at LBO can either be connected to OUT, or any other voltage rail in the voltage range of 0 V to 6 V. During start-up, the LBO output signal is invalid for the first 500 µs. LBO is high impedance when the device is disabled. If the low-battery comparator function is not used, connect LBI to ground. The low-battery detector is disabled when the device is disabled. Leave the LBO pin unconnected, or connect to GND when not used.

Feature Description (continued)

9.3.3 ENABLE / Low-Battery Detector (Enhanced Version) TPS62051 Only

The TPS62051 device offers an enhanced LBI functionality to provide a precise, user-programmable undervoltage shutdown. No additional supply voltage supervisor (SVS) is needed to provide this function.

When the enable (EN) pin is pulled high, only the internal bandgap voltage reference is switched on to provide a reference source for the LBI comparator. As long as the voltage at LBI is less than the LBI trip point, all other internal circuits are shut down, reducing the supply current to 5 µA. As soon as input voltage at LBI rises above the LBI trip point of 1.21 V, the device is completely enabled and starts switching.

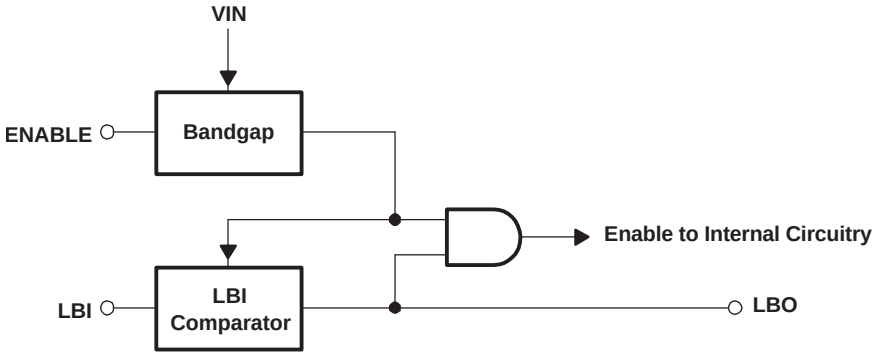


Figure 4. Block Diagram of ENABLE / LBI Functionality for TPS62051

The logic level of the LBO pin is not defined for the first 500 µs after EN is pulled high.

When the enhanced LBI is used to supervise the battery voltage and shut down the TPS62051 at low input voltages, the battery voltage rises again when the current drops to zero. The implemented hysteresis on the LBI pin may not be sufficient for all types of batteries. Figure 5 shows how an additional external hysteresis can be implemented.

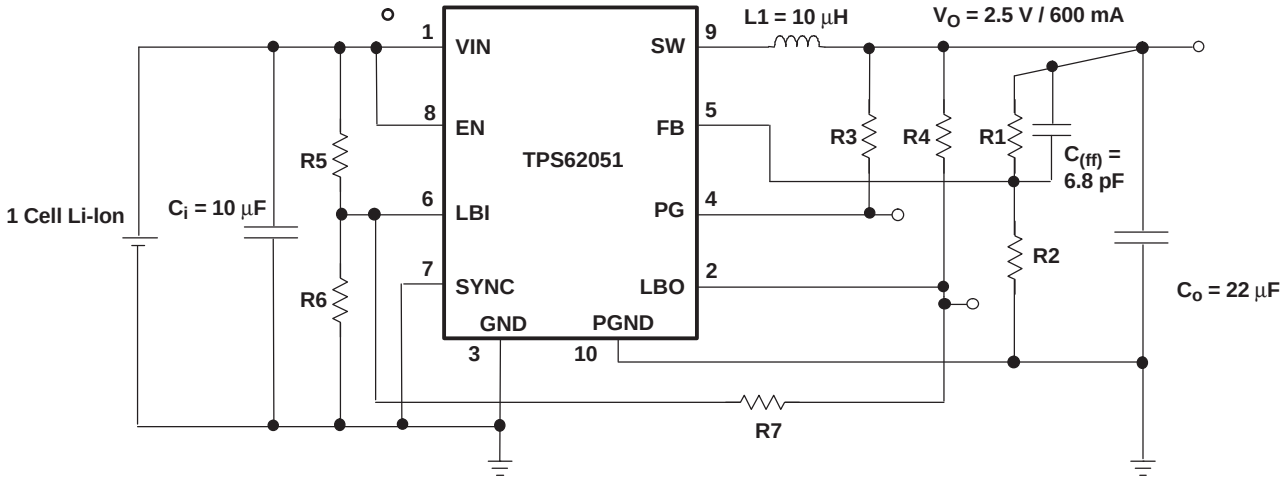


Figure 5. Enhanced LBI With Increased Hysteresis

A MATHCAD® file to calculate R7 can be downloaded from the product folder on the TI web.

9.3.4 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit prevents the device from misoperation at low input voltages. The circuit prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

Feature Description (continued)

9.3.5 Power Good Comparator

The power good (PG) comparator has an open-drain output capable of sinking typically 1 mA. The PG function is only active when the device is enabled (EN = high). When the device is disabled (EN = low), the PG pin is pulled to GND.

The PG output is only valid after a 250-µs delay after the device is enabled and the supply voltage is greater than 2.7 V. Power good is low during the first 250 µs after shutdown and in shutdown.

The PG pin floats high when the output voltage exceeds typically 98.5% of its nominal value. Leave the PG pin unconnected, or connect it to GND when not used.

9.3.6 Synchronization

If no clock signal is applied, the converter operates with a typical switching frequency of 850 kHz. It is possible to synchronize the converter to an external clock within a frequency range from 600 kHz to 1200 kHz. The device automatically detects the rising edge of the first clock and synchronizes to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation. The switchover is initiated if no rising edge on the SYNC pin is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 8.3 µs if the internal clock has its minimum frequency of 600 kHz. During this time, there is no clock signal available. The device stops switching until the internal circuitry is switched to the internal clock source.

When the device is switched between internal synchronization and external synchronization during operation, the output voltage may show transient overshoot or undershoot during switchover. The voltage transients are minimized by using 850 kHz as an initial external frequency, and changing the frequency slowly (>1 ms) to the value desired. The voltage drop at the output when the device is switched from external synchronization to internal synchronization can be reduced by increasing the output capacitor value.

If the device is synchronized to an external clock, the power-save mode is disabled and the device stays in forced PWM mode.

Connecting the SYNC pin to the GND pin enables the power-save mode. The converter operates in the PWM mode at moderate to heavy loads and in the PFM mode during light loads maintaining high-efficiency over a wide load current range.

9.4 Device Functional Modes

9.4.1 Soft-Start

The TPS6205x device have an internal soft-start circuit that limits the inrush current during start-up. This prevents possible voltage drops of the input voltage if a battery or a high impedance power source is connected to the input of the TPS6205x devices.

The soft-start is implemented as a digital circuit increasing the switch current in steps of 200 mA, 400 mA, 800 mA and then the typical switch current limit of 1.2 A. Therefore the start-up time mainly depends on the output capacitor and load current. Typical start-up time with a 22-µF output capacitor and a 200-mA load current is 1 ms.

9.4.2 Constant Frequency Mode Operation (SYNC = HIGH)

In the constant frequency mode, the output voltage is regulated by varying the duty cycle of the PWM signal in the range of 100% to 10%. Connecting the SYNC pin to a voltage greater than 1.5 V forces the converter to operate permanently in the PWM mode even at light or no load currents. The advantage is the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads (see Figure 7). The N-MOSFET of the devices stays on even when the current into the output drops to zero. This prevents the device from going into discontinuous mode. The device transfers unused energy back to the input. Therefore, there is no ringing at the output that usually occurs in the discontinuous mode. The duty cycle range in constant frequency mode is 100% to 10%.

Device Functional Modes (continued)

It is possible to switch from forced PWM mode to the power-save mode during operation by pulling the SYNC pin low. The flexible configuration of the SYNC pin during operation of the device allows efficient power management by adjusting the operation of the TPS6205x devices to the specific system requirements.

9.4.3 Power-Save Mode Operation (SYNC = LOW)

As the load current decreases, the converter enters the power-save mode operation. During power-save mode the converter operates with reduced switching frequency in PFM and with a minimum quiescent current to maintain high-efficiency. Whenever the average output current goes below the skip threshold, the converter enters the power-save mode. The average current depends on the input voltage. The current is 100 mA at low input voltages and up to 200 mA with maximum input voltage. The average output current must be less than the threshold for at least 32 clock cycles (t_{cy}) to enter the power-save mode. During the power save mode, the output voltage is monitored with a comparator. When the output voltage falls below the comparator low threshold set to 0.8% above V_O nominal, the P-channel switch turns on. The P-channel switch turns off as the peak switch current of typically 200 mA is reached. The N-channel rectifier turns on and the inductor current ramps down. As the inductor current approaches zero, the N-channel rectifier is turned off and the switch is turned on starting the next pulse. When the output voltage can not be reached with a single pulse, the device continues to switch with its normal operating frequency, until the comparator detects the output voltage to be 1.6% above the nominal output voltage. The converter wakes up again when the output voltage falls below the comparator low threshold. This control method reduces the quiescent current to typically to 12 µA and the switching frequency to a minimum achieving the highest converter efficiency. Having these skip current thresholds 0.8% and 1.6% above the nominal output voltage gives a lower absolute voltage drop during a load transient as anticipated with a standard converter operating in this mode.

9.4.4 100% Duty Cycle Low Dropout Operation

The TPS6205x devices offer the lowest possible input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode, the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated using Equation 1.

$$V_I(\min) = V_O(\max) + I_O(\max) \times \left(R_{DS(ON)}(\max) + R_L\right) \quad (1)$$

I_O (max) = Maximum output current plus inductor ripple current

$R_{DS(ON)}$(max) = Maximum P-Channel switch resistance

R_L = DC resistance of the inductor

V_O(max) = Nominal output voltage plus maximum output voltage tolerance

9.4.5 No Load Operation

If the converter operates in the forced PWM mode and there is no load connected to the output, the converter regulates the output voltage by allowing the inductor current to reverse for a short period of time.

10 Application and Implementation

NOTE

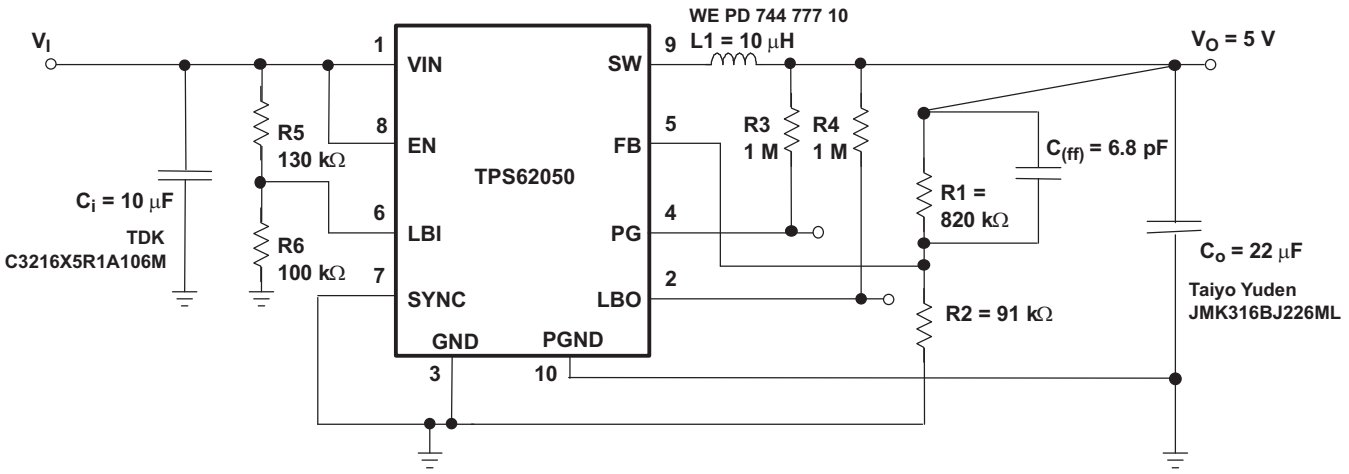
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6205x family of devices are high-efficiency synchronous step-down DC-DC converters ideally suited for systems powered from a 1-cell or 2-cell Li-Ion battery or from a 3-cell to 5-cell NiCd, NiMH, or alkaline battery.

10.2 Typical Applications

10.2.1 Standard Circuit for Adjustable Version



Quiescent Current Measurements and Efficiency Were Taken
With: R5 = Open, R4 = Open, LBI Connected to GND.

Figure 6. Standard Circuit for Adjustable Version

10.2.1.1 Design Requirements

The design guidelines provide a component selection to operate the adjustable device within the *Recommended Operating Conditions*.

Table 1. Bill of Materials for Adjustable Version

REFERENCE	PART NUMBER	VALUE	MANUFACTURER
Ci	C3216X5R1A106M	10 µF	TDK
Co	JMK316BJ226ML	22 µF	Taiyo Yuden
L1	WE PD 74477710	10 µH	Wurth
IC1	TPS62050	-	Texas Instruments
R1	generic metal film resistor; tolerance 1%	820 kΩ (depending on desired output voltage)	—
R2	generic metal film resistor; tolerance 1%	91 kΩ (depending on desired output voltage)	—
R3, R4	generic metal film resistor; tolerance 1%	1 MΩ	—
R5	generic metal film resistor; tolerance 1%	130 kΩ	—

Typical Applications (continued)

Table 1. Bill of Materials for Adjustable Version (continued)

REFERENCE	PART NUMBER	VALUE	MANUFACTURER
R6	generic metal film resistor; tolerance 1%	100 kΩ	—
C(ff)	generic ceramic capacitor; COG	6.8 pF	—

10.2.1.2 Detailed Design Procedure

All graphs have been generated using the circuit as shown unless otherwise noted. For output voltages other than 5 V, the fixed-voltage versions were used. The resistors R1, R2, and the feed forward capacitor (C_{ff}) are removed and the feedback pin is directly connected to the output.

$$V_O = V_{FB} \times \frac{R1 + R2}{R2} \qquad R1 = R2 \times \left(\frac{V_O}{V_{FB}}\right) - R2 \qquad V_{FB} = 0.5V \tag{2}$$

Table 2. Values for Resistor Combinations and Feedback Capacitors

NOMINAL OUTPUT VOLTAGE	EQUATION	POSSIBLE RESISTOR COMBINATION	TYPICAL FEEDBACK CAPACITOR
0.7 V	R1 = 0.4 × R2	R1 = 270 k, R2 = 680 k	$C_{(ff)}$ = 22 pF
1.2 V	R1 = 1.4 × R2	R1 = 510 k, R2 = 360 k (1.21 V)	$C_{(ff)}$ = 6.8 pF
1.5 V	R1 = 2 × R2	R1 = 300 k, R2 = 150 k (1.5 V)	$C_{(ff)}$ = 6.8 pF
1.8 V	R1 = 2.6 × R2	R1 = 390 k, R2 = 150 k (1.80 V)	$C_{(ff)}$ = 6.8 pF
2.5 V	R1 = 4 × R2	R1 = 680 k, R2 = 169 k (2.51 V)	$C_{(ff)}$ = 6.8 pF
3.3 V	R1 = 5.6 × R2	R1 = 560 k, R2 = 100 k (3.3 V)	$C_{(ff)}$ = 6.8 pF
5 V	R1 = 9 × R2	R1 = 820 k, R2 = 91 k (5 V)	$C_{(ff)}$ = 6.8 pF

10.2.1.2.1 Inductor Selection

A 10-µH minimum inductor must be used with the TPS6205x family of devices. Values larger than 22 µH or smaller than 10 µH may cause stability problems due to the internal compensation of the regulator. After choosing the inductor value of typically 10 µH, two additional inductor parameters must be considered: the current rating of the inductor and the DC resistance. The DC resistance of the inductance directly influences the efficiency of the converter. Therefore, an inductor with lowest DC resistance must be selected for highest efficiency. To avoid saturation of the inductor, the inductor must be rated at least for the maximum output current plus half the inductor ripple current which is calculated using Equation 3.

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_L(max) = I_O(max) + \frac{\Delta IL}{2} \tag{3}$$

f = Switching frequency (850 kHz typical)
L = Inductor value
ΔIL = Peak-to-peak inductor ripple current
I_L(max) = Maximum inductor current

The highest inductor current occurs at maximum VIN . A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS6205x device, which is 1.4 A maximum. See Table 3 for inductors that have been tested for operation with the TPS6205x devices.

Table 3. Inductors

MANUFACTURER	TYPE	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
TDK	SLF7032T-100M1R4 SLF7032T-220M96 SLF7045T-100M1R3 SLF7045T-100MR90	10 µH ±20% 22 µH ±20% 10 µH ±20% 22 µH ±20%	53 mΩ ±20% 110 mΩ ±20% 36 mΩ ±20% 61 mΩ ±20%	1.4 A 0.96 A 1.3 A 0.9 A

Table 3. Inductors (continued)

MANUFACTURER	TYPE	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
Sumida	CDR74B	10 µH	70 mΩ	1.65 A
	CDR74B	22 µH	130 mΩ	1.12 A
	CDH74	10 µH	49 mΩ	1.8 A
	CDH74	22 µH	110 mΩ	1.23 A
	CDR63B	10 µH	140 mΩ	1 A
	CDRH4D28	10 µH	128 mΩ	1 A
	CDRH5D28	10 µH	48 mΩ	1.3 A
	CDRH5D18	10 µH	92 mΩ	1.2 A
Coilcraft	DT3316P-153	15 µH	60 mΩ	1.8 A
	DT3316P-223	22 µH	84 mΩ	1.5 A
Wuerth	WE-PD 744 778 10	10 µH	72 mΩ	1.68 A
	WE-PD 744 777 10	10 µH	49 mΩ	1.84 A
	WE-PD 744 778 122	22 µH	190 mΩ	1.07A
	WE-PD 744 777 122	22 µH	110 mΩ	1.23 A

10.2.1.2.2 Output Capacitor Selection

The output capacitor must have a minimum value of 22 µF. For best performance, a low ESR ceramic output capacitor is needed.

For completeness, use Equation 4 to calculate the RMS ripple current.

$$I_{RMS(Co)} = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charge and discharging the output capacitor, as shown in Equation 5.

$$\Delta V_O = V_O \times \frac{1-\frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + R_{ESR} \right) \quad (5)$$

The highest output voltage ripple occurs at the highest input voltage V_I.

10.2.1.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The input capacitor must have a minimum value of 10 µF and can be increased without any limit for better input voltage filtering. The input capacitor must be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_O(max) \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I}\right)} \quad (6)$$

The worst-case RMS ripple current occurs at D = 0.5 and is calculated as: $I_{RMS} = I_O/2$. Ceramic capacitors have a good performance because of their low ESR value and they are less sensitive to voltage transients compared to tantalum capacitors. Place the input capacitor as close as possible to the input pin of the IC for best performance.

Table 4. Capacitors

MANUFACTURER	PART NUMBER	SIZE	VOLTAGE	CAPACITANCE	TYPE
Taiyo Yuden	JMK212BJ106MG	0805	6.3 V	10 µF	Ceramic
	JMK316BJ106ML	1206	6.3 V	10 µF	Ceramic
	JMK316BJ226ML	1206	6.3 V	22 µF	Ceramic
	LMK316BJ475ML	1206	10 V	4.7 µF(1)	Ceramic
	EMK316BJ475ML	1206	16 V	4.7 µF(1)	Ceramic
	EMK325BJ106KN-T	1210	16 V	10 µF	Ceramic
Kemet	C1206C106M9PAC	1206	6.3 V	10 µF	Ceramic
TDK	C2012X5R0J106M	0805	6.3 V	10 µF	Ceramic
	C3216X5R0J226M	1206	6.3 V	22 µF	Ceramic
	C3216X5R1A106M	1206	10 V	10 µF	Ceramic

(1) Connect two in parallel.

10.2.1.2.4 Feedforward Capacitor

The feedforward capacitor ($C_{(ff)}$ shown in Figure 5) improves the performance in SKIP mode. The comparator is faster; therefore, there is less voltage ripple at the output in SKIP mode. Use the values listed in Table 2. Larger values decrease stability in fixed frequency PWM mode. If the TPS6205x devices are only operated in fixed frequency PWM mode, the feedforward capacitor is not needed.

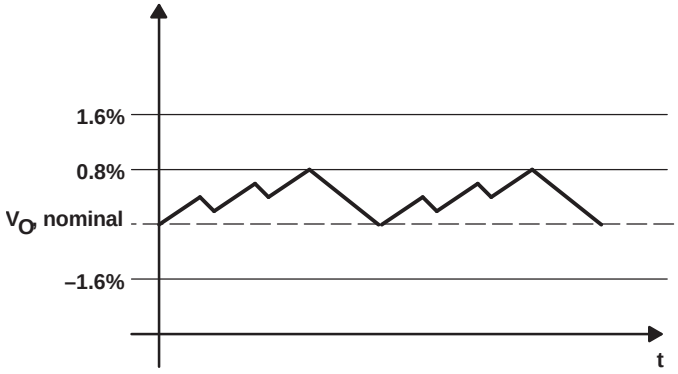


Figure 7. Power-Save Mode Output Voltage Thresholds

The converter enters the fixed frequency PWM mode again as soon as the output voltage falls below the comparator low 2 threshold set to 1.6% below V_O, nominal.

10.2.1.3 Application Curves

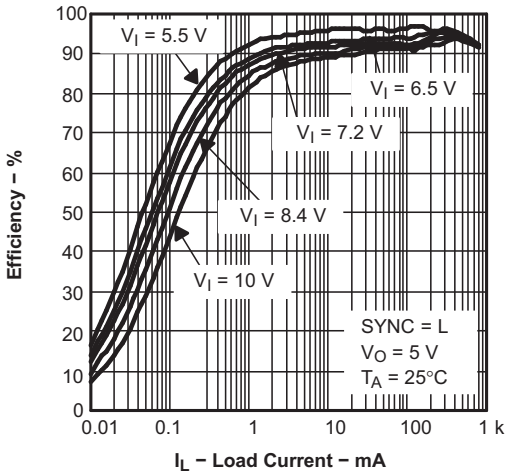


Figure 8. TPS62050 Efficiency vs Load Current

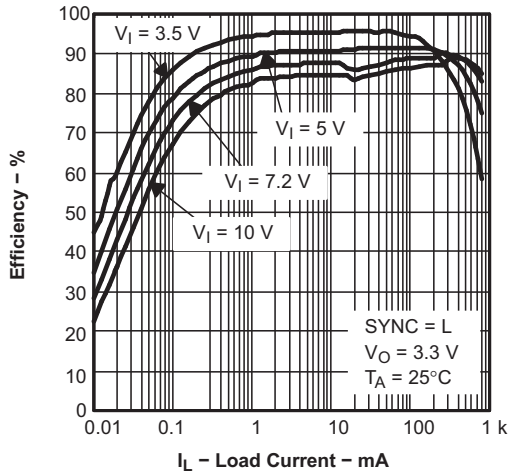


Figure 9. TPS62056 Efficiency vs Load Current

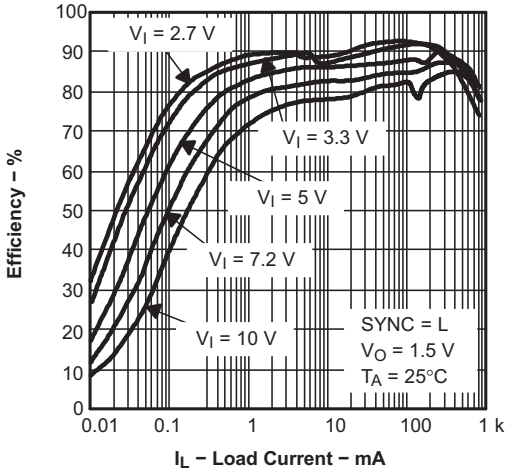


Figure 10. TPS62052 Efficiency vs Load Current

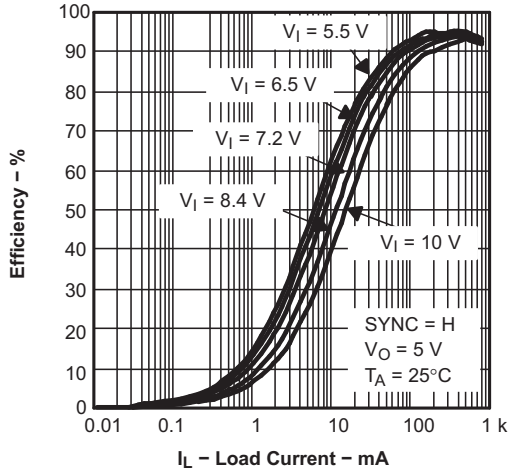


Figure 11. TPS62050 Efficiency vs Load Current

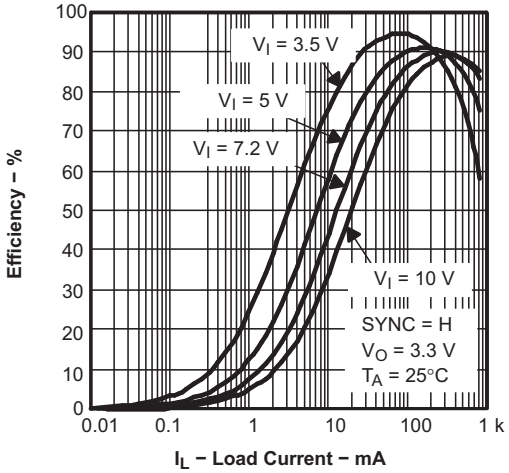


Figure 12. TPS62056 Efficiency vs Load Current

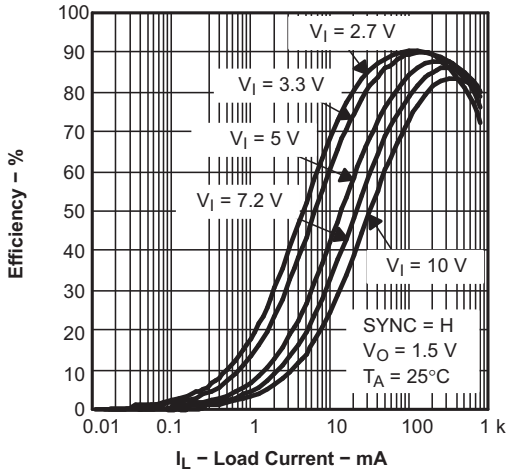


Figure 13. TPS62052 Efficiency vs Load Current

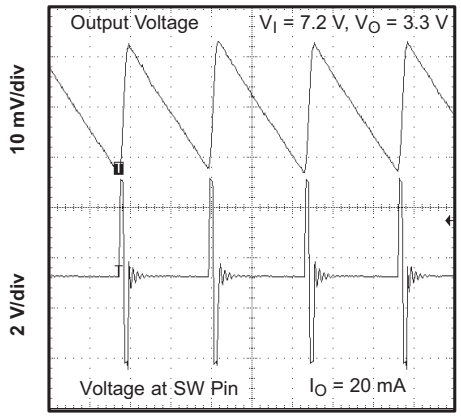


Figure 14. Output Voltage Ripple in Skip Mode

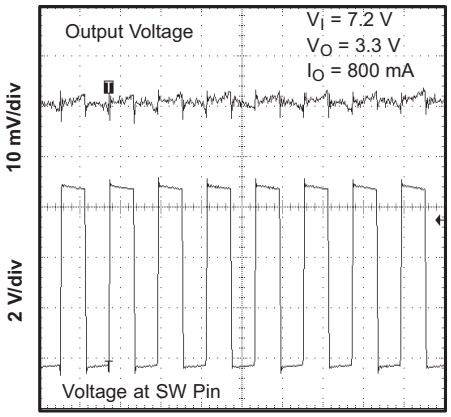


Figure 15. Output Voltage Ripple in PWM Mode

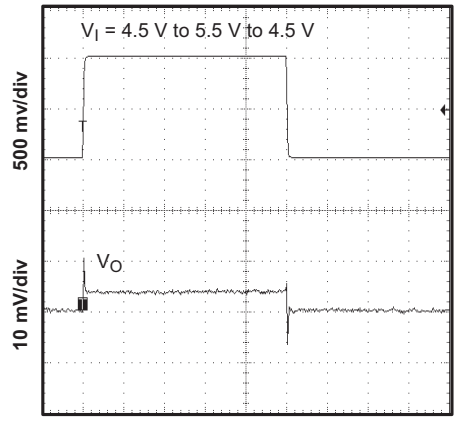


Figure 16. Line Transient Response in PWM Mode

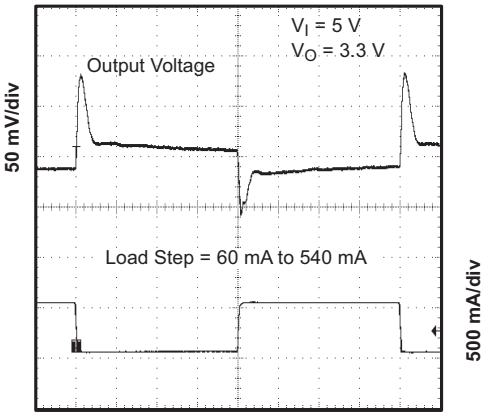


Figure 17. Load Transient Response

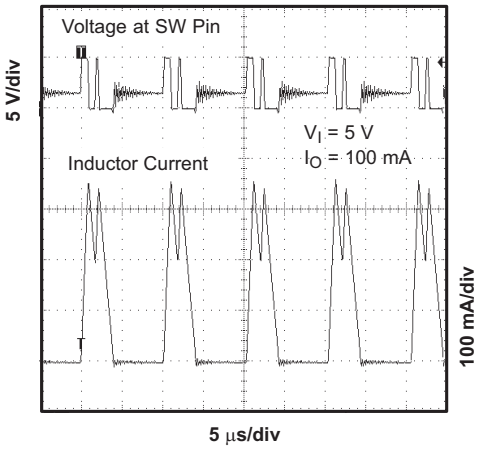


Figure 18. $V_{(SWITCH)}$ and I_L (Inductor Current) in Skip Mode

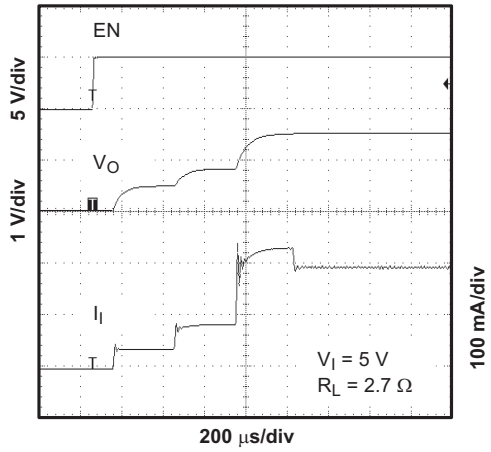


Figure 19. Start-up Timing

10.2.2 Standard Circuit for Fixed Voltage Version

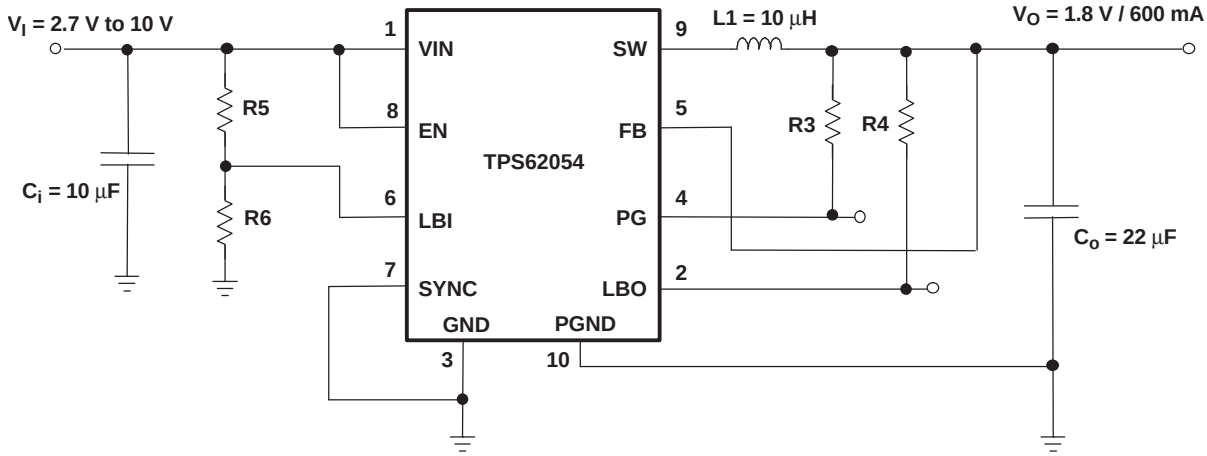


Figure 20. Standard Circuit for Fixed Voltage Version

10.2.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the *Recommended Operating Conditions*.

Table 5. Bill of Materials for Fixed Voltage Versions

REFERENCE	PART NUMBER	VALUE	MANUFACTURER
Ci	C3216X5R1A106M	10 µF	TDK
Co	JMK316BJ226ML	22 µF	Taiyo Yuden
L1	WE PD 74477710	10 µH	Wurth
IC1	TPS62054	—	Texas Instruments
R3, R4	generic metal film resistor; tolerance 1%	1 MΩ	—
R5	generic metal film resistor; tolerance 1%	130 kΩ	—
R6	generic metal film resistor; tolerance 1%	100 kΩ	—

10.2.2.2 Detailed Design Procedure

Connect the feedback pin (FB) to the pad of the output capacitor. The pullup resistors for pins PG and LBO are typically chosen as 100 kΩ each. The input capacitor must be placed as close to the VIN pin as possible.

10.2.2.3 Application Curves

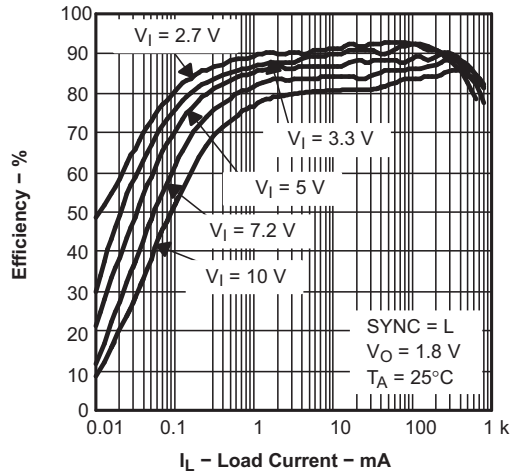


Figure 21. TPS62054 Efficiency vs Load Current in PFM Mode

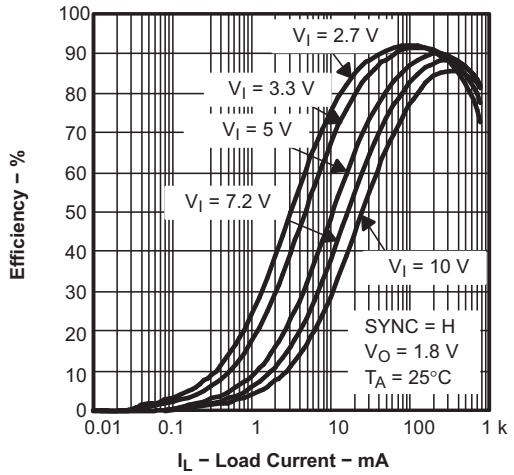


Figure 22. TPS62054 Efficiency vs Load Current in PWM Mode

10.3 System Examples

The TPS62050 device is used to generate an output voltage of 0.7 V. With such low output voltages, the inductor discharges very slowly. This leads to a high-output voltage ripple in power-save mode (SYNC = GND). Therefore, TI recommends using a larger output capacitor to keep the output ripple low. With an output capacitor of 47 µF, the output voltage ripple is less than 40 mV_{PP}.

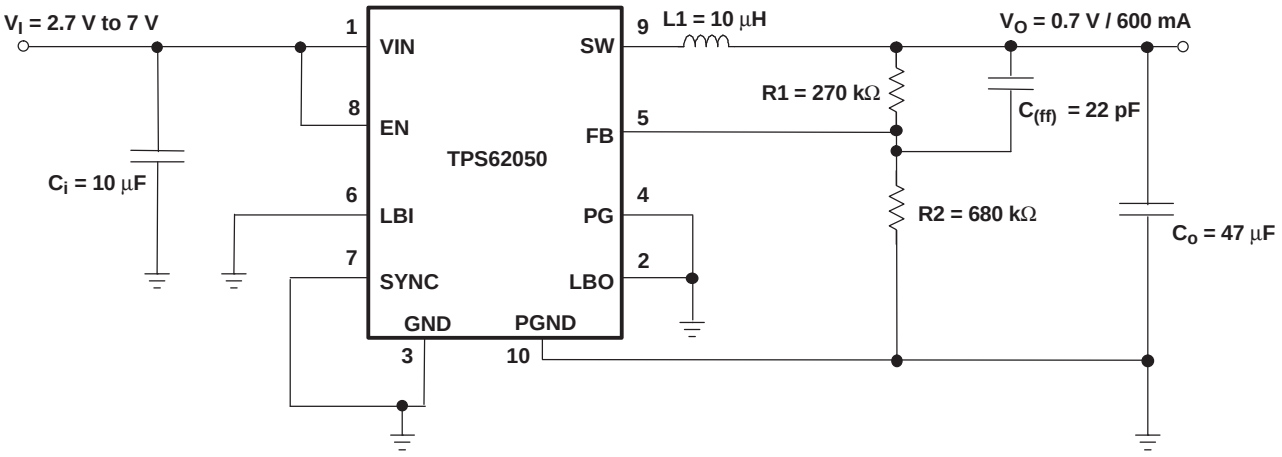


Figure 23. Converter for 0.7-V Output Voltage

11 Power Supply Recommendations

The TPS6205x family of devices has no special requirements for its power supply. The output current of the power supply must be rated according to the supply voltage, output voltage, and output current of the TPS6205x devices.

12 Layout

12.1 Layout Guidelines

All capacitors must be soldered as close as possible to the IC.

For information on the PCB layout, see the user's guide, SLVU081.

Keep the feedback track as short as possible. Any coupling to the FB pin may cause additional output voltage ripple. The feedback connection from the output capacitor C4 to R1 of the feedback network is made directly from the pad of C4 as shown by the via. The connection of GND with PGND is done similarly directly at the PGND pad of C4. Uncritical signals like the connections for LBI, LBO, and PG are not shown for better readability.

12.2 Layout Example

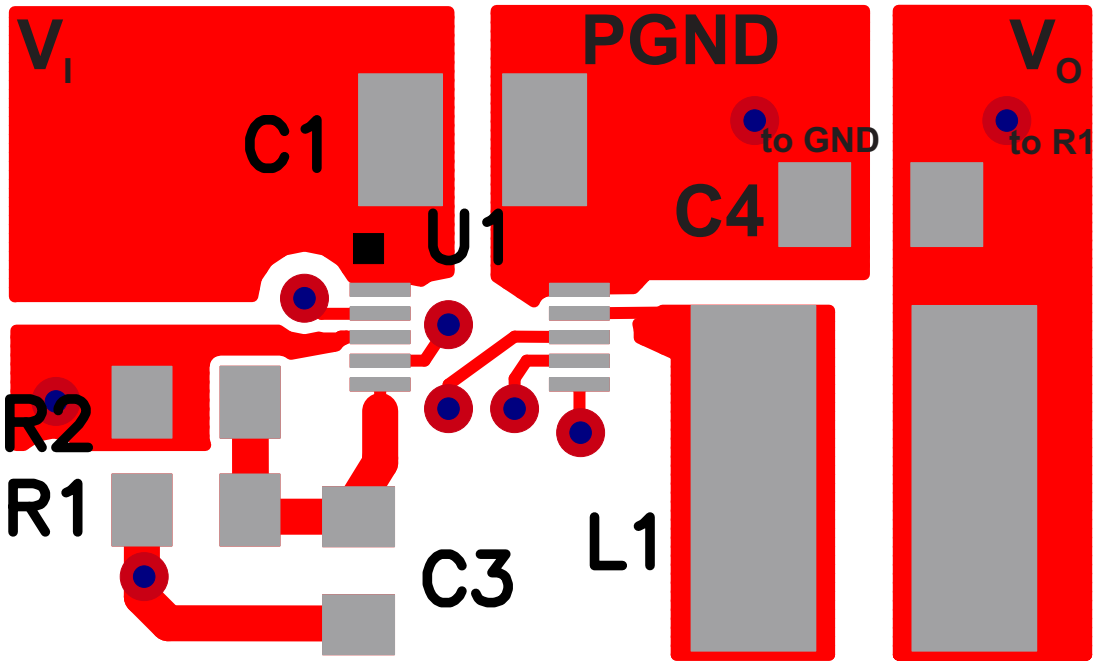


Figure 24. Layout

Layout Example (continued)

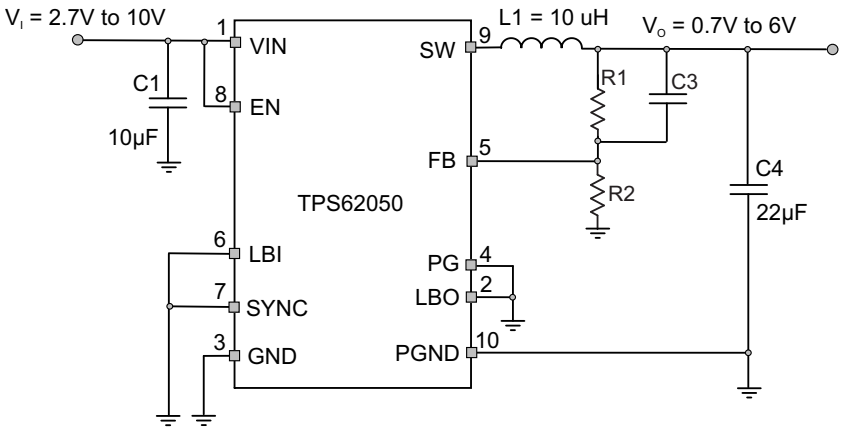


Figure 25. Associated Layout Schematic

13 Device and Documentation Support

13.1 Device Support

TPS6205xEVM User's Guide, SLVU081

13.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

13.2 Related Links

Table 6 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62050	Click here	Click here	Click here	Click here	Click here
TPS62051	Click here	Click here	Click here	Click here	Click here
TPS62052	Click here	Click here	Click here	Click here	Click here
TPS62054	Click here	Click here	Click here	Click here	Click here
TPS62056	Click here	Click here	Click here	Click here	Click here

13.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
MATHCAD is a registered trademark of Mathsoft Incorporated.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62050DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BFM	Samples
TPS62050DGSG4	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BFM	Samples
TPS62050DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BFM	Samples
TPS62050DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BFM	Samples
TPS62051DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BGB	Samples
TPS62051DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BGB	Samples
TPS62051DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BGB	Samples
TPS62052DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BGC	Samples
TPS62052DGSG4	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BGC	Samples
TPS62052DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BGC	Samples
TPS62054DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BGE	Samples
TPS62054DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BGE	Samples
TPS62056DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BGG	Samples
TPS62056DGSG4	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BGG	Samples
TPS62056DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	BGG	Samples
TPS62056DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BGG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

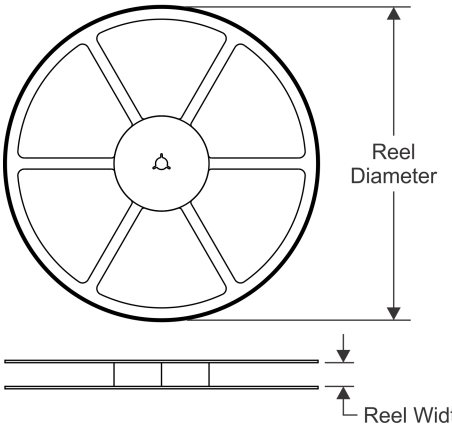
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

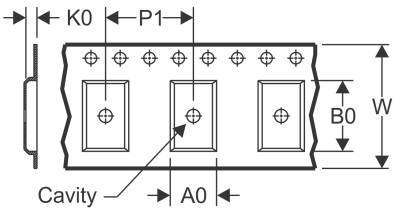
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

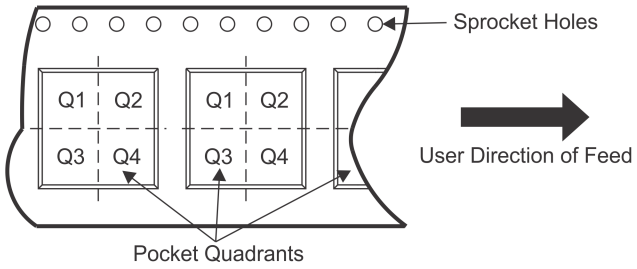


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

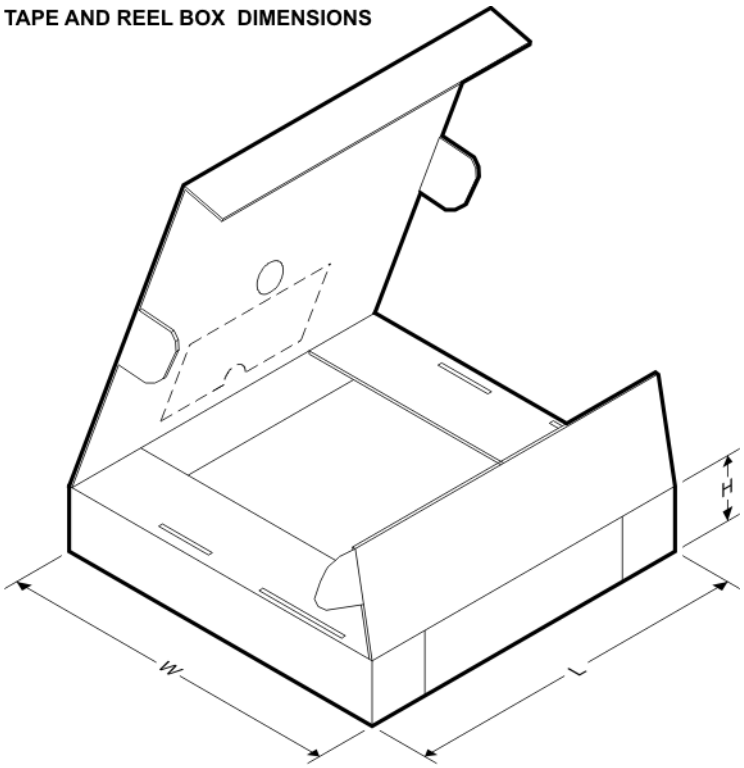
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62050DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62051DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62052DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62054DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62054DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62056DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

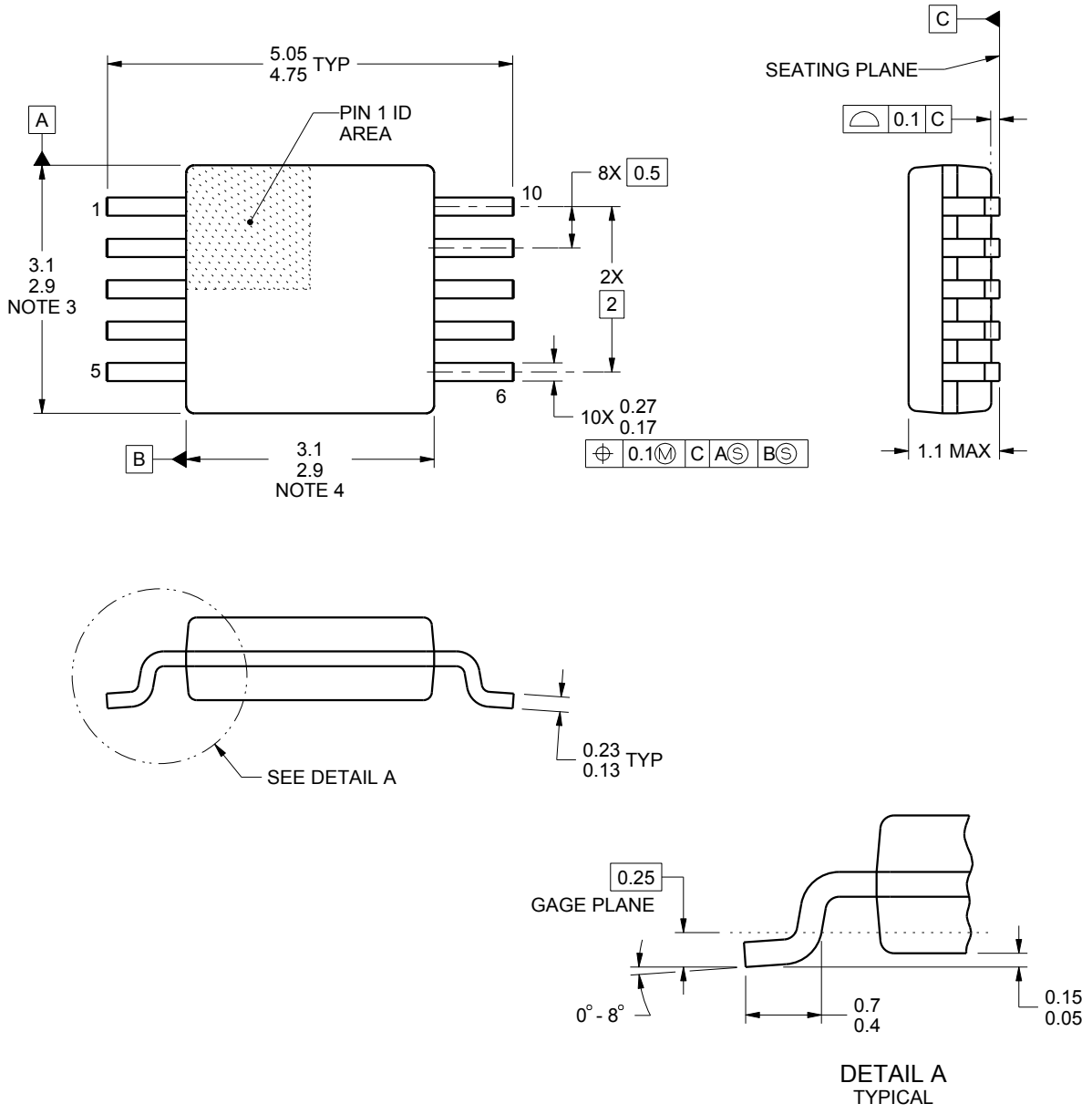
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62050DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62051DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62052DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62054DGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TPS62054DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62056DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

PACKAGE OUTLINE

DGS0010A

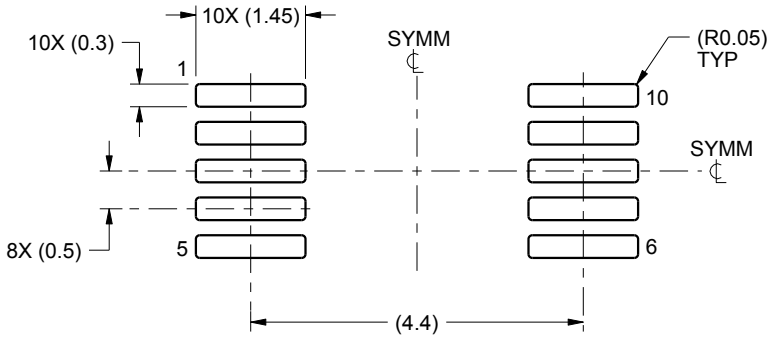
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

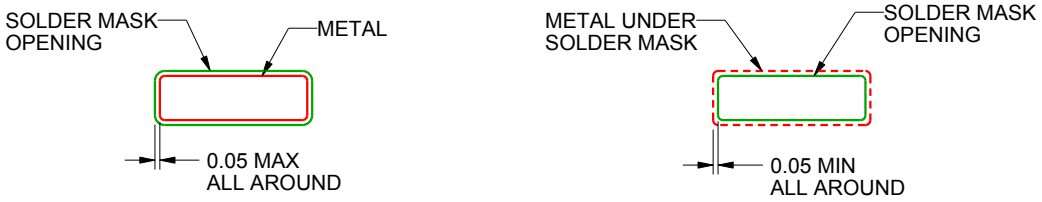


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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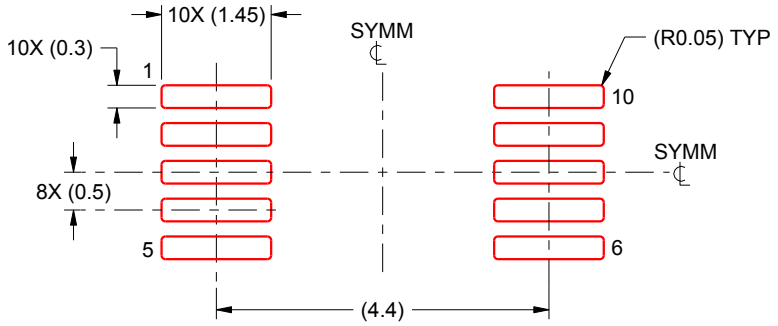
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265