PESD5V0X1BL-N

ESD Protection Diode

»Features

- 120Watts peak pulse power (tp = 8/20μs)
- Tiny DFN1006 package
- Bidirectional configurations
- Solid-state silicon-avalanche technology
- Low clamping voltage
- Low leakage current
- Low capacitance (Cj=0.7pF typ.)
- Protection one data/power line
- IEC 61000-4-2 ±30V contact ±30kV air
- 1.2/50μs 12ohm 2kV (GbE PHY side)
- 10/700μs 40ohm 4kV (GbE PHY side)

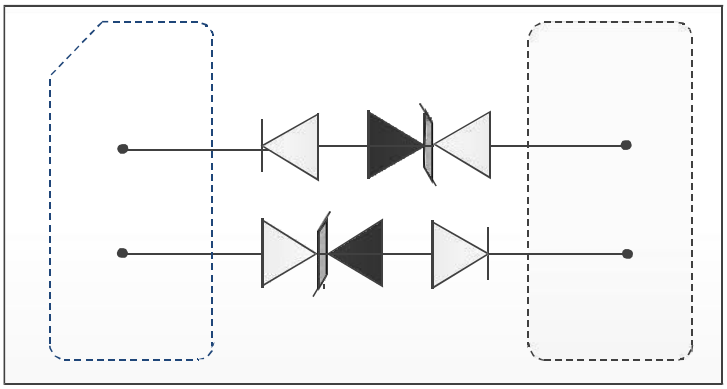
»Applications

- 10/100/1000Ethernet
- Intergated Magnetics/RJ45Connectors
- LAN/WAN Equipment
- Notebooks, Desktops, and Servers
- Portable Instrumentation

»Mechanical Data

- DFN1006 package
- Molding compound flammability rating: UL 94V-0
- Packaging: Tape and Reel
- RoHS/WEEE Compliant

»Schematic & PINConfiguration



DFN1006

»Absolute Maximum Rating

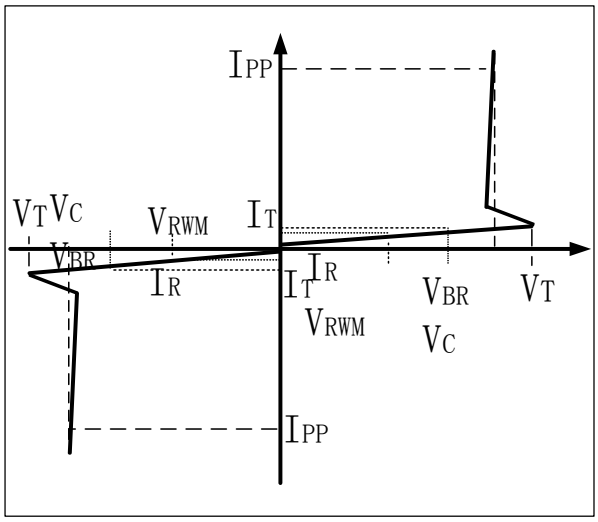
Rating	Symbol	Value	Units
Peak Pulse Power (t_p =8/20μs)	P_{PP}	120	Watts
Peak Pulse Current (t_p =8/20μs)(note1)	I_{pp}	7	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2(Contact)	V_{ESD}	30 30	kV
Lead Soldering Temperature	T_L	260(10seconds)	℃
Junction Temperature	T_J	-55 to +125	℃
Storage Temperature	T_{stg}	-55 to +125	℃

»Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Trigger Voltage	V_T	I_T=1mA	7.5	8.4		V
Reverse Leakage Current	I_R	V_{RWM}=5V,T=25℃		20	100	nA
Peak Pulse Current	I_{PP}	tp=8/20μs			7	A
Clamping Voltage	V_C	I_{PP}=7A,t_p=8/20μs		16	20	V
Junction Capacitance	C_j	V_R = 0V, f=1MHz		0.7	0.8	pF

»Electrical Parameters (TA = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_T	Trigger Voltage @ I_T
I_T	Test Current



Note:. 8/20μs pulse waveform.

»Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

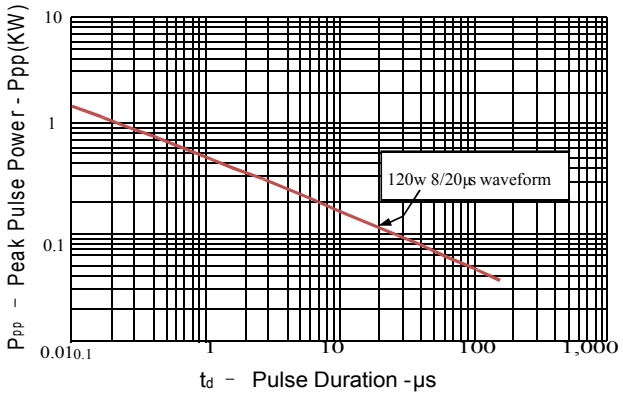


Figure 2: Power Derating Curve

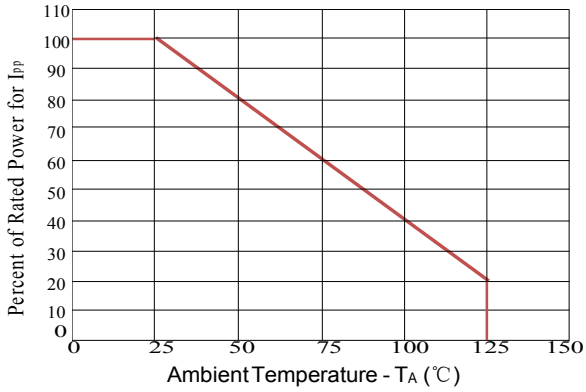


Figure3: Pulse Waveform

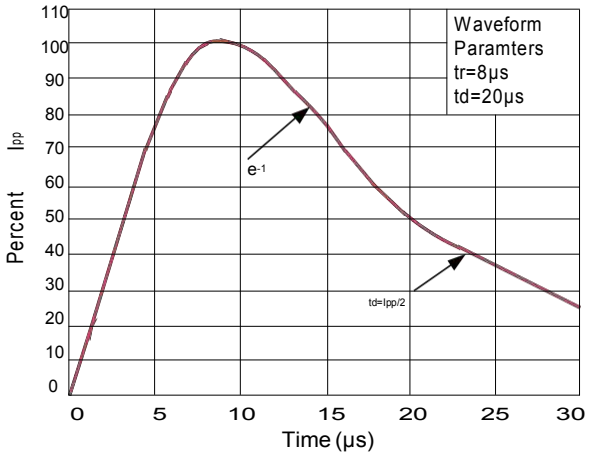
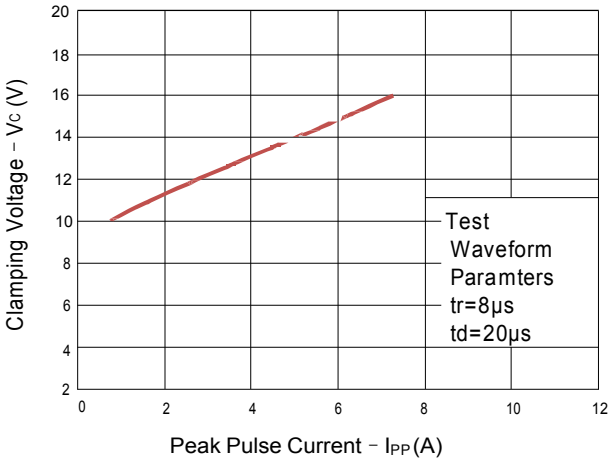


Figure 4: Clamping Voltage vs.Ipp



»Lightning Surge Test Results for Gigabit Ethernet

During the metallic (line-to-line) surge test, the line being stressed is tied to the surge generator with the remaining lines tied together and connected to the generator ground. Current will flow through the line transformer transferring energy to the PHY side of the transformer. Figure 5 shows the test set-up for measuring the clamping voltage of the device.This set up is designed to test the surge in an actual gigabit Ethernet (GbE) circuit. Two 4.7 Ohm resistors is usedfor decoupling. The clamping voltage of the PESD5V0X1BL-N for a metallic mode 4000V (10/ 700μs) surge.The clamping voltage, measured at less than 13 volts, provides sufficient clamping margin to minimize electrical stress and is well below the failure voltage range of typical GbE PHY chips .

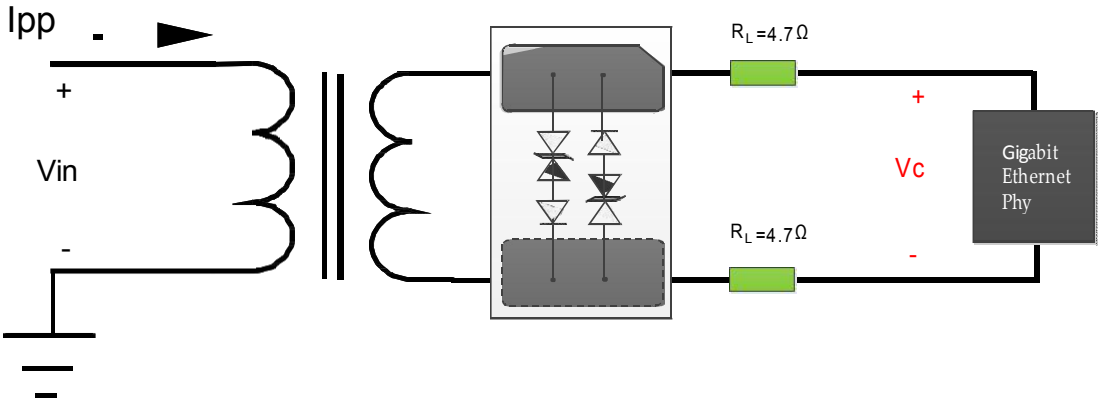


Figure5-Clamping Voltage Test Set-Up

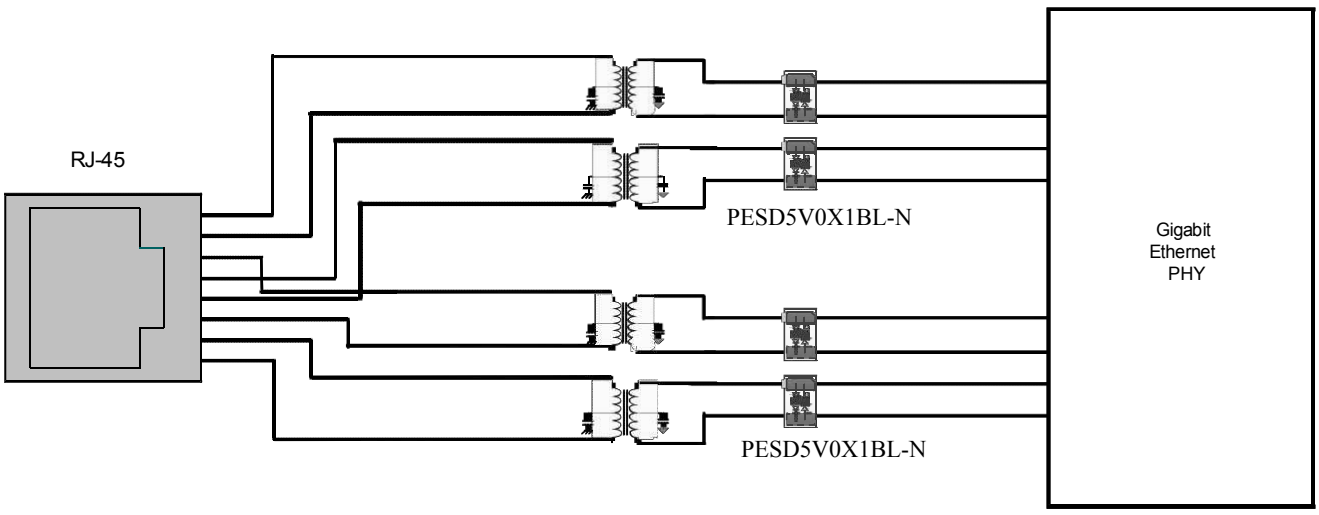
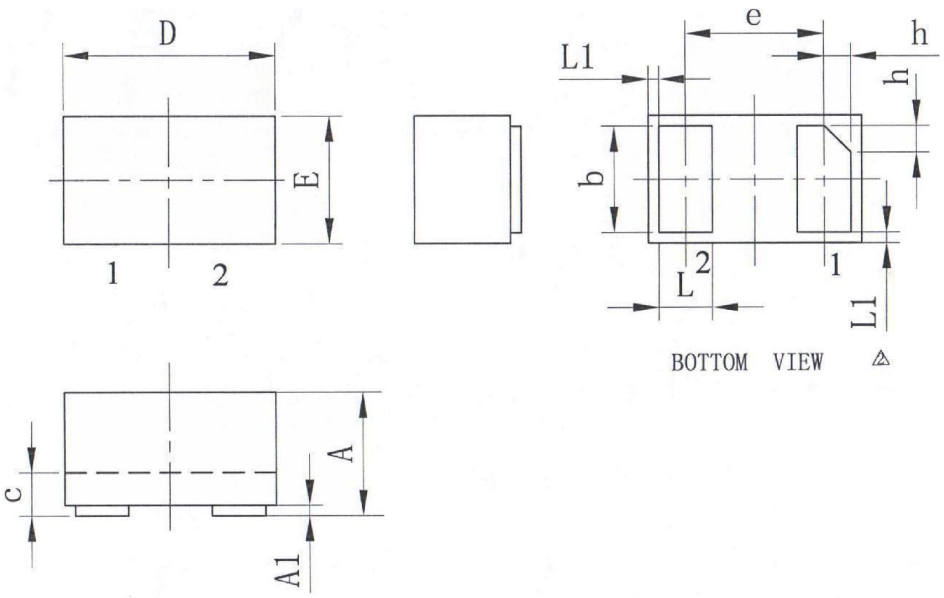


Figure 6 - GbE Protection to Lightning, ESD, and CDE

»Outline Drawing –DFN1006



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.45	0.50	0.55
c	0.12	0.15	0.18
D	0.95	1.00	1.05
e	0.65BSC		
E	0.55	0.60	0.65
L	0.20	0.25	0.30
L1	0.05REF		
h	0.07	0.12	0.17
载体尺寸 (Mil)	20*20		

Marking

Ordering information

Ordercode	Package	Base qty	Delivery mode
PESD5V0X1BL-N	DFN1006	10k	Tape and reel