

1. Electrical Specification

1-1 Test condition

| | |
|--|---|
| Varistor voltage | $I_n = 1 \text{ mA DC}$ |
| Leakage current | $V_{dc} = 24 \text{ V DC}$ |
| Maximum clamping voltage | $I_c = 1 \text{ A}$ |
| Rated peak single pulse transient current | 8 / 20 μs waveform, +/- each 1 time induce |
| Capacitance | 10/1000 μs waveform |
| Insulation resistance after reflow soldering | $f = 1\text{MHz}, V_{rms} = 0.5 \text{ V}$ |

Reflow soldering condition

Soldering paste : Tamura (Japan) RMA-20-21L
 Stencil : SUS, 120 μm thickness
 Pad size : 0.8 (Width) x 0.9 (Length)
 0.8 (Distance between pads)
 Soldering profile : $260 \pm 5 \text{ }^\circ\text{C}$, 5 sec.

1-2 Electrical specification

| | | | |
|--|-------------|-----------------------------|---------|
| Maximum allowable continuous DC voltage | 24 | V | |
| trigger voltage / Varistor voltage / breakdown voltage | 100-150 | V | |
| Maximum clamping voltage | 180 | V | Maximum |
| Rated peak single pulse transient current | 1 | A | Maximum |
| Nonlinearity coefficient | > 12 | | |
| Leakage current at continuous DC voltage | < 0.1 | μA | |
| Response time | < 1.0 | ns | |
| Varistor voltage temperature coefficient | < 0.05 | $\%/\text{ }^\circ\text{C}$ | |
| Capacitance measured at 1MHz | 3.0 | pF | Typical |
| Capacitance tolerance | 40 | % | |
| Insulation resistance after reflow soldering on PCB | > 10 | $\text{M}\Omega$ | |
| Operating ambient temperature | -55 to +85 | $^\circ\text{C}$ | |
| Storage temperature | -55 to +125 | $^\circ\text{C}$ | |

1-3 Reliability testing procedures

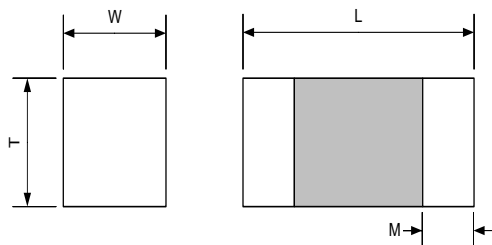
| Reliability parameter | Test | Test methods and remarks | Test requirement |
|------------------------------------|-----------------------------|--|--|
| Pulse current capability | I _{max} 8/20 μs | <u>IEC 1051-1, Test 4.5.</u> 10 pulses in the same direction at 2 pulses per minute at maximum peak current | d V _n / V _n ≤ 10% no visible damage |
| Electrostatic discharge capability | ESD C=150 pF, R=330Ω | <u>IEC 1000-4-2</u> Each 10 times in positive/negative direction in 10 sec at 8KV contact discharge (Level 4) | d V _n / V _n ≤ 10% no visible damage |
| Environmental reliability | Thermal shock | <u>IEC 68-2-14</u> Condition for 1 cycle Step 1 : Min. -40°C, 30±3 min. Step 2 : Max. +125°C, 30±3 min. Number of cycles: 30 times | d V _n / V _n ≤ 5% no visible damage |
| | Low temperature | <u>IEC 68-2-1</u> Place the chip at -40±5°C for 1000±12hrs. Remove and place for 24±2hrs at room temp. condition, then measure | d V _n / V _n ≤ 5% no visible damage |
| | High temperature | <u>IEC 68-2-2</u> Place the chip at 125±5°C for 1000±24hrs. Remove and place for 24±2hrs at room temp. condition, then measure | d V _n / V _n ≤ 5% no visible damage |
| | Heat resistance | <u>IEC 68-2-3</u> Apply the rated voltage for 1000±48hrs at 85±3°C. Remove and place for 24 ±2hrs at room temp. condition, then measure | d V _n / V _n ≤ 5% no visible damage |
| | Humidity resistance | <u>IEC 68-2-30</u> Place the chip at 40±2°C and 90 to 95% humidity for 1000±24hrs. Remove and place for 24±2hrs at room temp. condition, then measure | d V _n / V _n ≤ 10% no visible damage |
| | Pressure cooker test | Place the chip at 2 atm, 120°C, 85%RH for 60 hrs. Remove and place for 24±2hrs at room temp. condition, then measure | d V _n / V _n ≤ 10% no visible damage |

| | | | |
|-------------------------------|------------------------------|---|---|
| | Operating life | Apply the rated voltage for 1000±48hrs at 125±3°C. Remove and place for 24±2hrs at room temp. condition, then measure | $d V_n /V_n \leq 10\%$ no visible damage |
| Mechanical Reliability | Solderability | <u>IEC 68-2-58</u> Solder bath method, 230±5°C, 2s | At least 95% of terminal electrode is covered by new solder |
| | Resistance to soldering heat | <u>IEC 68-2-58</u> Solder bath method, 260±5°C, 10±0.5s, 270±5°C, 3±0.5s | $d V_n /V_n \leq 5\%$ no visible damage |
| | Bending strength | <u>IEC 68-2-21</u> Warp:2mm, Speed:0.5mm/sec, Duration: 10sec. The measurement shall be made with board in the bent position | $d V_n /V_n \leq 5\%$ no visible damage |
| | Adhesive strength | <u>IEC 68-2-22</u> Applied force on SMD chip by fracture from PCB | Strength>10 N no visible damage |

2. Material Specification

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|----------------------------------|---------------------------|
| Body | ZnO based ceramics |
| Internal electrode | Silver – Palladium |
| External electrode | Silver – Nickel – Tin |
| Thickness of Ni/Sn plating layer | Nickel > 1 μm, Tin > 2 μm |

3. Dimension Specification

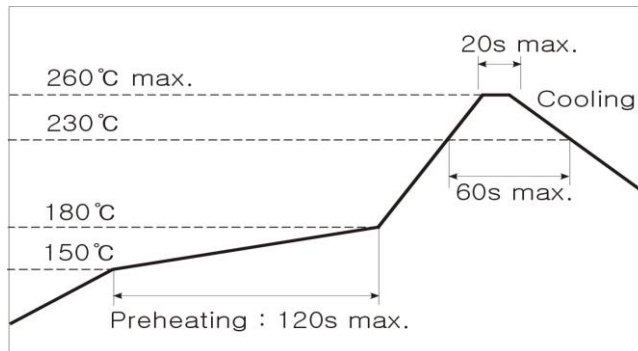


| Size | L(mm) | W(mm) | T(mm) | M(mm) |
|------|----------|----------|-------|-----------|
| 0402 | 1.0±0.10 | 0.5±0.10 | ≤ 0.6 | 0.20±0.10 |
| 0603 | 1.6±0.15 | 0.8±0.15 | ≤ 0.9 | 0.35±0.10 |

4. Soldering Recommendations

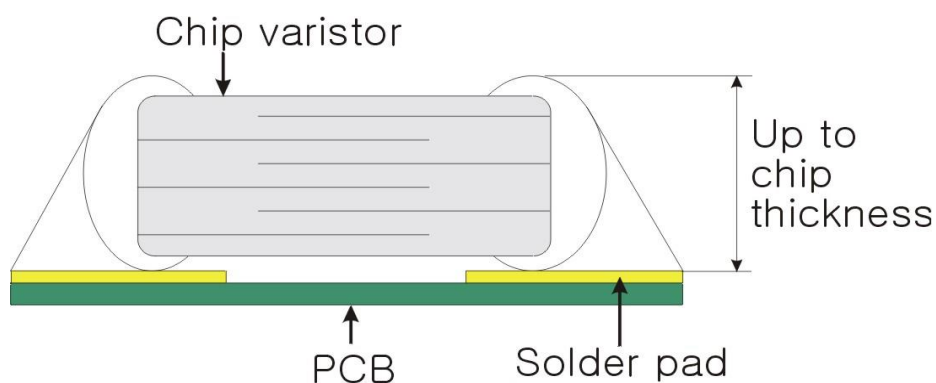
4-1 Soldering profile

4-1-1 Pb free solder paste



4-1-2 Repair soldering

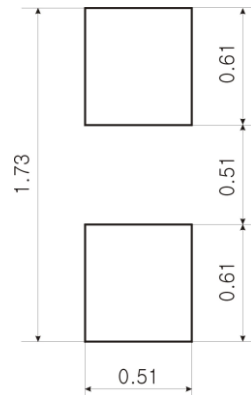
- Allowable time and temperature for making correction with a soldering iron : 350 ± 10 °C, 3 sec.
- Optimum solder amount when corrections are made using a soldering iron



4-2 Soldering guidelines

- Our chip varistors are designed for reflow soldering only. Do not use flow soldering
- Use non-activated flux (Cl content 0.2% max.)
- Follow the recommended soldering conditions to avoid varistor damage.

4-3 Solder pad layout



5. Storage condition

- Storage environment must be at an ambient temperature of 25~35 °C and an ambient humidity of 40~60 % RH
- Chip varistors can experience degradation of termination solderability when subjected to high temperature of humidity, or if exposed to sulfur or chlorine gases.
- Avoid mechanical shock (ex. Falling) to the chip varistor to prevent mechanical cracking inside of the ceramic dielectric due to its own weight.
- Use chips within 6 months.
If 6 months of more have elapsed, check solderability before use.-