ULC0544T

Ultra Low Capacitance TVS Arrays

Description

Leiditech® are ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by **ESD** (electrostatic discharge), **CDE** (Cable Discharge Events), and **EFT** (electrical fast transients).

The Leiditech®0544T has a typical capacitance of only 0.30pF between I/O pins. This allows it to be used on circuits operating in excess of 3GHz without signal attenuation. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge). Each device is designed to protect four lines (two differential pairs).

The ULC0544T is in a 8-pin, RoHS/WEEE compliant, SLP2010P8T package. It measures 2.0 x 1.0 x 0.4mm. The leads are spaced at a pitch of 0.4mm and are finished with lead-free NiPdAu. They are designed for easy PCB layout by allowing the traces to run straight through the device. The combination of small size, low capacitance, and high level of ESD protection makes them a flexible solution for applications such as mini HDMI, MDDI, USB, and eSATA interfaces.

Features

- ESD protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-5 (Lightning) 5A (8/20μs)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Package design optimized for high speed lines
- Flow-Through design
- Protects four I/O lines
- Low capacitance: **0.3pF** typical (I/O to I/O)
- Low clamping voltage
- Low operating voltage: 5V
- Solid-state silicon-avalanche technology

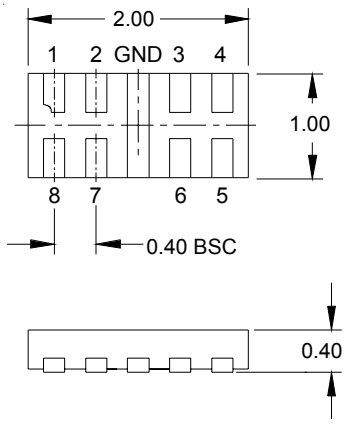
Mechanical Characteristics

- SLP2010P8T 8-pin package (2.0 x 1.0 x 0.4mm)
- RoHS/WEEE Compliant
- Lead Pitch: 0.4mm
- Lead finish: NiPdAu
- Marking: Marking code + date code
- Packaging: Tape and Reel

Applications

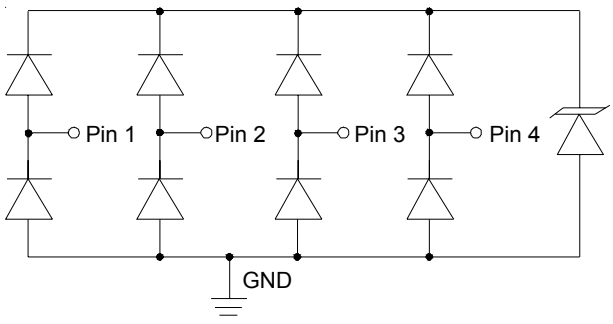
- Cell Phones and Accessories
- Mini HDMI
- MDDI Ports
- USB
- LVDS
- eSATA
- PCI Express

Dimensions



Nominal Dimensions in mm

Circuit Diagram



Note: Pins 5-8 not internally connected

4-Line Protection

Absolute Maximum Rating

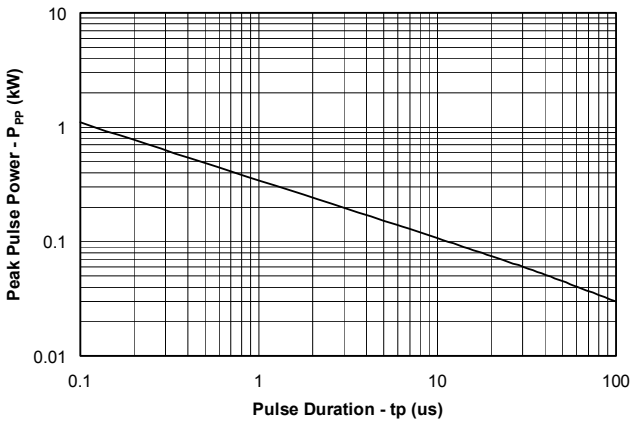
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	75	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	+/- 18 +/- 12	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C)

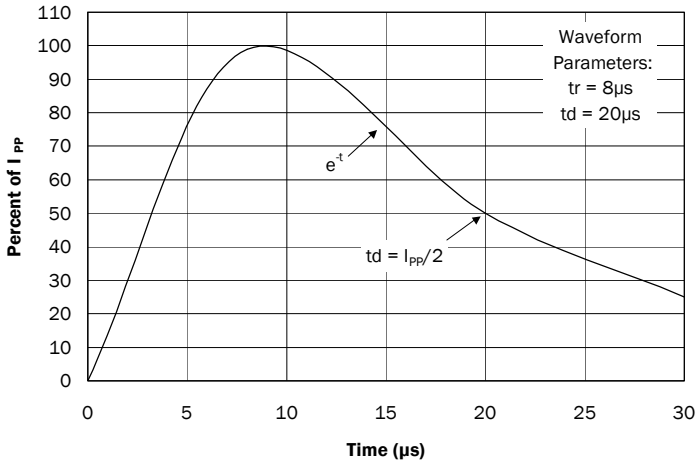
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}	Pin 1, 2, 3, or 4 to GND			5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA, Pin 1, 2, 3, or 4 to GND	6.5	8	11	V
Reverse Leakage Current	I_R	V_{RWM} = 5.0V, Pin 1, 2, 3, or 4 to GND		0.005	0.100	μA
Clamping Voltage	V_C	I_{PP} = 1A, tp = 8/20μs Pin 1, 2, 3, or 4 to GND			12	V
Clamping Voltage	V_C	I_{PP} = 5A, tp = 8/20μs Pin 1, 2, 3, or 4 to GND			15	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz, Pin 1, 2, 3, or 4 to GND		0.7	0.80	pF
		V_R = 0V, f = 1MHz, Between I/O pins		0.3	0.4	pF

Typical Characteristics

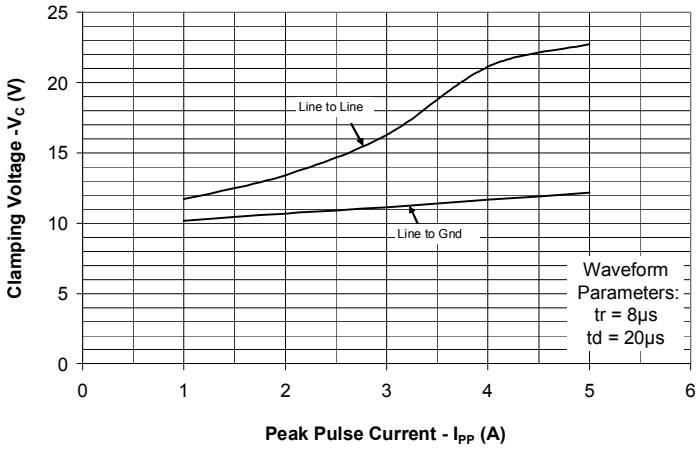
Non-Repetitive Peak Pulse Power vs. Pulse Time



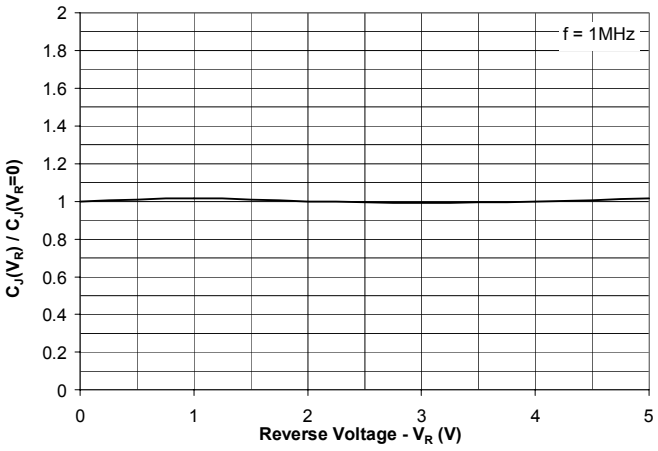
Pulse Waveform



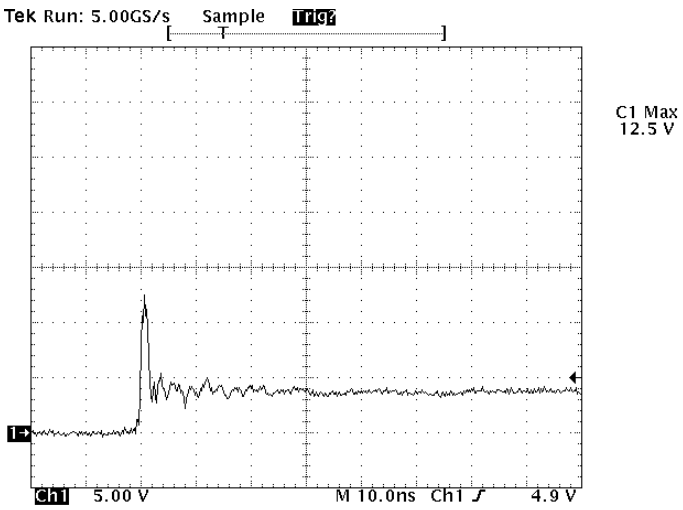
Clamping Voltage vs. Peak Pulse Current



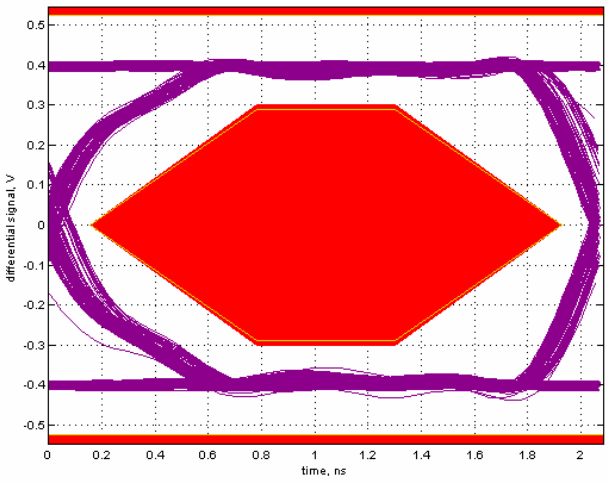
Normalized Capacitance vs. Reverse Voltage



ESD Clamping (Pin 1, 2, 3, or 4 to GND) (+8kV Contact per IEC 61000-4-2)

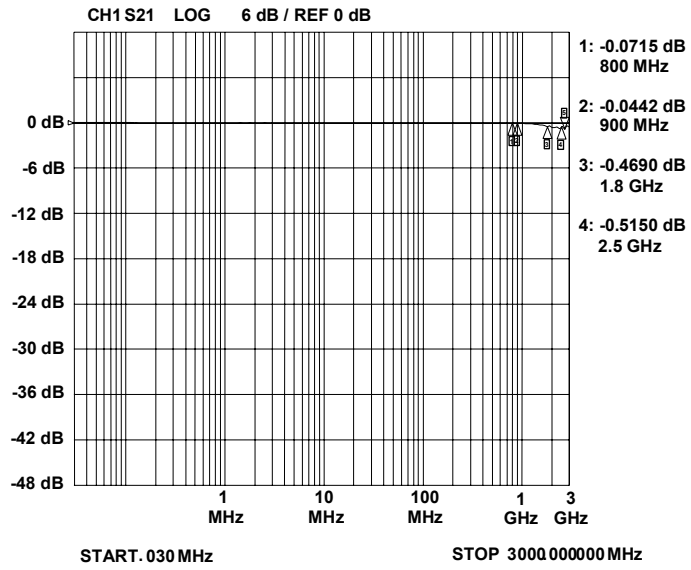


USB 2.0 Eye Pattern with ULC0544T

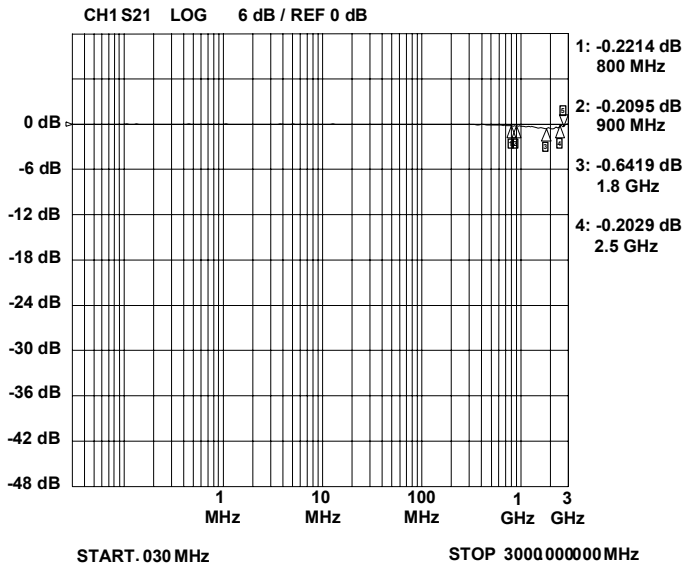


Typical Characteristics (Con't)

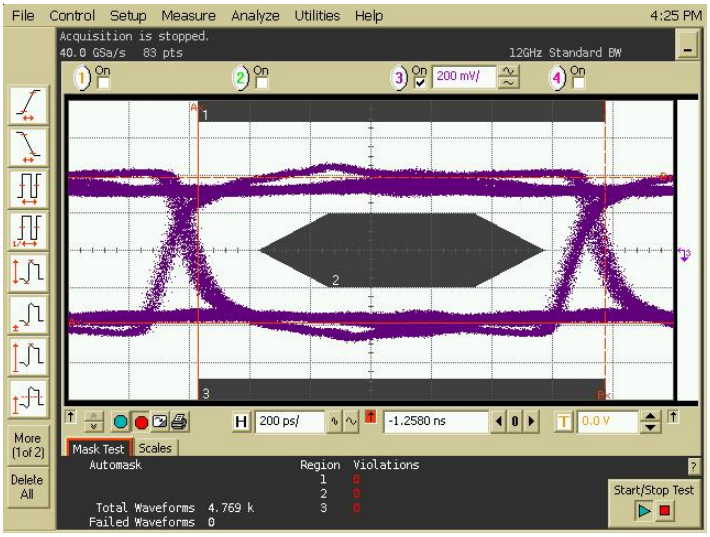
Insertion Loss S21 - I/O to I/O



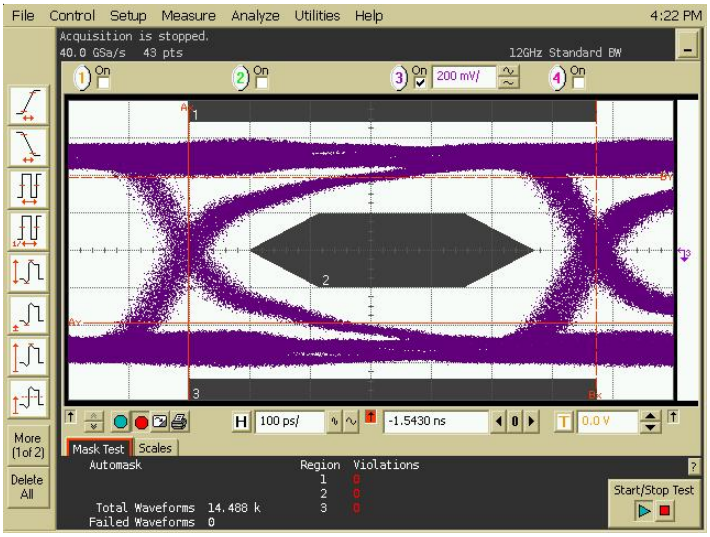
Insertion Loss S21 - I/O to GND



HDMI Eye Pattern (720p with ULC0544T)



HDMI Eye Pattern (1080p with ULC0544T)



Applications Information

Design Recommendations for HDMI Protection

Adding external ESD protection to HDMI ports can be challenging. First, ESD protection devices have an inherent junction capacitance. When adding even a small amount of capacitance, it will cause the impedance of the differential pair to drop. Second, large packages and land pattern requirements can cause discontinuities that adversely affect signal integrity. The ULC0544T is specifically designed for protection of high-speed interfaces, such as HDMI. It presents <0.3pF capacitance between the pairs while being rated to handle >±8kV ESD contact discharges (>±15kV air discharge) as outlined in IEC 61000-4-2. The device is in a leadless SLP package that is less than 1.1mm wide. It is designed such that the traces flow straight through the device. The narrow package and flow-through design reduce discontinuities and minimize impact on signal integrity. This becomes even more critical as signal speeds increase.

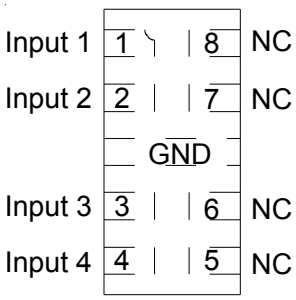


Figure 1 - SLP2010P8T Pin Configuration (Top View)

Pin	Identification
1, 2, 3, 4	Input Lines
5, 6, 7, 8	Output Lines (No Internal Connection)
Center Tab	Ground

Pin Configuration

Figure 2 is an example of how to route the high speed differential traces through the ULC0544T. The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 8, pin 2 to pin 7, pin 3 to pin 6, pin 4 to pin 5). For example, line 1 enters at pin 1 and exits at Pin 8, and the PCB trace connects pin 1 and 8 together. This is true for lines connected at pins 2, 3, and 4 also. Note that there are no internal connections to pins 5 - 8. Ground is connected at the center tabs. One large ground pad should be used in lieu of two separate pads.

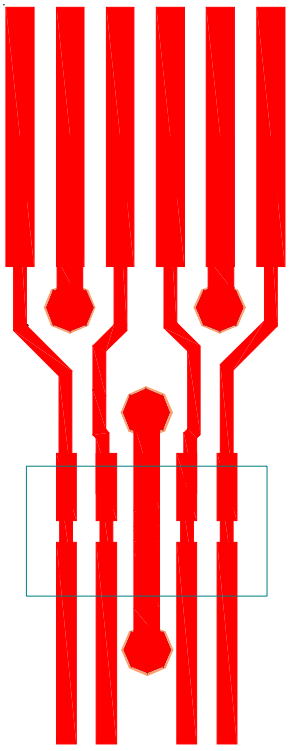


Figure 2 - Flow through Layout Using ULC0544T

TDR Measurements for HDMI

The combination of low capacitance, small package, and flow-through design means it is possible to use these devices to meet the HDMI impedance requirements of 100 Ohm ±15% without any PCB board modification.

For signal integrity purposes, the best results will be obtained by using the ULC0544T to protect the high-speed differential pairs. This is because the device is designed such that the data lines from the connector line up with the I/O pins of the device without altering the trace routing.

Applications Information

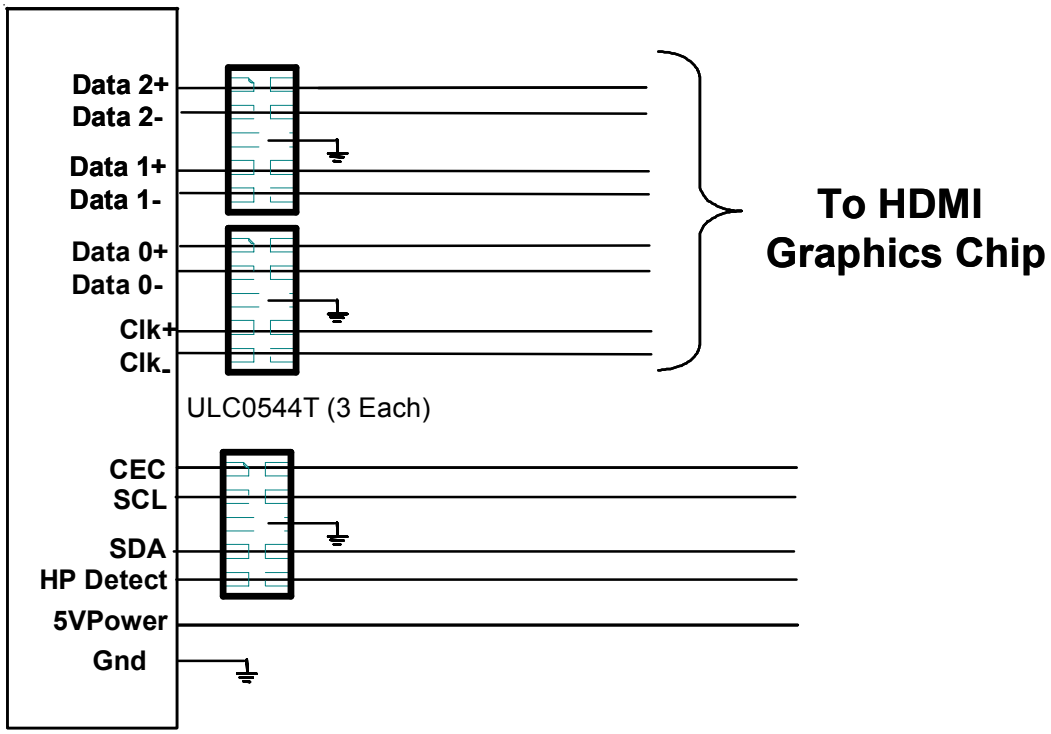
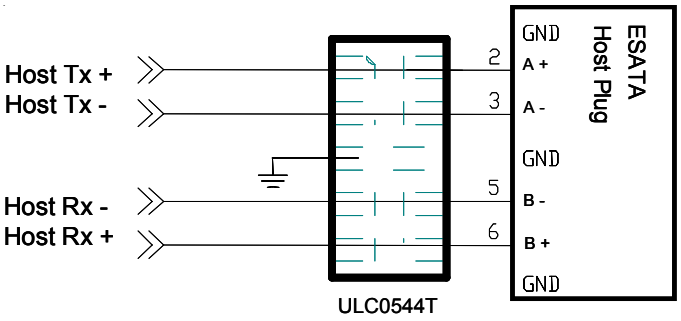


Figure 3. HDMI Protection Example



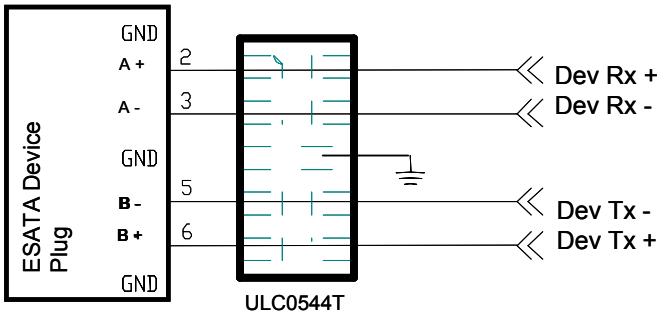


Figure 4. eSATA Protection Example

Applications Information

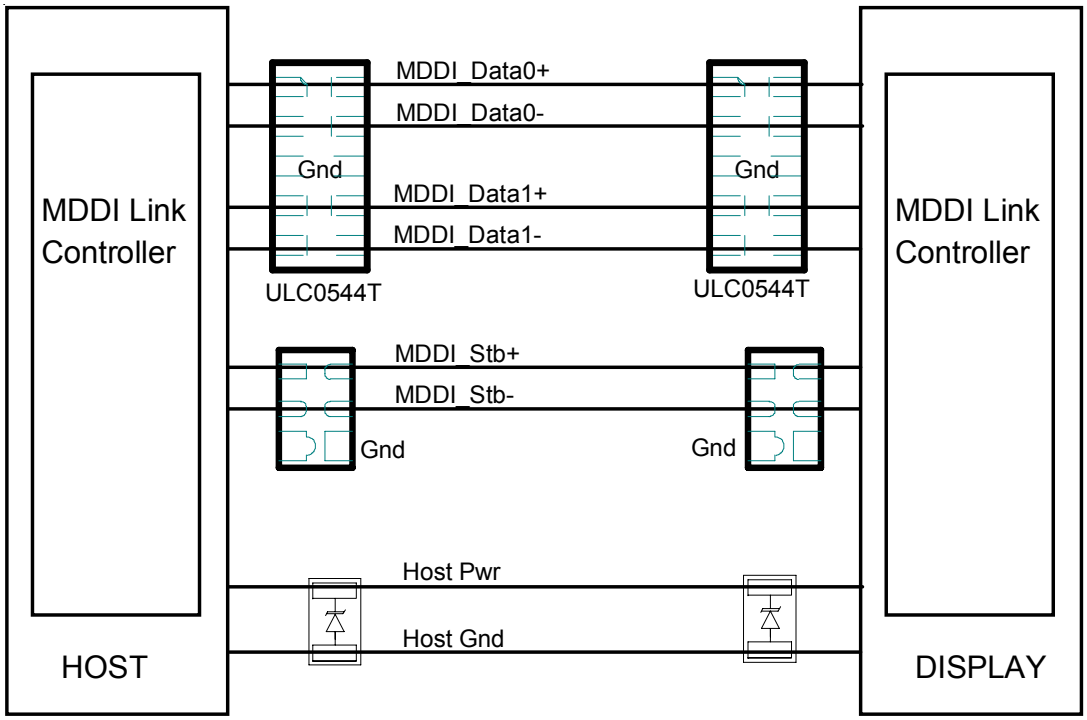
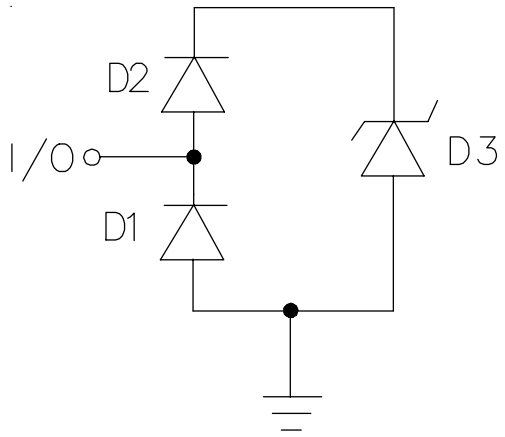


Figure 5. MDDI Protection Example

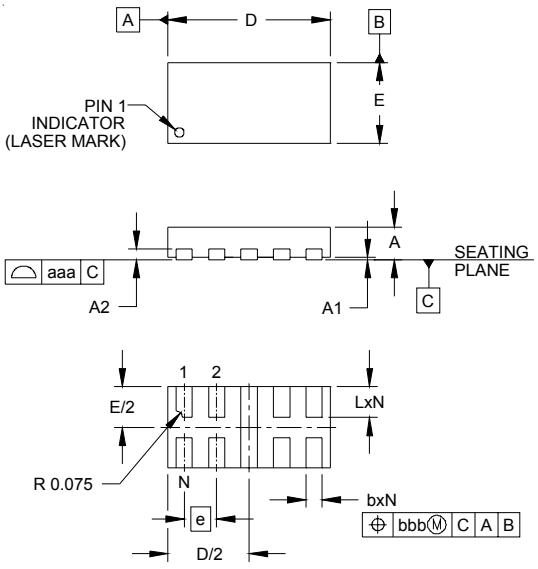
Applications Information - Spice Model



ULC0544T Spice Model

ULC0544T Spice Parameters				
Parameter	**Unit**	**D1**	**D2**	**D3**
IS	Amp	1E-20	1E-20	2E-12
BV	Volt	100	100	8.2
VJ	Volt	0.83	0.83	0.6
RS	Ohm	1.5	0.6	0.2
IBV	Amp	1E-3	1E-3	1E-3
CJO	Farad	0.25E-12	0.25E-12	56E-12
TT	sec	2.541E-9	2.541E-9	2.541E-9
M	--	0.01	0.01	0.23
N	--	1.1	1.1	1.1
EG	eV	1.11	1.11	1.11

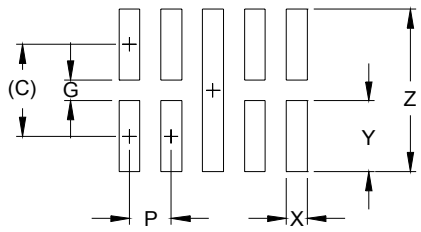
Outline Drawing - SLP2010P8T



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.015	.016	.017	0.37	0.40	0.43
A1	0.00	.001	.002	0.00	0.02	0.05
A2		(.005)			(0.13)	
b	.006	.008	.010	0.15	0.20	0.25
D	.077	.079	.082	1.95	2.00	2.08
E	.037	.039	.043	0.95	1.00	1.08
e	.016 BSC			0.40 BSC		
L	.013	.015	.017	0.32	0.38	0.43
N	8			8		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

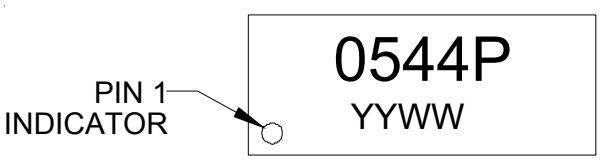
Land Pattern - SLP2010P8T



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.035)	(0.88)
G	.008	0.21
P	.016	0.40
X	.008	0.20
Y	.026	0.67
Z	.061	1.55

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Codes



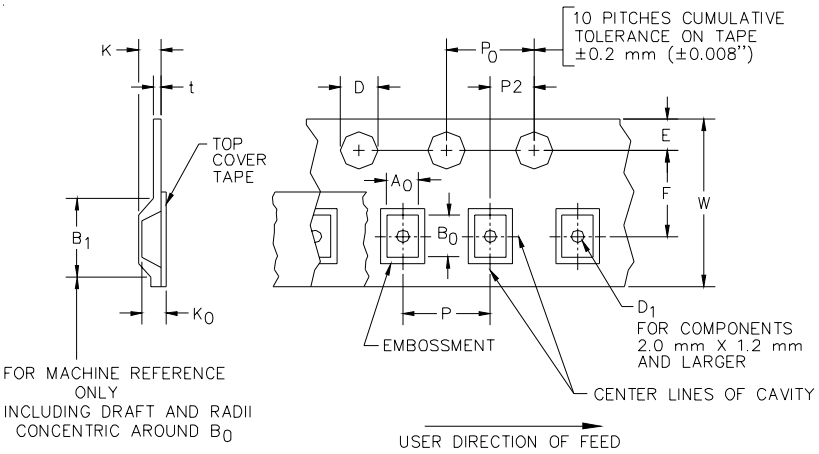
YYWW = Date Code

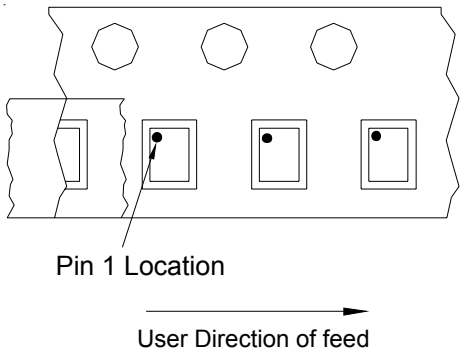
Ordering Information

Part Number	Qty per Reel	Reel Size
ULC0544T	3000	7 Inch

RailClamp and RClamp are marks of Semtech Corporation

Tape and Reel Specification





Device Orientation in Tape

A0	B0	K0
1.21 +/-0.05 mm	2.21 +/-0.05 mm	0.66 +/-0.05 mm

Tape Width	B, (Max)	D	D1	E	F	K (MAX)	P	P0	P2	T(MAX)	W
8 mm	4.2 mm	1.5 + 0.1 mm - 0.0 mm)	0.5 mm ±0.05	1.750±.10 mm	3.5±0.05 mm	2.4 mm	4.0±0.1 mm	4.0±0.1 mm	2.0±0.05 mm	0.4 mm	8.0 mm + 0.3 mm - 0.1 mm

Shanghai Leiditech Electronic Co.,Ltd
Email: sale1@leiditech.com
Tel : +86- 021 50828806
Fax : +86- 021 50477059