Non-Synchronous PWM Boost Converter

Halogen Free

General Description

The FP5217 is boost topology switching regulator for wide operating voltage applications. Its built-in 15mΩ power MOSFET makes this regulator highly power efficient. The non-inverting input of error amplifier connects to a 1.2V precision reference voltage. It has programmable switching frequency set by external resistor, and programmable inductor peak current limit connects a resistor from CS to GND. Current mode control and external compensation network make is easy and flexible to stabilize the system.

The FP5217 is available in the small footprint TSSOP-14L(EP) package to fit in space-saving PCB layout for application fields.

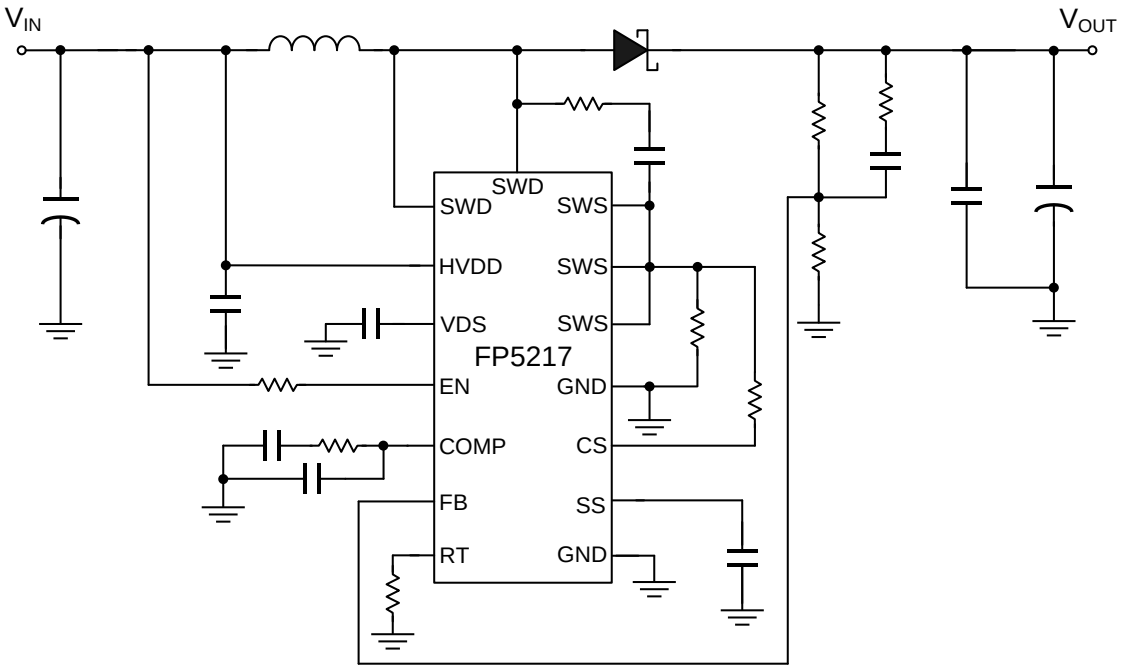
Features

- Start-up Voltage: 2.8V
- Wide Supply Voltage Operating Range: 5V to 24V
- Adjustable Output up to 26V
- Precision Feedback Reference Voltage: 1.2V (±2%)
- Shutdown Current: <3μA
- Programmable Switching Frequency: 200KHz~1000KHz
- Programmable Soft Start Function (SS)
- Input Under Voltage Protection(UVP)
- Adjustable Switching MOSFET Over Current Protection (OCP)
- Over Temperature Protection (OTP)
- MOSFET: 30V/8A/15mΩ (peak current 10A)
- Package: TSSOP-14L(EP)

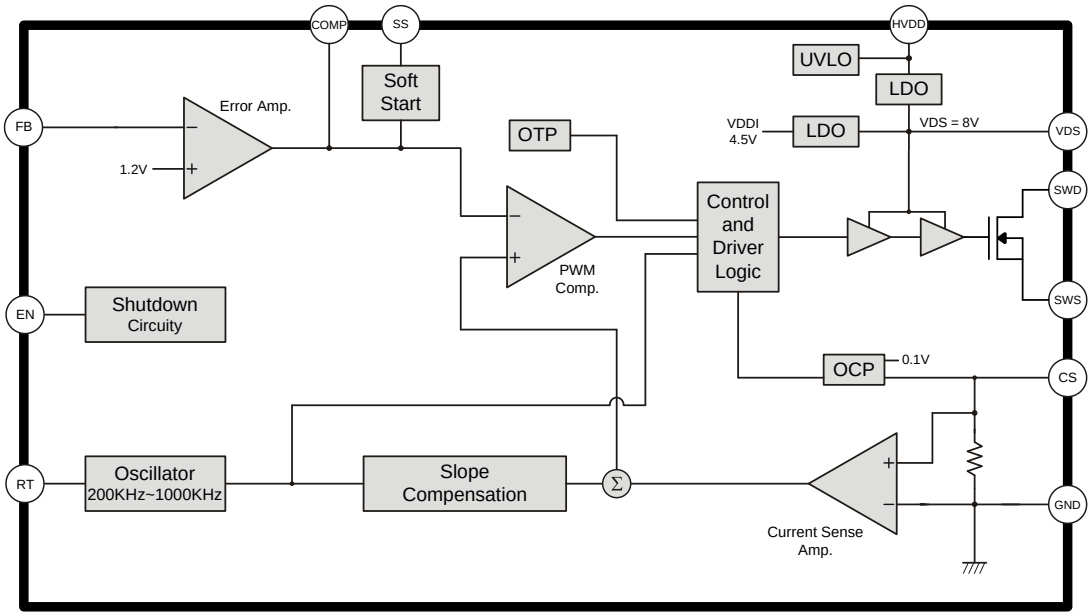
Applications

- Chargers
- Handheld Devices
- Portable Products
- Power Bank
- Bluetooth Speaker

Typical Application Circuit



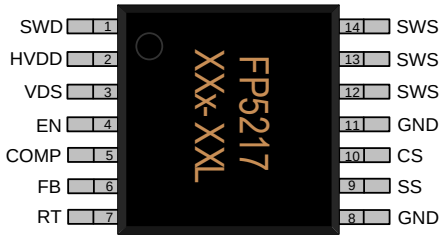
Function Block Diagram



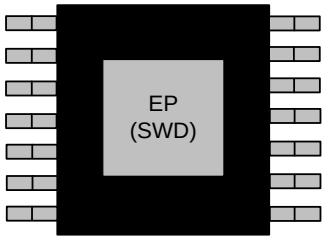
Pin Descriptions

TSSOP-14L (EP)

Top View



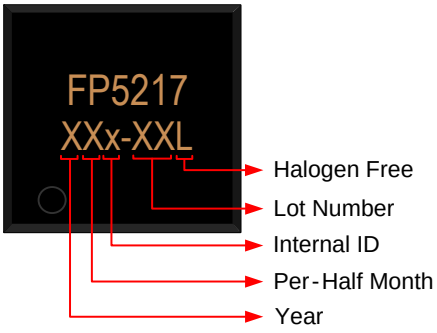
Bottom View



Name	No.	I / O	Description
SWD	1	O	Power Switch Drain
HVDD	2	P	IC Power Supply
VDS	3	P	Power Supply for Internal Control Circuits and Gate Drivers
EN	4	I	Enable Control
COMP	5	O	Compensation
FB	6	I	Error Amplifier Inverting Input
RT	7	I	Frequency Programming
GND	8	P	IC Ground
SS	9	I	Soft Start Programming
CS	10	I	MOSFET Switch Current Sense
GND	11	P	IC Ground
SWS	12	O	Power Switch Source
SWS	13	O	Power Switch Source
SWS	14	O	Power Switch Source
SWD	15(EP)	O	Power Switch Drain

Marking Information

TSSOP-14L(EP)



Halogen Free: Halogen free product indicator

Lot Number: Wafer lot number's code

Internal ID: Internal Identification Code

Per-Half Month: Production period indicator in half month time unit

For Example : A → First Half Month of January
B → Second Half Month of January
C → First Half Month of February
D → Second Half Month of February

Year: Production year's last digit

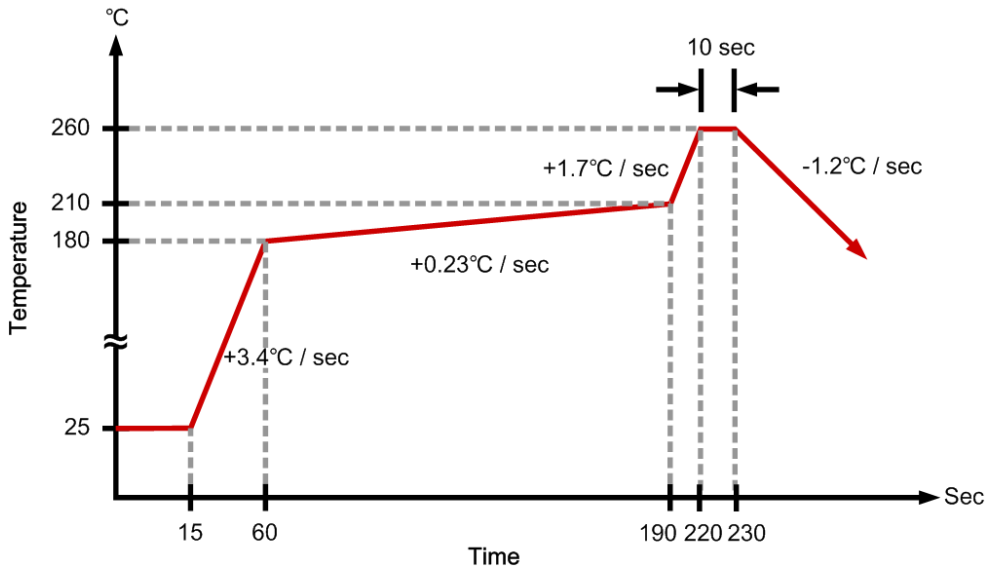
Ordering Information

Part Number	Operating Temperature	Package	MOQ	Description
FP5217mR-G1	-25°C ~ 85°C	TSSOP-14L(EP)	2500EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	HVDD		-0.3		25	V
VDS Voltage			-0.3		16	V
SWD Voltage	V_{SWD}				33	V
Others Pin Voltage			-0.3		6	V
Thermal Resistance (Junction to Ambient)	θ_{JA}	TSSOP-14L(EP)			+55	°C / W
Thermal Resistance (Junction to Case)	θ_{JC}	TSSOP-14L(EP)			+9	°C / W
Junction Temperature	T_J				+150	°C
Operating Temperature	T_{OP}		-25		+85	°C
Storage Temperature	T_{ST}		-65		+150	°C
Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



Recommended Operating Conditions

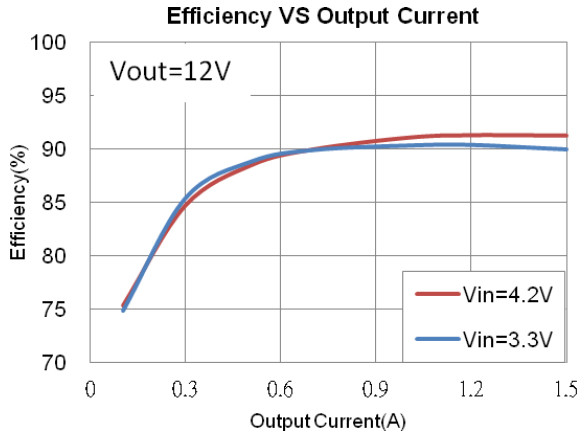
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	HVDD		5		24	V
Operating Temperature Range	T_A	Ambient Temperature	-25		+85	°C

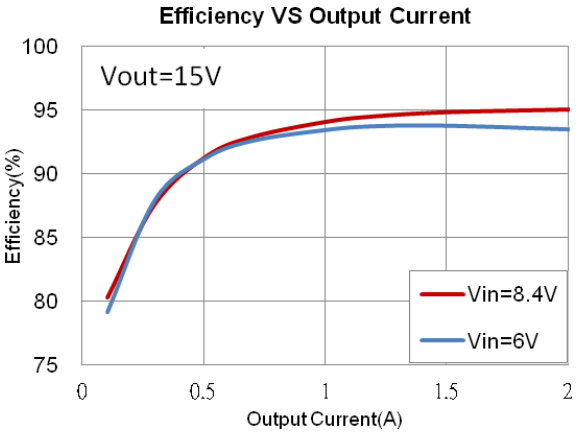
DC Electrical Characteristics (HVDD=12V, T_A=25°C, unless otherwise specified)

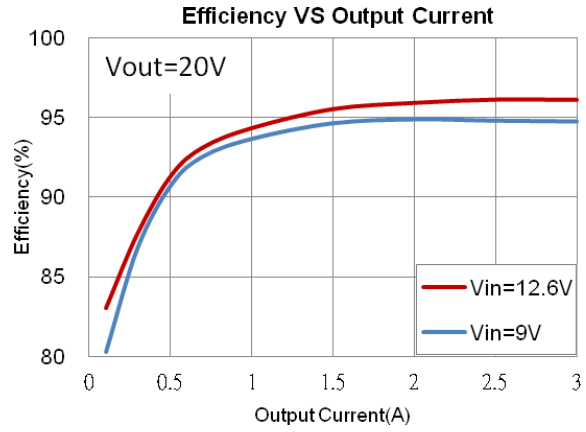
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System Supply Input						
Start-up Voltage	HV_{DD}		2.8			V
Input Supply Range	HV_{DD}		5		24	V
Under Voltage Lockout	V_{UVLO}			2.6		V
UVLO Hysteresis				0.2		V
Average Current	I_{CC}	FB=1.0V, Switching		5		mA
Quiescent Current	I_{CC}	FB=1.3V, No Switching		0.8		mA
Shutdown Current	I_{CC}	V_{EN}=GND			3	μA
Input Supply Voltage	V_{DS}	HV_{DD}=12V, I_{DS}=0A	7.5	8	8.5	V
Oscillator						
Operation Frequency	f_{OSC}	RT=100KΩ		200		KH_Z
		RT=51KΩ	320	370	420	KH_Z
Maximum Duty Ratio	%	FB=1.0V		90		%
Soft Start						
Soft-Start bias Current	I_{SS}	V_{ss}=0V		3.5		μA
Reference Voltage						
Feedback Voltage	V_{FB}	HV_{DD}=12V	1.176	1.2	1.224	V
Enable Control						
Enable Voltage	V_{EN}		1.42	1.50	1.58	V
Shutdown Voltage	V_{EN}			1.3		V
UVEN Hysteresis				0.2		V
MOSFET						
ON Resistance of Driver	$R_{DS(ON)}$			15		mΩ
Current Sense						
Sense Voltage	V_{CS}		85	100	115	mV
Switching Current Limit	I_{SW}	R_{CS}=12.5mΩ		8		A
Thermal Shutdown						
Thermal Shutdown Threshold	T_{TS}			+150		°C
Thermal Shutdown Threshold Hysteresis	T_{TSH}			30		°C

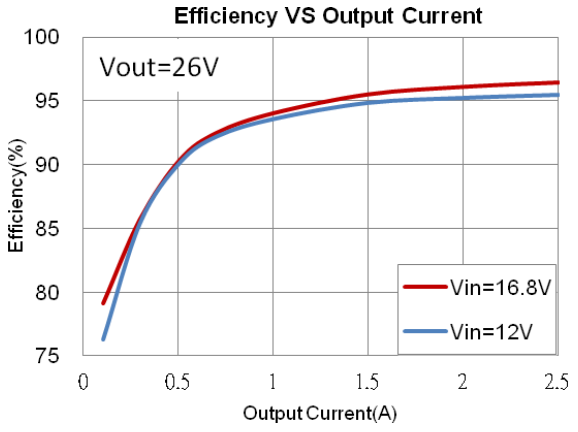
Typical Operating Characteristics

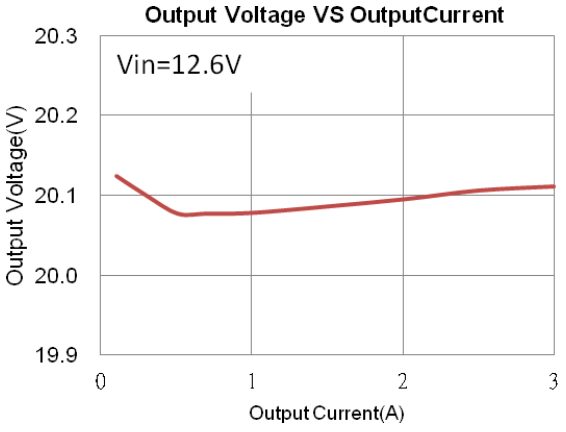
(T_A=25°C, unless otherwise specified)

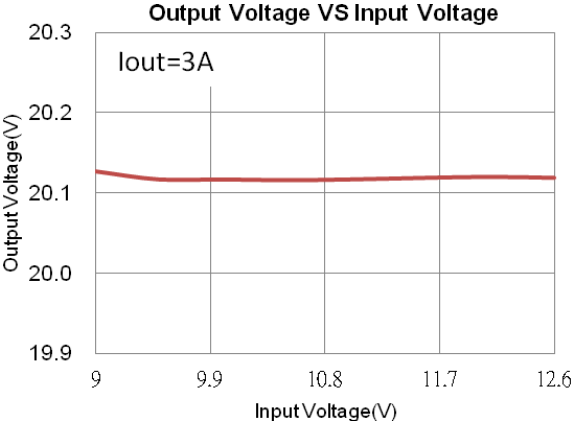












Function Description

Operation

The FP5217 is current mode boost converter. It operates with pulse width modulation (PWM). The internal resistive divider provides 1.2V reference for the error amplifier. It changes to PSM mode when the output is light load. In PSM mode, it can reduce switching lose to raise efficiency, but the output ripple is bigger.

Soft Start Function

Soft start time is programmable to connect capacitor between SS pin to ground. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current during power on. The soft start bias current is 3.5μA.

Oscillator

The oscillator frequency can be set from 200KHz to 1000KHz by external resistance. Acceptable resistance values range from 100KΩ to 17KΩ. The RT pin can't float must connect a resistance to ground. The relationship between the timing resistance RT and frequency is shown in Figure1. The oscillator frequency can be calculated using formula below.

$$RT(K\Omega) = \frac{17000}{f_{OSC}(KHz) - 25}$$

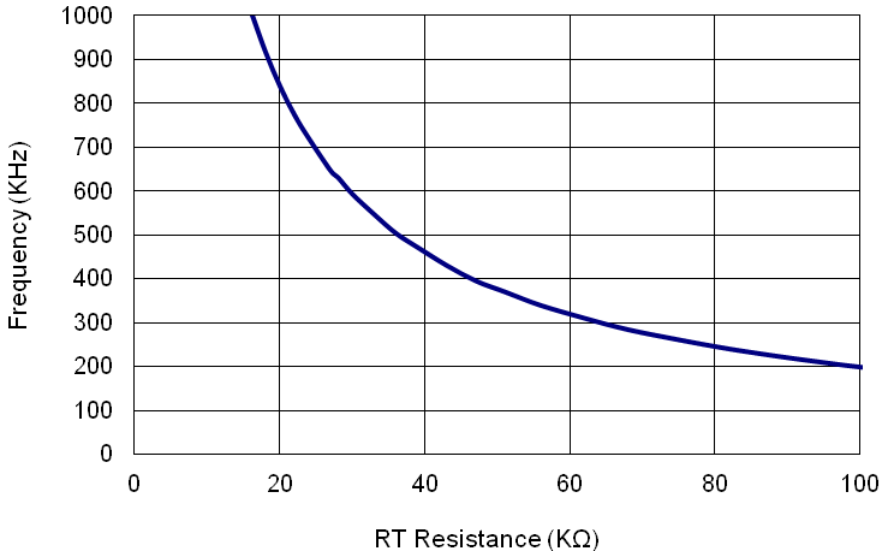


Figure 1. Frequency vs. RT Resistance

Enable Mode / Shutdown Mode

Input voltage connects to EN pin through a resistive divider to set UVLO threshold. FP5217 is enabled when EN voltage greater than 1.5V. The EN voltage is lower than 1.3V to shutdown it. In shutdown mode, to turn off circuitry includes SW signal, VDS voltage, and supply current of HVDD reduces less than 3μA. The EN hysteresis voltage is 0.2V. HVDD voltage may be lower than 5V, it can't use a resistive divider to set UVLO threshold. For instance, input voltage is from 3V to 4.2V, HVDD pin connects to output 12V, when UVLO is triggered to shutdown FP5217, HVDD and output are approximately input voltage. If the applications don't need to set UVLO, the EN connects to input voltage through resistance 200KΩ.

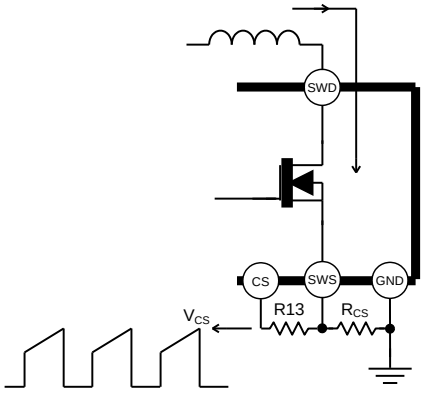
Current Sense Control

Internal switching MOSFET is turned on inductor current flows across the current sense resistor to generate V_{CS}. V_{CS} provides part of current mode control loop. Internal leading-edge blanking is provided to prevent premature turn off the switching MOSFET in each switching cycle.

Current Limit Setting Resistor (R_{CS})

R_{CS} is connected between SWS and ground, and then CS connects to R_{CS} through R13. Its calculation formula is as below. Where 0.085V is minimum threshold voltage of current sense, ILp is peak inductor current, and the factor 1.3 provides a 30% margin for tolerances.

$$R_{cs}(\Omega) = \frac{0.085V}{ILp(A) \times 1.3}$$



According to following equations calculate the peak inductor current ILp. Where ILavg is the average inductor current, ILpp is the peak-to-peak inductor current, Vout is the output voltage, Iout(max) is the output maximum current, Eff is the efficiency, Fs is the switching frequency, and the L is inductance.

$$ILp = ILavg + \frac{ILpp}{2}$$

$$ILavg = \frac{Vout \times Iout(max)}{Vin \times Eff}$$

$$ILpp = \left(\frac{Vin}{Vout}\right)^2 \times \left(\frac{Vout - Vin}{Fs \times Iout(max)}\right) \times \left(\frac{Eff}{L}\right) \times ILavg$$

Thermal Shutdown Protection

The IC will shutdown automatically when the internal junction temperature exceeds +150°C. The device can restart until the junction temperature drops below +120°C approximately.

Application Information

Inductor Selection

The Inductance value is decided based on different condition. 3.3µH to 47uH inductance value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency. The inductance is calculated using formula. Where Vout is output voltage, Fs is switching frequency, Iout is output maximum current, Eff is boost efficiency and r is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at full load current. r is recommended between 0.3 and 0.5.

$$L = \left(\frac{Vin}{Vout}\right)^2 \times \left(\frac{Vout - Vin}{Fs \times Iout(max)}\right) \times \left(\frac{Eff}{r}\right)$$

Capacitor Selection

Output capacitor is required to maintain the DC voltage during switching. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

Diode Selection

Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

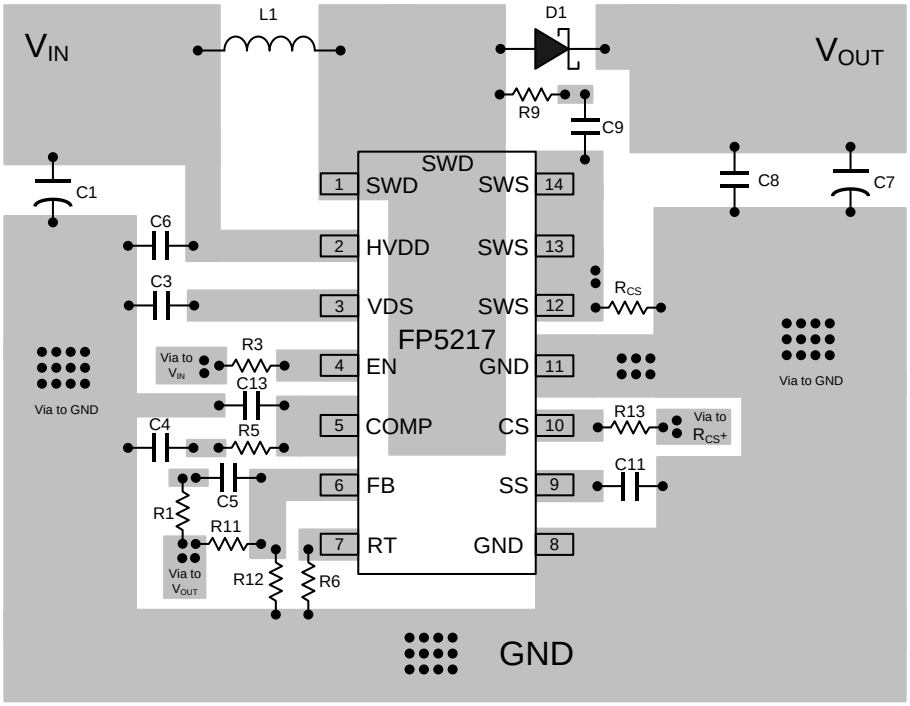
Output Voltage Programming

The output voltage is set by a resistive voltage divider from the output voltage to FB. The output voltage is:

$$V_{OUT} = 1.2V \times \left(1 + \frac{R11}{R12}\right)$$

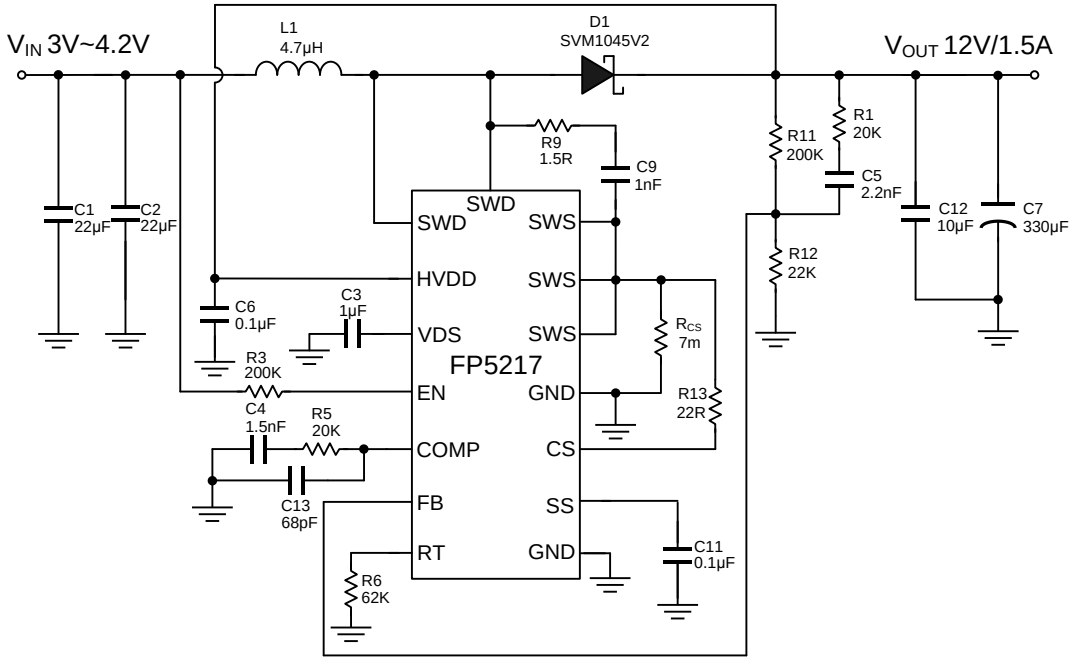
Layout Considerations

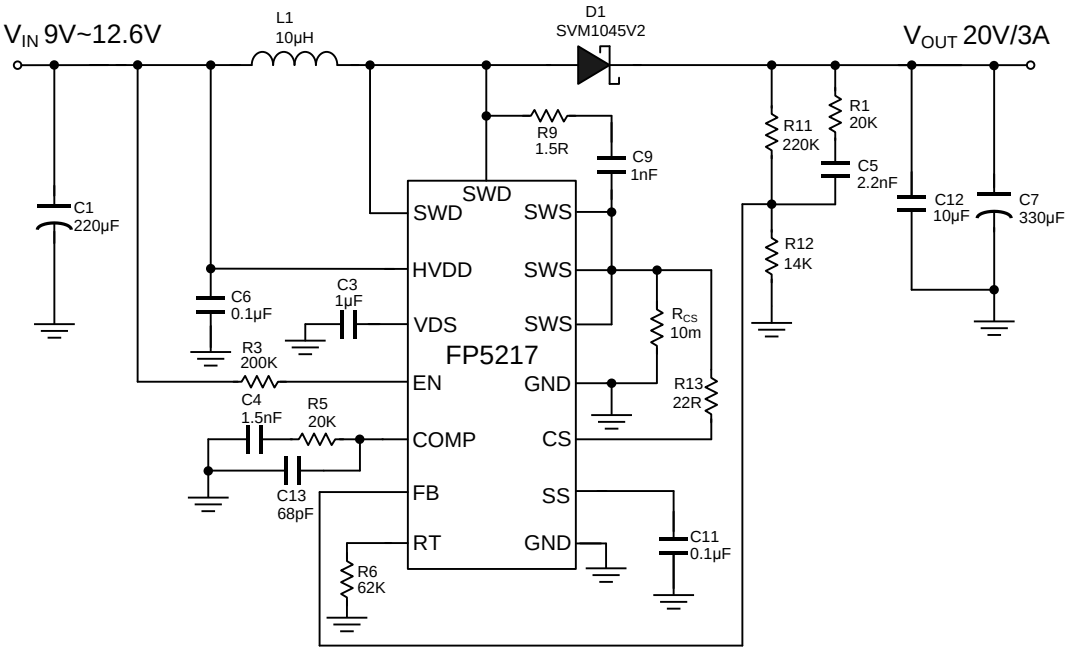
1. The power traces, consisting of the GND trace, the SWD pin trace and the V_{IN} trace should be kept short, direct and wide.
2. Layout switching node SWD pin, inductor and schottky diode connection traces wide and short to reduce EMI.
3. Place C6 nearby HVDD pin as closely as possible to maintain input voltage steady and filter noise.
4. Resistive divider R11 and R12 must be connected to FB and GND pin directly and as closely as possible.
5. FB is a sensitive node. Please keep it away from switching node, SWD pin.
6. The GND of the R_{CS}, C1, C6, C7 and C8 should be connected close and together directly to a ground plane.
7. R_{CS} must be connected to CS and GND pin directly and as closely as possible.
8. The output capacitor C7 and C8 should be connected close and together directly to the ground of R_{CS}.



Suggested Layout

Application Information



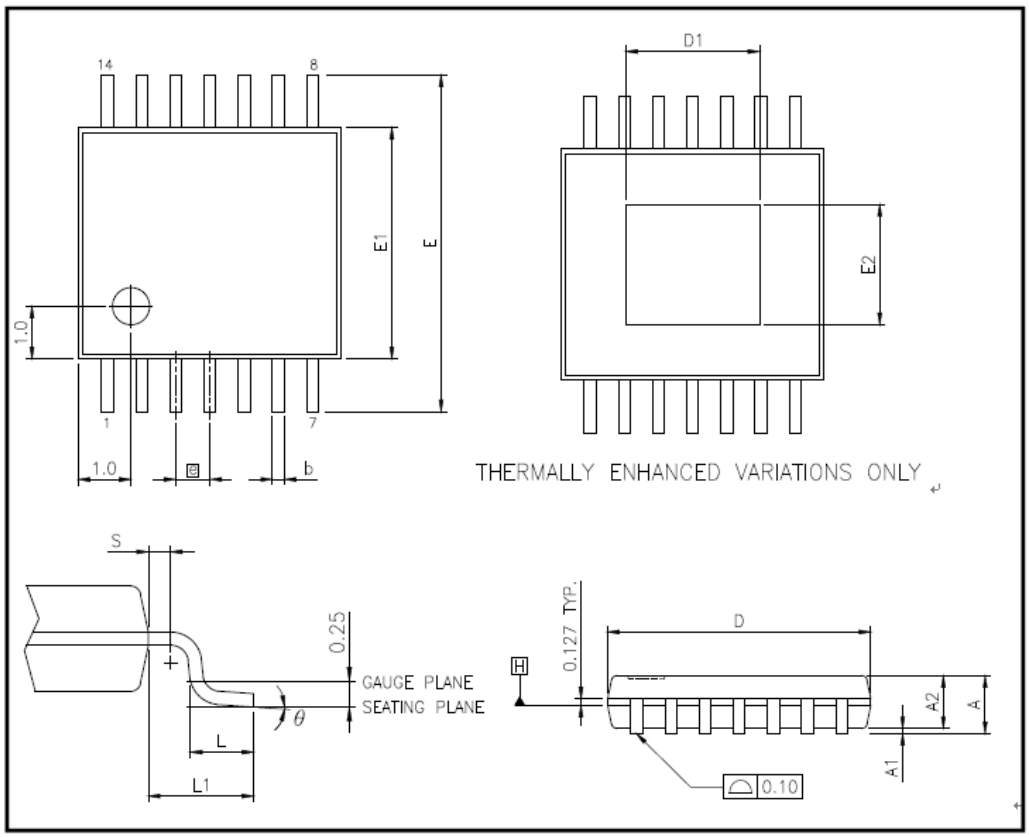


Note:

1. The X5R and X7R of ceramic capacitors are recommended to choose.
2. R9 and C9 are added for reducing EMI (Electromagnetic Interference).

Package Outline

TSSOP-14L(EP)



UNIT: mm

Symbols	Min. (mm)	Nom.(mm)	Max. (mm)
A	-	-	1.20
A1	0.00	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.50	0.60	0.75
S	0.20	-	-
θ	0°	-	8°

Exposed PAD Dimensions:

Symbols	Min. (mm)	Max. (mm)
E2	2.55	3.15
D1	2.64	3.25

Note:

1. All dimensions are in millimeters.
2. Dimension ”D” does not include mold flash, protrusions or gate burrs. Mold flash,protrusions or gate burrs shall not exceed 0.15 pre side.
3. Dimension ”E1” does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 pre side.
4. Dimension ”b” does not include interlead dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the ”b” dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension ”D” and ”E1” to be determined at datum plane.