1. Electrical Specification

1-1 Test condition

Varistor voltage	In = 1 mA DC
Leakage current	Vdc = 5.5 V DC
Maximum clamping voltage	Ic = 1 A
Rated peak single pulse transient current	8 / 20 µs waveform, +/- each 1 time induce
Capacitance	10/1000 µs waveform
Insulation resistance after reflow soldering	f = 1MHz, Vrms = 0.5 V
Reflow soldering condition	Soldering paste : Tamura (Japan) RMA-20-21L Stencil : SUS, 120 ㎛ thickness Pad size : 0.8 (Width) x 0.9 (Length) 0.8 (Distance between pads) Soldering profile : 260±5 ℃, 5 sec.

1-2 Electrical specification

Maximum allowable continuous DC voltage	5.5	V	
trigger voltage / Varistor voltage / breakdown voltage	12	V	
Maximum clamping voltage	25	V	Maximum
Rated peak single pulse transient current	1	A	Maximum
Nonlinearity coefficient	> 12		
Leakage current at continuous DC voltage	< 0.1	µA	
Response time	< 0.5	ns	
Varistor voltage temperature coefficient	< 0.05	%/℃	
Capacitance measured at 1MHz	5	pF	Typical
Capacitance tolerance	-50 to +80	%	
Insulation resistance after reflow soldering on PCB	> 10	MΩ	
Operating ambient temperature	-55 to +125	℃	
Storage temperature	-55 to +125	℃	

1-3 Reliability testing procedures

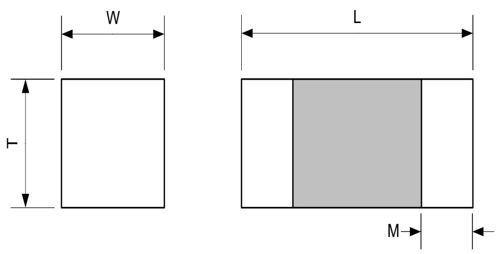
Reliability parameter	Test	Test methods and remarks	Test requirement
Pulse current capability	Imax 8/20 µs	IEC 1051-1, Test 4.5. 10 pulses in the same direction at 2 pulses per minute at maximum peak current	$d\|V_n\|/V_n \leq 10\%$ no visible damage
Electrostatic discharge capability	ESD C=150 pF, R=330Ω	IEC 1000-4-2 Each 10 times in positive/negative direction in 10 sec at 8KV contact discharge (Level 4)	$d\|V_n\|/V_n \leq 10\%$ no visible damage
Environmental reliability	Thermal shock	IEC 68-2-14 Condition for 1 cycle Step 1 : Min. –40℃, 30±3 min. Step 2 : Max. +125℃, 30±3 min. Number of cycles: 30 times	$d\|V_n\|/V_n \leq 5\%$ no visible damage
	Low temperature	IEC 68-2-1 Place the chip at -40±5℃ for 1000±12hrs. Remove and place for 24±2hrs at room temp. condition, then measure	$d\|V_n\|/V_n \leq 5\%$ no visible damage
	High temperature	IEC 68-2-2 Place the chip at 125±5℃ for 1000±24hrs. Remove and place for 24±2hrs at room temp. condition, then measure	$d\|V_n\|/V_n \leq 5\%$ no visible damage
	Heat resistance	IEC 68-2-3 Apply the rated voltage for 1000±48hrs at 85±3℃. Remove and place for 24±2hrs at room temp. condition, then measure	$d\|V_n\|/V_n \leq 5\%$ no visible damage
	Humidity resistance	IEC 68-2-30 Place the chip at 40±2℃ and 90 to 95% humidity for 1000±24hrs. Remove and place for 24±2hrs at room temp. condition, then measure	$d\|V_n\|/V_n \leq 10\%$ no visible damage
	Pressure cooker test	Place the chip at 2 atm, 120℃, 85%RH for 60 hrs. Remove and place for 24±2hrs at room temp. condition, then measure	$d\|V_n\|/V_n \leq 10\%$ no visible damage

	Operating life	Apply the rated voltage for 1000±48hrs at 125±3℃. Remove and place for 24±2hrs at room temp. condition, then measure	$d\lvert Vn\rvert/Vn \leq 10\%$ no visible damage
Mechanical Reliability	Solderability	IEC 68-2-58 Solder bath method, 230±5℃, 2s	At least 95% of terminal electrode is covered by new solder
	Resistance to soldering heat	IEC 68-2-58 Solder bath method, 260±5℃, 10±0.5s, 270±5℃, 3±0.5s	$d\lvert Vn\rvert/Vn \leq 5\%$ no visible damage
	Bending strength	IEC 68-2-21 Warp:2mm, Speed:0.5mm/sec, Duration: 10sec. The measurement shall be made with board in the bent position	$d\lvert Vn\rvert/Vn \leq 5\%$ no visible damage
	Adhesive strength	IEC 68-2-22 Applied force on SMD chip by fracture from PCB	Strength>10 N no visible damage

2. Material Specification

Body	ZnO based ceramics
Internal electrode	Silver – Palladium
External electrode	Silver – Nickel – Tin
Thickness of Ni/Sn plating layer	Nickel ＞ 1 ㎛, Tin ＞ 2 ㎛

3. Dimension Specification

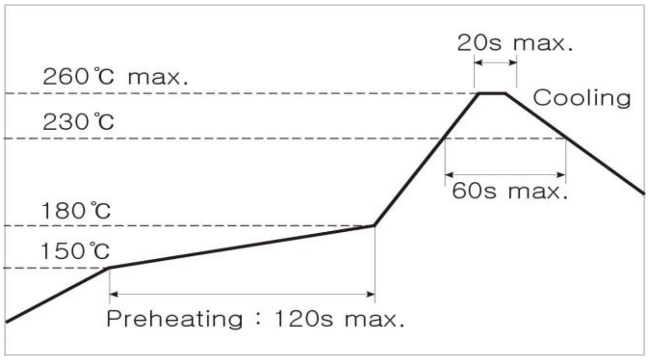


Size	L(mm)	W(mm)	T(mm)	M(mm)
0402	1.0±0.10	0.5±0.10	≤ 0.6	0.20±0.10
0603	1.6±0.15	0.8±0.15	≤ 0.9	0.35±0.10

4. Soldering Recommendations

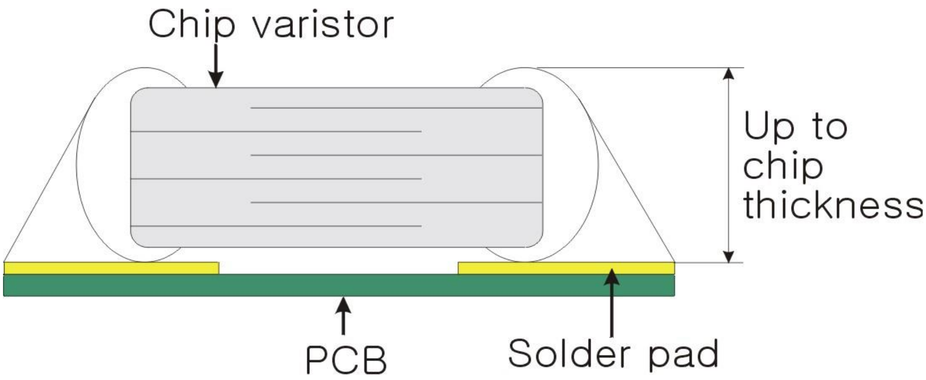
4-1 Soldering profile

4-1-1 Pb free solder paste



4-1-2 Repair soldering

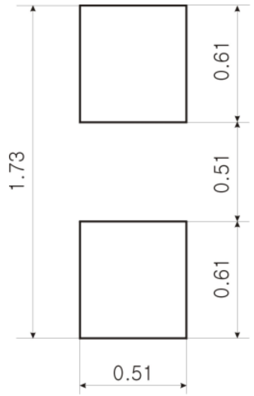
- Allowable time and temperature for making correction with a soldering iron
  : 350 ± 10 ℃, 3 sec.
- Optimum solder amount when corrections are made using a soldering iron



4-2 Soldering guidelines

- Our chip varistors are designed for reflow soldering only. Do not use flow soldering
- Use non-activated flux (Cl content 0.2% max.)
- Follow the recommended soldering conditions to avoid varistor damage.

4-3 Solder pad layout



5. Storage condition

- Storage environment must be at an ambient temperature of 25~35 ℃ and an ambient humidity of 40~60 % RH
- Chip varistors can experience degradation of termination solderability when subjected to high temperature of humidity, or if exposed to sulfur or chlorine gases.
- Avoid mechanical shock (ex. Falling) to the chip varistor to prevent mechanical cracking inside of the ceramic dielectric due to its own weight.
- Use chips within 6 months.

  If 6 months of more have elapsed, check solderability before use.-

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