

### GENERAL DESCRIPTION

OB2571x is an excellent primary side regulation controller with CC/CV operation for medium level power AC/DC charger and adapter applications. The device integrates an internal power MOSFET and operates in QR mode to provide high efficiency along with several functions of built-in protections. It removes the need for secondary feedback circuitry to lower the total bill of material cost. Proprietary Constant Voltage (CV) and Constant Current (CC) control is integrated as shown in the figure below.

In CV control, the controller changes the mode of operation according to load condition. At full loading, the controller operates in quasi-resonant (QR) mode in the universal line voltage. The primary side regulation power supplies up to high power without the efficiency limitation of DCM or audible noise.

In CC control, OB2571x samples the  $V_{cs}$  peak current and the demagnetization pulse to regulation the output current. The current and output power setting can be adjusted externally by the sense resistor  $R_s$  at CS pin.

OB2571x offers comprehensive protection coverage with auto-recovery feature including Cycle-by-Cycle current limiting, VDD OVP, OLP, SCP, OTP etc.

OB2571x consumes less than 75mW input power at no-load condition with high line voltage. OB2571x is offered in SOP8 package.

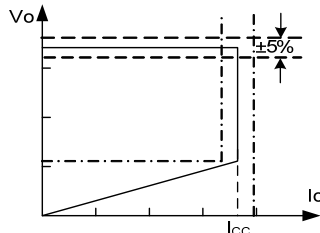
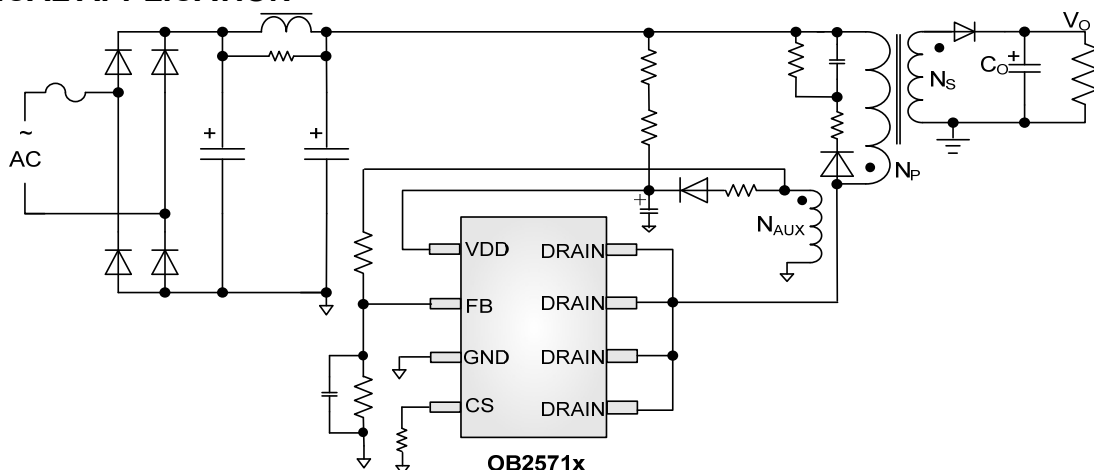


Figure.1. Typical CC/CV Curve

### TYPICAL APPLICATION



### FEATURES

- Primary-side sensing and regulation operates in QR mode without TL431 and opto-coupler
- High precision constant voltage and current regulation at universal AC input
- Programmable CV and CC regulation
- Integrated power MOSFET
- Good dynamic response
- Programmable Brownout Protection and Line OVP Protection (For 2571Lx only)
- Built-in line compensation for tight CC regulation
- Built-in fixed cable compensation
- Built-in primary winding inductance compensation
- Built-in control loop compensation
- Built-in leading edge blanking (LEB)
- Ultra low start-up current and low operating current
- Comprehensive protection coverage with auto-recovery
  - VDD over voltage protection (VDD OVP)
  - VDD under voltage lockout with hysteresis (UVLO)
  - Cycle-by-cycle current limiting
  - Feedback open loop protection (OLP)
  - Output short circuit protection (SCP)

### APPLICATIONS

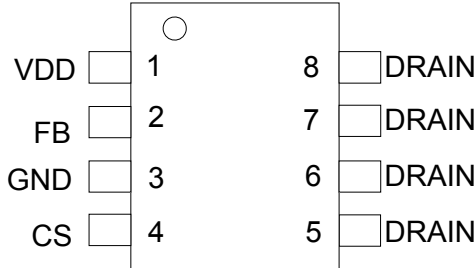
Medium level Power AC/DC offline SMPS for

- Cell phone charger
- Tablet PC
- AC/DC adapter
- Set-top box power supplies

### GENERAL INFORMATION

#### Pin Configuration

The pin map is shown as below for SOP8.



#### Ordering Information

Part Number	Description
OB2571TCP	SOP8, Halogen-free in Tube
OB2571TCPA	SOP8, Halogen-free in T&R
OB2571ATCP-H	SOP8, Halogen-free in Tube
OB2571ATCPA-H	SOP8, Halogen-free in T&R
OB2571LTCP	SOP8, Halogen-free in Tube
OB2571LTCPA	SOP8, Halogen-free in T&R
OB2571ALTCP	SOP8, Halogen-free in Tube
OB2571ALTCPA	SOP8, Halogen-free in T&R

#### Package Dissipation Rating

Package	R $\theta$ JA (°C/W)
SOP8	85

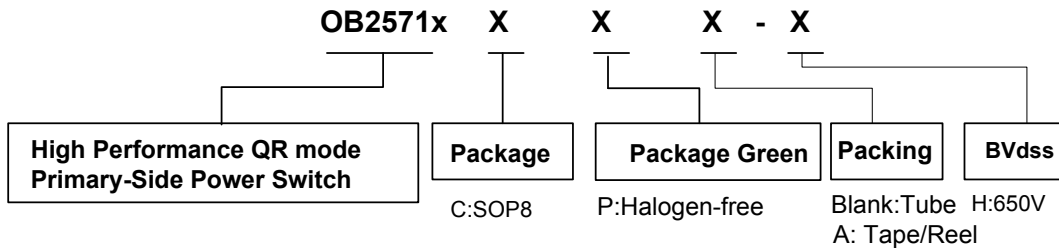
#### Absolute Maximum Ratings

Parameter	Value
VDD Voltage	-0.3 to 30V
FB Input Voltage	-0.3 to 7V
Drain Voltage (off state)	-0.3 to Bvdss
CS Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T <sub>J</sub>	-40 to 150 °C
Operating Temperature T <sub>A</sub> Ambient	-20 to 85 °C
Min/Max Storage Temperature T <sub>stg</sub>	-55 to 150 °C
Lead Temperature (Soldering, 10secs)	260 °C

**Note:** Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

#### Recommended Operating Condition

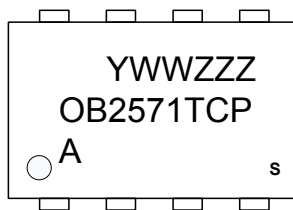
Symbol	Parameter	Range
VDD	VDD Supply Voltage	9 to 25V



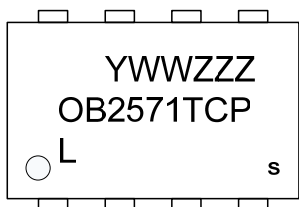
## Marking Information



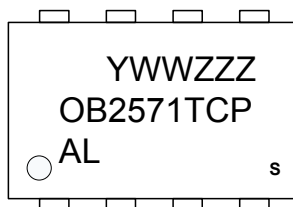
Y:Year Code  
WW:Week Code(01-52)  
ZZZ:Lot Code  
C:SOP8 Package  
P:Halogen-free Package  
S:Internal Code(Optional)



Y:Year Code  
WW:Week Code(01-52)  
ZZZ:Lot Code  
C:SOP8 Package  
P:Halogen-free Package  
A:Character Code  
S:Internal Code(Optional)



Y:Year Code  
WW:Week Code(01-52)  
ZZZ:Lot Code  
C:SOP8 Package  
P:Halogen-free Package  
L:Character Code  
S:Internal Code(Optional)

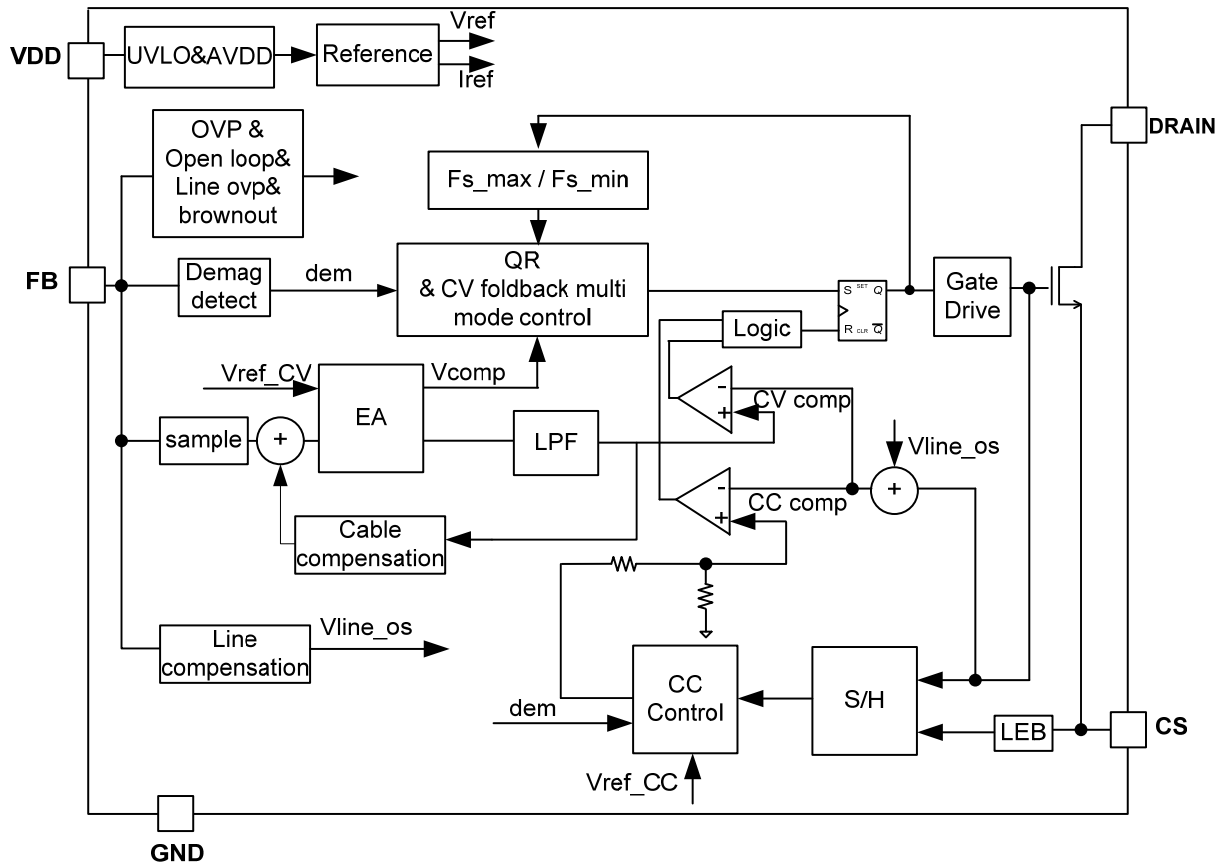


Y:Year Code  
WW:Week Code(01-52)  
ZZZ:Lot Code  
C:SOP8 Package  
P:Halogen-free Package  
AL:Character Code  
S:Internal Code(Optional)

## TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	VDD	P	Power Supply
2	FB	I	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
3	GND	P	Ground
4	CS	I	Current sense input. Connect a sense resistor from this pin to ground.
5,6,7,8	DRAIN	O	Internal MOSFET DRAIN output

**BLOCK DIAGRAM**

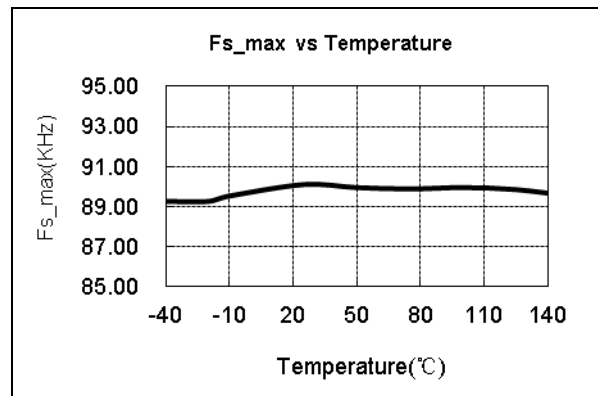
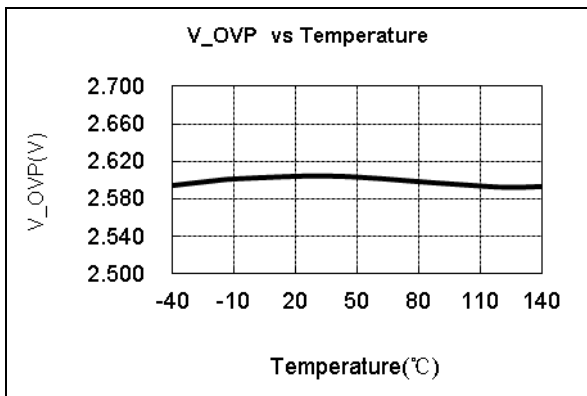
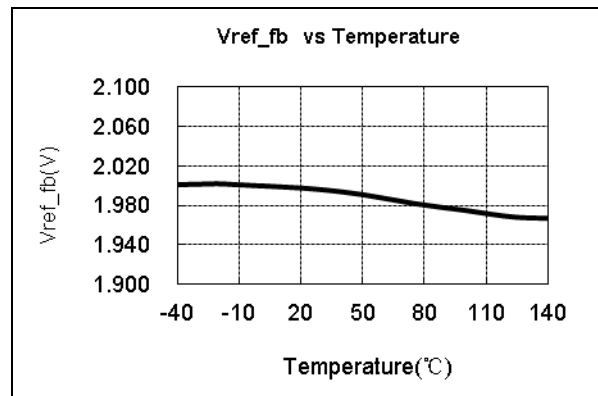
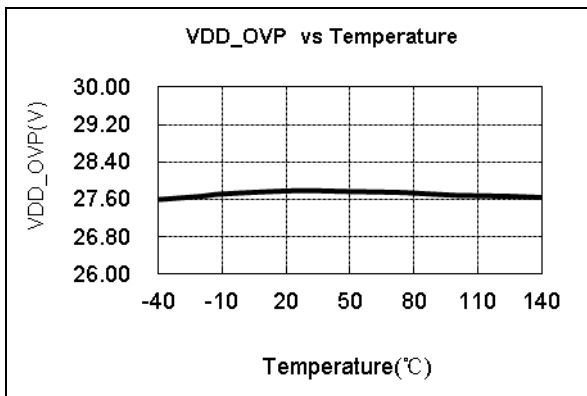
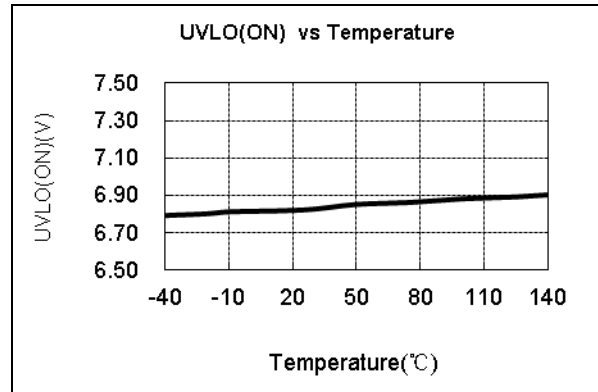
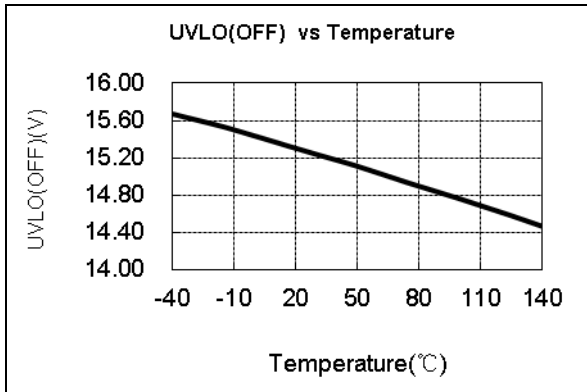


## ELECTRICAL CHARACTERISTICS

(TA = 25°C, VDD=18V, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
<b>Supply Voltage (VDD) Section</b>						
I <sub>start-up</sub>	Start up current	VDD=UVLO_OFF-1V		5	15	uA
I <sub>standby</sub>	Standby current			0.9	1.0	mA
I <sub>op_s</sub>	Operating current	FB=1V		2.2	2.5	mA
UVLO(OFF)	VDD under voltage lockout exit		13.8	15.4	16.6	V
UVLO(ON)	VDD under voltage lockout enter		6.5	7	7.5	V
VDD_OVP	VDD over voltage protection		26	28	30	V
<b>Current Sense Input Section</b>						
TLEB	LEB time			325		ns
TD_OC	OCP propagation delay			100		ns
V <sub>th_ocp_max</sub>	Maximum over current threshold			800		mV
V <sub>cs_dpfm</sub>	DPFM mode Minimum CS threshold			175		mV
<b>FB Input Section</b>						
V <sub>ref_fb</sub>	Reference voltage for feedback threshold		1.98	2	2.02	V
V_OVP	Output Over voltage threshold		2.5	2.6	2.7	V
I_BO	Brown-out threshold current	For OB2571Lx only		675		uA
T <sub>d_BO</sub>	Brown-out protection debounce Time	For OB2571Lx only		40		ms
I <sub>lineovp</sub>	Line OVP threshold current	For OB2571Lx only		2.4		mA
T <sub>d_lineovp</sub>	Line OVP debounce time	For OB2571Lx only		120		ms
V <sub>th_cc_shutdown</sub>	CC mode shut down threshold			1.2		V
T <sub>db<sub>s</sub>_cc_shutdown</sub>	CC mode shut down debounce time		39	45	50	ms
Δ <sub>cable_max</sub> /V <sub>out</sub>	Maximum cable compensation to V <sub>out</sub> ratio	OB2571xCP		2		%
		OB2571AxCP		4		%
<b>CC Loop Section</b>						
V <sub>ref_cc</sub>	CC loop reference		329	335	341	mV
G <sub>m</sub>	CC loop integrator transconductance			1		us
<b>Timer Section</b>						
F <sub>s_max</sub>	CV QR maximum frequency		85	90	95	KHz
F <sub>min</sub>	Minimum switch frequency		0.35	0.4	0.45	KHz
<b>Internal OTP Section</b>						
OTP_int_enter	internal OTP enter temperature			150		°C
OTP_int_exit	internal OTP exit temperature			130		°C
<b>MOSFET Section</b>						
BV <sub>dss</sub>	Mosfet Drain-Source Breakdown Voltage		600			V
		For OB2571AT only	650			V
R <sub>dson</sub>	Static drain to source on resistance			2		Ω
		For OB2571AT only		2.2		Ω

## CHARACTERIZATION PLOTS



### OPERATION DESCRIPTION

OB2571x is an excellent integrated multi-mode (see Figure 2) PWM controller optimized for off-line middle power AC/DC applications. It operates in quasi-resonant mode (QR) to provide high efficiency with primary side sensing and regulation thus provides cost effective solution for energy efficient power supplies.

At full loading, the IC operates in QR mode in the universal line input voltage. In this way, high efficiency in the universal input range at full loading can be achieved.

At normal load condition, it operates in QR mode. To minimize switching loss, the maximum switching frequency in QR mode is internally limited to 90 KHz (typical). When the load goes low, it operates in PFM mode with valley switching for high power conversion efficiency. When the load is very small, the IC switch frequency can be reduced to 0.4KHz to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

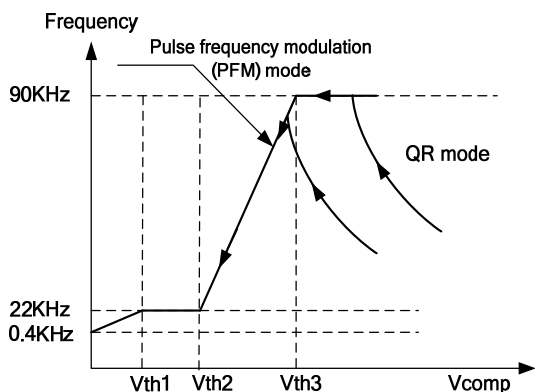


Figure 2 Multi-mode operation diagram  
Proprietary built-in CV and CC control can achieve high precision CC/CV control meeting most charger application requirements.

#### Startup Current and Start Up Control

Startup current of OB2571x is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

#### Operating Current

The Operating current of OB2571x is as low as around 850uA @ no load mode. Good efficiency and less than 75mW standby power is achieved with the low operating current.

#### CV Mode Operation

OB2571x is designed to produce good CC/CV control characteristic as shown in the Figure. 1. In charger applications, a discharged battery

charging starts in the CC portion of the curve until it is nearly full charged and smoothly switches to operate in CV portion of the curve. The CC portion provides output current limiting. In CV operation, the output voltage is regulated through the primary side control. In CC operation mode, OB2571x will regulate the output current constant regardless of the output voltage drop.

#### Principle of Operation

With OB2571x proprietary CC/CV control, system can be designed in QR/DCM mode for flyback system (Refer to the Typical Application Diagram in page1).

In the flyback converter, the output voltage can be sensed via the auxiliary winding. During MOSFET turn-on time, the load current is supplied from the output filter capacitor and the current in the primary winding ramps up. When MOSFET turns off, the energy stored in the primary winding is transferred to the secondary side and the current in the secondary winding is

$$I_S = \frac{N_P}{N_S} \cdot I_P \tag{1}$$

The auxiliary winding voltage reflects the output voltage as shown in Figure.3 and it is given by

$$V_{AUX} = \frac{N_{AUX}}{N_S} \cdot (V_O + \Delta V) \tag{2}$$

Where  $\Delta V$  indicates the voltage drop of the output Diode.

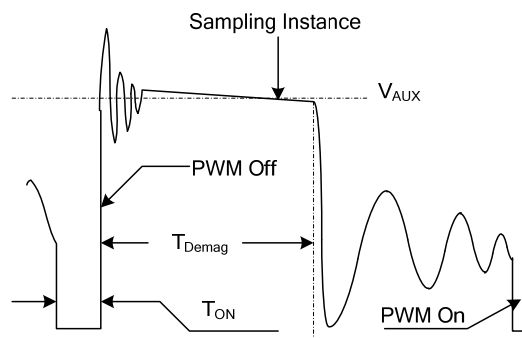


Figure.3. Auxiliary winding voltage waveform  
Via a resistor divider connected between the auxiliary winding and FB PIN, the auxiliary voltage is sampled and hold during the demagnetization cycle. The sampling instance is variable according to the demagnetization width. The output voltage can be monitored when the secondary current is small. Thus  $\Delta V$  can be ignored. The sampled voltage is compared with reference voltage Vref (typical 2.0V) and the difference is amplified. The error amplifier output reflects the load condition and controls the switching off time to regulate the output voltage, thus constant output voltage can

be achieved.

### CC Mode Operation

OB2571x sample the CS peak and the transformer core demagnetization period to regulate to output current. The primary CS peak is adaptively controlled according to  $v_{ref\_cc}$  and the internal CC comp voltage.

$$I_o = \frac{1}{2} \cdot N \cdot I_{pk} \cdot \frac{T_{demag}}{T_s} = \frac{1}{2} \cdot N \cdot \frac{1}{R_{cs}} \cdot \frac{V_{cs} T_{demag}}{T_s} \quad (3)$$

Where  $I_{pk}$  is the peak current of primary winding,  $T_{demag}$  is the transformer core demagnetization period, and  $T_s$ , the switch period.

Refer to the equation 3, Regulating the  $I_{pk}$  can achieve the constant output current. The constant output current is independent of the primary

winding inductance. The ratio of  $\frac{V_{cs} T_{demag}}{T_s}$  will

be modulated equal to  $v_{ref\_cc}$  which is 0.335V. Then  $I_o$  can be determined by

$$I_o = \frac{1}{2} \cdot N \cdot \frac{1}{R_{cs}} \cdot \frac{V_{cs} T_{demag}}{T_s} = \frac{1}{2} \cdot N \cdot \frac{v_{ref\_cc}}{R_{cs}} \quad (4)$$

### Adjustable CC Point and Output Power

In OB2571x, the CC point and maximum output power can be externally adjusted by external current sense resistor  $R_s$  at CS pin as illustrated in the typical application diagram. The larger the  $R_s$  is, the smaller CC point is, and the smaller output power becomes, and vice versa as shown in Figure.4.

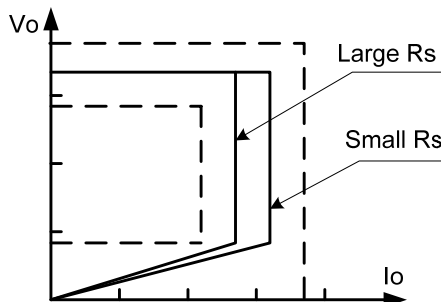


Figure.4. Adjustable output power by changing  $R_s$

### CC Line Voltage Compensation

The variation of maximum output current in CC mode can be rather large at high input voltage (such as 264Vac) if no compensation is provided. The CC threshold value is self adjusted higher at higher AC voltage due to CC propagation delay. In OB2571x, the AC line voltage information is sampled through detecting FB sourcing current when gate turns on, and the AC line voltage information is added to the CS pin voltage. So the maximum CS threshold voltage  $V_{cs\_max}$  in OB2571x is a function of the CC threshold and AC line voltage information as shown in Figure5.

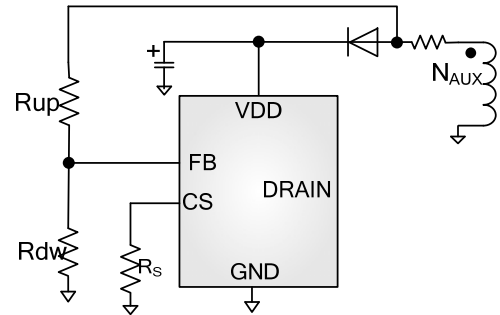


Figure.5. CC line voltage compensation

The CS threshold voltage  $V_{cs}$  is given by

$$V_{cs} = V_{th\_cc} - \frac{1}{M} \cdot \frac{N_{aux}}{N_p} \cdot \sqrt{2} \cdot V_{ac} \cdot \frac{R_{os}}{R_{up}} \quad (5)$$

Where  $V_{th\_cc}$  threshold determined by internal CC comp voltage,  $M$  is the FB current mirror ratio ( $M=150$ ),  $N_{aux}/N_p$  is the auxiliary winding to primary winding turns ratio,  $V_{ac}$  is the effective voltage of input voltage,  $R_{os}$  is the internal line compensation offset resistor ( $R_{os}=3.45Kohm$ ),  $R_{up}$  is the external FB PIN up side resistor.

### Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2571x. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on state so that the external RC filtering on sense input is no longer needed.

### Programmable Brownout Protection and Line OVP Protection

By monitoring the current flowing out of FB PIN ( $I_{fb}$ ) when the primary MOS is turned on, the controller protects the SMPS against the abnormal condition, as shown in Fig.5. When  $I_{fb}$  falls below  $I_{BO}$  (675uA), brownout is triggered, the controller stops pulsing after 40ms later. when  $I_{fb}$  is above  $I_{lineovp}$  (2.4mA), line OVP is triggered and stops pulsing after 120ms later.

The current flowing out of FB PIN ( $I_{fb}$ ) is

$$I_{fb} = I_{dw} + I_{up} = \frac{V_{FB}}{R_{dw}} + \frac{V_{FB} + V_{aux}}{R_{up}}$$

The protection voltage of brownout is:

$$V_{in\_BO} = (I_{BO} - \frac{V_{FB}}{R_{dw}} - \frac{V_{FB}}{R_{up}}) \cdot \frac{R_{up} \cdot N_p}{\sqrt{2} \cdot N_{aux}}$$

The protection voltage of line ovp is:

$$V_{in\_lineovp} = (I_{lineovp} - \frac{V_{FB}}{R_{dw}} - \frac{V_{FB}}{R_{up}}) \cdot \frac{R_{up} \cdot N_p}{\sqrt{2} \cdot N_{aux}}$$

Where  $N_p$  is the turns of primary inductor,  $N_{aux}$  is the turns of auxiliary inductor,  $R_{up}$  is the external FB PIN up side resistor,  $R_{dw}$  is the external FB PIN low side resistor,  $V_{FB}$  is the clamping voltage of FB PIN when the primary MOS is turned on,



$V_{AUX}$  is the voltage of auxiliary inductor when the primary MOS is turned on.

### Internal Over Temperature Protection with GATE Shutdown

The internal OTP circuit of OB2571x is triggered and only shuts down the internal MOSFET when the chip temperature rises above 150°C, and the internal MOSFET will resume switching after the chip temperature falls below 130°C.

### Protection Control

Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting, Output over voltage protection, VDD over voltage protection, short circuit protection, Under Voltage Lockout on VDD.

VDD is supplied by transformer auxiliary winding output after startup. The output of OB2571x is shut down when VDD drops below UVLO (ON) and the power converter enters power on start-up sequence thereafter.

### CC mode shutdown function

In OB2571x, to prevent the controller operating under abnormal conditions, the minimum output voltage of CC mode is limited to predetermined voltage. The CC output voltage is sampled through FB pin from auxiliary winding at the middle of the de-magnetization. When the FB sampled voltage

is below 1.2V and last 45ms, the controller will shut down.

### PCB Layout Consideration

The following rules should be followed in OB2571x PCB Layout:

**The Area of Power Loop:** The area of the main current loop should be as small as possible to reduce EMI radiation, such as the primary current loop, the snubber circuit and the secondary rectifying loop (Red wire as shows in Fig.6). Drain pin increases the copper area of the drain terminal for heat dissipation (Green region as shows in Fig.7). And the PCB trace must be wide and short for thermal consideration.

**Bypass Capacitor and FB Divider Resistor:** The bypass capacitor on VDD and the FB divider resistor should be placed as close as possible to pin out. And the negative node of VDD capacitor and the FB down resistor should be connected directly to the IC GND pin before single point connected to the negative node of the output capacitor. (Blue wire as shows in Fig.6)

**Ground Path:** The GND path of the input power loop and IC controller path should be separated and connected at the negative terminal of input capacitor by single point, such as power sense resistor, the negative of the auxiliary winding and the IC GND. (White region as shows in Fig.7)

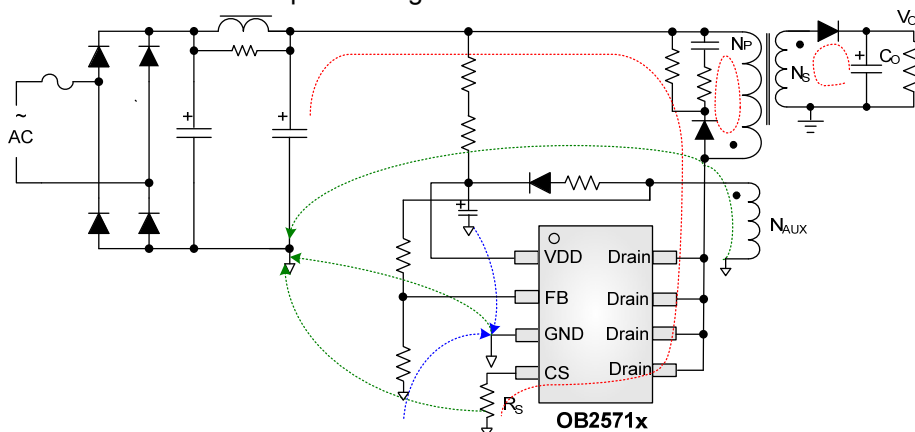


Fig.6 Flyback Schematic with OB2571x

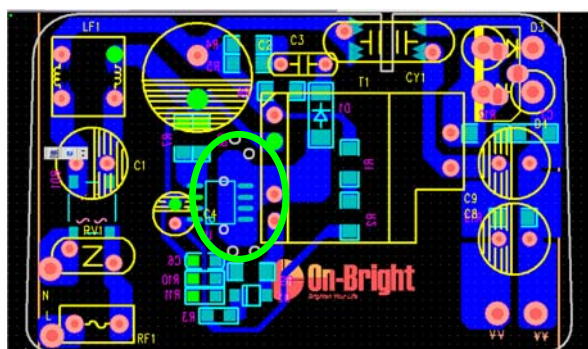
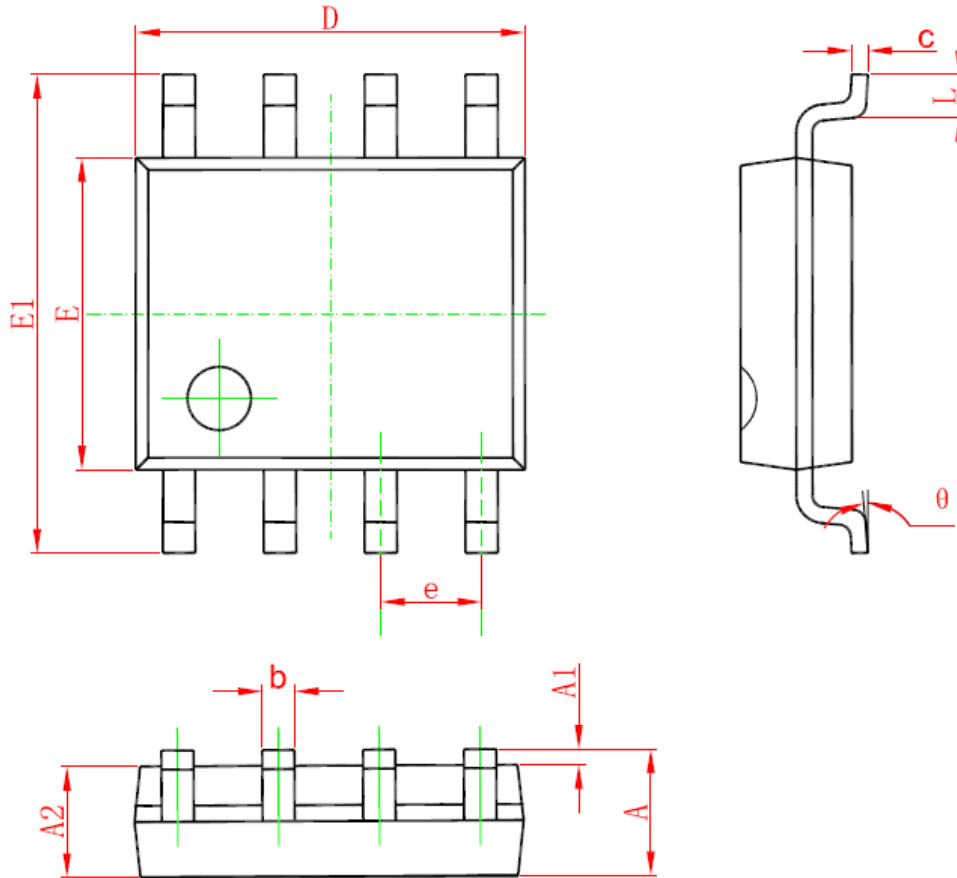


Fig.7 Recommend PCB Layout of OB2571x

**PACKAGE MECHANICAL DATA**

**SOP8 PACKAGE OUTLINE DIMENSIONS**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	4.700	5.150	0.185	0.203
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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