Description

The SMDAxxC series of TVS arrays are designed to provide bidirectional protection for sensitive electronics from damage or latch-up due to ESD, lightning and other voltage-induced transient events. Each device will protect four data or I/O lines. They are available with operating voltages of 5V, 12V, 15V and 24V.

TVS diodes are solid-state devices designed specifically for transient suppression. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage and no device degradation. The low profile SO-8 package allows the user to protect up to four independent lines with one package. The SMDAxxC series is suitable protection for sensitive semiconductors components such as microprocessors, ASICs, transceivers, transducers, and CMOS memory.

The SMDAxxC series devices may be used to meet the ESD immunity requirements of IEC 61000-4-2, level 4 for air and contact discharge.

Mechanical Characteristics

- JEDEC SO-8 package
- Molding compound flammability rating：UL 94V-0
- Marking：Part number
- Packaging: Tube or Tape and Reel per EIA 481

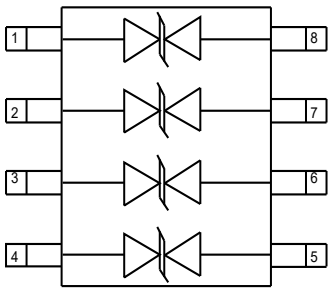
Features

- Transient protection for data lines to
  IEC 61000-4-2(ESD) ±15KV(air), ±8KV(contact)
  IEC 61000-4-4(EFT) 40A(5/50ns)
  IEC 61000-4-5(Lightning)12A(8/20μs)
- Bidirectional protection
- Small SO-8 package
- Protects four I/O lines
- Working voltages: 5V, 12V, 15V and 24V
- Low leakage current
- Low operating and clamping voltages
- Solid-state silicon avalanche technology

Applications

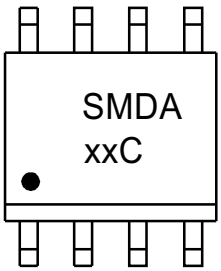
- Data and I/O lines
- Microprocessor based equipment
- Notebooks, Desktops, and Servers
- Instrumentation
- LAN/WAN equipment
- Peripherals
- Serial and Parallel Ports

Dimensions and Pin Configuration



SO-8（ Top View）

Marking Information



xx represents the voltage
Dot denotes Pin1

Ordering Information

Part Number	Marking	Packaging	Reel Size
SMDAxxC	SMDAxxC	2500/Tape & Reel	13 inch

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power(8/20μs)	Ppk	300	W
Esd Voltage (HBM per IEC 61000-4-2)	V_{ESD}	>25	KV
Lead Soldering Temperature	T_L	260(10 sec.)	°C
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

SMDA05C (Marking Code:SMDA05C)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
Reverse Working Voltage	V_{RWM}			5	V	
Reverse Breakdown Voltage	V_{BR}	6			V	I_T = 1mA
Reverse Leakage Current	I_R			20	μA	V_{RWM} = 5V,T=25°C
Clamping Voltage	V_C			9.8	V	I_{PP} = 1A (8 x 20μs pulse)
Clamping Voltage	V_C			11	V	I_{PP} = 5A (8 x 20μs pulse)
Maximum Peak Pulse Current	I_{PP}			17	A	tp=8/20μs
Junction Capacitance	C_J			350	pF	VR = 0V, f = 1MHz

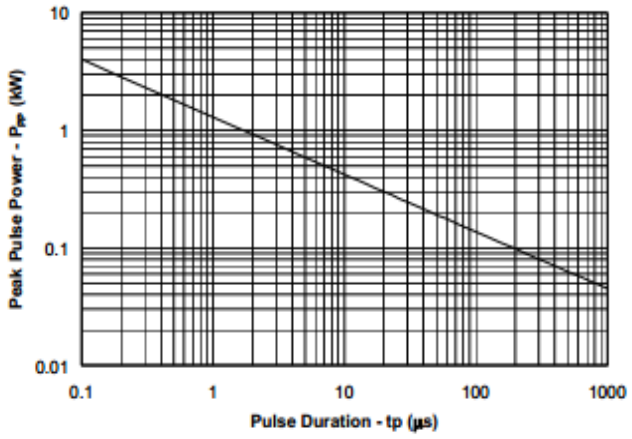
SMDA12C (Marking Code:SMDA12C)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
Reverse Working Voltage	V_{RWM}			12	V	
Reverse Breakdown Voltage	V_{BR}	13.3			V	I_T = 1mA
Reverse Leakage Current	I_R			1	μA	V_{RWM} = 12V,T=25°C
Clamping Voltage	V_C			19	V	I_{PP} = 1A (8 x 20μs pulse)
Clamping Voltage	V_C			24	V	I_{PP} = 5A (8 x 20μs pulse)
Maximum Peak Pulse Current	I_{PP}			12	A	tp=8/20μs
Junction Capacitance	C_J			120	pF	VR = 0V, f = 1MHz

SMDA15C (Marking Code:SMDA15C)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
Reverse Working Voltage	V_{RWM}			15	V	
Reverse Breakdown Voltage	V_{BR}	16.7			V	I_T = 1mA
Reverse Leakage Current	I_R			1	μA	V_{RWM} = 15V,T=25°C
Clamping Voltage	V_C			24	V	I_{PP} = 1A (8 x 20μs pulse)
Clamping Voltage	V_C			30	V	I_{PP} = 5A (8 x 20μs pulse)
Maximum Peak Pulse Current	I_{PP}			10	A	tp=8/20μs
Junction Capacitance	C_J			75	pF	VR = 0V, f = 1MHz

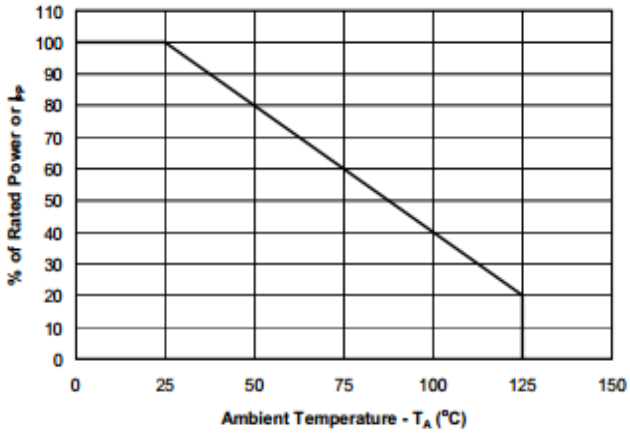
SMDA24C (Marking Code:SMDA24C)						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Condition**
Reverse Working Voltage	V_{RWM}			24	V	
Reverse Breakdown Voltage	V_{BR}	26.7			V	I_T = 1mA
Reverse Leakage Current	I_R			1	μA	V_{RWM} = 24V,T=25°C
Clamping Voltage	V_C			43	V	I_{PP} = 1A (8 x 20μs pulse)
Clamping Voltage	V_C			55	V	I_{PP} = 5A (8 x 20μs pulse)
Maximum Peak Pulse Current	I_{PP}			5	A	tp=8/20μs
Junction Capacitance	C_J			50	pF	VR = 0V, f = 1MHz

Typical Characteristics

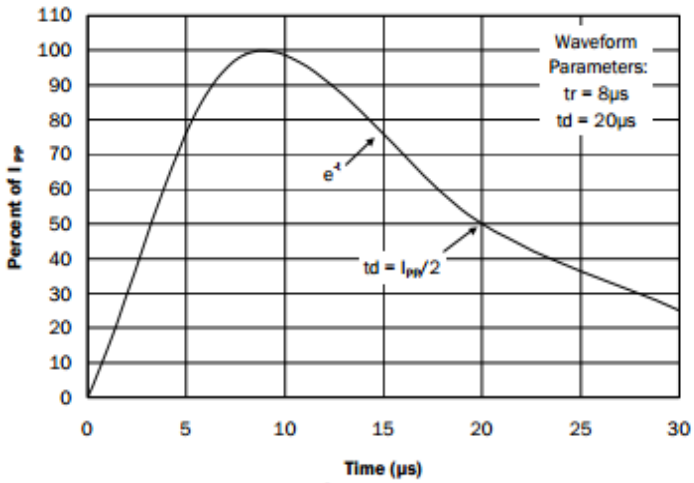
Non-Repetitive Peak Pulse Power vs. Pulse Time



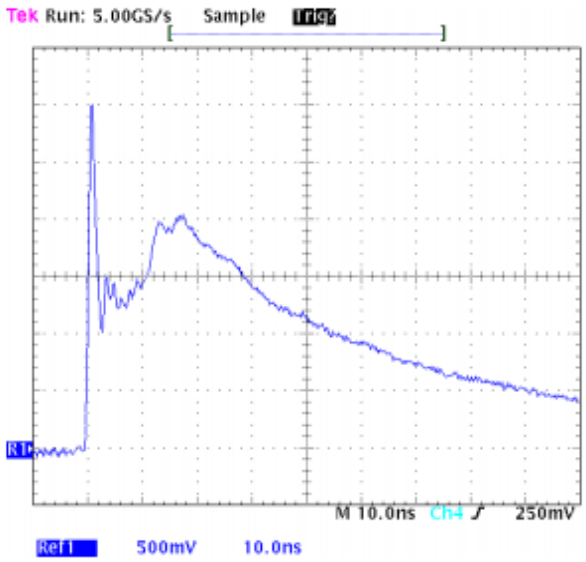
Power Derating Curve



Pulse Waveform



ESD Pulse Waveform (IEC 61000-4-2)



IEC 61000-4-2 Discharge Parameters

Level	First Peak Current (A)	Peak Current at 30 ns (A)	Peak Current at 60 ns (A)	Test Voltage (Contact Discharge) (kV)	Test Voltage (Air Discharge) (kV)
1	7.5	4	8	2	2
2	15	8	4	4	4
3	22.5	12	6	6	8
4	30	16	8	8	15

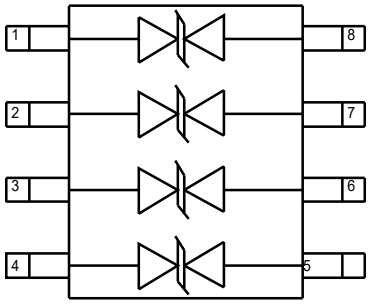
Applications Information

Device Connection for Protection of Four Data Lines

The SMDAxxC series of devices are designed to protect up to four data lines. The devices are connected as follows:

- The SMDAxxC are bidirectional devices and are designed for use on lines where the normal operating voltage is above and below ground. Pins 1, 2, 3 and 4 are connected to the protected lines. Pins 5, 6, 7 and 8 are connected to ground. Since the device is electrically symmetrical, these connections may be reversed. The ground connections should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

Circuit Diagram

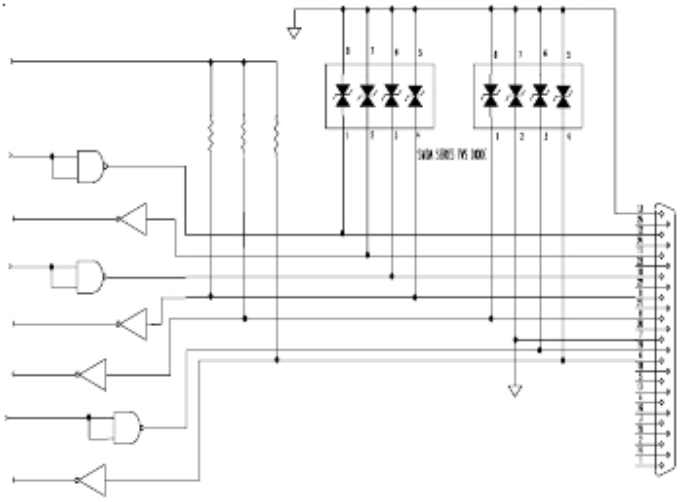


I/O Line Protection

Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induces transients. The following guidelines are recommended:

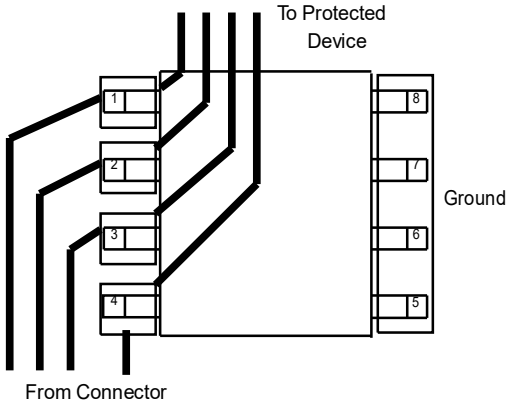
- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- THE ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.



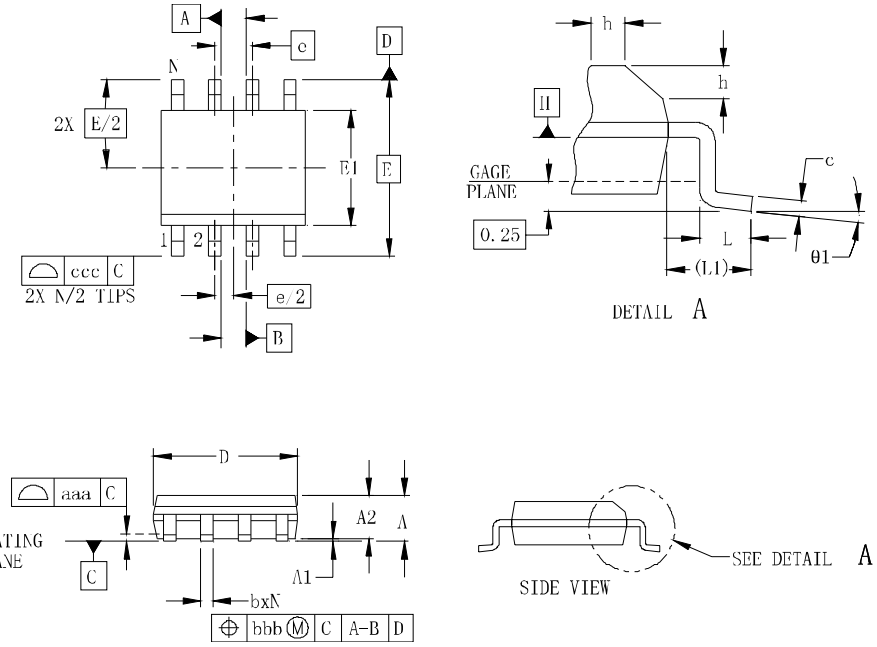
Typical Connection

Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin dose not have any added alloys that cause degradation of the solder joint.

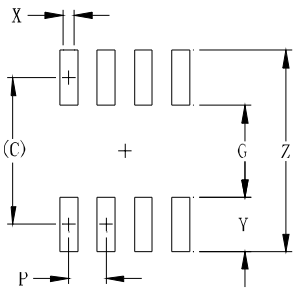


SO-8 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
E	6.00 BSC			0.236 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.40	0.72	1.04	0.016	0.028	0.041
L1	(1.04)			(0.041)		
N	8			8		
θ1	0°		8°	0°		8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	(5.20)	0.205
G	3.00	0.118
P	1.27	0.050
X	0.60	0.024
Y	2.20	0.087
Z	7.40	0.291

Contact Information

Changzhou D-first Electronics CO.,Ltd.
www.first-electronic.com
Email: yf@first-electronic.cn
Phone: +86（0519）8817 1671