TF Semiconductor Solutions

TF2190(4)M

High-Side and Low-Side Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in a half-bridge configuration**
- **Output drivers capable of 4.5A/4.5A typ sink/source**
- **Logic input (HIN and LIN) 3.3V capability**
- **Schmitt triggered logic inputs with internal pulldown**
- **Undervoltage lockout for high and low-side drivers**
- **Extended temperature range: -40°C to +125°C**

Description

The TF2190M is a high voltage, high speed gate driver capable of driving N-channel MOSFET's and IGBTs in a half-bridge configuration. TF Semi's high voltage process enables the TF2190M's high side to switch to 600V in a bootstrap operation under high dV/dt conditions.

The TF2190M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The TF2190M is offered in space saving 8-pin SOIC and the TF21904M in the 14-pin SOIC and operates over an extended -40°C to +125°C temperature range.

Applications

- Motor Controls
- DC-DC Converters
- AC-DC Inverters
- Class D Power Amplifiers

SOIC-8(N)

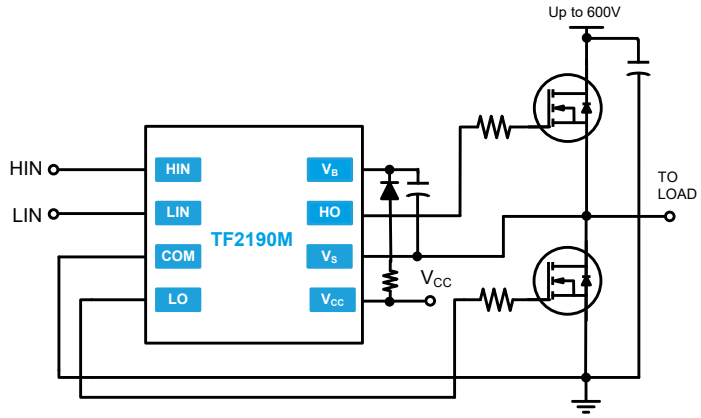
SOIC-14(N)

Ordering Information

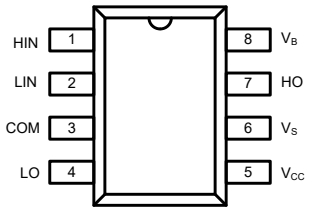
Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF2190M-TAH	SOIC-8(N)	T&R / 2500	YYWW TF2190M Lot ID
TF21904M-TUH	SOIC-14(N)	T&R / 2500	YYWW TF21904M Lot ID

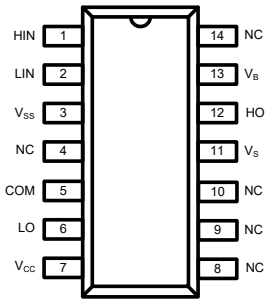
Typical Application



Pin Diagrams



Top View: SOIC-8(N), TF2190M

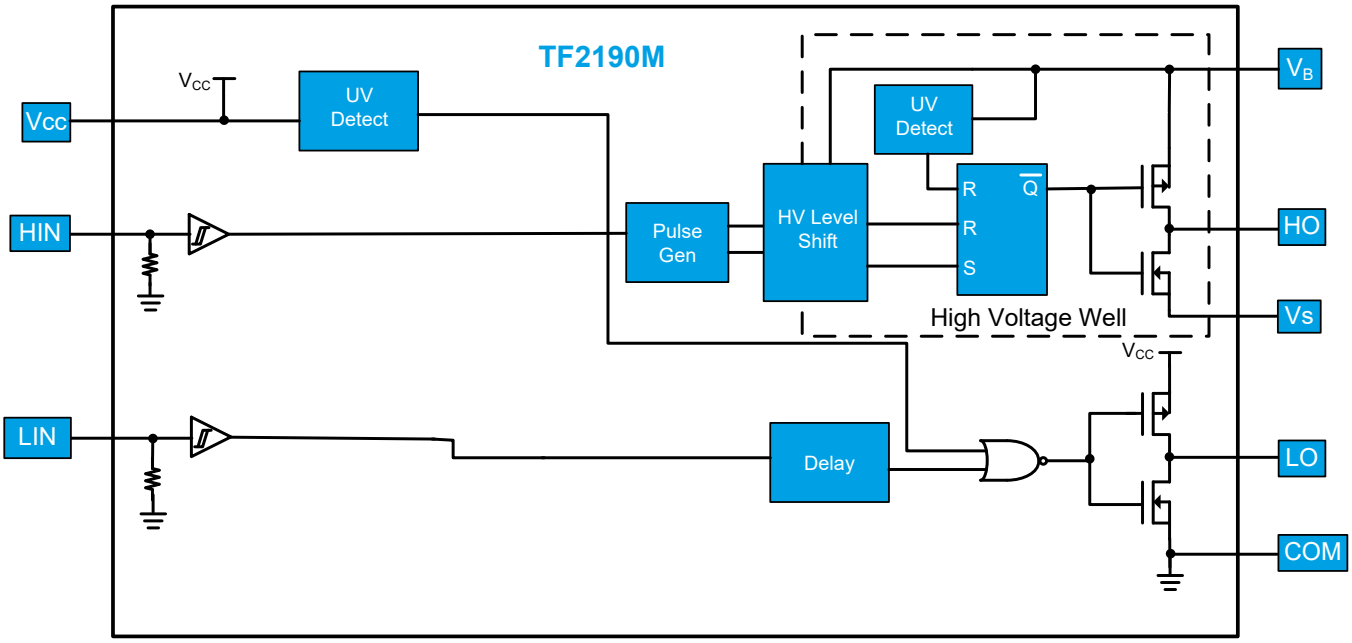


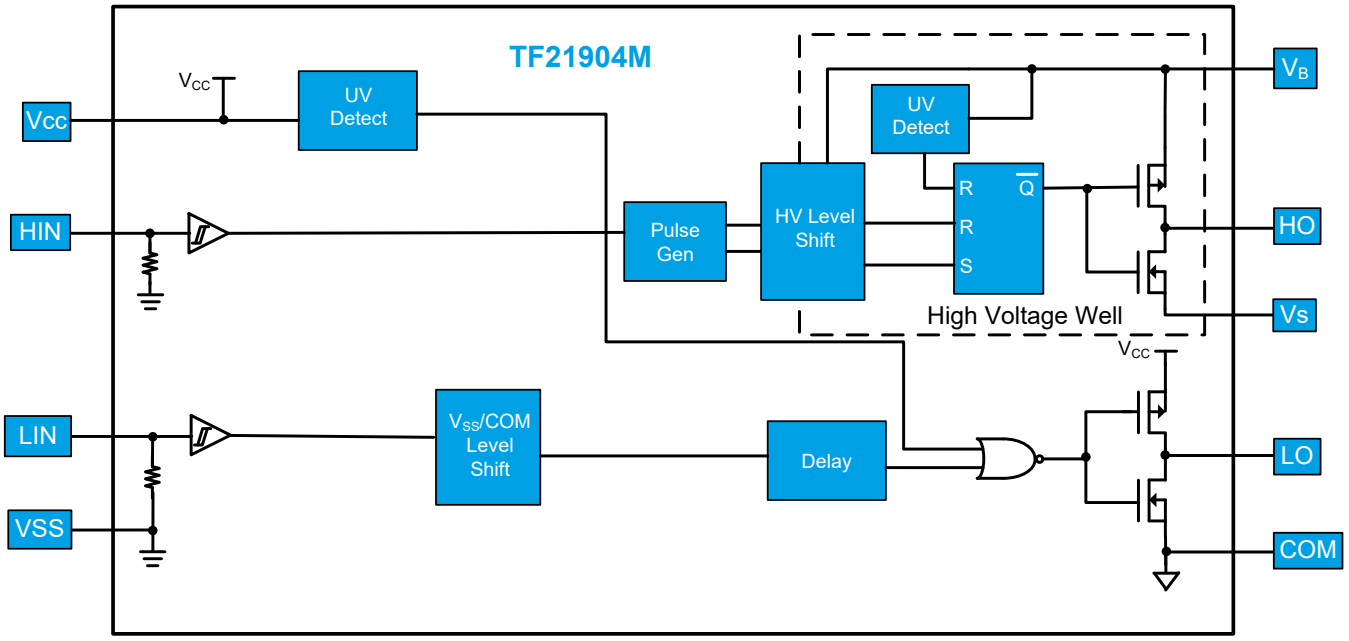
Top View: SOIC-14(N), TF21904M

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output, in phase with HO
LIN	Logic input for low-side gate driver output, in phase with LO
COM	Low-side and logic return
LO	Low-side gate drive output
V_{CC}	Low-side and logic fixed supply
V_S	High-side floating supply return
HO	High-side gate driver output
V_B	High-side floating supply
V_{SS}	Logic Ground (TF21904M only)

Functional Block Diagrams





Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{SS} - Logic Supply offset voltage.....V_{CC} -24V to V_{CC} + 0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient.....50 V/ns

V_{CC} - Low side and logic fixed supply voltage.....-0.3V to +24V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN)... -0.3V to V_{CC}+0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-8.....0.625W
SOIC-14.....0.862W

SOIC-8 Thermal Resistance ***(NOTE2)***
θ_{JC}.....45 °C/W
θ_{JA}.....200 °C/W

SOIC-14 Thermal Resistance ***(NOTE2)***
θ_{JA}.....145 °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***	600	
V_{SS}	Logic ground (TF21904 only)	-5	5	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN and LIN)	0	5	
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5V to +600V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V *NOTE5*	2.5			V
V_{IL}	Logic "0" input voltage				0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 0mA			0.1	
V_{OL}	Low level output voltage, V_O	I_O = 0mA			0.035	
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V		45	80	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V		75	200	
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		25	50	
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V		1.0	2.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		7.6	8.4	9.8	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		6.9	7.8	9.0	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		7.6	8.4	9.8	
V_{BSUV-}	V_{CC} supply under-voltage negative going threshold		6.9	7.8	9.0	
V_{CCUVH}	V_{CC} and V_{BS} under-voltage hysteresis			0.6		
V_{BSUVH}						
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 ms	3.5	4.5		A
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 ms	3.5	4.5		

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are applicable to the two logic input pins: HIN and LIN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO-*

NOTE5 *For optimal operation, it is highly recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum with a pulse width of 280ns minimum.*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propogation delay	V_S = 0V		140	200	ns
t_{off}	Turn-off propogation delay	V_S = 0V		140	200	
t_{DM}	Delay matching, HS & LS turn on/off			0	50	
t_r	Turn-on rise time	V_S = 0V		25	50	
t_f	Turn-off fall time			20	45	

Timing Waveforms

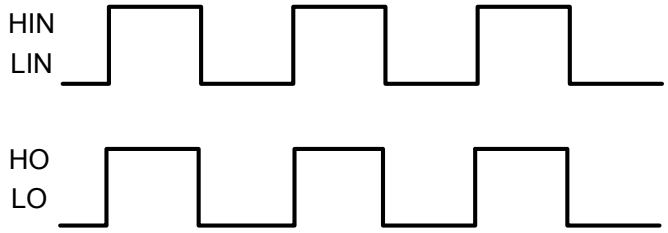


Figure 1. Input / Output Timing Diagram

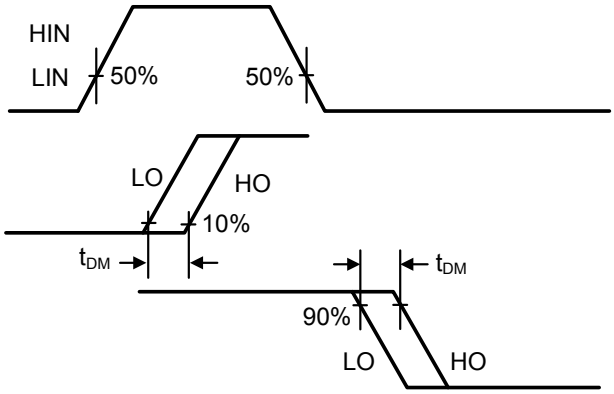


Figure 2. Delay Matching Waveform Definitions

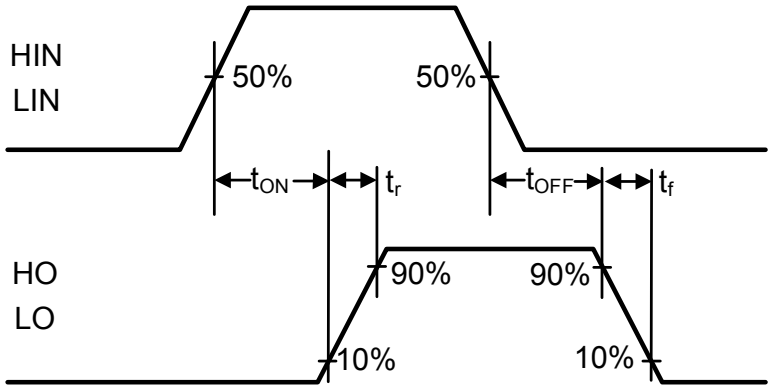


Figure 3. Switching Time Waveform Definitions

Application Information

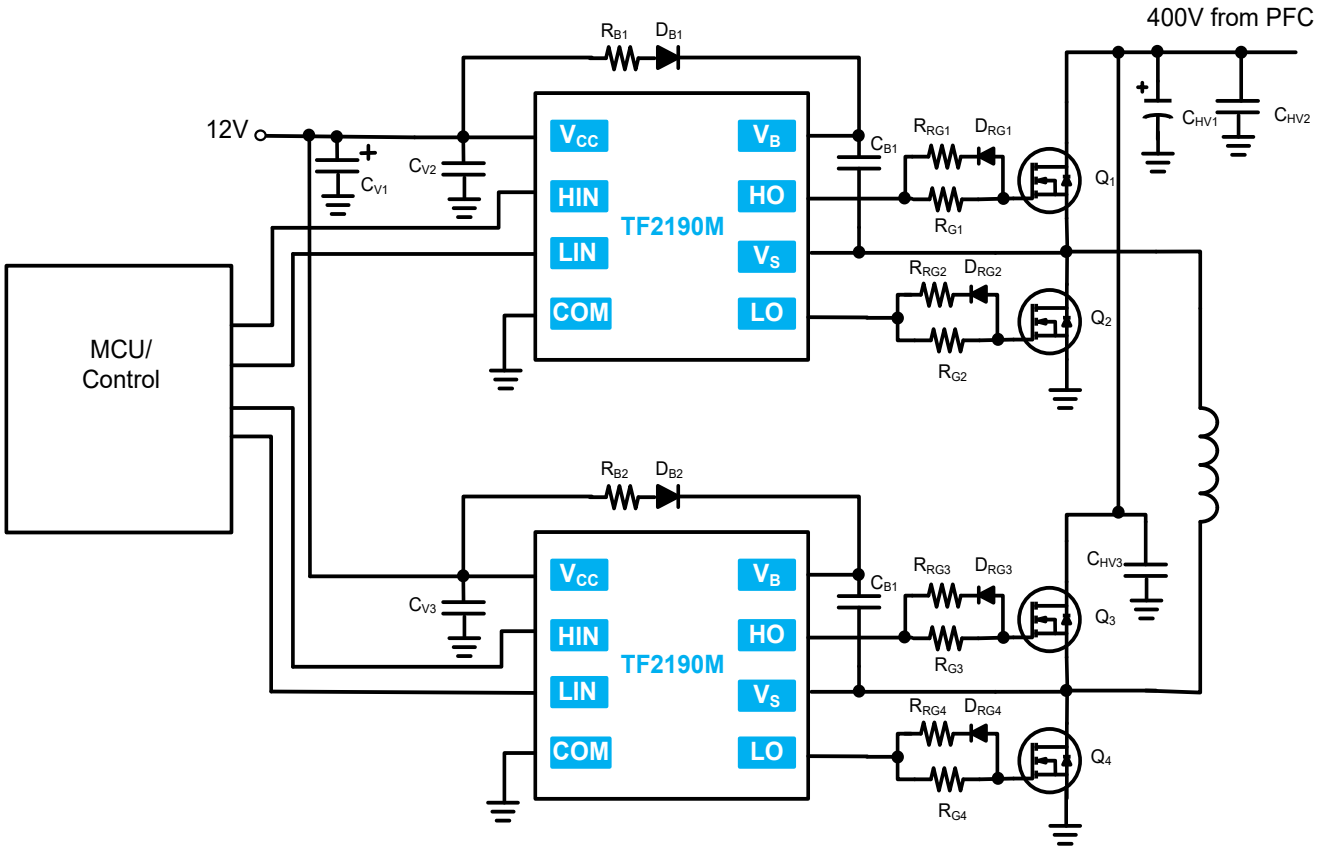


Figure 4. Primary side of Full Bridge converter using TF2190

- RRG1, RRG2, RRG3, and RRG4 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

- It is **highly recommended** that the input pulse (to HIN and LIN) should have an amplitude of 2. 5V minimum (for VDD=15V) with a minimum pulse width of 280ns

- RG1, RG2, RG3, and RG4 values are typically between 20Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RB1 and RB2 value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB1 and DB2 should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

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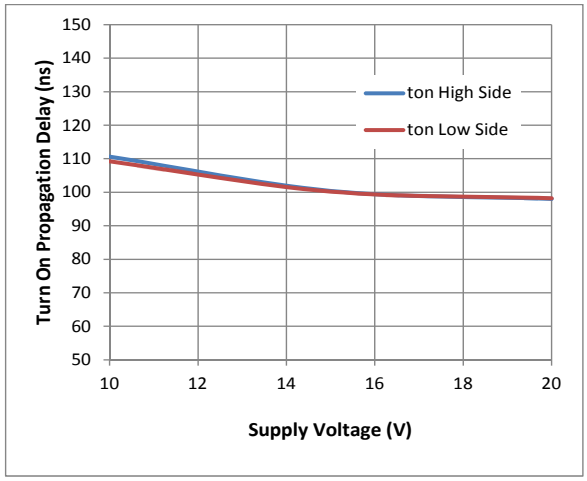


Figure 5. Turn-on Propagation Delay vs. Supply Voltage

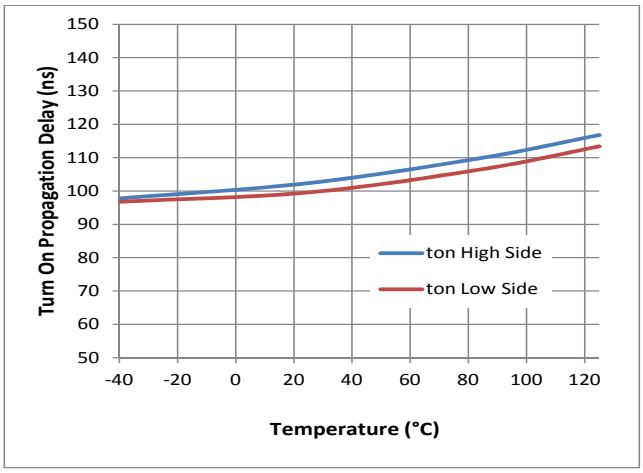


Figure 6. Turn-on Propagation Delay vs. Temperature

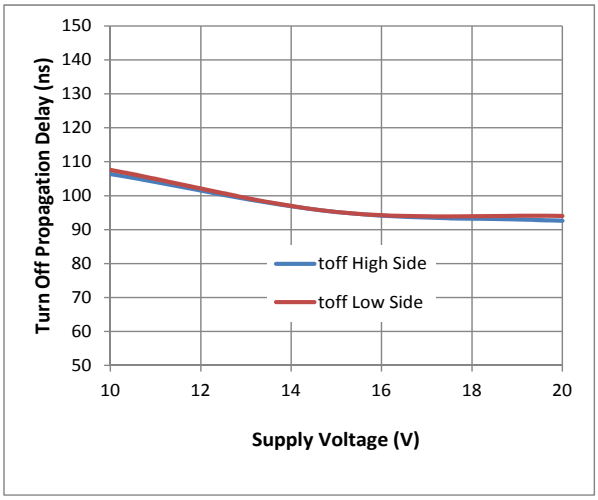


Figure 7. Turn-off Propagation Delay vs. Supply Voltage

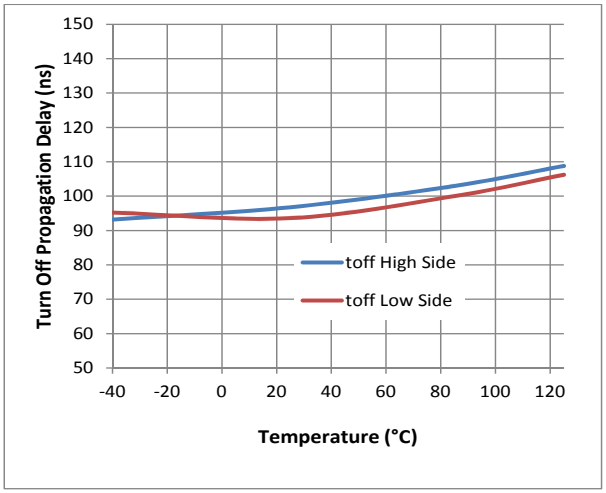


Figure 8. Turn-off Propagation Delay vs. Temperature

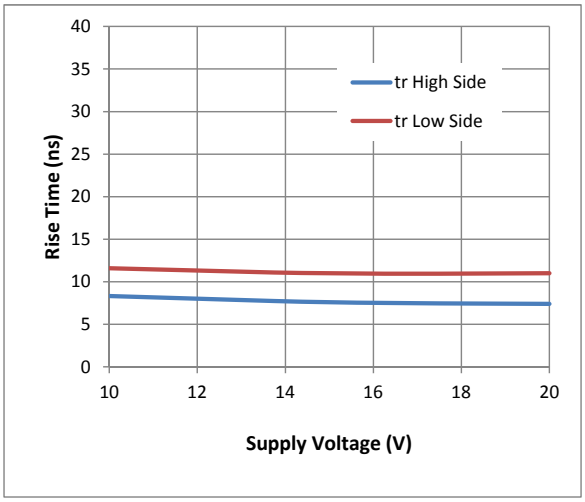


Figure 9. Rise Time vs. Supply Voltage

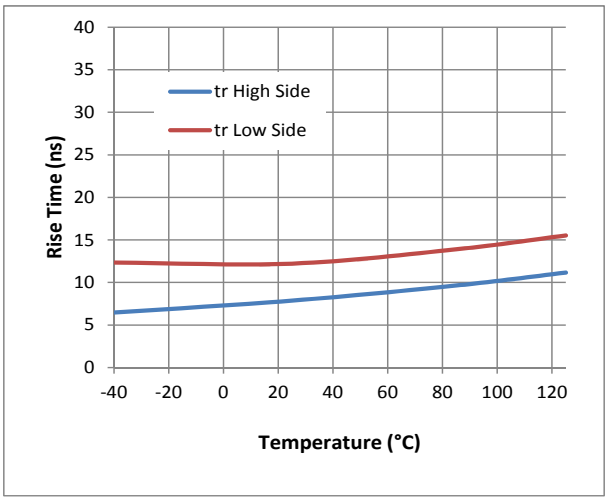


Figure 10. Rise Time vs. Temperature

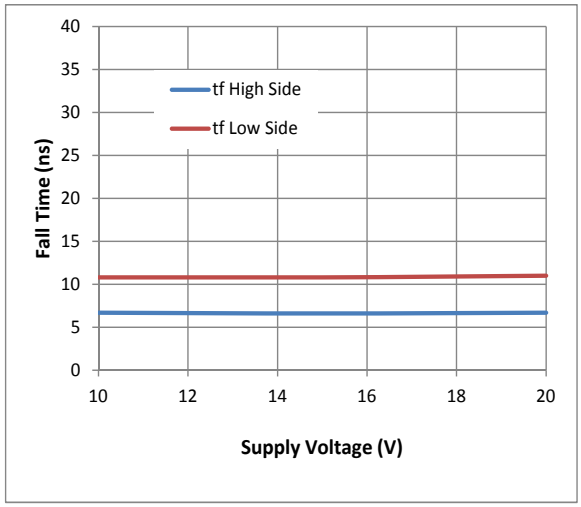


Figure 11. Fall Time vs. Supply Voltage

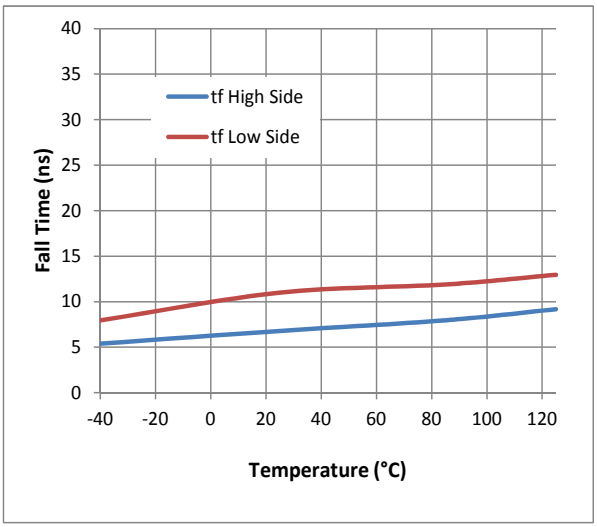


Figure 12. Fall Time vs. Temperature

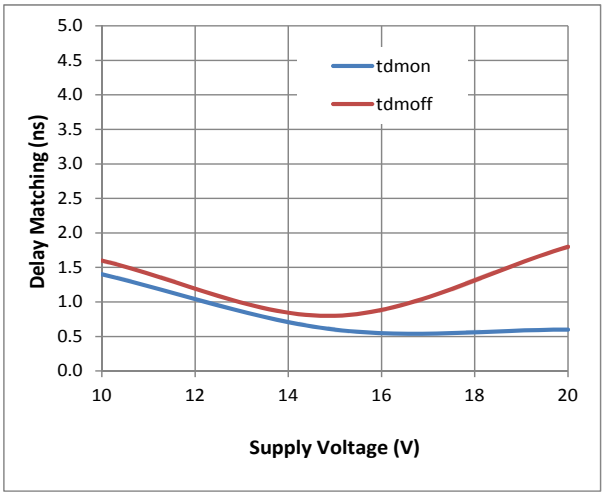


Figure 13. Delay Matching vs. Supply Voltage

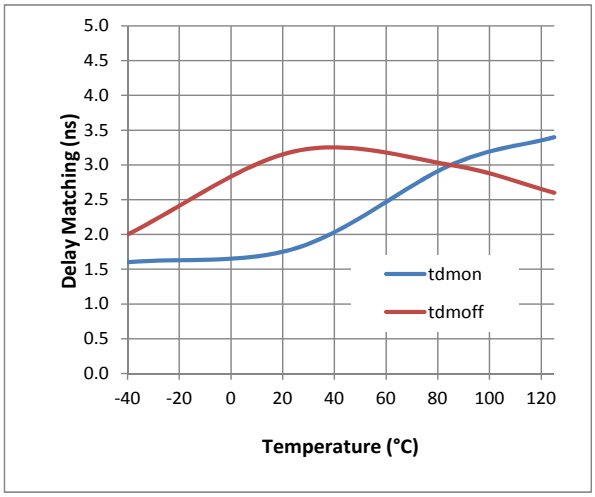


Figure 14. Delay Matching vs. Temperature

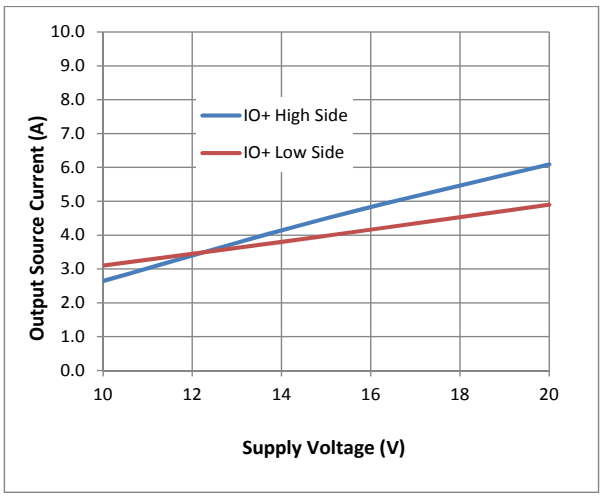


Figure 15. Output Source Current vs. Supply Voltage

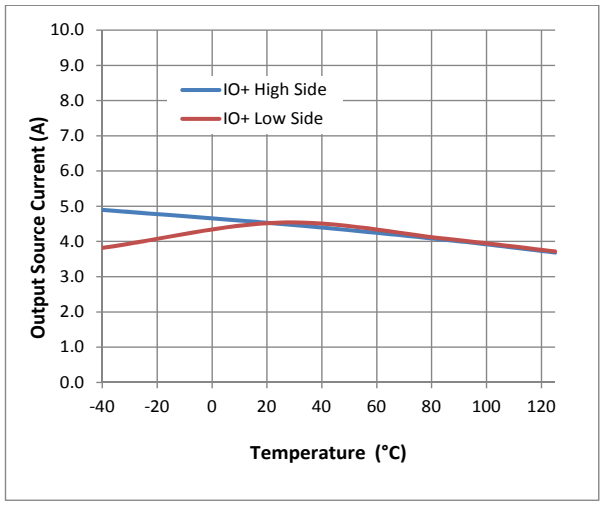


Figure 16. Output Source Current vs. Temperature

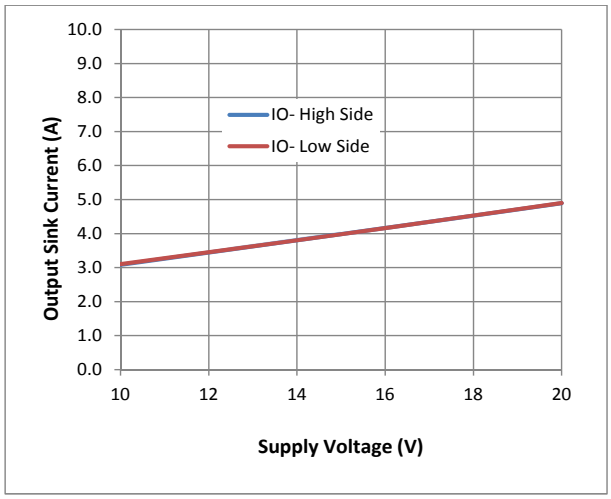


Figure 17. Output Sink Current vs. Supply Voltage

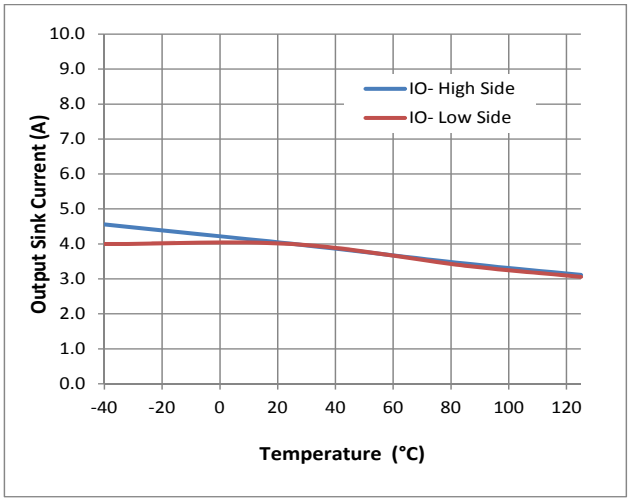


Figure 18. Output Sink Current vs. Temperature

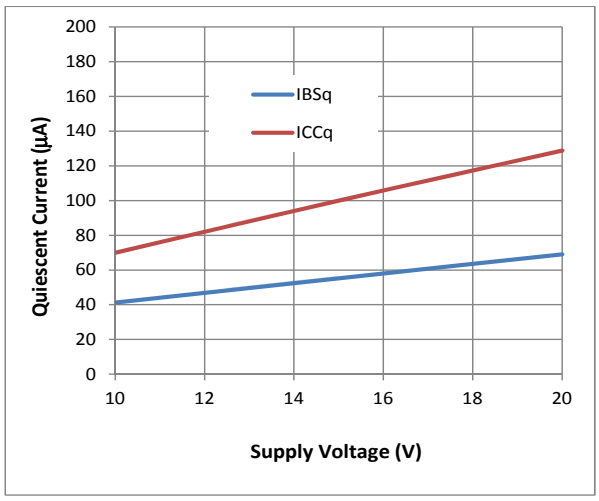


Figure 19. Quiescent Current vs. Supply Voltage

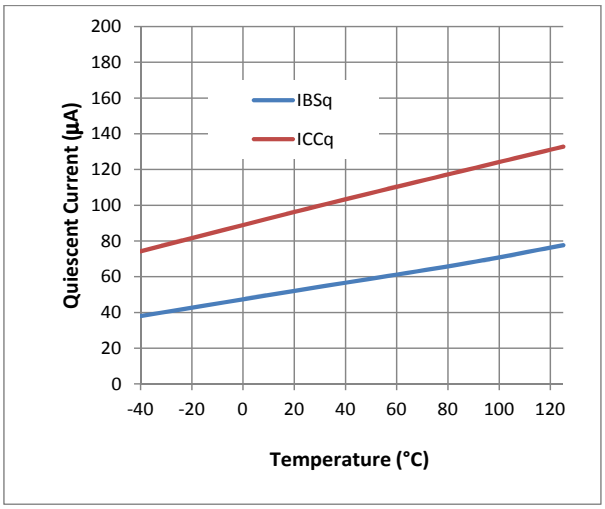


Figure 20. Quiescent Current vs. Temperature

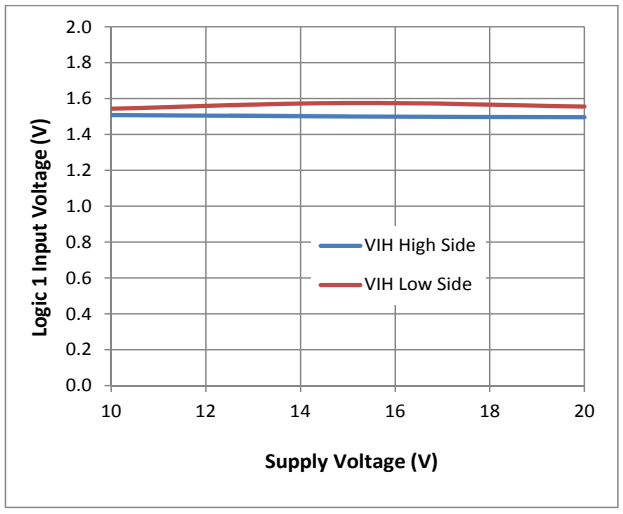


Figure 21. Logic 1 Input Voltage vs. Supply Voltage

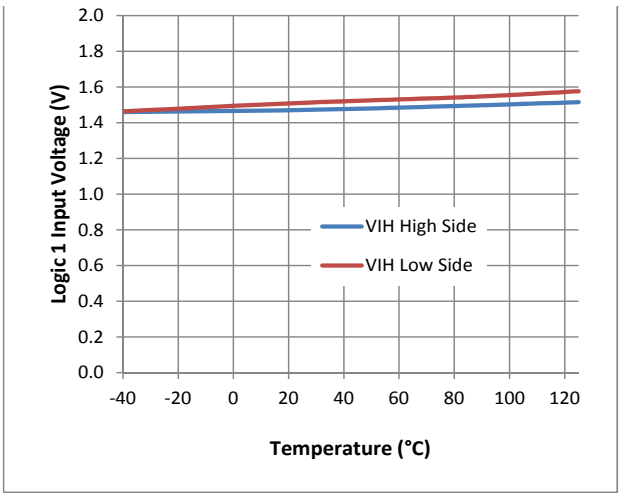


Figure 22. Logic 1 Input Voltage vs. Temperature

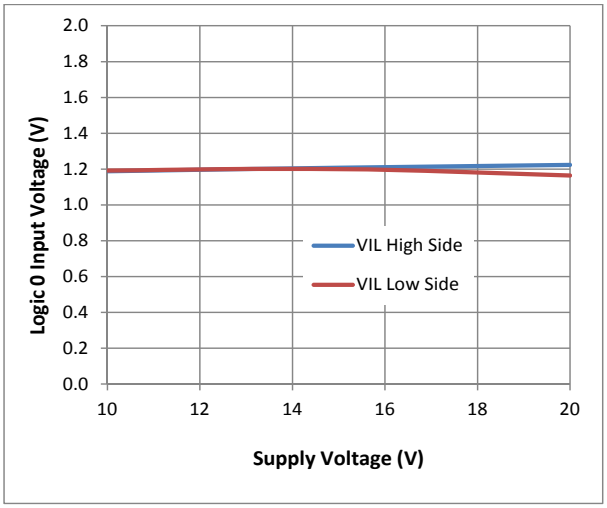


Figure 23. Logic 0 Input Voltage vs. Supply Voltage

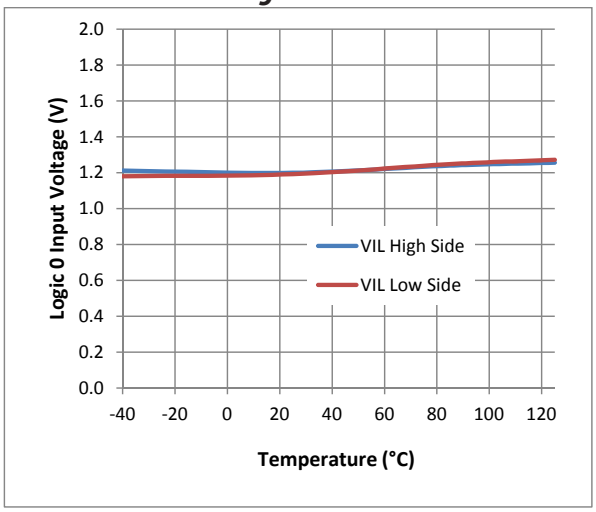


Figure 24. Logic 0 Input Voltage vs. Temperature

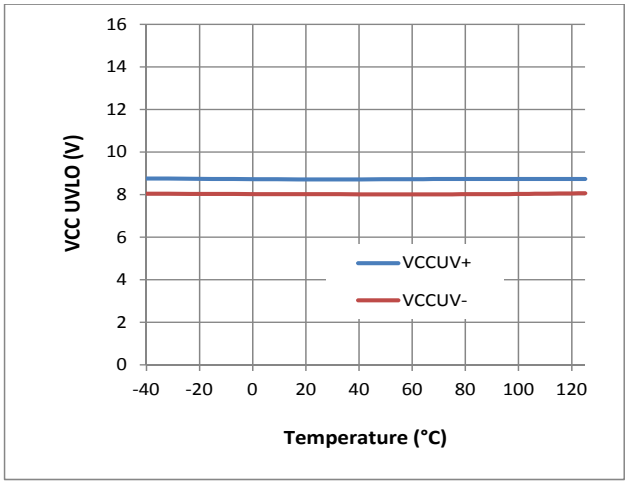


Figure 25. V_{CC} UVLO vs. Temperature

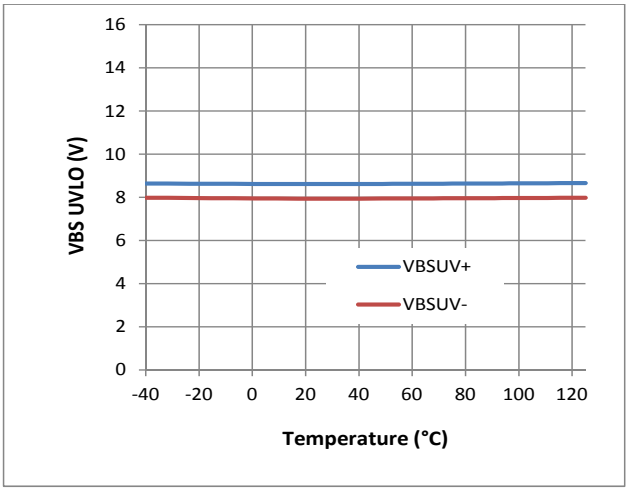


Figure 26. V_{BS} UVLO vs. Temperature

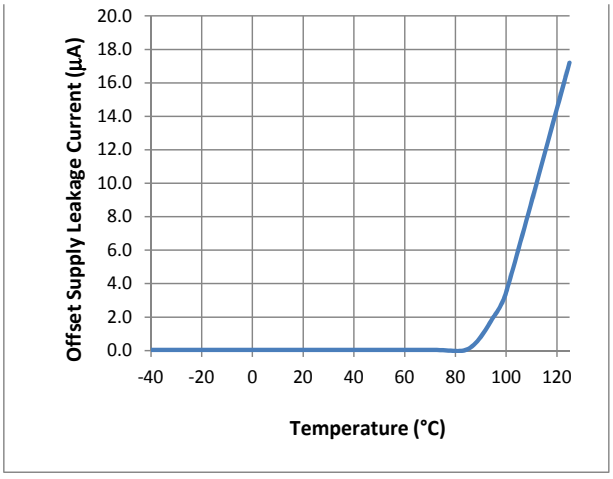


Figure 27. Offset Supply Leakage Current Temperature, VB=VS= 600V

Operation

Halfbridge Configuration

A common configuration used for the TF2190 is a half-bridge (see fig. 29). In a half-bridge configuration the source of the high-side MOSFET (Q_H) and the drain of the low-side MOSFET (Q_L) are connected. That line (V_S) is both the return for the high side in the gate driver IC as well as the output of the half-bridge. When Q_H is on and Q_L is off, V_S swings to high voltage, and when Q_H is off and Q_L is on, V_S swings to GND. Hence the output switches from GND to high voltage at the frequency of HIN and LIN, this line drives a transformer for a power supply, or a coil on a motor.

In this half-bridge configuration, high voltage DC is input to the MOSFETs, and converted to a high voltage switching signal to output to load (fig 29). The MOSFETs operate in saturation mode and an important function of the gate driver is to turn on the MOSFET quickly to minimize switching losses from the linear region of the MOSFET (turn on and turn off); the TF2190 has a typical rise/fall time of 25ns/20ns into a 1nF load.

Another important function of the gate driver IC in the half-bridge configuration is to convert the logic signals of control (TF2190 operates at logic 3V), to a voltage level and current capacity to drive the gate of the MOSFET and IGBT; this requires driving large currents initially to turn on/turn off the MOSFET quickly. Also the floating well of the high-side allows high voltage operation in the bootstrap operation.

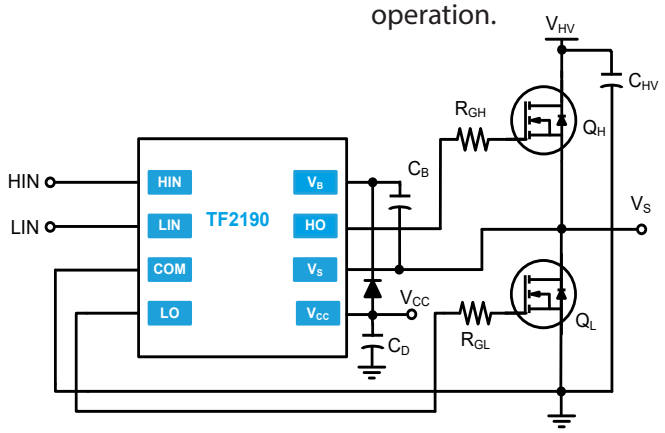


Figure 29. TF2190 in a half-bridge configuration

Bootstrap Operation

The supply for the TF2190 High Side is provided by the bootstrap capacitor C_B (see fig 30). In the half-bridge configuration, V_S swings from 0V to V_{HV} depending on the PWM input ot the IC. When V_S is 0V, V_{BS} will go below V_{CC} and V_{CC} will charge C_B. When HO goes high, V_S swings to V_{HV}, and V_{BS} remains at V_{CC} minus a diode drop (D_B) due to the voltage on C_B. This is the supply for the high side gate driver and allows the gate driver to function with the floating well (V_S) at the high voltage.

When considering the **value of the bootstrap capacitor C_B**, it is important that it is sized to provide enough energy to quickly drive the gate of Q_H. Values of 1µF to 10µF are recommended, exact value depending on gate capacitance, and the noise in application. It is key to use a low ESR capacitor that is close to the device. This will best quickly supply charge to the gate of the MOSFET.

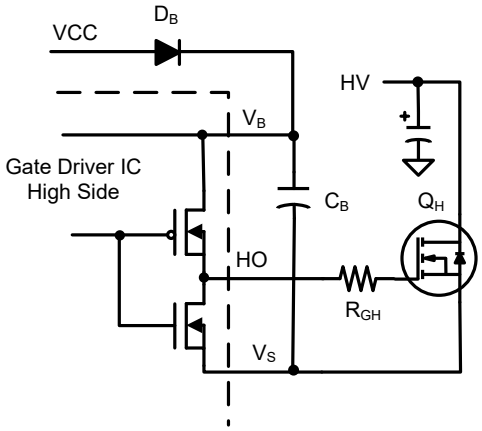


Figure 30. TF2190 high side in bootstrap operation

For a more detailed description on Gate Resistor Selection and Bootstrap Capacitor Selectrion, see the TF Semiconductor's High Voltage Gate Driver Application Note (AN1347).

Gate Drive Control

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing, and too slow a rise/fall time will increase switching losses in the MOSFET.

An example of just the high side gate driver is shown in figure 31 (any selection of gate driver components should be the same for high side and low side drive); two extra components are seen, R_{DH} and D_H. With the careful selection of R_{GH} and R_{DH}, it is possible to selectively control the rise time and fall time of the gate drive. For turn on, all current will go from the IC through R_{GH} and charge the MOSFET gate capacitor, hence increasing or decreasing R_{GH} will increase or decrease rise time in the application. With the addition of D_H, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitor, through D_H and R_{DH} to the driver in the IC to VS. So increasing or decreasing R_{DH} will increase or decrease the fall time.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. For **gate resistor value selection** the exact value depends on the type of application, level of noise and ringing expected, and EMI requirements. Generally, power supplies switch at a fast speed, and want to squeeze out efficiency of the MOSFETs, so lower values are recommended, for example RGH = 5Ω - 20Ω. For motors, the switching speed is generally slower, and the application has more inherent noise, so higher values are recommended, for example RGH = 20Ω - 100Ω.

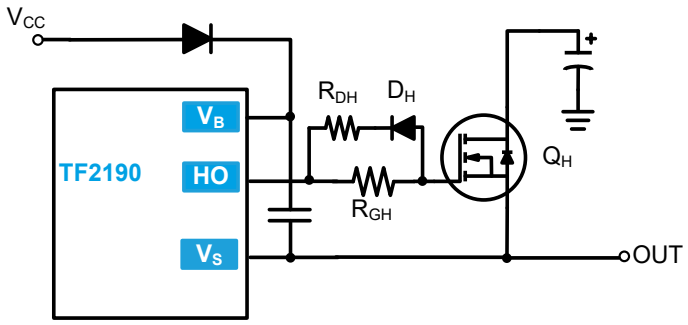


Figure 31. Gate Drive Control

Application Information

Layout Considerations

Layout plays a considerable role in noise and ringing in a circuit; unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 31 shows a halfbridge schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering fig. 32, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible. Low ESR ceramic capacitors should be used to minimize inductance. And finally the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

Generally, for the **decoupling capacitor** (C_D), at least one low ESR capacitor is recommended close to the VCC pin. Recommended values are 1μF to 10μF. A second smaller decoupling capacitor in parallel is sometimes added to provide better high frequency response (for example 0.1μF).

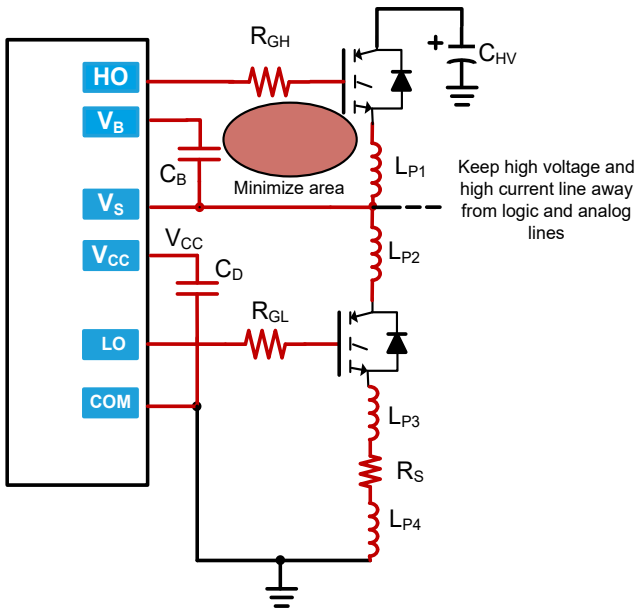


Figure 32. Layout Suggestions for TF2190 in a halfbridge

Application Example

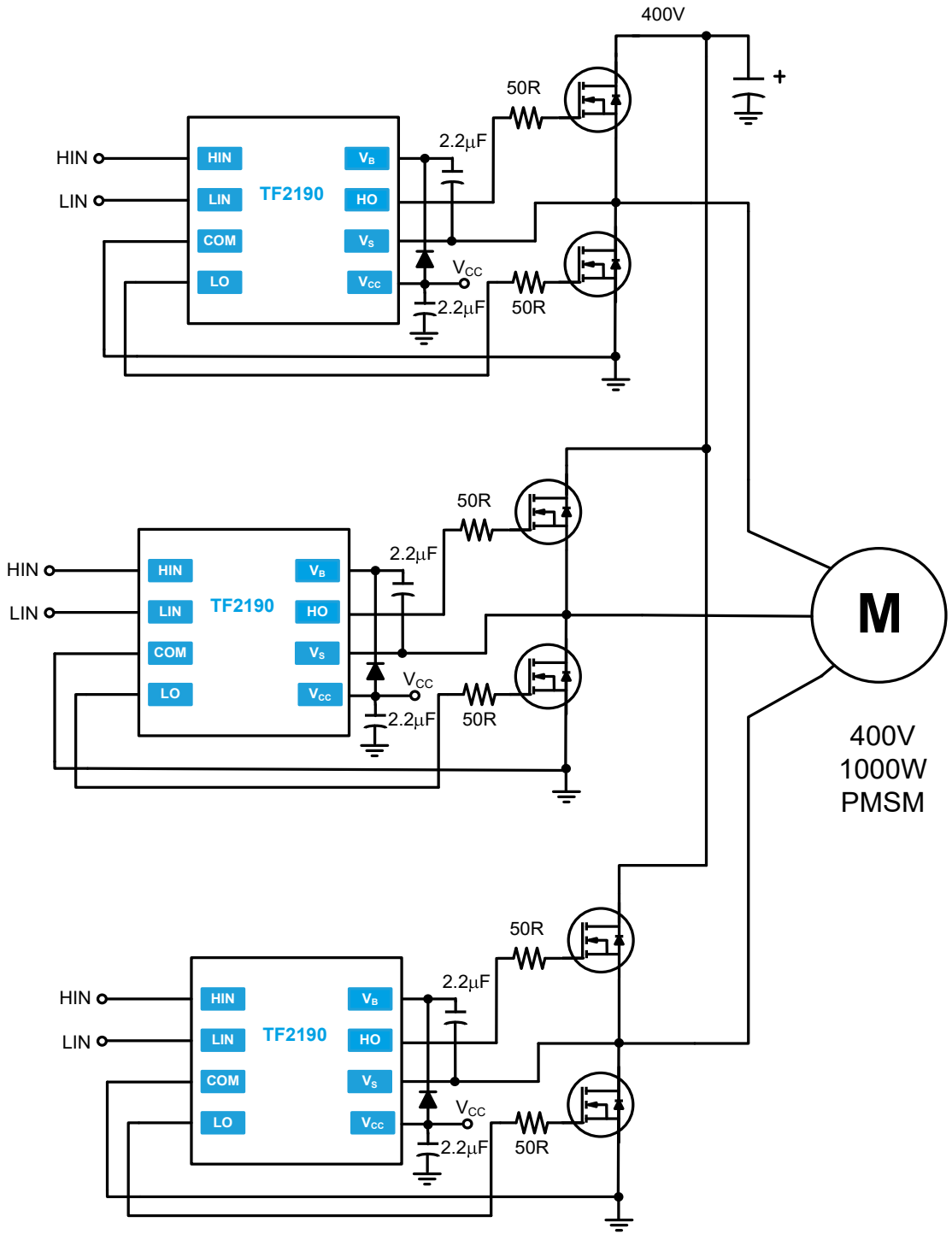


Figure 33. Three Phase Motor Driver using the TF2190

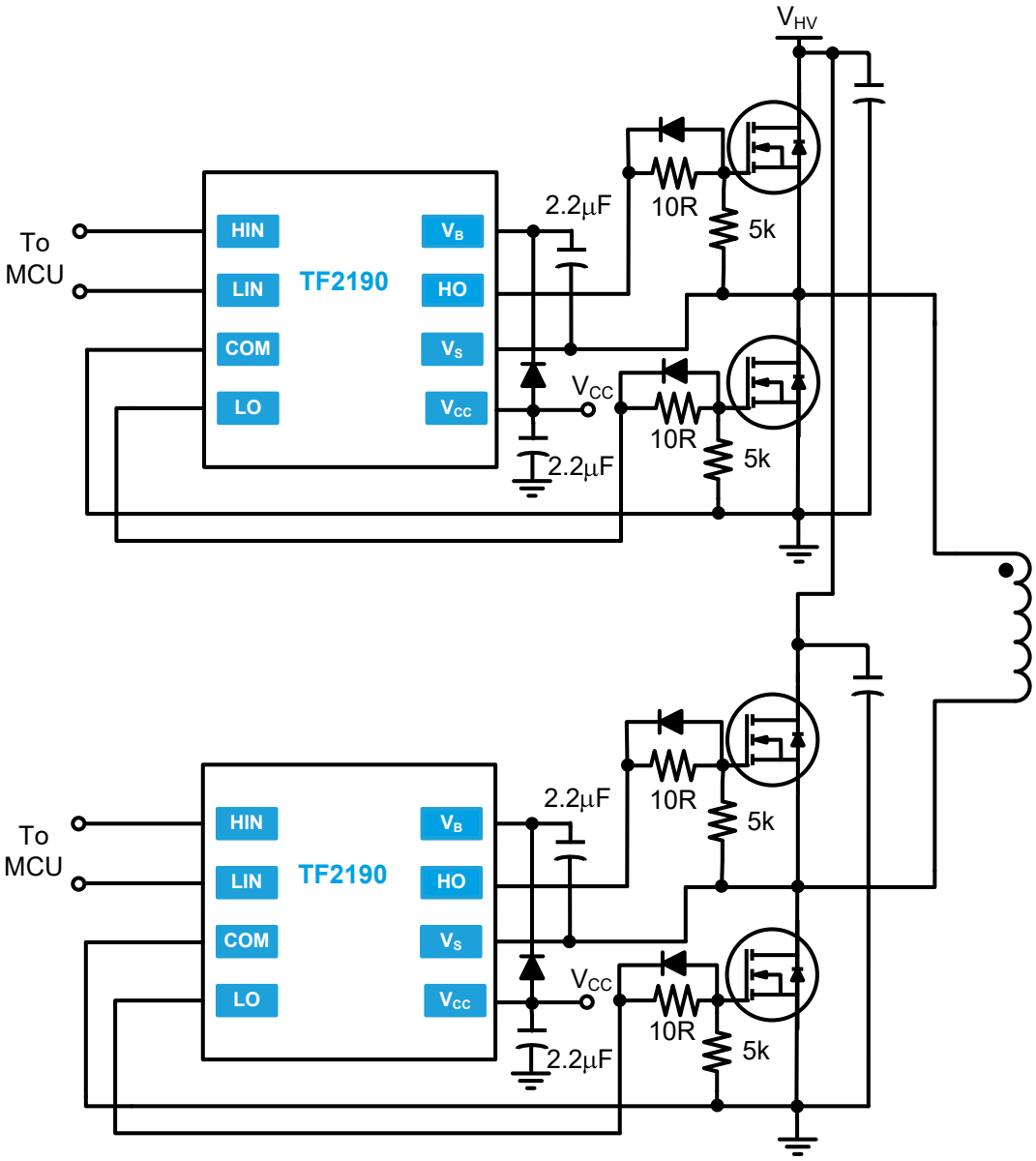
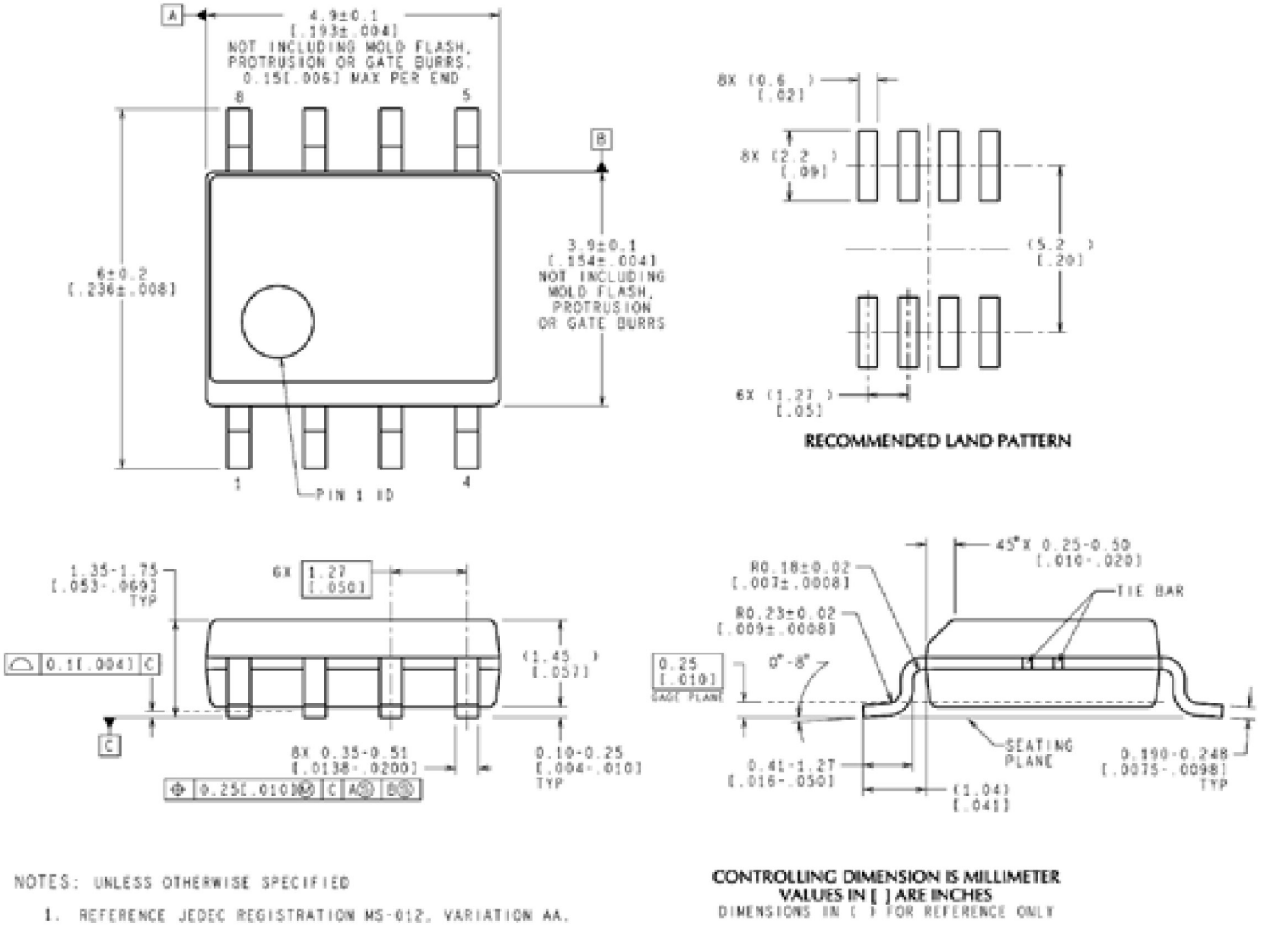


Figure 34. The TF2190 full bridge configuration for 1kW - 3kW power supply

Package Dimensions (SOIC-8 N)

Please contact support@tfsemi.com for package availability.



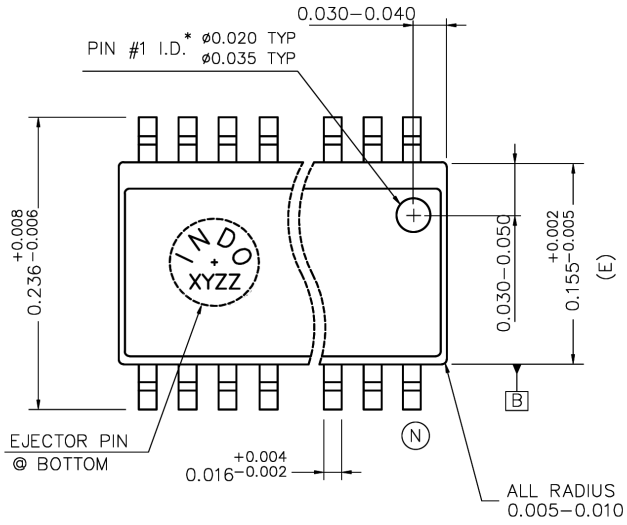
NOTES: UNLESS OTHERWISE SPECIFIED

1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Package Dimensions (SOIC-14)

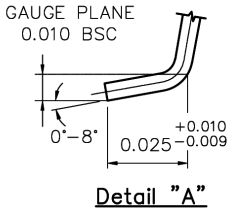
Please contact support@tfsemi.com for package availability.



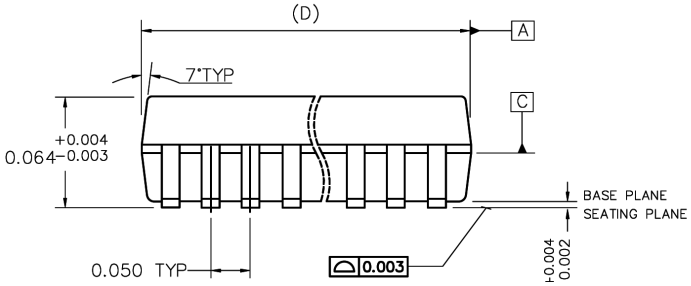
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

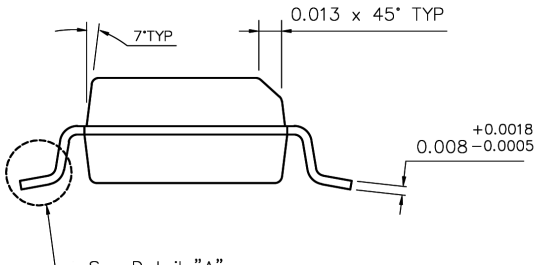
NOTES:

1. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 6 MILS PER SIDE.
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 3 MILS (@ SEATING PLANE) OUTGOING ASSEMBLY & 4 MILS AFTER TEST.
4. THE BOTTOM PACKAGE LEAD SIDE MAY BE BIGGER THAN THE TOP PACKAGE LEAD SIDE BY 4 MILS (2 MILS PER SIDE). BOTTOM PACKAGE DIMENSION SHALL FOLLOW DIMENSION STATED IN THIS DRAWING.
5. THE BOTTOM EJECTOR PIN CONTAINS COUNTRY OF ORIGIN "INDO" AND MOLD ID. (REFER TO TABLE FOR OPTION).
6. THIS DRAWING CONFORMS TO JEDEC REF. MS–012 REV. E



N	D VARIATION			MGP MOLD			
				STANDARD		MATRIX	
	MIN	NOM	MAX	PIN 1 I.D.	EJECT PIN	PIN 1 I.D.	EJECT PIN
08	0.189	0.193	0.196	N/A		YES	YES
14	0.337	0.339	0.344	YES	NO	YES	YES
⚠ 16	0.386	0.390	0.393	N/A		YES	YES





Revision History

Rev.	Change	Owner	Date
1.0	First release, final datasheet	Keith Spaulding	5/20/2016
1.1	Text edit	Keith Spaulding	11/24/2017
1.2	Add Note 5	Duke Walton	7/30/2019
1.3	Add Applications information, pg 7.	Keith Spaulding	2/2/2021
1.4	Application notes update	Raj Selvaraj	06/22/2021

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