Prat No:BD9515NUX-E2

VSON008X2020

ROHS

Halogen Free

MOSFET Gate Driver for DC/DC Converter

BD9515NUX

● General Description

BD9515NUX is a synchronous buck converter MOSFET driver with integrated boost switch.
This low on-resistance output driver is capable of driving high-side and low-side N-channel FETs at high speeds with minimum switching loss.
Adaptive dead-time control and shoot-through protection are included.
The PWM pin is a tri-state input. When the input is Hi-z, both FETs turn off. The IC can provide skip-mode for light-load current.
EN pin can provide a low standby current. When input is low or Hi-z, PVCC current is 0μA.

.

● Features

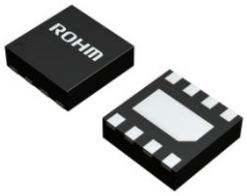
- Under Voltage Lock Out
- Tri-State PWM Input
- High Frequency Operation (up to 1.2 MHz)

● Key Specifications

- Input voltage range: 4.5V to 5.5V
- HG High Side On-resistance: 0.6Ω (Typ.)
- HG Low Side On-resistance: 0.5Ω (Typ.)
- LG High Side On-resistance: 0.6Ω (Typ.)
- LG Low Side On-resistance: 0.5Ω (Typ.)
- Standby Current: 0μA (Typ.)
- Operating Temperature Range: -30℃ to +85℃

● Package

Thermally Enhanced VSON008X2020 Package



L(Typ.) x W(Typ.) x H(Max.)
2.00mm x 2.00mm x 0.60mm

● Applications

- Note Book PC(Ultrabook™, Laptop PC, Ultra Mobile PC, Net Book PC, Tablet PC)

● Application Circuit Example

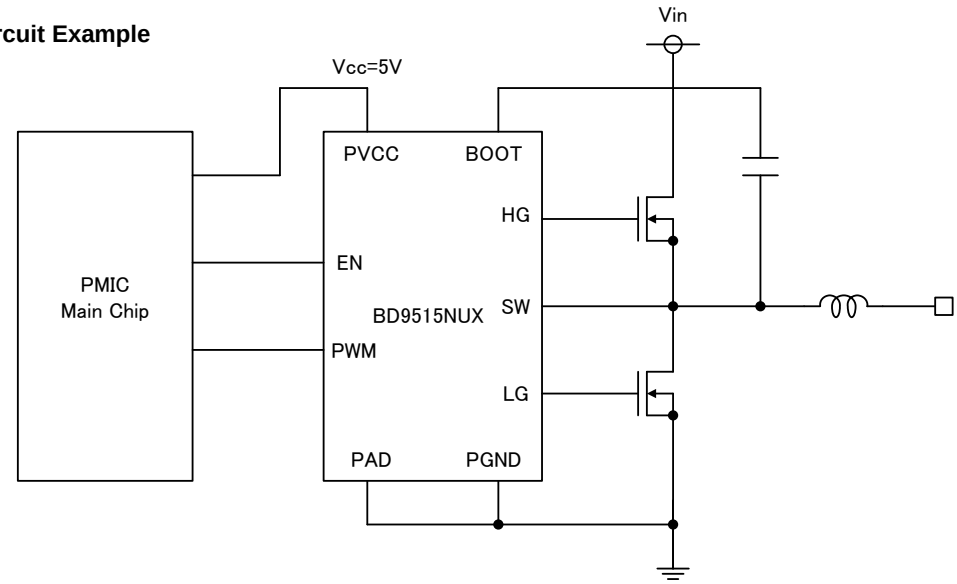


Figure 1. Application Circuit

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● **Pin Configuration**

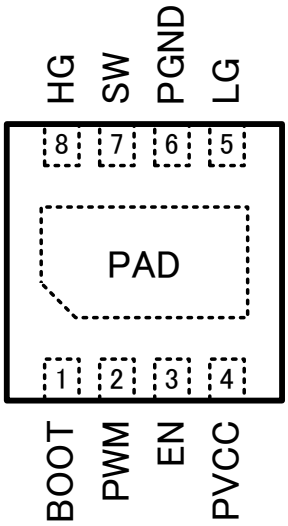

Figure 2. Pin Configuration
(TOP VIEW)

● **Pin Descriptions**

No.	Name	Description
1	BOOT	Bootstrap capacitor connection: Connect a 0.1μF (min.) ceramic capacitor between the BOOT and SW pins. The bootstrap capacitor provides the charge necessary to activate the high-side FET. The bootstrap diode is integrated.
2	PWM	Pulse width modulated three state input from external controller. PWM = input high to high-side FET enabled PWM = Middle to go into diode mode (both high and low side gate drive signals are low) PWM = input low to low-side FET enabled
3	EN	Enable input pin. EN = High to enable the gate driver EN = Hi-z or low to disable the driver
4	PVCC	Supply voltage to gate drivers and internal circuits.
5	LG	Low-side N-channel FET gate drive output.
6	PGND	Power ground.
7	SW	Voltage switching node. Connection to the output inductor.
8	HG	High-side N-channel FET gate drive output.
PAD	PAD	Thermal pad provides optional heat sinking

● **Truth Table**

Input		Output	
EN	PWM	LG	HG
Hi-z or Low	X(don't care)	Low	Low
High	Low	High	Low
High	Hi-z or Middle	Low	Low
High	High	Low	High

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● Block Diagram

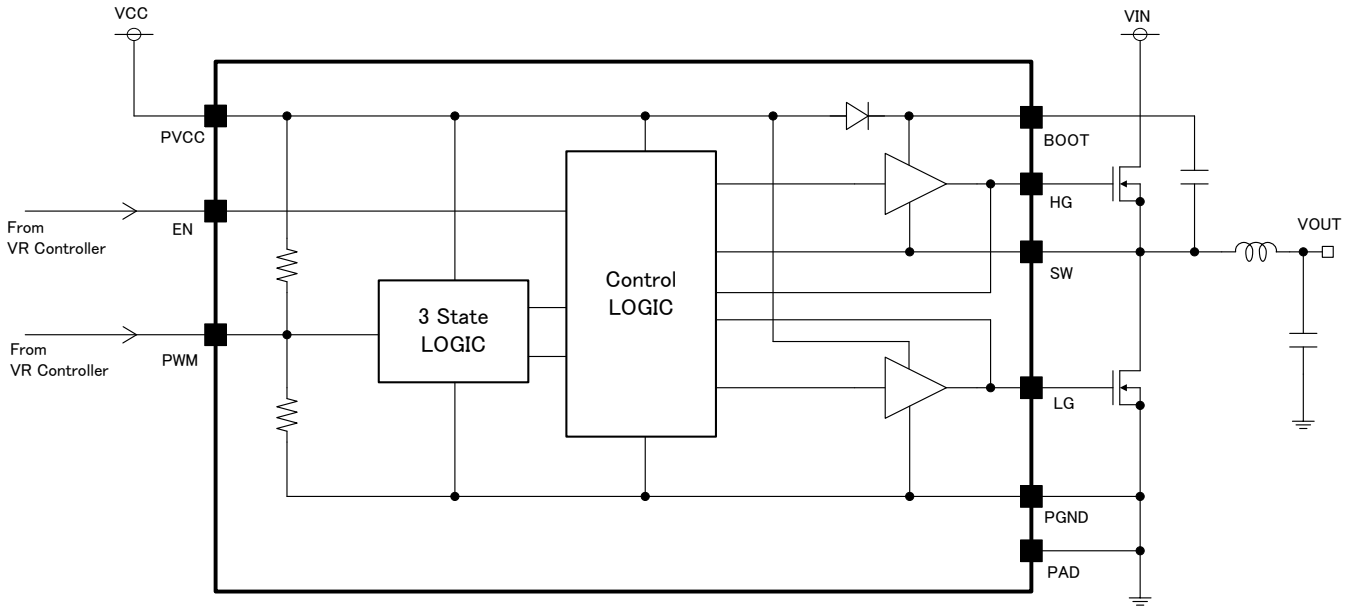

Figure 3. Block Diagram

● Absolute Maximum Ratings

Parameter	Rating			Unit	Conditions
PVCC, EN, PWM, LG	-0.3	to	6.0	V	
BOOT – SW	-0.3	to	7.0	V	
BOOT	-0.3	to	35.0	V	
SW	-1.3	to	30.0	V	
HG	SW -0.3	to	BOOT+0.3	V	
Power Dissipation	1.04			W	Board dimension: 114.3mm x 76.2mm x 1.6mmt Four layer Surface cupper area 2.25mm^2 2nd and 3rd cupper area 5505mm^2
Storage Temperature range (Tj)	-55	to	150	℃	
Junction Temperature (Tjmax)	125			℃	

● Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Input Voltage Range	PVCC	4.5	5.0	5.5	V
SW Input Voltage	SW	-1.0	7.4	24	V
Operating Temperature Range	Ta	-30	-	+85	℃

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● **Electrical Characteristics (PVCC=5V, SW=0V, PGND=0V, T_A=25℃)**

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
SUPPLY, UNDERVOLTAGE LOCKOUT						
PVCC Quiescent Current	Iq	-	0	5	μA	EN=L, PWM=Float
PVCC Circuit Current	Icch	80	180	300	μA	EN=H, PWM=H
	Iccl	210	420	630	μA	EN=H, PWM=L
	Iccm	45	90	180	μA	EN=H, PWM=Float
PVCC UVLO Threshold	UVLO	-	-	4.5	V	
PVCC UVLO Hysteresis	UVLOhys	-	0.2	-	V	
PWM INPUT						
High-Level PWM Input	PWMh	4.3	-	5.5	V	
Low-Level PWM Input	PWMl	-	-	0.6	V	
PWM Tri-State Voltage	PWMm	2.0	2.5	3.0	V	PWM=Float
EN INPUT						
High-Level EN Input	EN	2.1	-	5.5	V	
EN Hysteresis	ENhys	-	0.09	-	V	
GATE DRIVE OUTPUT						
HG On-Resistance	RHH	-	0.6	1.1	Ω	
	RHL	-	0.5	1.0	Ω	
LG On-Resistance	RLH	-	0.6	1.1	Ω	
	RLL	-	0.5	1.0	Ω	
TIMING CHARACTERISTICS						
Driver Non-Overlap Time	Thl	-	20	-	ns	LG Low to HG High
	Tlh	-	20	-	ns	HG Low to LG High
Driver Delay	Tdly	-	35	-	ns	PWM High to HG High
Minimum LG On-Time	Tminlg	-	350	-	ns	
Tri-State Shutdown Hold-Off Time	Tho	-	100	-	ns	
BOOT-STRAP SWITCH						
BOOT Diode Vf Voltage	V	0.15	0.5	0.85	V	

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● **Timing Charts**

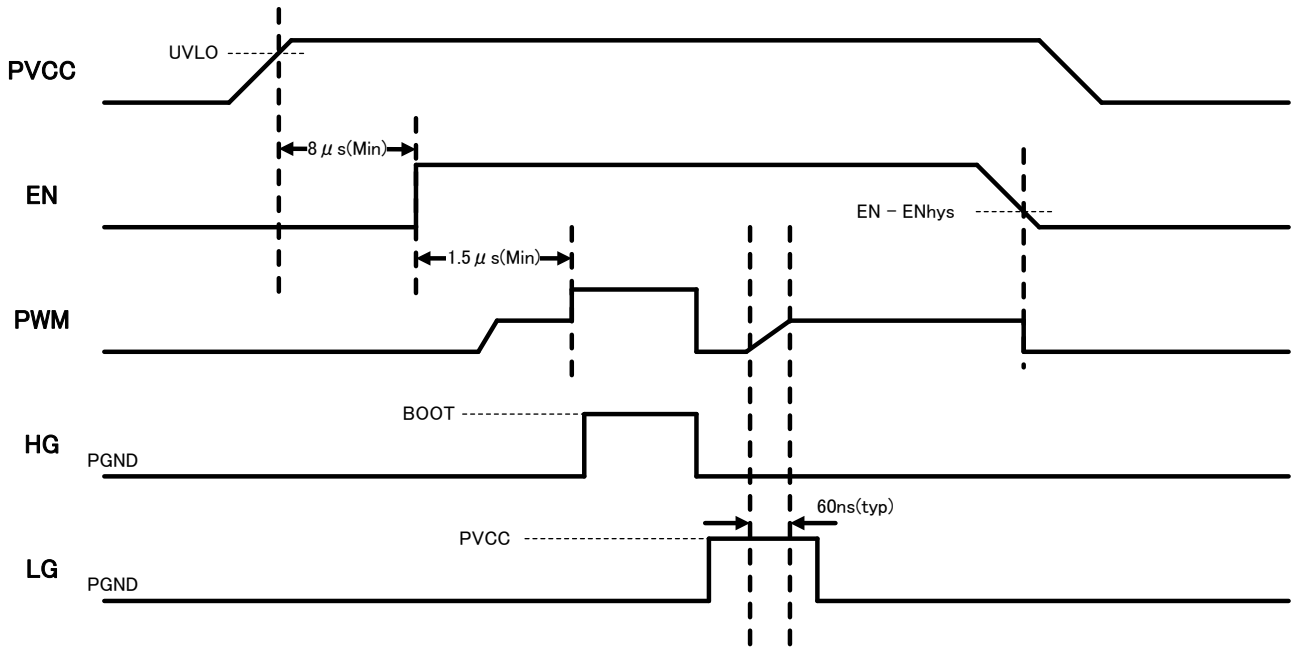

Figure 4. Startup and Shutdown Sequence

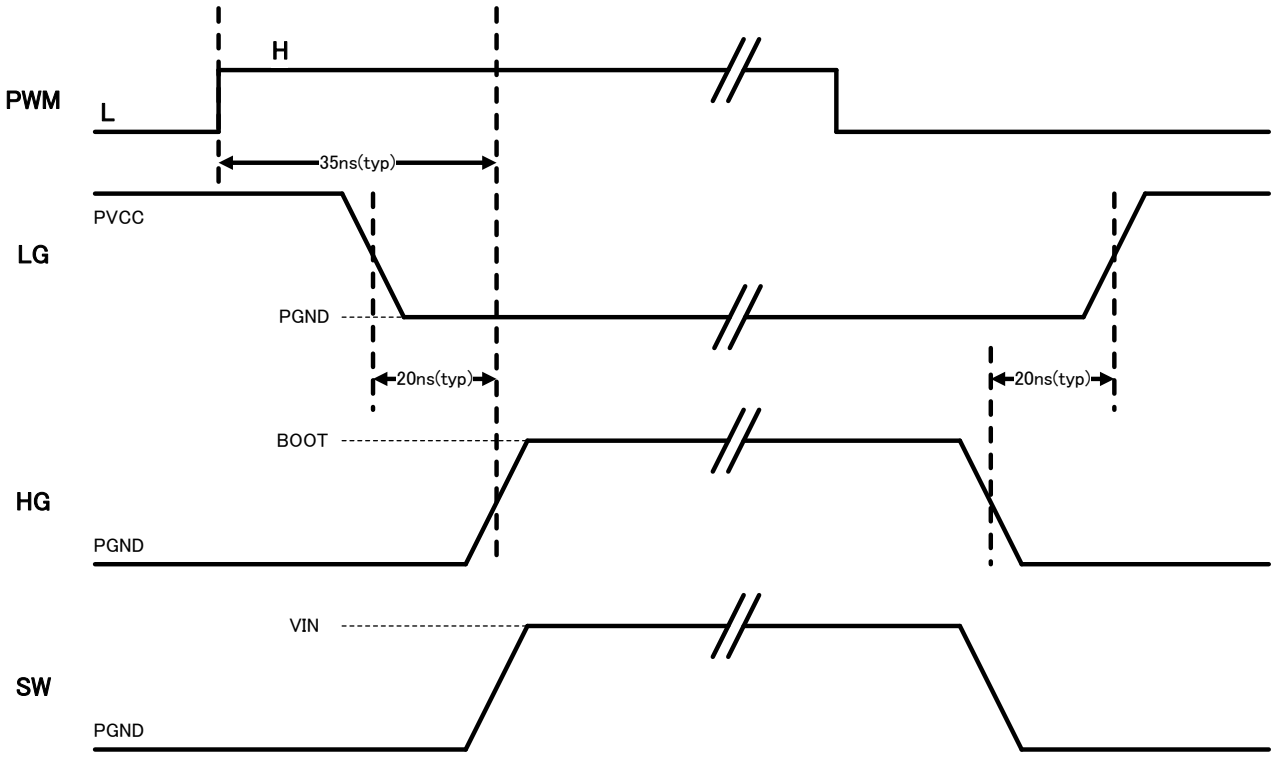

Figure 5. Driver Non-Overlap Timing

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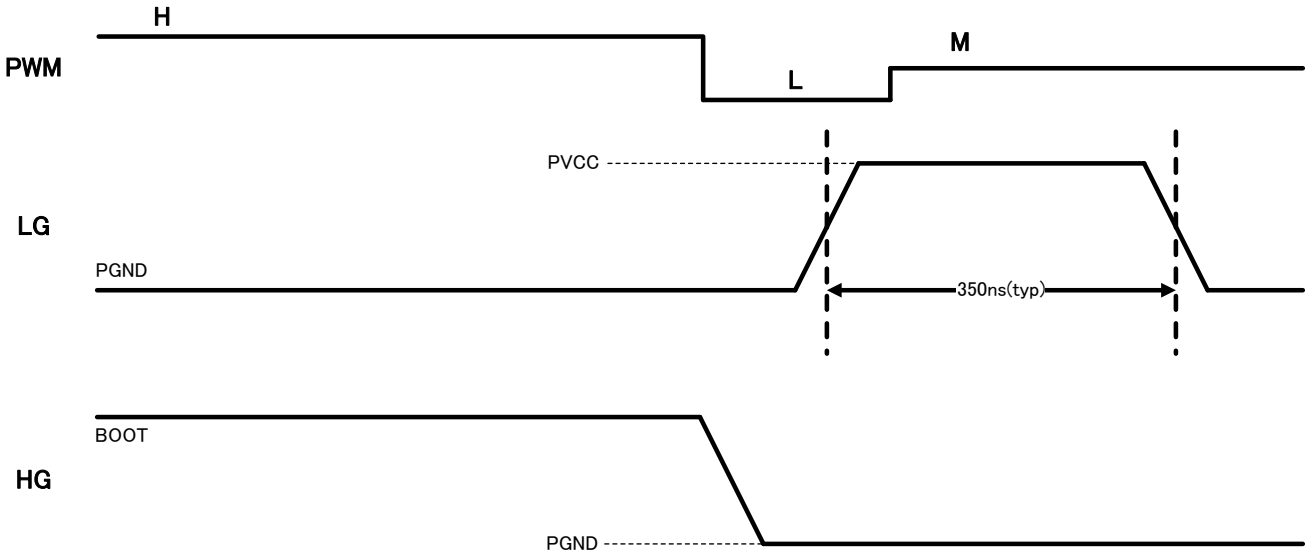

Figure 6. Minimum LG Time

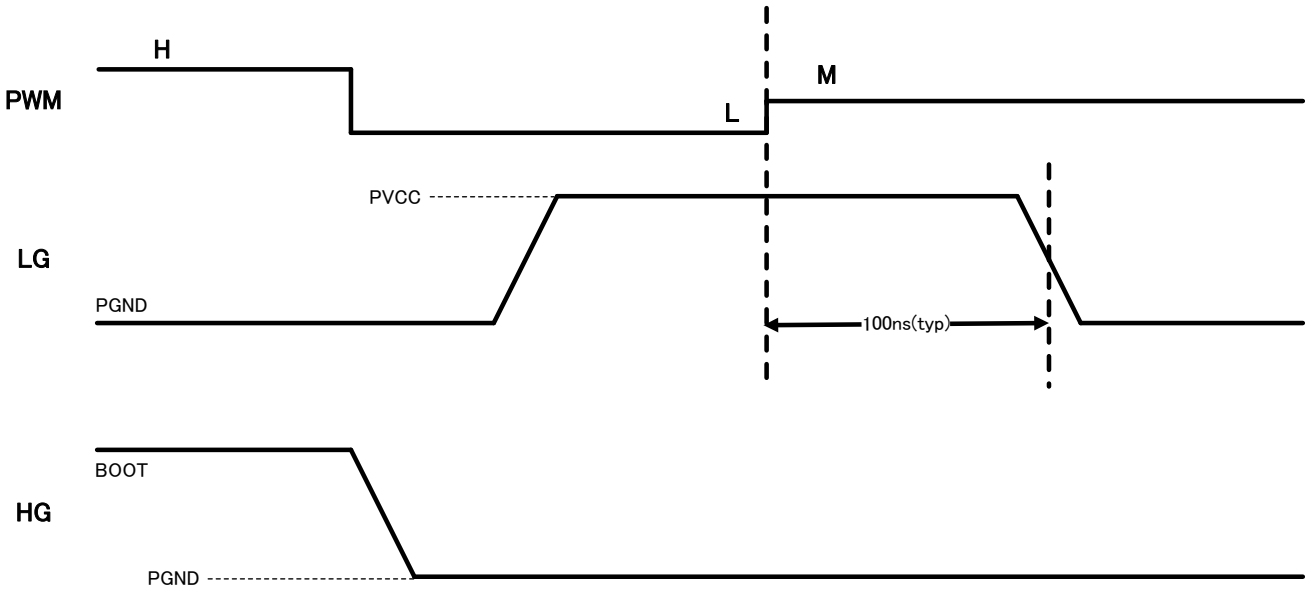

Figure 7. Tri-State Hold Off Time

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● **Application Example**

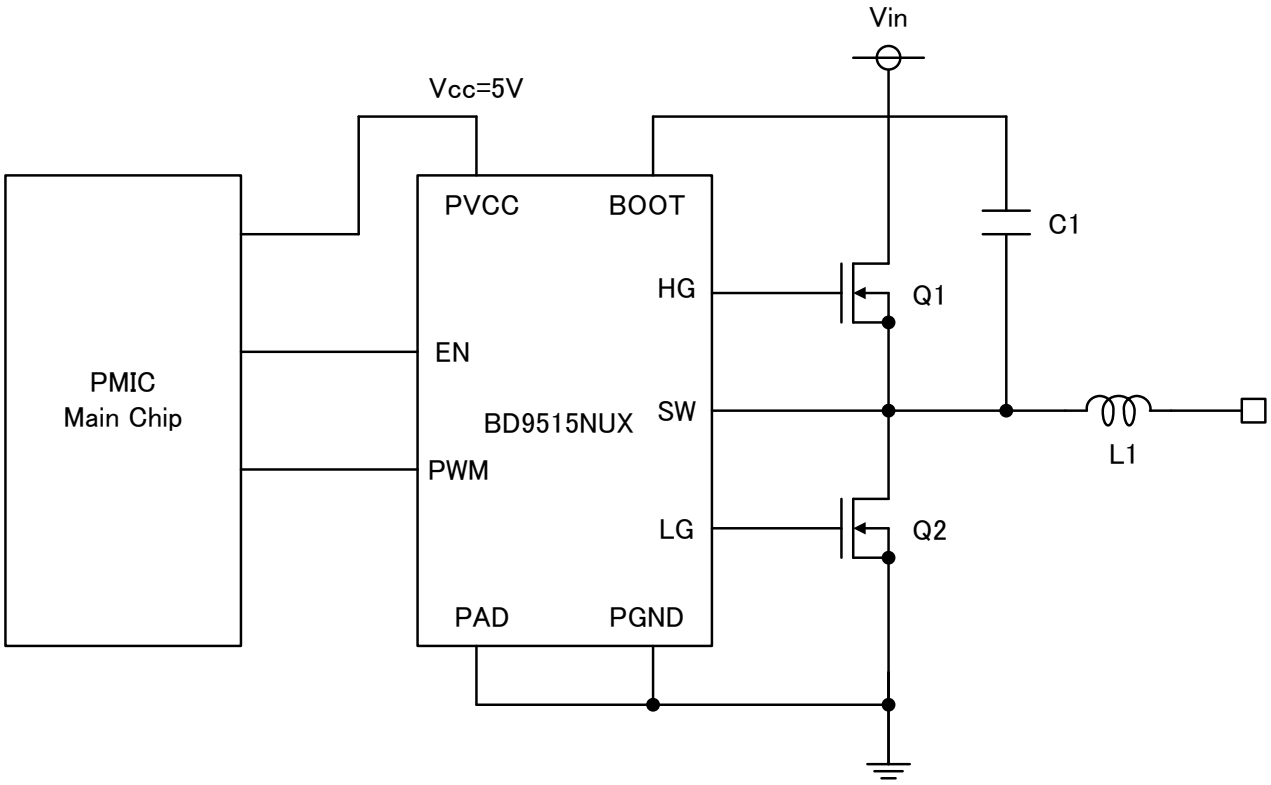

Figure 8. Application Circuit Example

Ref Des	Value	Voltage	Manufacture	Part number
Q1	-	30V	ROHM	RQ3C165AG
Q2	-	30V	ROHM	RQ3C165AG
L1	0.47µH	-	TOKO	FCUL0624-H-R47M
C1	0.22µF	16V	Std.	-

Above application is important to turn the power MOSFET(Q1, Q2) off quickly to minimize power loss due to transition time.

Self Turn-On

When LG turns the low-side FET off and HG turns the high-side FET on, the voltage on the SW pin will rise to Vin very rapidly. This transient response will couple through the Cgd capacitance of the low-side FET to the LG pin.
If adaptive FETs are not used, and the LG pin is not held low, the voltage on the LG pin will rise above the threshold voltage of the low-side FET and momentarily turn it back on.
In this scenario, both the high-side and low-side FETs will be conducting, which will cause significant cross-conduction current to flow through the FETs from Vin to GND, thereby introducing substantial power loss.

Switching Loss

FET's capacitive power dissipation can be calculated using its gate charge, Qg.
When identical MOSFETs are connected to HG and LG

$$P_{Qg} = 2(PVCC)(Qg)(f_{pwm})$$

P_{Qg} : Switching loss
$PVCC$: Supply voltage
Qg : FET gate capacitance
f_{pwm} : Switching frequency

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● **Power Dissipation**

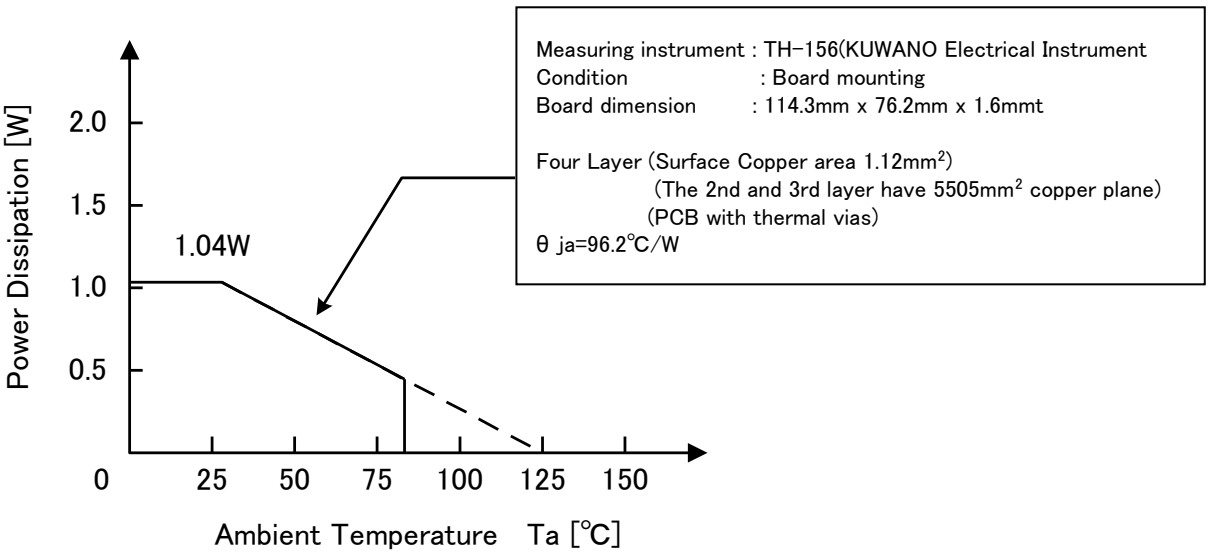

Figure 9. Derating Curve

● **I/O Equivalent Circuits**

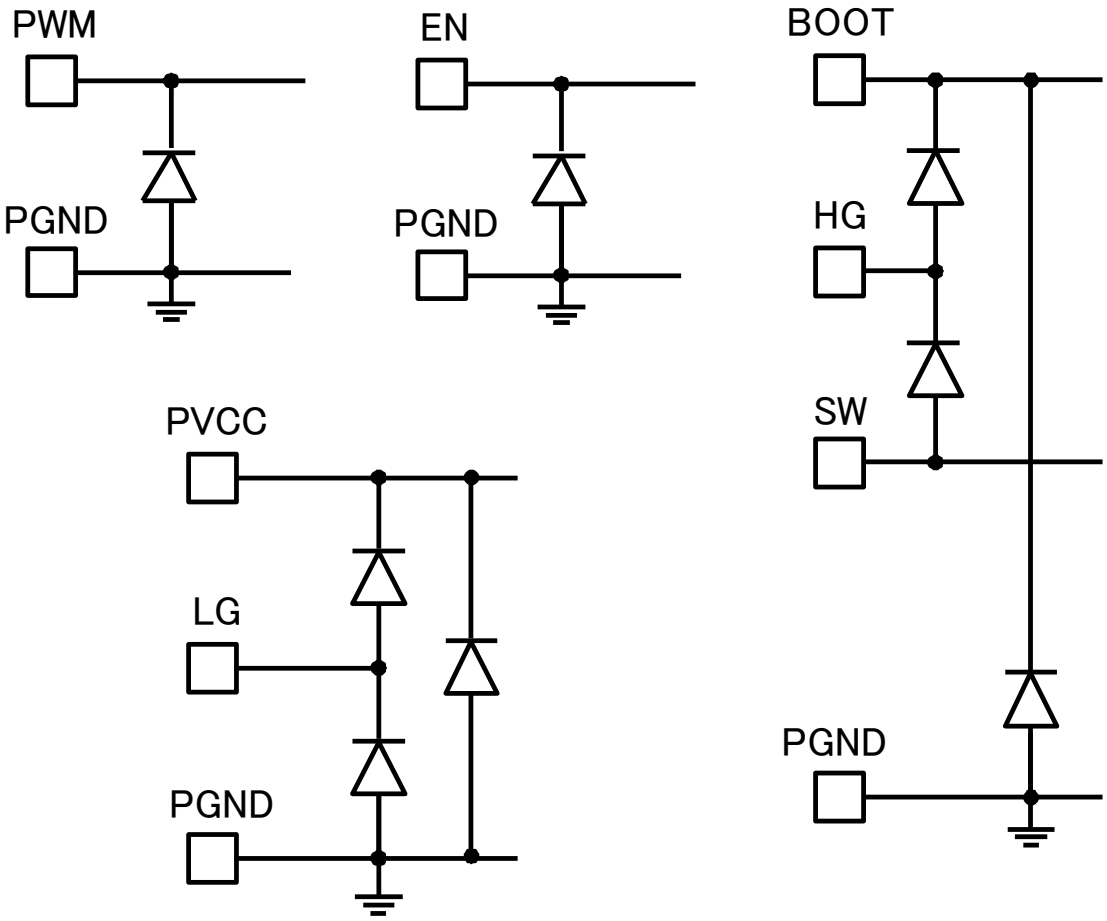

Figure 10. I/O Equivalent circuits

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● Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
OR

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Rush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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● Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

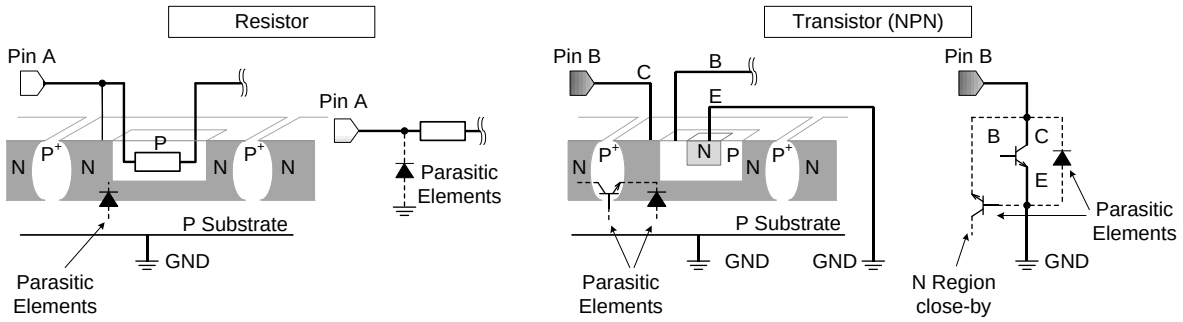

Figure 11. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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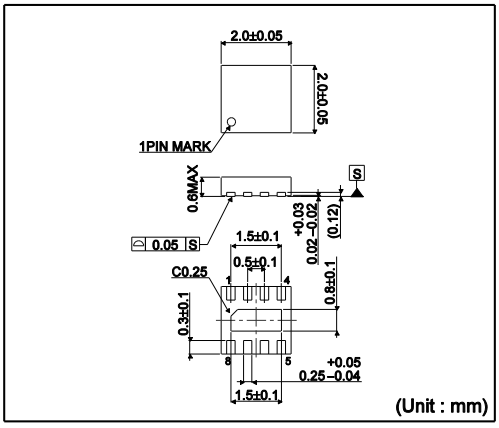
● Ordering Information

B D 9 5 1 5 N U X	-	E 2
Part Number		Package NUX: VSON008X2020
		Packaging and forming specification E2: Embossed tape and reel

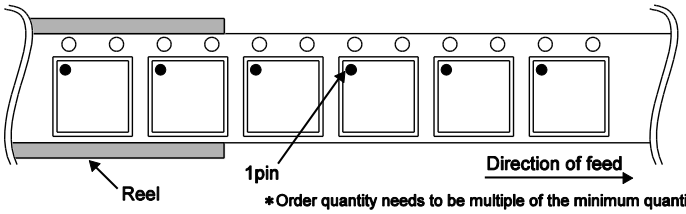
● Physical Dimensions, Tape and Reel Information

VSON008X2020



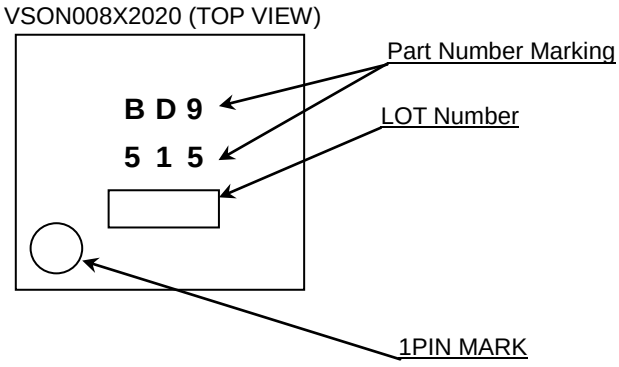
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

● Part Marking



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● **Revision History**

Date	Revision	Changes
2.May.2013	1	New Release
18.Sep.2014	2	Document Adjustment

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— Jisso Infomation —

Package : VSON ×××X series (E2)

< A table of contents >

1. Structure

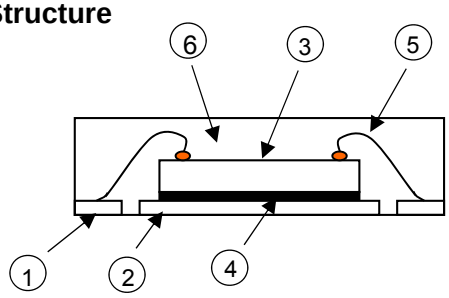


Fig. 1 Structure

No.	Compositional element
①	Lead (External lead : Pb free solder plating)
②	Die Pad
③	Die
④	Die Attach
⑤	Bonding Wire
⑥	Molding Resin

2. Tape and Reel information

2. 1. Packing specification

Tape	Embossed carrier tape
Quantity	See the table on page 4/4
Direction of feed	E2 (See Fig. 2)

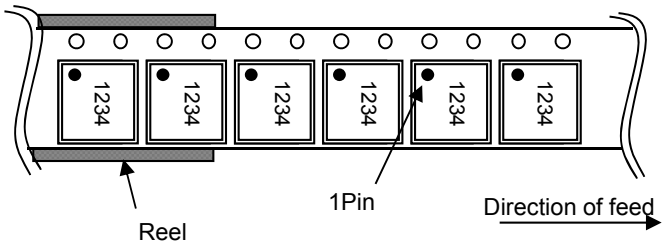


Fig. 2 Typical Tape and Reel configuration

2. 2. Tape and Reel specification

2. 2. 1. Tape and reel dimensions (See the table on page 4/4)

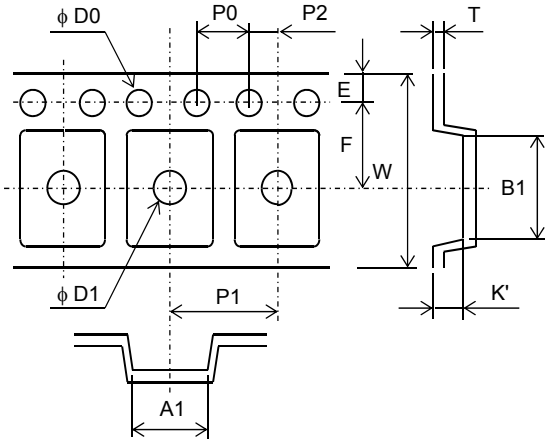


Fig. 3 Tape dimensions

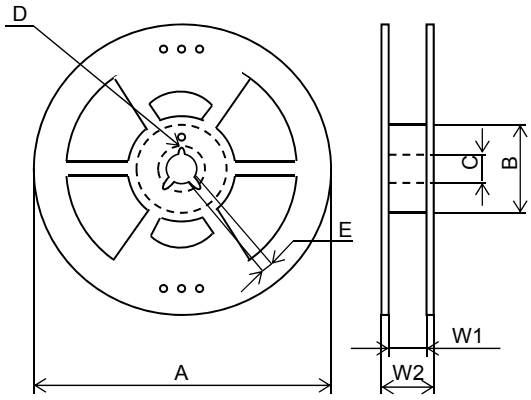


Fig. 4 Reel dimensions

2. 3. Leader and Trailer

2. 3. 1. Leader

No component pockets are 25 pockets or more.

2. 3. 2. Trailer

No component pockets are 10 pockets or more.

Tape is free from reel.

2. 4. Label for Reel and Box

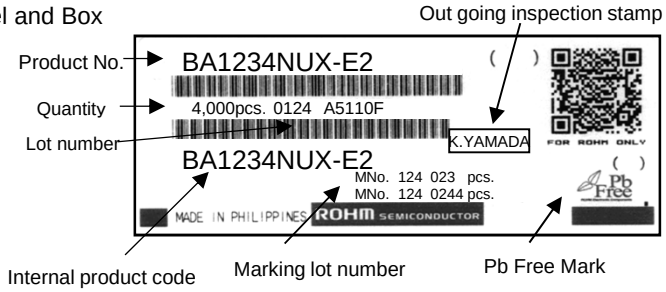


Fig. 5 Label example

2. 5. Packing style

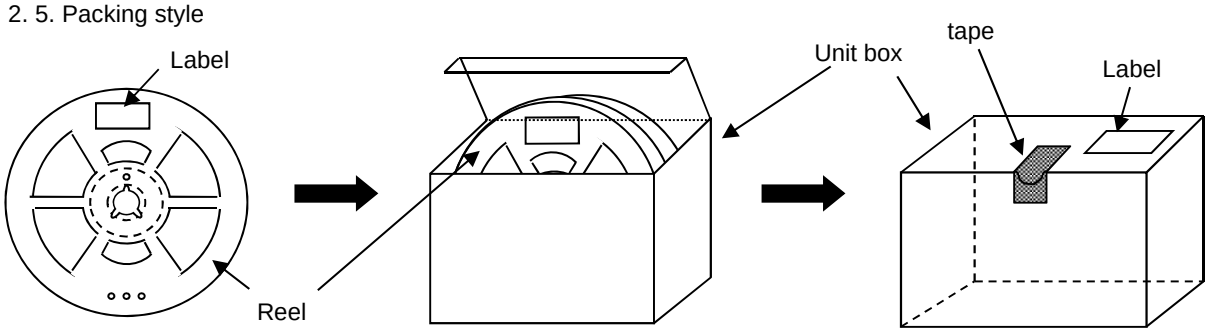
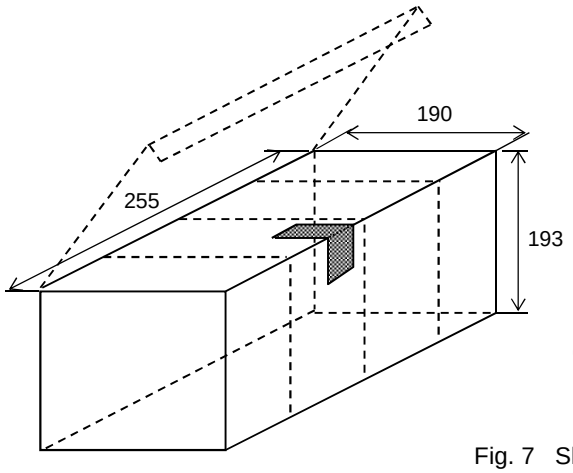


Fig. 6 Packing style

2. 6. Shipping style

4 unit boxes or less per shipping box



(all dimensions in mm)

2. 7. Packing materials

Item	Material
Embossed carrier tape	PS
Cover tape	PET + PE
Reel	PS
Unit box	Cardboard
Shipping box	Cardboard

Fig. 7 Shipping box dimensions and Shipping style

2. 8. Others

2. 8. 1. Peelback strength

Cover tape peelback strength is 0.2 to 0.7N.

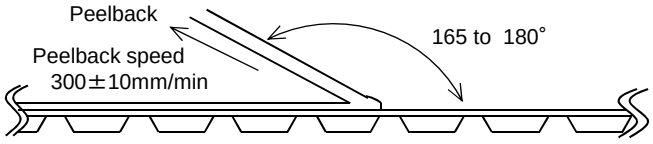


Fig. 8 Test method

2. 8. 2. Missing Ics
(1) No consecutive dropouts.
(2) A maximun 0.1% of specified number of products in each packing may be missing.

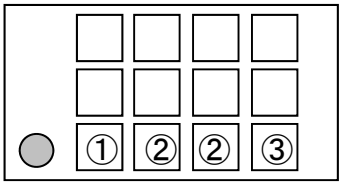
3. Storage conditions

3. 1. Storage environment
Recommended storage conditions are as follows :
-Temperature : 5 to 30°C
-Humidity : 40 to 70% RH

3. 2. Storage period
-Specified storage period : 1 year

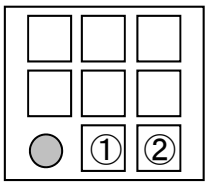
4. Marking lot number

VSON010X3020



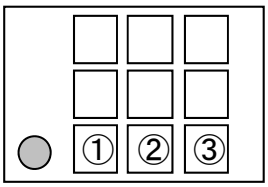
① Production year code
② week number
③ Production lot number

VSON010X3030



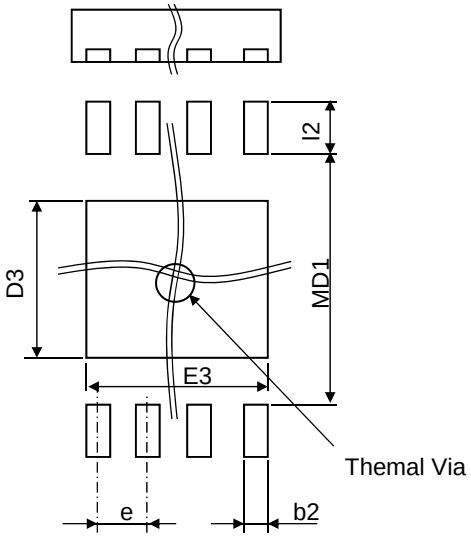
① Production year's month code
② Production lot number

VSON008X2020



① Production year code
② One last digit of week number
③ Production lot number

5. Footprint dimensions (Optimize footprint dimensions to the board design and soldering condition)



(all dimensions in mm)

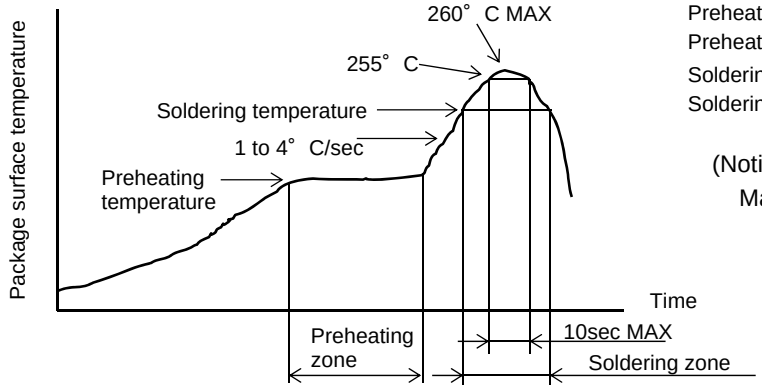
Package	Land pitch e	Land space MD1	Land length ≧l2	Land width b2
VSON010X3020	0.50	1.00	0.60	0.27
VSON010X3030	0.50	2.00	0.80	0.27
VSON008X2020	0.50	1.20	0.60	0.27

Package	Radiaton land length D3	Radiaton land width E3	Thermal via	
			Pitch	Diameter
VSON010X3020	0.54	2.49	-	ϕ0.3
VSON010X3030	1.00	2.10	-	ϕ0.3
VSON008X2020	0.70	1.60	-	ϕ0.3

*The lead toe and lead side fillet may not be achieved because of non-lead packeges.

6. Soldering conditions

6. 1. Recommended temperature profile for reflow



Preheating temperature ; 130° C to 190° C
Preheating zone ; 120sec MAX
Soldering temperature ; 220° C to 230° C
Soldering zone ; 60sec MAX

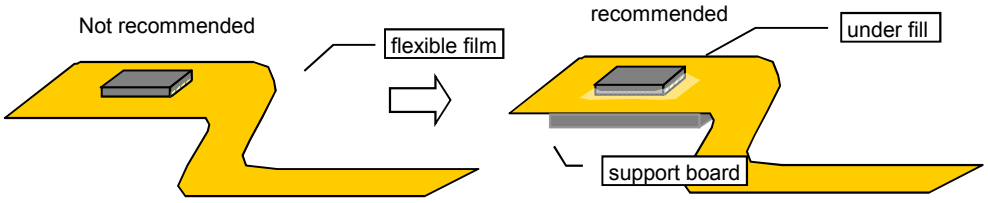
(Notice)
Maximum 2-timessoldering

6. 2. The wave soldering method is not supported.

6. 3. Notice information of board mounting

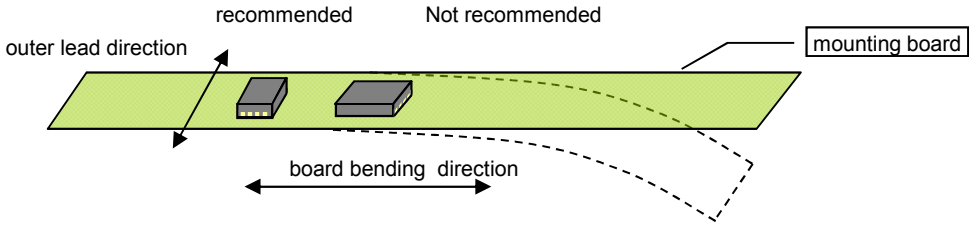
Mounting on flexible film

Mounting on flexible film, film bend may occur lack of lead from package, usage of support board and under fill is recommended.

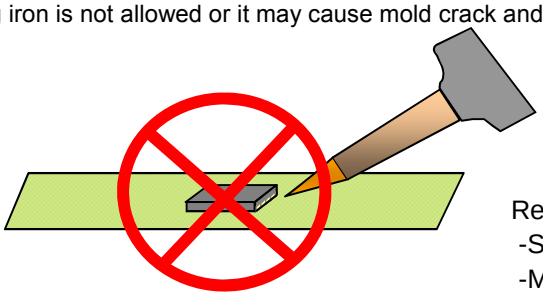


Mounting on long and narrow board

Mounting on long and narrow board, bending stress may occur a luck of lead from package, bending board direction and outer lead direction is recommended as drawing (vertically layout) and under fill usage is recommended.



6. 4. Rework by solering iron is not allowed or it may cause mold crack and terminal open.



Recommended condition for solder iron
-Solder iron temperature : 380° or less
-Mounting time : 4sec or less

< Tape dimensions >

Package	Quantity (pcs)	Tape dimensions (all dimensions in mm)											
		A1	B1	D0	D1	E	F	K'	P1	P2	T	W	P0
VSON010X3020	4000	2.25	3.25	φ1.5	φ1.0	1.75	5.5	0.85	4.0	2.0	0.3	12.0	4.0
VSON010X3030	4000	3.30	3.30	φ1.5	φ1.1	1.75	5.5	0.75	4.0	2.0	0.25	12.0	4.0
Tolerance		±0.1	±0.1	$^{+0.1}_{-0}$	±0.1	±0.1	±0.05	±0.1	±0.1	±0.05	±0.05	±0.2	±0.1

Package	Quantity (pcs)	Tape dimensions (all dimensions in mm)											
		A1	B1	D0	D1	E	F	K'	P1	P2	T	W	P0
VSON008X2020	4000	2.20	2.20	φ1.5	φ0.8	1.75	3.5	0.85	4.0	2.0	0.3	8.0	4.0
Tolerance		±0.05	±0.05	$^{+0.1}_{-0}$	±0.1	±0.1	±0.05	±0.05	±0.1	±0.05	±0.05	±0.2	±0.1

< Reel dimensions >

Package	Reel dimensions (all dimensions in mm)						
	A	B	C	D	E	W1	W2
VSON010X3020	φ180	φ60	φ13.0	φ21.0	2.0	13.0	15.4
VSON010X3030	φ180	φ60	φ13.0	φ21.0	2.0	13.0	15.4
VSON008X2020	φ180	φ60	φ13.0	φ21.0	2.0	9.0	11.4
Tolerance	$^{+0}_{-1.5}$	$^{+1.0}_{-0}$	±0.2	±0.8	±0.5	$^{+1.0}_{-0}$	±1.0

< Dehydrated weight >

Dehydrated weight
0.009
0.014
0.006