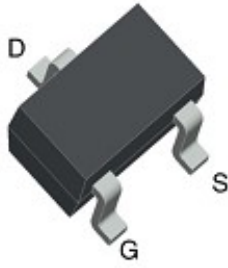
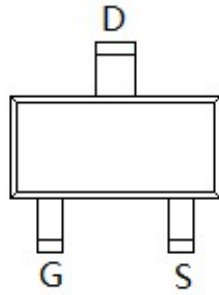


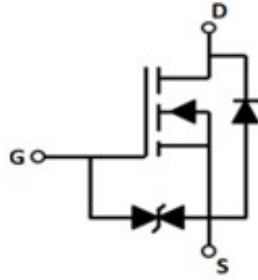
## N-Channel Enhancement Mode Field Effect Transistor



Top View



**SOT-523**



### Product Summary

- $V_{DS}$  20V
- $I_D$  0.77A
- $R_{DS(ON)}$ ( at  $V_{GS}= 4.5V$ ) < 260mohm
- $R_{DS(ON)}$ ( at  $V_{GS}= 2.5V$ ) < 360mohm
- $R_{DS(ON)}$ ( at  $V_{GS}= 1.8V$ ) < 700mohm
- ESD Protected >4.0KV(HBM)

### General Description

- Trench Power LV MOSFET technology
- High Density Cell Design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Load switch
- Power management

### ■ Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	20	V
Gate-source Voltage		$V_{GS}$	$\pm 12$	V
Drain Current	$T_A=25^\circ C$	$I_D$	0.77	A
	$T_A=70^\circ C$		0.62	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	3.0	A
Total Power Dissipation @ $T_A=25^\circ C$ Steady State		$P_D$	0.29	W
Thermal Resistance Junction-to-Ambient <sup>B</sup>		$R_{\theta JA}$	430	$^\circ C/W$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ C$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL1012E	F2	C.	3000	30000	120000	7" reel



# YJL1012E

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> = 250μA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ± 10V, V <sub>DS</sub> =0V		± 2.5	± 10	μA
		V <sub>GS</sub> = ± 8V, V <sub>DS</sub> =0V		± 500	± 2000	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	0.35	0.75	1.1	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 0.50A		160	260	mΩ
		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 0.40A		211	360	
		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 0.20A		300	700	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 0.77A, V <sub>GS</sub> =0V			1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =9V, V <sub>GS</sub> =0V, f=1MHZ		56		pF
Output Capacitance	C <sub>oss</sub>			20		
Reverse Transfer Capacitance	C <sub>rss</sub>			2.5		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 10V, I <sub>D</sub> = 0.5A		1		nC
Gate-Source Charge	Q <sub>gs</sub>			0.3		
Gate-Drain Charge	Q <sub>gd</sub>			0.2		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =4A, di/dt=100A/us		0.4		
Reverse Recovery Time	t <sub>rr</sub>			14		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =9V, I <sub>D</sub> =1A R <sub>GEN</sub> =2.5Ω		2		ns
Turn-on Rise Time	t <sub>r</sub>			19		
Turn-off Delay Time	t <sub>D(off)</sub>			10		
Turn-off fall Time	t <sub>f</sub>			23		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJL</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

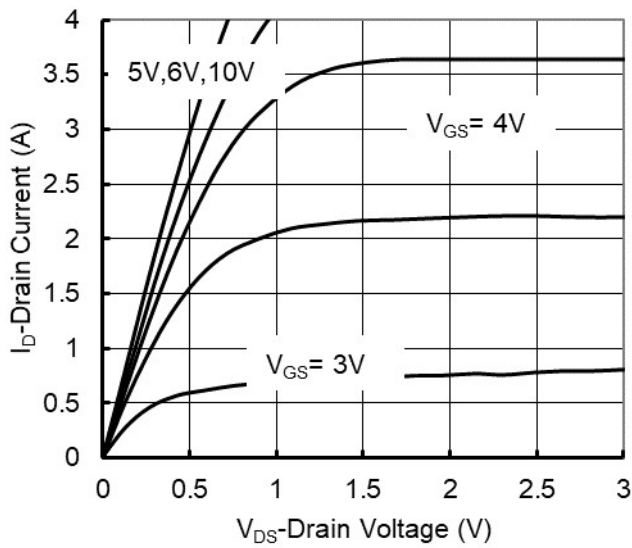


Figure1. Output Characteristics

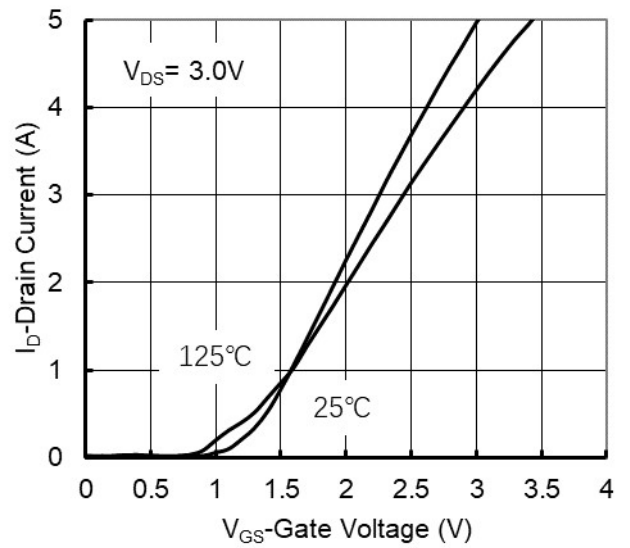


Figure2. Transfer Characteristics

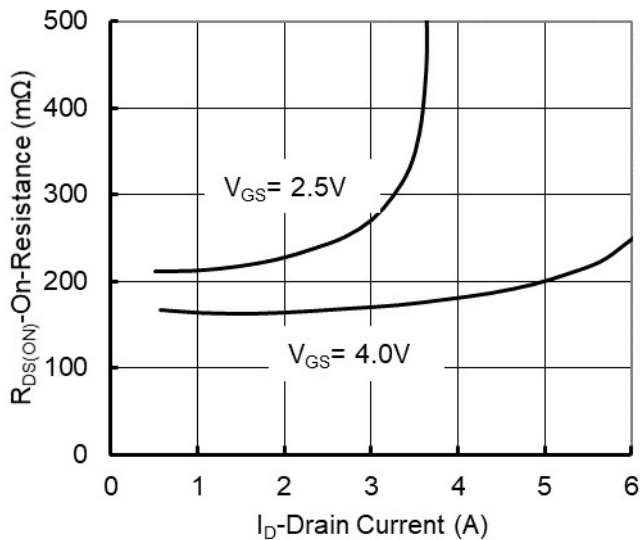


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

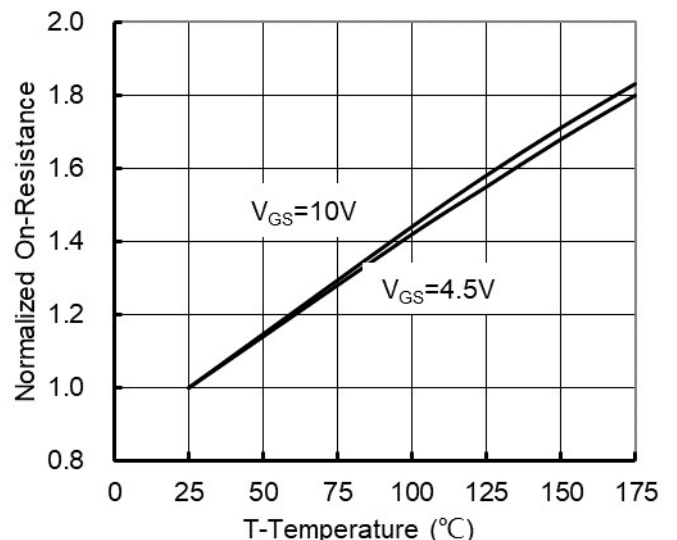


Figure 4: On-Resistance vs. Junction Temperature

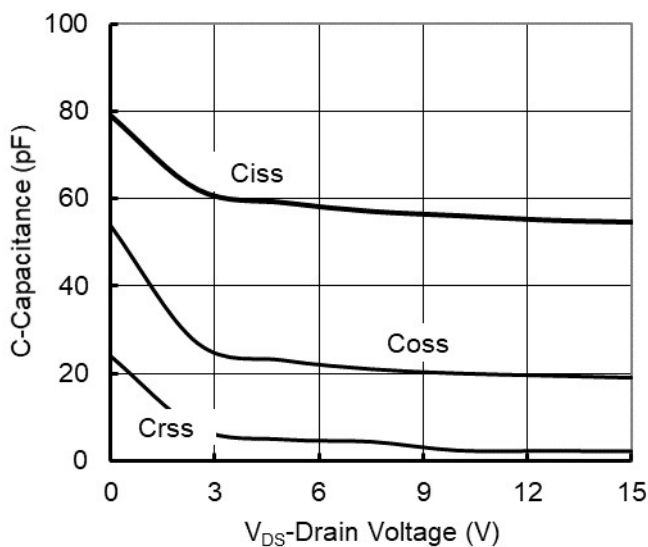


Figure5. Capacitance Characteristics

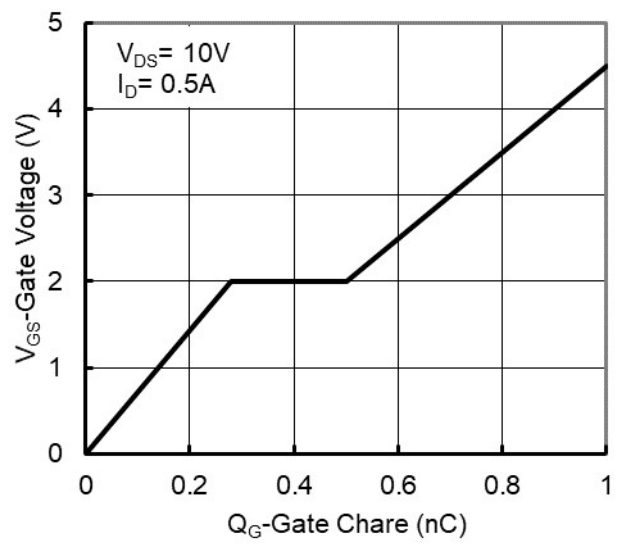


Figure6. Gate Charge

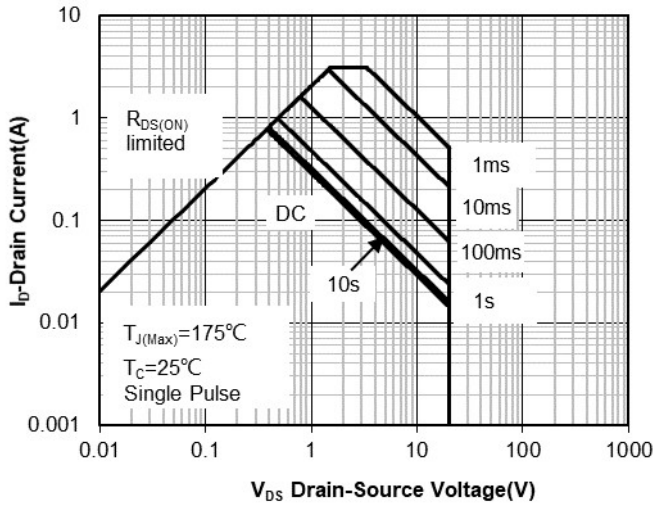


Figure7. Safe Operation Area

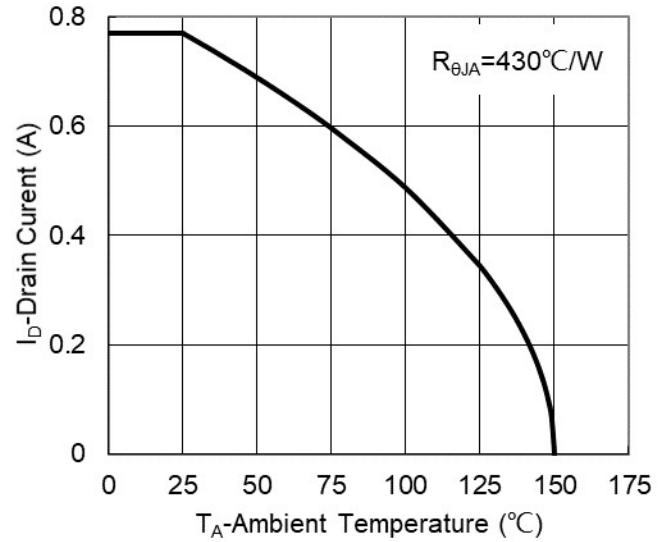


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

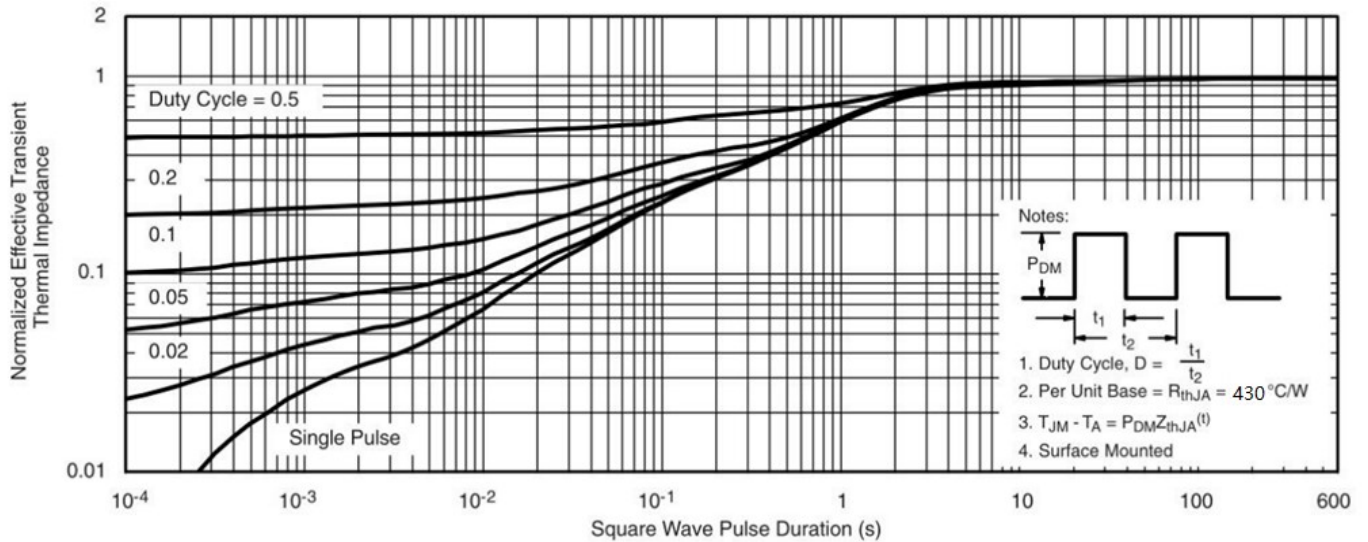
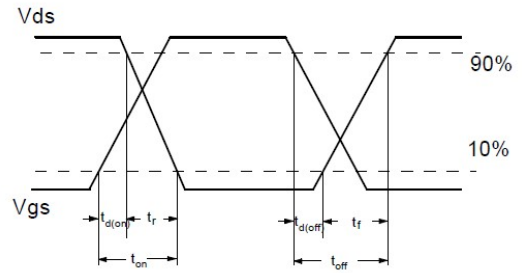
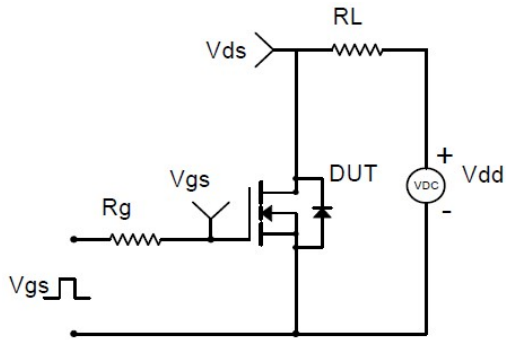
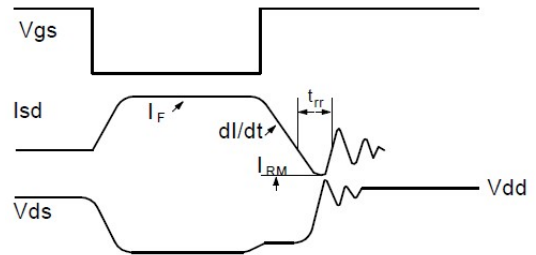
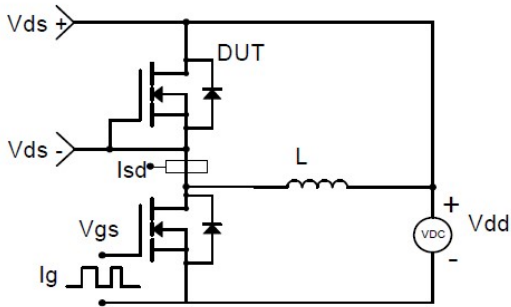


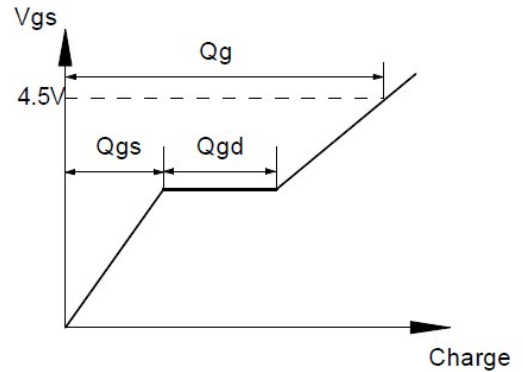
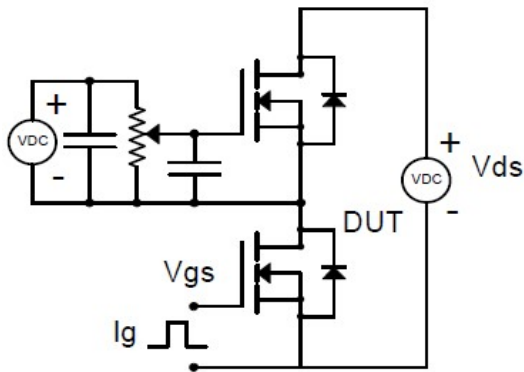
Figure9. Normalized Maximum Transient Thermal Impedance



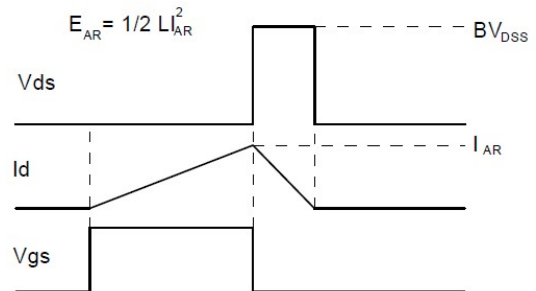
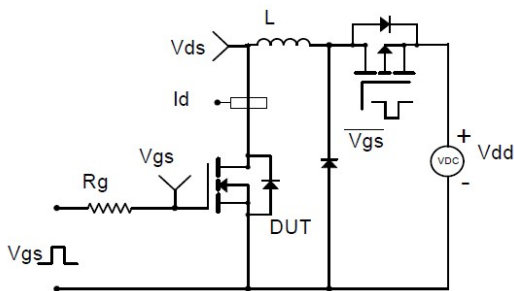
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

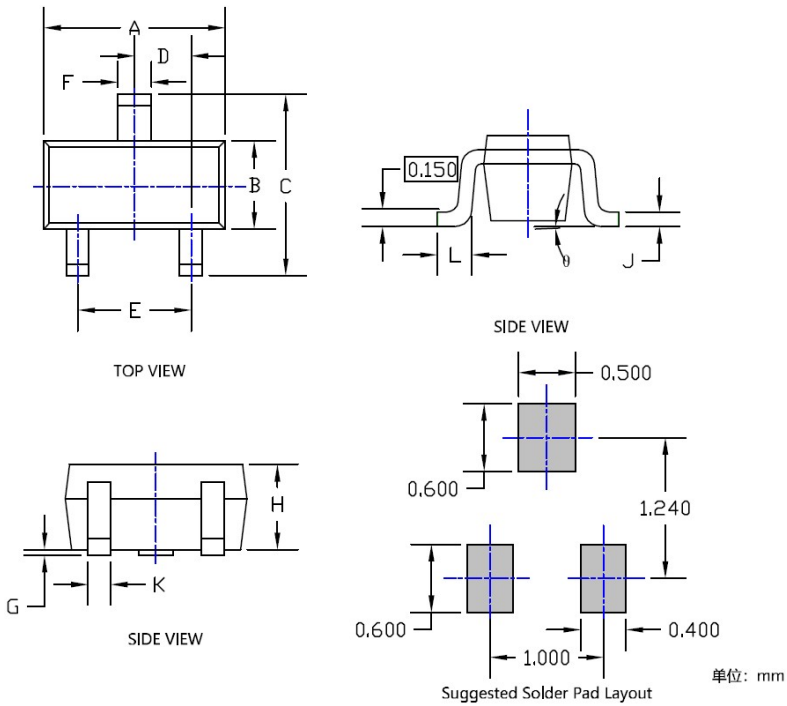


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



# YJL1012E

## ■ SOT-523 Package Information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A	0.059	0.063	0.067	1.500	1.600	1.700
B	0.030	0.031	0.033	0.750	0.800	0.850
C	0.057	0.063	0.069	1.450	1.600	1.750
D	0.020TYP			0.500TYP		
E	0.035	0.039	0.043	0.900	1.000	1.100
F	0.010	0.014	0.018	0.250	0.350	0.450
G	0.000	---	0.004	0.000	---	0.100
H	0.024	0.028	0.031	0.600	0.700	0.800
J	0.004	---	0.008	0.100	---	0.200
K	0.006	0.010	0.014	0.150	0.250	0.350
L	0.010	---	0.018	0.260	---	0.460
θ	0°	---	8°	0°	---	8°

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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