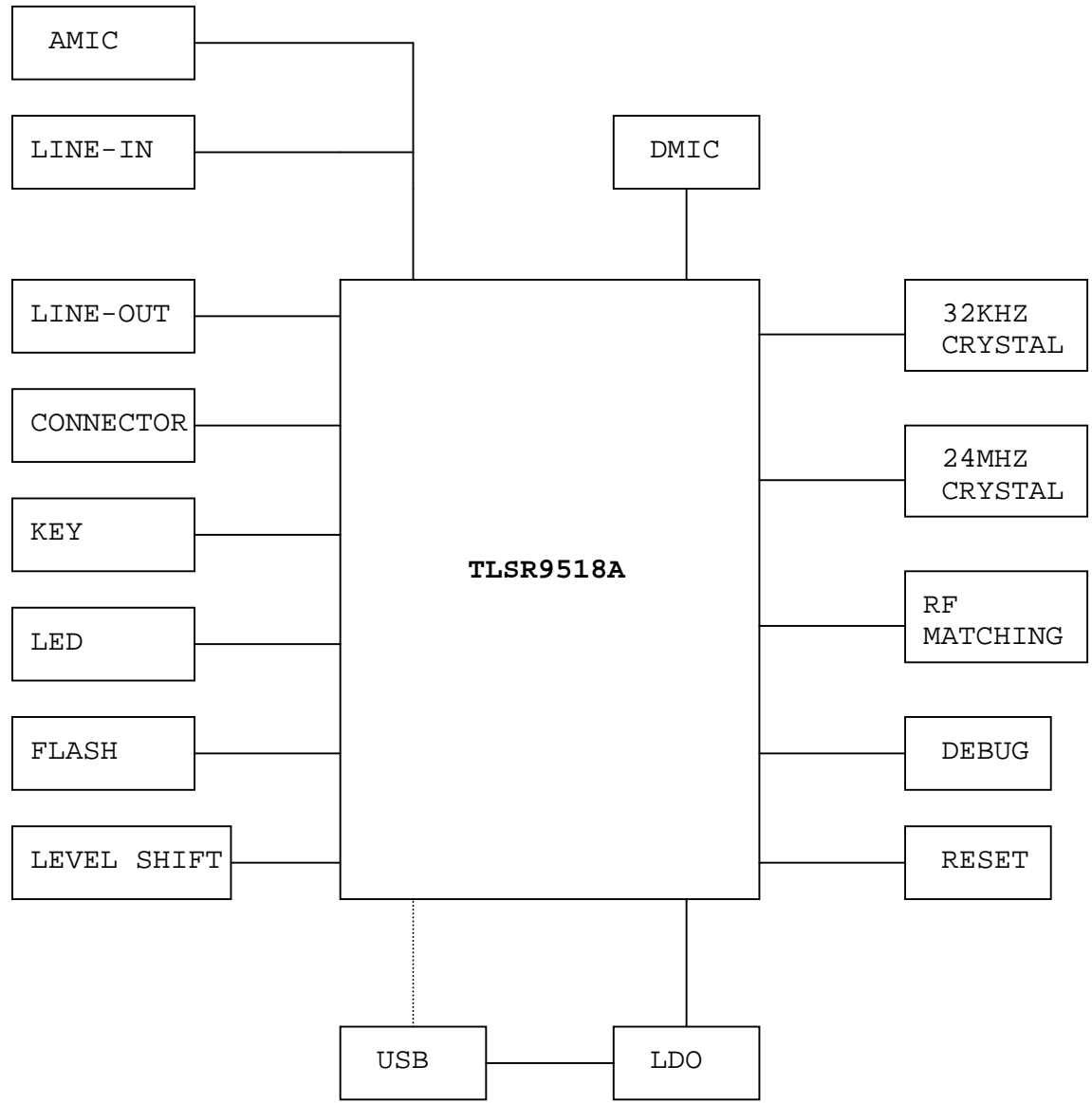
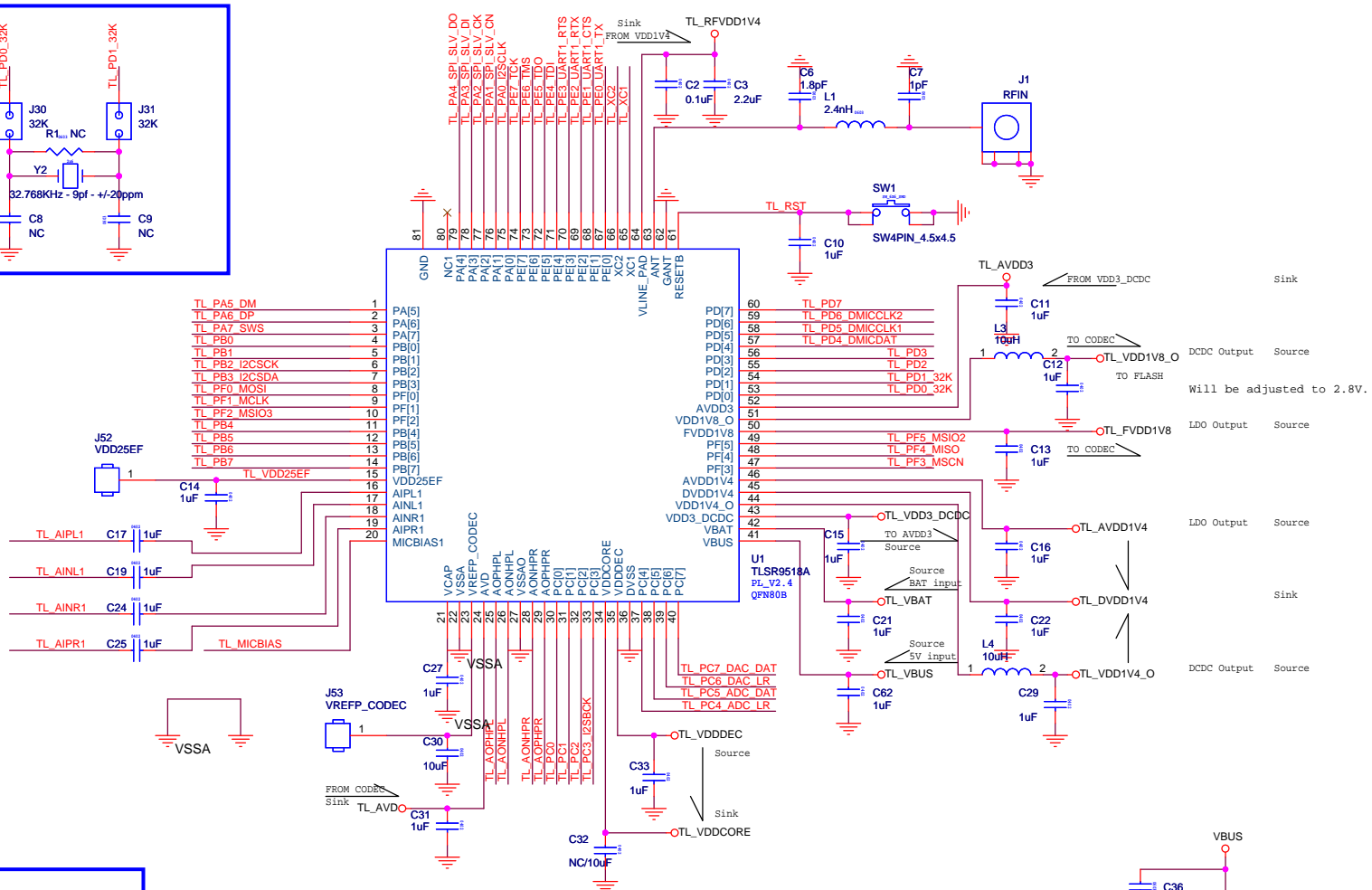
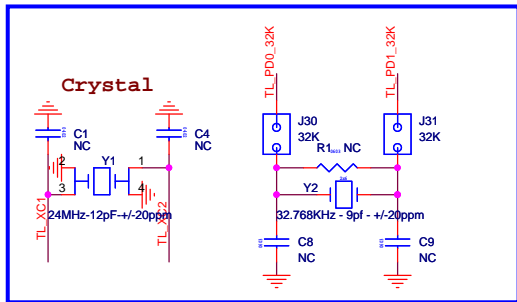


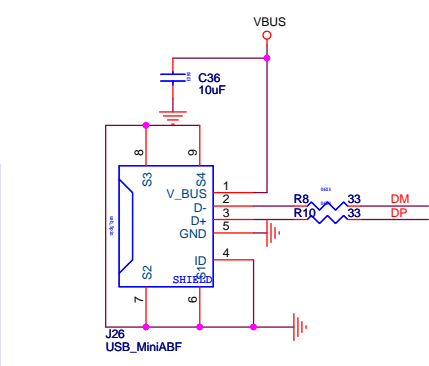
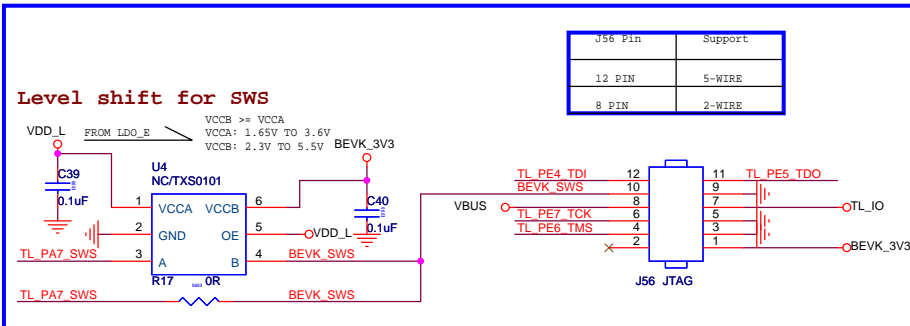
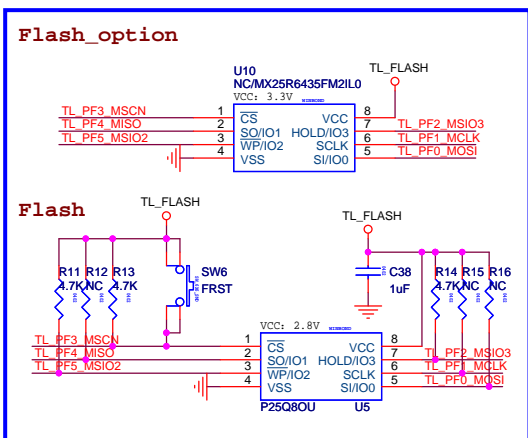
	Author	Approved by
	Xiang	Xiang
	Date	Note
REV1.0	2018/04/17	Initial Version
REV1.1	2018/05/30	<ol style="list-style-type: none"> 1. remove network on PIN23 2. remove network on PIN7 and PIN8 of J50 3. add adjusted 4.2V LDO 4. U5 is changed to GD25Q16E 5. add 3V3 LDO 6. change C30 footprint to 0603C 7. add Flash RESET button 8. add JTAG connector and PE3 9. change C29 and C12 to 1uF/0402
REV1.2	2018/06/24	<ol style="list-style-type: none"> 1. swap J56 2. network of TL_VBAT on J56 is changed to VBUS. 3. add resistor on J57 4. update symbol of J57 5. add a sop-208mil flash 6. add note about SW1 and SW2 7. add note about Line-in/out jack 8. add note about J56 9. change footprint of button 10. change footprint of U8 11. update resistor value used in LDO-4.2V 12. update symbol of TLR9518A
REV1.3	2018/07/27	<ol style="list-style-type: none"> 1. the network of J56`s PIN1 and U4`s PIN6 are changed to BEVK_3V3 2. the network of U4`s PIN1 and PIN5 are changed to VDD_L 3. the network of J51`s PIN9 and PIN11 are changed to VDD_L 4. the network of J51`s PIN10 is changed to TL_IO 5. the network of J51`s PIN12 is changed to TL_VBAT 6. swap the network of J24`s PIN2 and J24`s PIN3 7. correct the silkscreen of J20`s PIN1/3/5/7/9 8. update the value of C6/7, L1 9. update the value of L3/4.



Title		
TELINK		
Size	Document Number	Rev
A4	C1T213A20	V1.3
Date:	Thursday, August 20, 2020	Sheet 2 of 4



- <<DM
- <<DP
- <<TL_PA5_DM
- <<TL_PA6_DP
- <<TL_PB0
- <<TL_PB1
- <<TL_PB2_I2CSCK
- <<TL_PB3_I2CSDA
- <<TL_PB3_I2CSDA
- <<TL_PB4
- <<TL_PB5
- <<TL_PB6
- <<TL_PB7
- <<TL_AIPL1
- <<TL_AINL1
- <<TL_AINR1
- <<TL_AIPR1
- <<TL_MICBIAS
- <<TL_AOPHPL
- <<TL_AONHPL
- <<TL_AONHPL
- <<TL_AONHPR
- <<TL_AOPHPR
- <<TL_PC0
- <<TL_PC1
- <<TL_PC2
- <<TL_PC3_I2SBCK
- <<TL_PC4_ADC_LR
- <<TL_PC5_ADC_DAT
- <<TL_PC6_DAC_LR
- <<TL_PC7_DAC_DAT
- <<TL_PD2
- <<TL_PD3
- <<TL_PD4_DMICDAT
- <<TL_PD5_DMICCLK1
- <<TL_PD6_DMICCLK2
- <<TL_PD7
- <<TL_PE0_UART1_TX
- <<TL_PE1_UART1_CTS
- <<TL_PE2_UART1_RTX
- <<TL_PE3_UART1_RTS
- <<TL_PA0_I2SCLK
- <<TL_PA1_SPI_SLV_CN
- <<TL_PA2_SPI_SLV_CK
- <<TL_PA4_SPI_SLV_DO
- <<TL_RST



J56 Pin	Support
12 PIN	5-WIRE
8 PIN	2-WIRE

- << DM
- << DP
- << TL_PA5_DM
- << TL_PA6_DP
- << TL_PB0
- << TL_PB1
- << TL_PB2_I2CSCK
- << TL_PB3_I2CSDA
- << TL_PB3_I2CSDA
- << TL_PB4
- << TL_PB5
- << TL_PB6
- << TL_PB7
- << TL_AIPL1
- << TL_AINL1
- << TL_AINR1
- << TL_AIPR1
- << TL_MICBIAS
- << TL_AOPHPL
- << TL_AONHPL
- << TL_AONHPR
- << TL_AOPHPR
- << TL_PC0
- << TL_PC1
- << TL_PC2
- << TL_PC3_I2SBCK
- << TL_PC4_ADC_LR
- << TL_PC5_ADC_DAT
- << TL_PC6_DAC_LR
- << TL_PC7_DAC_DAT
- << TL_PD2
- << TL_PD3
- << TL_PD4_DMICDAT
- << TL_PD5_DMICCLK1
- << TL_PD6_DMICCLK2
- << TL_PD7
- << TL_PE0_UART1_TX
- << TL_PE1_UART1_CTS
- << TL_PE2_UART1_RTX
- << TL_PE3_UART1_RTS
- << TL_PA0_I2SCLK
- << TL_PA1_SPL_SLV_CN
- << TL_PA2_SPL_SLV_OK
- << TL_PA3_SPL_SLV_DI
- << TL_PA4_SPL_SLV_DO
- << TL_RST

