

## General Description

The LTP3558 is a high voltage, low power consumption and high performance LDO. The family uses an advanced CMOS process and a P-MOSFET pass device to achieve fast start-up, with high output voltage accuracy. The LTP3558 is stable with a 1.0 $\mu$ F~10 $\mu$ F ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations.

## Features

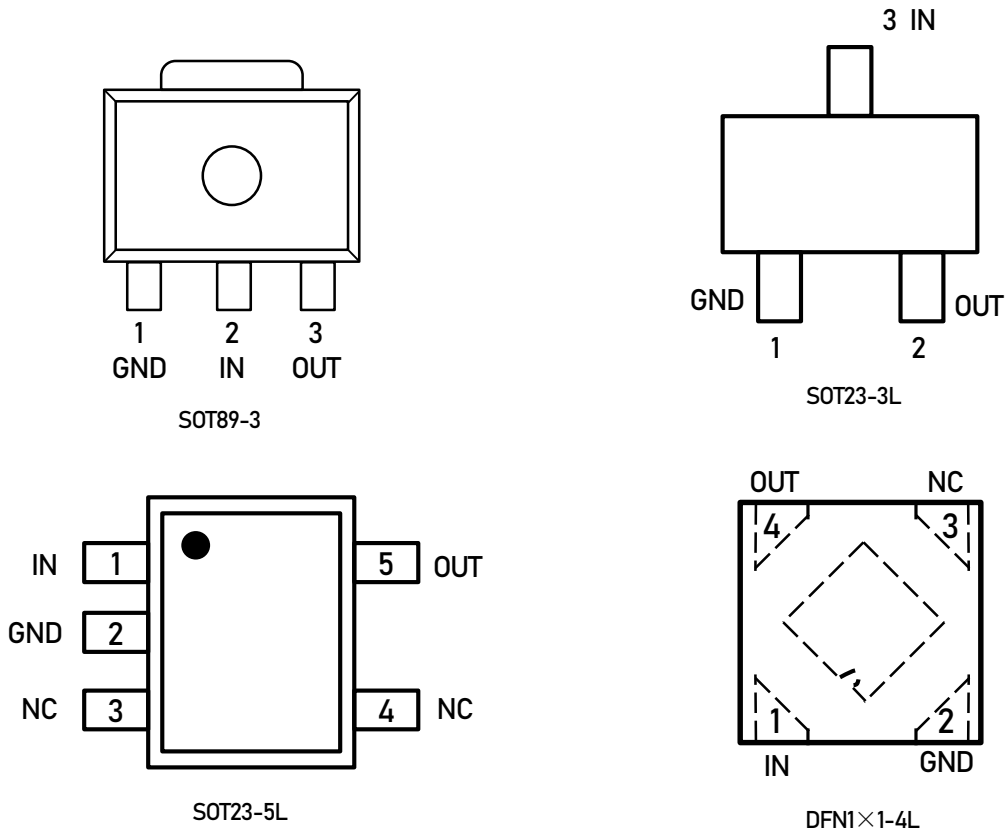
- Wide Input Voltage Range: up to 36V
- Output Current: 200mA
- Standard Fixed Output Voltage Options: 1.8V, 2.5V, 3.0V, 3.3V, 3.6V, and 5.0V
- Other Output Voltage Options Available on Request
- Low I<sub>Q</sub>: 1.5 $\mu$ A
- Low Dropout Voltage
- Short current protection: 100mA
- Excellent Load and Line Transient Response
- Line Regulation: 0.01%/V Typically
- Available Packages:

## Order Information

Model	Package	Ordering Number <sup>Note1</sup>	Packing Option
LTP3558	SOT23-3L	LTP3558-xxXT3	Tape and Reel, 3000
	SOT23-5L	LTP3558-xxXT5	Tape and Reel, 3000
	DFN1x1-4L	LTP3558-xxXF4	Tape and Reel, 10000
	SOT89-3	LTP3558-xxXT4	Tape and Reel, 1000

Note1: xx stands for output voltage, e.g. if xx = 18, the output voltage is 1.8V; if xx = 30, the output voltage is 3.0V.

## Pin Configuration



TOP VIEW

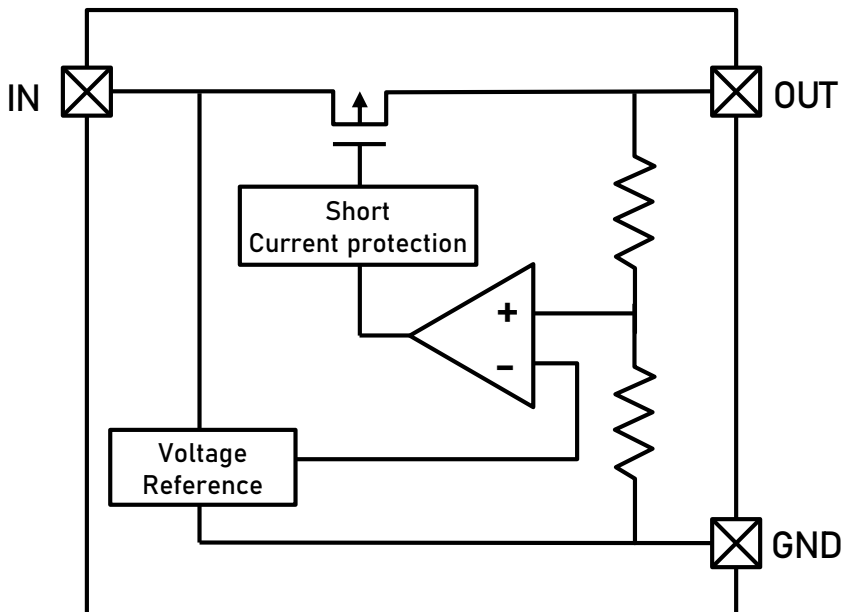
## Pin Function

Pin No.		Pin Name	Pin Function
SOT-89	SOT23-3L		
1	1	GND	Ground.
2	3	IN	Supply input pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor.
3	2	OUT	Output pin. Bypass a 1μF or greater ceramic capacitor from this pin to ground.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.  
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Pin No.		Pin Name	Pin Function
SOT23-5L	DFN1x1-4L		
1	1	IN	Supply input pin. Must be closely decoupled to GND with a 1 $\mu$ F or greater ceramic capacitor.
2	2	GND	Ground.
3	3	NC	No connection.
4		NC	No connection.
5	4	OUT	Output pin. Bypass a 1 $\mu$ F or greater ceramic capacitor from this pin to ground.

## Block Diagram



## Functional Description

### Input Capacitor

A 1 $\mu$ F-10 $\mu$ F ceramic capacitor is recommended to connect between  $V_{in}$  and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both  $V_{in}$  and GND.

## Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 $\mu$ F to 10 $\mu$ F, Equivalent Series Resistance (ESR) is from 5m $\Omega$  to 100m $\Omega$ , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

## Low Quiescent Current

The LTP3558, consuming only around 1.5 $\mu$ A for all input range and output loading, provides great power saving in portable and low power applications.

## Short Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the short current limit protection will be triggered and clamp the output current to approximately 100mA to prevent over-current and to protect the regulator from damage due to overheating.

## Absolute Maximum Ratings

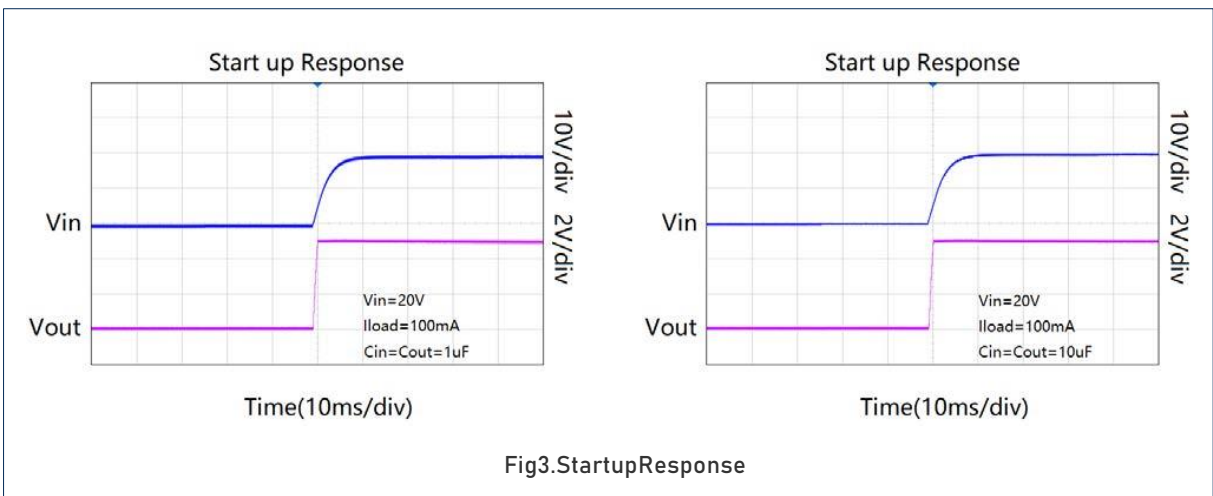
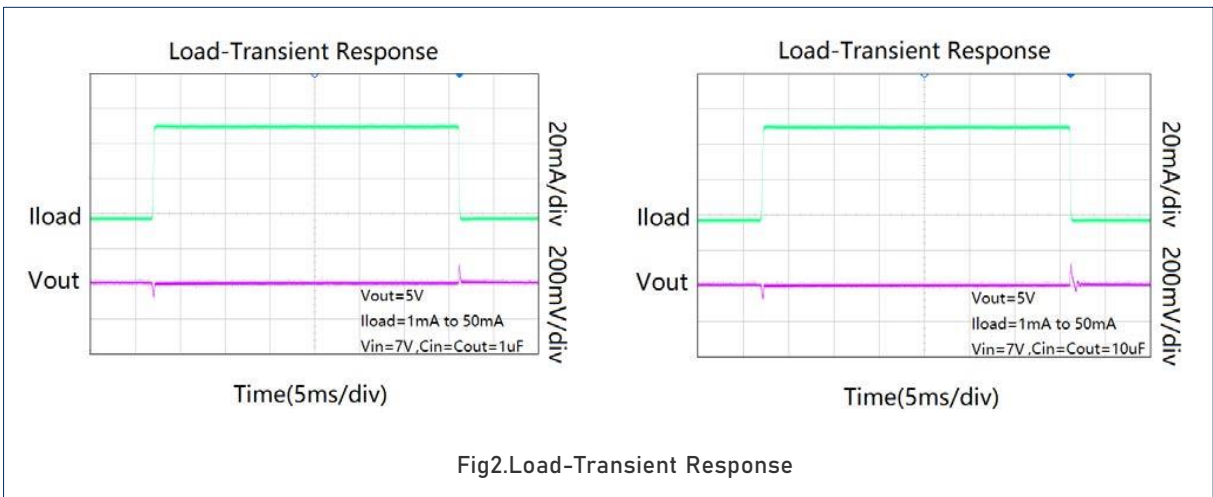
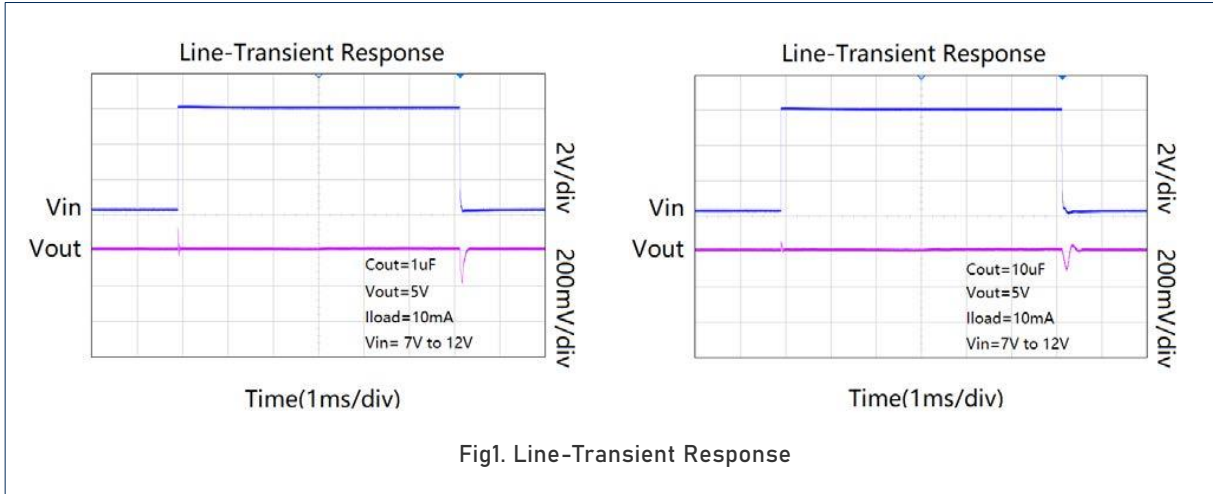
Parameter	Rating	Unit
IN pin to GND pin	-0.3 to 40	V
OUT pin to GND pin	-0.3 to 6	V
Thermal Resistance (Junction to Ambient)	SOT23-3L	360
	SOT23-5L	250
	DFN1X1-4L	180
	SOT-89	135
Operating Junction Temperature	-40 to 125	$^{\circ}$ C
Storage Temperature	-65 to 150	$^{\circ}$ C
Lead Temperature (Soldering, 10 sec)	300	$^{\circ}$ C
ESD (HBM mode)	ESDA/JEDEC JS-001-2017	$\pm$ 2000V

## Electrical Characteristics

( $V_{IN} = V_{OUT} + 2V$ ,  $T_a = 25^\circ C$ ,  $C_{IN} = 10\mu F$ ,  $C_{OUT} = 10\mu F$  unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Operation Range	$V_{IN}$				36	V
Dropout Voltage	$V_{DROPO}$	$V_{OUT} = 5V$ , $I_{OUT} = 150mA$		720		mV
		$V_{OUT} = 5V$ , $I_{OUT} = 100mA$		420		
		$V_{OUT} = 3.3V$ , $I_{OUT} = 150mA$		820		
		$V_{OUT} = 3.3V$ , $I_{OUT} = 100mA$		520		
DC Supply Quiescent Current	$I_Q$			1.5	3	$\mu A$
Regulated Output Voltage	$V_{OUT}$	$I_{OUT} = 1mA$	$V_{OUT} \times 0.98$		$V_{OUT} \times 1.02$	V
Output Voltage Line Regulation	$Reg_{LINE}$	$V_{IN} = V_{OUT} + 1V$ to 30V, $I_{OUT} = 10mA$ ( $\Delta V_{OUT} / \Delta V_{IN} / V_{OUT}$ )		0.01	0.04	%/V
Output Voltage Load Regulation	$Reg_{LOAD}$	$I_{OUT}$ from 1mA to 150mA $V_{IN} = V_{OUT} + 2V$		5	20	mV
		$I_{OUT}$ from 1mA to 150mA $V_{IN} = 10V$		25	60	mV
Maximum Output Current	$I_{OUT}$	$V_{IN} = V_{OUT} + 1V$	200			mA
Short Current Protection	$I_{SHORT}$	OUT short to GND		100		mA
Output Noise	$e_N$	10Hz to 100kHz, $I_{OUT} = 30mA$ ,		90		$\mu V_{RMS}$

## TYPICAL PERFORMANCE CHARACTERISTICS



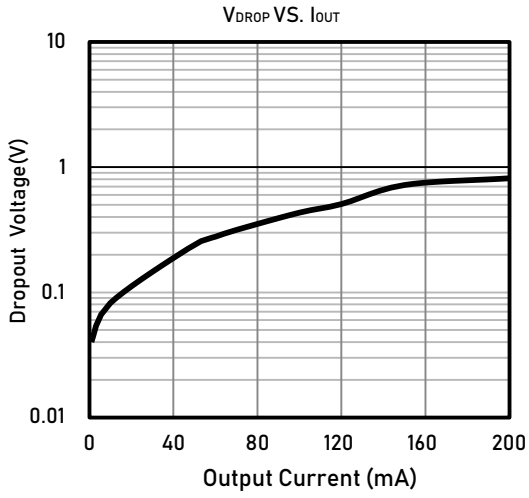


Fig4. Dropout Voltage VS Output Current

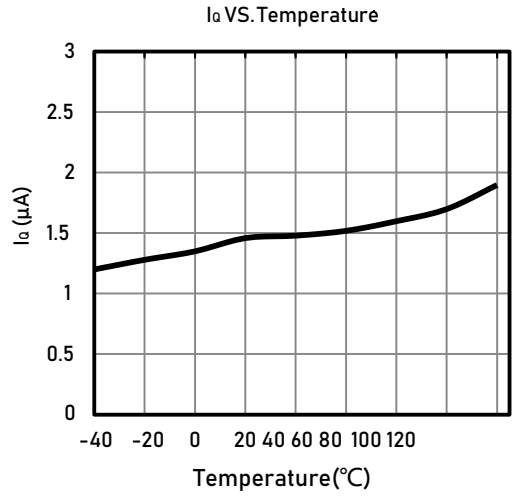
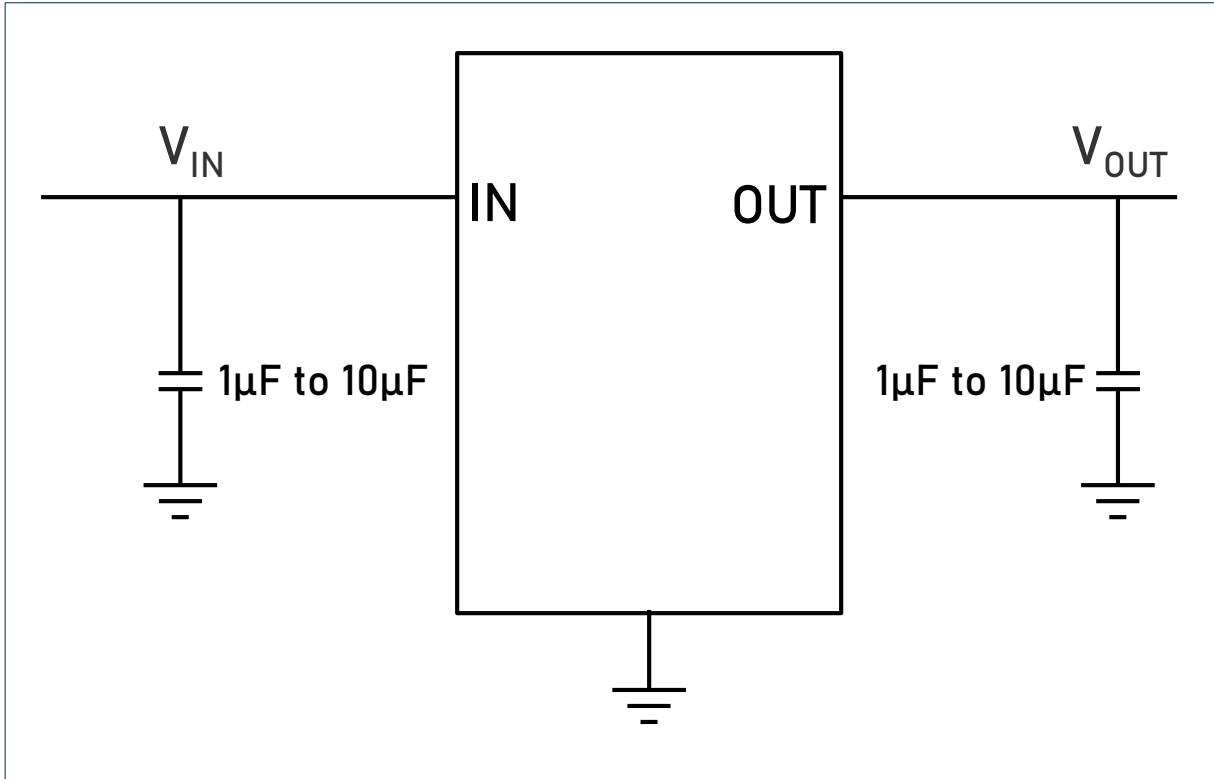


Fig5. DC Supply Quiescent Current VS Temperature

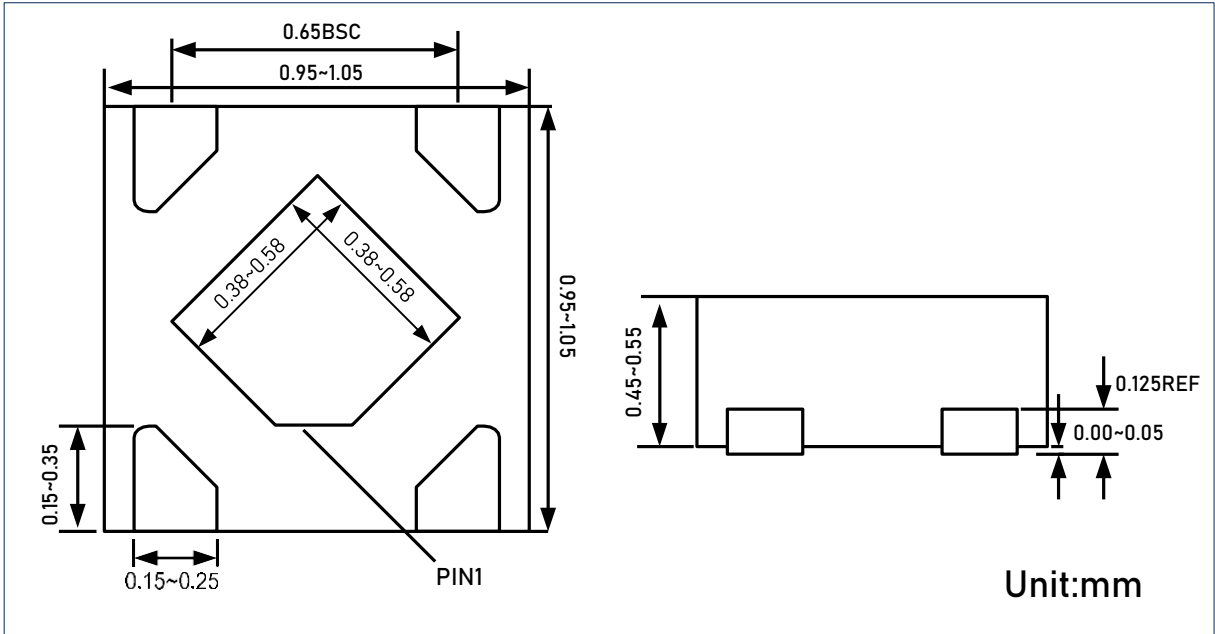
## Application Circuits



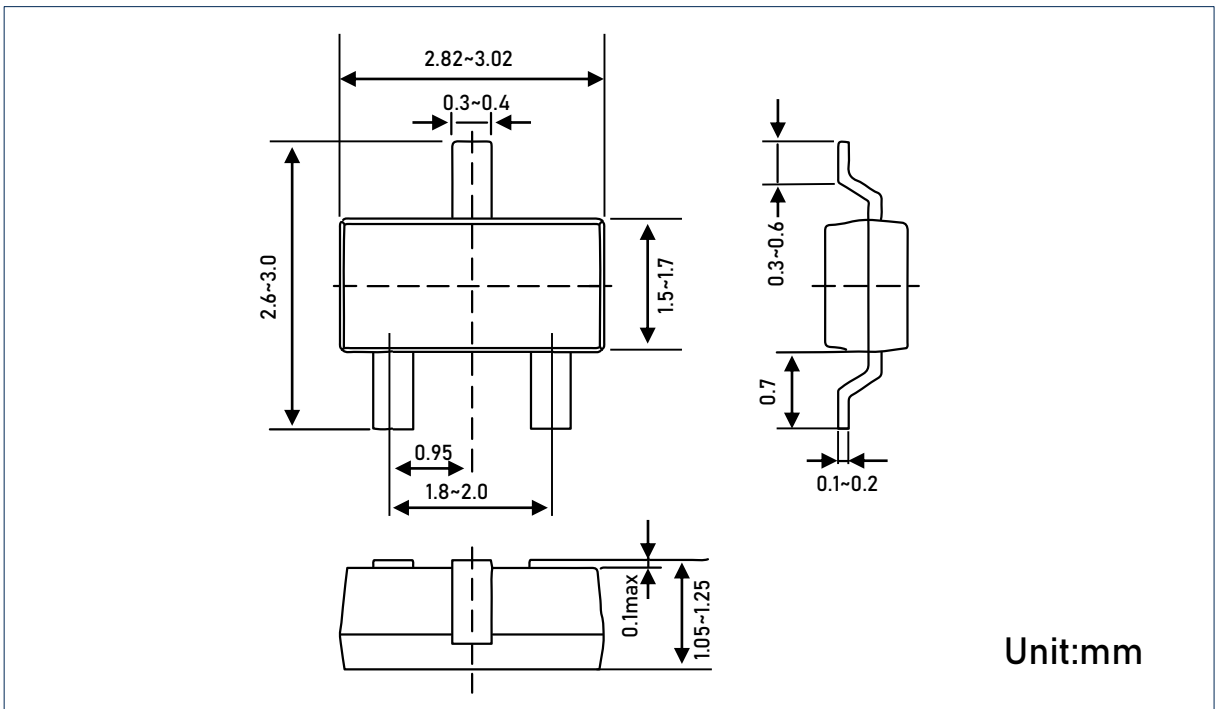


## Package Dimension

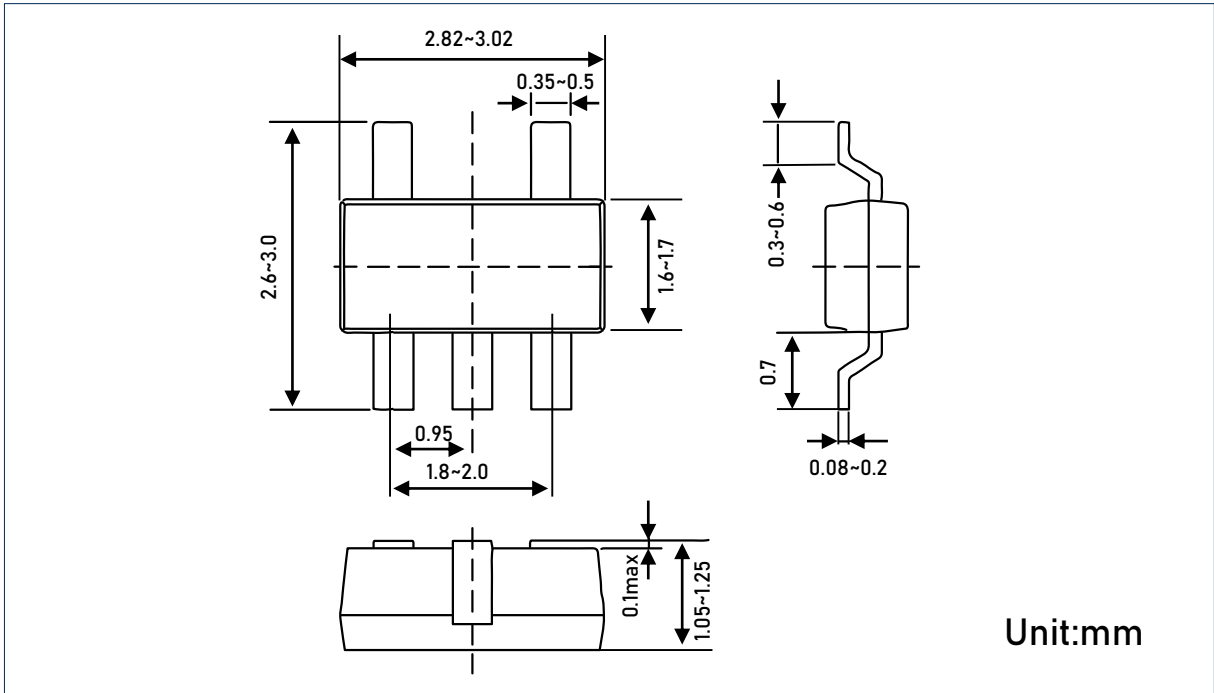
DFN1x1-4L



SOT23-3L



SOT23-5L



SOT-89

