

Ultra-Low Jitter Differential Oscillator

7.0*5.0 S7 Series



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SPECIFICATION

PN:SJK- S7B0000M3C0420F5

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Page 1

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Applications

- 10/40/100 Gbps Ethernet, SONET, SATA, SAS, Fibre Channel
- Telecom, networking, instrumentation, storage, servers

ELECTRICAL SPECIFICATIONS

No	Parameters	Symbol	Condition	Electrical Specifications			
				MIN	TYP	MAX	UNITS
1	Nominal Frequency	-		200.000			MHz
2	Output			HCSL			
3	Operating Temperature	Topr		-40	~	85	°C
4	Storage Temperature	Tstg		-55	~	125	°C
5	Frequency Stability	-		±10			ppm
6	Supply Voltage	VDD		2.97	3.3	3.63	V
7	Current Consumption	I _{dd}	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V			89	mA
8	OE Disable Supply Current	I _{OE}	OE = Low			58	mA
9	Duty Cycle	DC	All V _{dds}	45		55	%
10	Input Voltage High	V _{IH}	Pin 1, OE or ST	70%	-	-	VDD
11	Input Voltage Low	V _{IL}	Pin 1, OE or ST	-	-	30%	VDD
12	Input Pull-up Impedance	Z _{in}	Pin 1, OE logic high or logic low, or ST logic high		100		KΩ
13	Maximum Output Current	I _{driver}	Maximum average current drawn from OUT+ or OUT			35	mA
14	Startup Time	T _{start}	Measured from the time V _{dd} reaches its rated minimum value			3.0	mS
15	OE Enable/Disable Time	T _{oe}				3.8	μs
16	Output Disable Leakage Current	I _{leak}	OE = Low		0.15		μA
17	Output High Voltage	V _{OH}		0.60		0.90	V
18	Output Low Voltage	V _{OL}		-0.05		0.08	
19	Output Differential Voltage Swing	V _{Swing}		1.2	1.4	1.8	V
20	Rise/Fall Time	T _r , T _f	20% to 80%		360	465	ps
21	RMS Period Jitter	T _{jitt}	f = 100, 156.25 or 212.5 MHz, V _{dd} = 3.3V or 2.5V		1.0	1.6	ps
23	First Year Aging	F _{aging1}	85°C	-0.7	±0.4	+0.7	ppm
24	10-year Aging	F _{aging10}	85°C	-1.3	±0.8	+1.3	ppm

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Page 2

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Pin Description

Pin	Map		Functionality
1	OE/NC	Output Enable (OE)	H ^[4] : specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage ^[5]

Top View

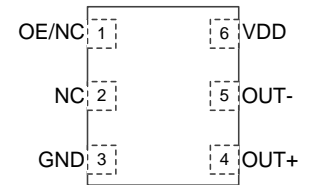


Figure 1. Pin Assignments

Notes:

- In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
- A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 pF capacitor between Vdd and GND is required for the best phase jitter performance

Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Vdd	-0.5	4.0	V
VIH		Vdd + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

Thermal Consideration

Package	θJA, 4 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050, 6-pin	52	19

Note:

- Refer to JESD51-7 for θJA and θJC definitions, and reference layout used to determine the θJA and θJC values in the above table.

Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	G
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	G
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

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Waveform Diagrams

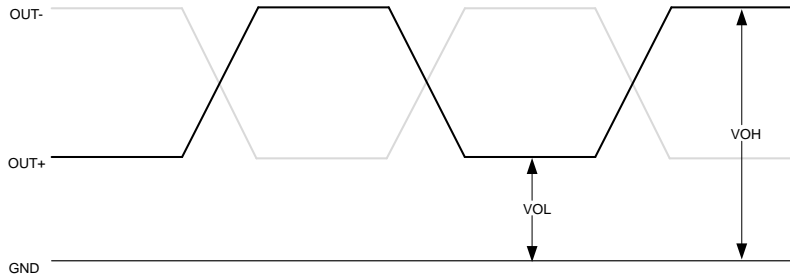


Figure 2. LVPECL, Low-swing LVPECL, and HCSL Voltage Levels per Differential Pin (i.e. OUT+, or OUT-)

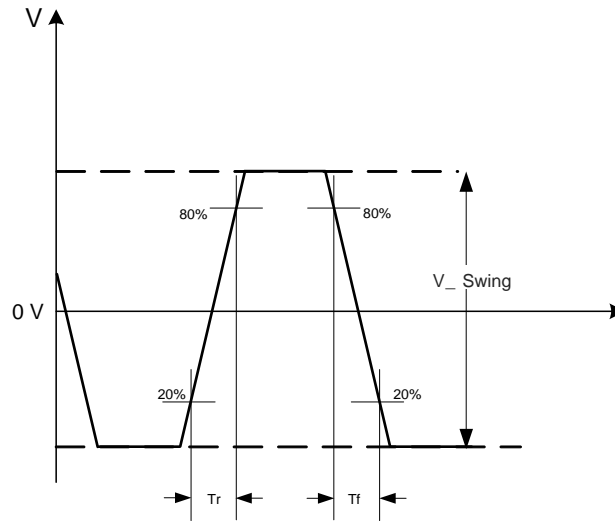


Figure 3. LVPECL, Low-swing LVPECL, and HCSL Voltage Levels Across Differential Pair (i.e. OUT+ minus OUT-)

Termination Diagrams

HCSL:

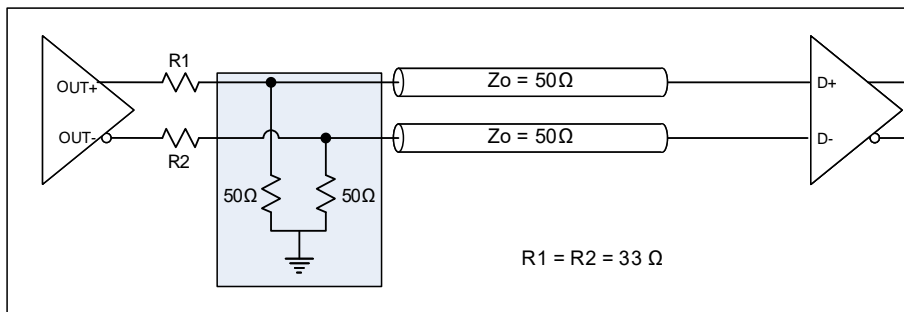


Figure 4. HCSL Typical Termination

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Dimensions and Patterns

