

DESCRIPTION

The CB2402 is a fully integrated, single-chip, single die RF Front-end Integrated Circuit. which incorporates all the RF functionality needed for today's wireless communications.

The CB2402 architecture integrates the PA, LNA, Transmit and Receive switching circuitry, the associated matching network, and the harmonic filter all in a CMOS single-chip device. The CB2402 is designed for use in 802.11b/g/n applications operating at 2.4GHz. Combining superior performance, high sensitivity and efficiency, low noise, small form factor, and low cost, the CB2402 is the ideal solution for single antenna applications, and the ideal building block for MIMO applications.

CB2402 has simple and low-voltage CMOS control logic, and requires minimal external components for system implementation. The PA power detector circuit is also integrated.

BLOCK DIAGRAM

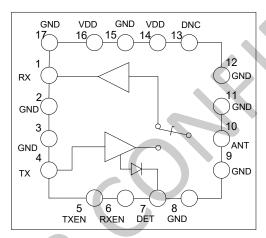


Figure 1. CB2402 Block Diagram

FEATURES

- 2.4GHz ISM, Single Chip, Single-Die RF Front-End IC
- Separate TX and RX Transceiver Port and Single Antenna Port
- 2.4GHz Power Amplifier with Low-Pass Harmonic Filter
- Low Noise Amplifier
- Transmit / Receive Switch Circuitry
- High Transmit Signal Linearity Meeting Standards for OFDM and CCK Modulation
- Integrated Power Detector for Transmit Power Monitor and Control
- Compatible with Low Voltage (1.2V) CMOS
 Control Logic or levels up to VDD
- ESD Protection Circuitry on All Ports
- DC Decoupled RF Ports
- Internal RF Decoupling on All VDD Bias Pins
- Low Noise Figure for Receive Channels

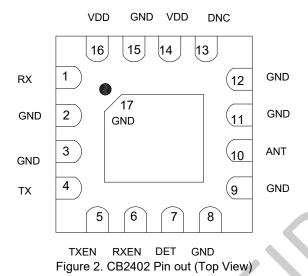
- High Power Capability for Received Signals
- Very Low DC Power Consumption
- Full On-chip Matching and Decoupling Circuitry
- Minimal External Components Required
- 50-Ohm Input / Output Matching
- Market Proven CMOS Technology
- 3 x 3 x 0.55mm Small Outline QFN-16 Package with Exposed Ground Pad

APPLICATIONS

- 802.11b/g/n Embedded Applications
- 802.11b/g/n NIC PC Card
- 802.11b/g/n Multimedia Applications
- 802.11b/g/n Mobile Platforms
- Other 2.4GHz Transceivers
- 802.11b/g/n Access Point



PIN-OUT DIAGRAM



PIN ASSIGNMENTS

Pin	Name	Description		
1	RX	Received RF Signal from the LNA to the Transceiver; DC Shorted to GND		
2, 3, 8, 9,11,12, 15, 17	GND	Ground – Must be connected to Ground in the Application Circuit		
4	TX	Transmitted RF signal from the Transceiver to the PA: DC Shorted to GND		
5	TXEN	CMOS Input to Enable the PA		
6	RXEN	CMOS Input to Enable the LNA		
7	DET	Analog Voltage Proportional to the PA Power Output		
10	ANT	Antenna port RF Signal from the PA or RF Signal Applied to the LNA; DC Shorted to GND		
13	DNC	Reserved – Do Not Connect in the Application Circuit		
14,16	VDD	Voltage Supply Connection		



CB2402 ABSOLUTE MAXIMUM RATINGS

Parameters	Conditions	Minimum	Maximum	Units
DC VDD Voltage Supply	All VDD Pins	0	4.5	V
DC Control Pin Voltage	Through 1Kohm resistor	0	3.6	٧
DC VDD Current Consumption	Through VDD Pins when TX is "ON"		350	mA
DC Control Pin Current Consumption			1	uA
TX RF Input Power	All Operating Modes		+10	dBm
ANT RF Input Power	When RX is "ON"		+5	dBm
Storage Ambient Temperature	No RF and DC Voltages Applied Appropriate care required according to JEDEC Standards	-50	+150	ပ္
ESD Voltage (HBM)	Human Body Model	1000		V

NOTE:

Sustained operation at or above the Absolute Maximum Ratings for any single or combinations of the above parameters may result in permanent damage to the device and is not recommended. All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.

RECOMMENDED OPERATING CONDITIONS

Parameters	Conditions	Minimum	Typical	Maximum	Units
Operating Frequency		2.4		2.5	GHz
DC VDD Voltage Supply	All VDD Pins	2.7	3.3	3.6	V
Control Voltage "High"		1.2	2.0	VDD	V
Control Voltage "Low"			0	0.3	V
Control Pin Current Consumption			1		μΑ
DC Shutdown Current				5	μA
PA Turn On/Off Time			8.0		µsec
Input/Output Single-Ended Impedance			50		Ω
Operating Ambient Temperature	All Operating Modes	-40		+85	°C



CB2402 ELECTRICAL SPECIFICATIONS¹

Parameters	Test Condition	Min	Тур.	Max	Units
Transmit Mode: (VDD=3.3V; T=+25℃)					
Operating Frequency Band	All RF Pins Terminated by 50 Ohms	2.4		2.525	GHz
Output P1dB	CW		+22		dBm
Linear Output Power 802.11b	1Mbps CCK, Mask Compliance	+20	+21		dBm
Linear Output Power 802.11n	54Mbps OFDM, EVM< -33dB at ANT		16		dBm
Linear Output Power 802.11g	54Mbps OFDM, EVM<-30 dB at ANT	16	17		dBm
Large-Signal Power Gain in All Modes	POUT = +18dBm		26		dB
Small-Signal Power Gain in All Modes	POUT = 0dBm		26.5		dB
TX Quiescent Current	No RF Input Signal		95		mA
TX Linear Current	POUT = +17.5dBm		160		mA
Power Detector Voltage Output	POUT = +5 to +20dBm	250		2500	mV
Second Harmonic	POUT = +20dBm, CW at ANT Pin		-35		dBc
Third Harmonic	POUT = +20dBm, CW at ANT Pin		-35		dBc
Input Return Loss			-10		dB
Output Return Loss			-10		dB
Input / Output Impedance Single-Ended			50		Ohm
TX Leakage to RX Port	POUT = +20dBm at ANT		-7		dBm
Load VSWR for Stability (CW, Fix Pin for POUT = +20dBm with 50Ω Load)	All non-harmonically related spurs less than -43 dBm/Hz	4:1	6:1		N/A
Load VSWR for Ruggedness (CW, Fix Pin for POUT = +20dBm with 50Ω Load)	No damage	8:1	10:1		N/A

Parameters	Test Condition	Min	Typ.	Max	Units	
Receive Mode: (VDD=3.3V; T=+25	Receive Mode: (VDD=3.3V; T=+25℃)					
Operating Frequency Band	All RF Pins Terminated by 50 Ohms	2.4		2.525	GHz	
Gain			10		dB	
Noise Figure			3.5		dB	
Input Return Loss			-10		dB	
Output Return Loss			-10		dB	
RF Port Impedance			50		Ohm	
RX Quiescent Current	No RF Applied		10mA		mA	
Input P1dB	No RF Applied		2		dBm	

Parameters	Test Condition	Min	Тур.	Max	Units
Standby Mode:					
DC Shutdown Current				5	uA
TX-ANT Insertion Loss (S21)	Pin < -20dBm		-50		dB
TX Port Return Loss (S11)	From TX Port		-5		dB
ANT-RX Insertion Loss (S21)	Pin < -20dBm		-27		dB
RX Port Return Loss (S22)	From RX Port		-1.5		dB
Transmit-Receive Switching Time			800		ns
Shut-Down and "ON" State Switching Time			800		ns



LOGIC TRUTH TABLE

Mode	LEN	PEN
TX Active	1	X
RX Active	0	1
Chip is Shut-down	0	0

NOTE:

- 1. "1" denotes high voltage state (> 1.2V)
- 2. "0" denotes low voltage stage (<0.3V) at Control Pins
- 3. "X" denotes do not care: either "1" or "0" can be applied



EVALUATION BOARD SCHEMATIC

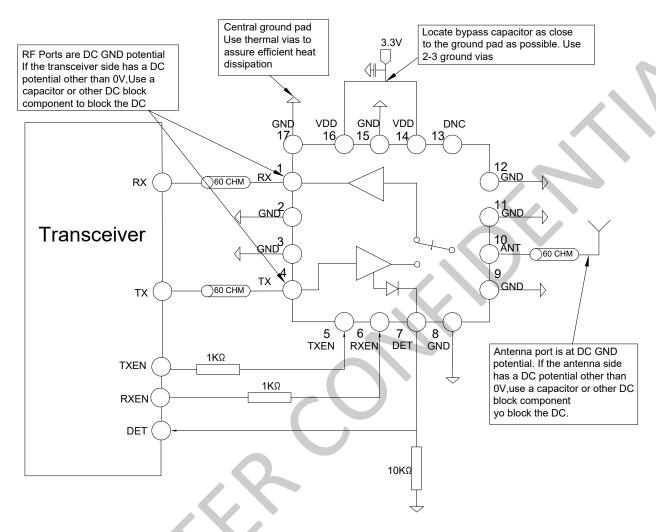


Figure 3. CB2402 Evaluation Board Schematic



EVALUATION BOARD ASSEMBLY DRAWING

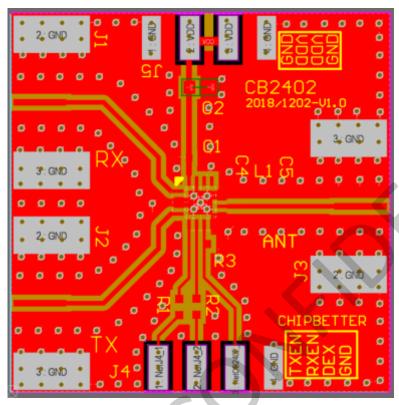
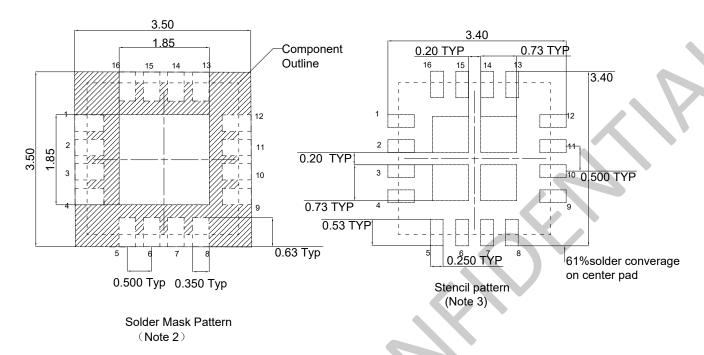


Figure 4. CB2402 Evaluation Board Assembly Drawing



PCB LAND PATTERN



NOTES:

- 1. Via hole recommendations:0.025mm Cu via wall plating(minimum). solder mask oon the far side should tent or plug via holes.
- 2. Soldermask recommendations:contact board fabricator for recommended soldermask offset and tolerance.
- Stencil recommenfations:
 0.125 mm stencil thickness laser cut apertrues,
 trapezoidal walls and rounded comers offer better paste release.

Figure 5. CB2402 PCB Layout Footprint



TYPICAL PART MARKING

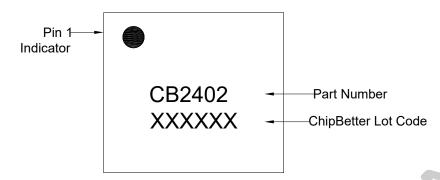


Figure 6. Typical Part Marking for the CB2402

PACKAGE DIMENSIONS (All Dimensions in mm):

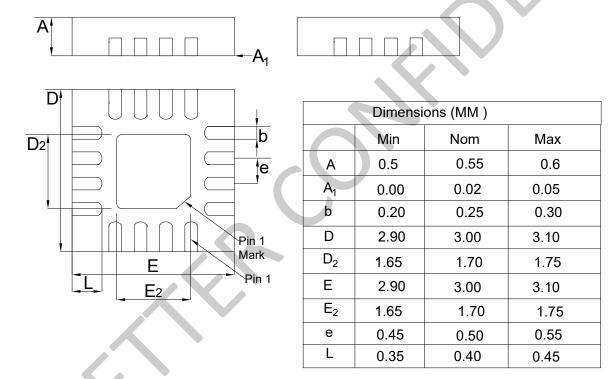
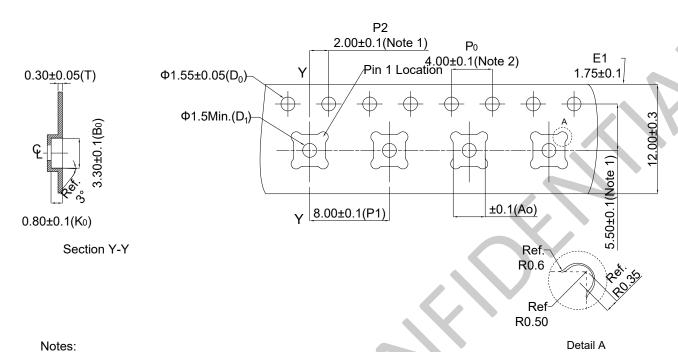


Figure 7. CB2402 Package Dimension



TAPE AND REEL DIMENSIONS



- 1. Measured from center line of sprocket hole to center line of pocket.
- 2. Cumulative toelrance of 10 sprocket holes is \pm 0.20mm.
- 3. Other material available.
- 4. Typical ESD surface resistivity is from 10⁵ to 10¹¹ Ohms/square per EIA,JEDEC.

All measurements are in millimeters.

Figure 8. CB2402 Tape and Reel Dimensions



CONTACT INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

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