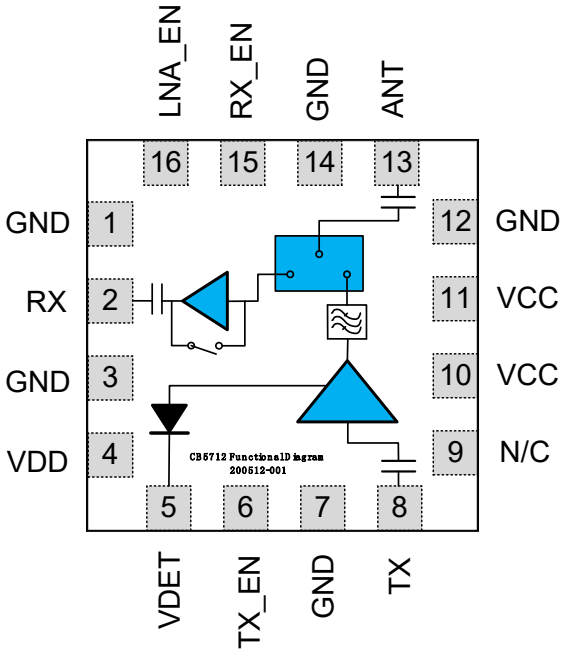


Figure 1. CB5712 Block Diagram

Description

CB5712 is a highly integrated RF Front-End Integrated Circuit which incorporates key RF functionality needed for IEEE 802.11a/n/ac WLAN systems operating in the 5.15-5.9GHz range. CB5712 integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device.

CB5712 has simple and low-voltage control logic, and requires minimal external components. A power detector is also integrated for accurate monitoring of output power from the PA.

CB5712 is assembled in a compact, low-profile 3x3x0.55mm 16-lead QFN package. CB5712 is the ideal RF front-end solution for implementing 5GHz high-power WLAN systems supporting multiple standards including 802.11ac.

Applications

- 802.11ac Wi-Fi Devices
- Tablets / MIDs
- Wi-Fi Media Gateways
- Consumer Electronics
- Notebook / Netbook / Ultrabook
- Access Points / Routers
- Set Top Boxes / Wireless IPTVs
- Other 5GHz ISM Platforms

FEATURES

- Integrated high performance 5GHz PA, LNA with bypass and T/R switch
- Fully-matched input and output
- Integrated power detector
- Transmit gain: 30dB
- Receive gain: 13dB
- Output power: +20dBm @ 1.8% EVM, VHT80/MCS9, 5V
- Output power: +21dBm @ 3% EVM, HT40/MCS7, 5V
- Integrated 2.4GHz Notch Filter
- ESD protection circuitry on all PINs
- DC decoupled RF ports
- Minimal external components required
- Small package: QFN16 3mm x 3mm x0.55mm (MSL3, 260℃ per JEDEC J-STD-020)
- RoHS and REACH Compliant

Table 1. PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1,3,7,12,14	GND	Ground – Must Be Connected to GND in the Application Circuit
2	RX	RF Output Port from LNA or Bypass
4	VDD	LNA/Switch/Regulator Supply Voltage
5	VDET	Analog Voltage Proportional to the PA Power Output
6	TX_EN	Input to Control TX Enable
8	TX	RF Input Port from the Transceiver
9	NC	Internally Not Connected
10,11	VCC	PA Supply Voltage
13	ANT	Antenna Port RF Signal from the PA or RF Signal Applied to the LNA
15	RX_EN	Input to Control RX Enable
16	LNA_EN	Input to Control LNA Enable or Bypass Mode

PIN-OUT DIAGRAM

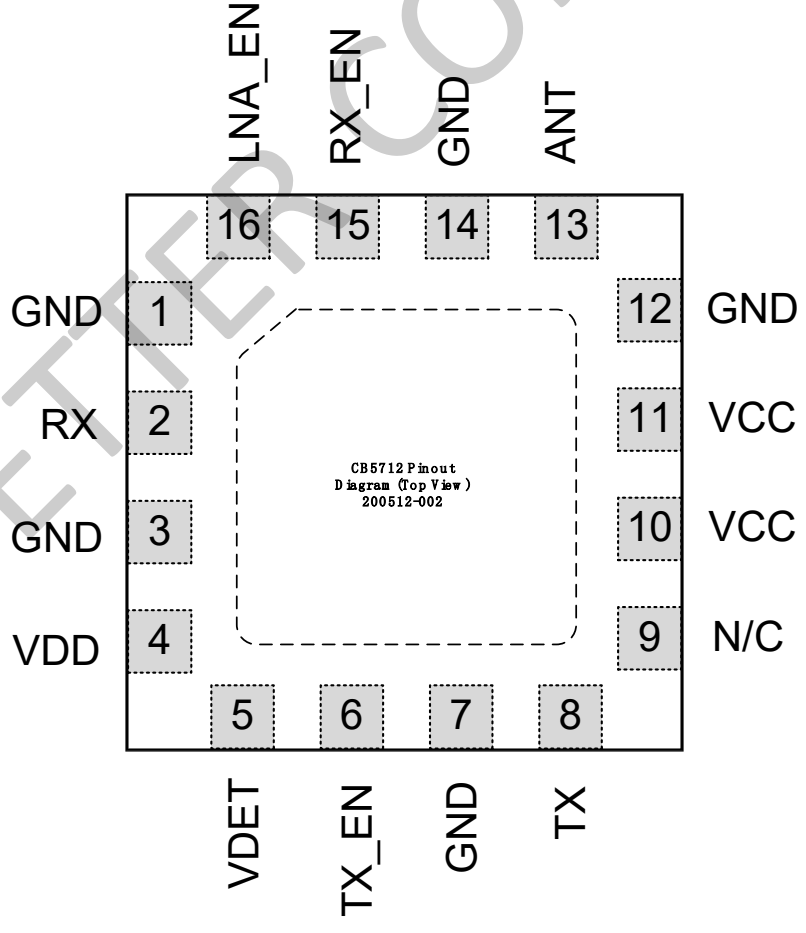


Figure 2. CB5712 Pin out-16 Pin QFN (Top View)

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Units	Min	Max	Conditions
DC Supply Voltage	V	0	6.0	VDD and VCC
Control Pin Voltage	V	0	3.6	All Control Pins
DC Current Consumption	mA		400	
Input Power (50 ohm load)	dBm		+5	
Storage Temperature	℃	-40	150	
Operation Temperature	℃	-40	85	
Junction Temperature	℃		150	
ESD	V		1000	All PINs, HBM

NOTE: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended.

All Maximum RF Input Power Ratings assume 50-ohm terminal impedance.

Table 3. NOMINAL OPERATING CONDITIONS

Parameters	Units	Min	Typ	Max	Conditions
DC Supply Voltage	V	4.5	5	5.5	VDD and VCC
Control Pin Voltage “High”	V		2.8		
Control Pin Voltage “Low”	V	0		0.3	
Control Pin DC Current	uA		50		
Operation Temperature	℃	-40		85	

Table 4. CB5712 ELECTRICAL SPECIFICATIONS

(VDD=VCC= 5V, T = 25℃, Unless Otherwise Noted)

Parameters	Units	Min	Typ	Max	Conditions
Frequency range	GHz	5.15		5.9	Main frequency band
Transmit Mode					
Gain	dB	28	30	31	
Gain Flatness	dB	-0.5		+0.5	Over Any 80MHz Bandwidth
Output Power	dBm	+19.5 +20 +22	+20 +21 +23		With -45dB EVM source VHT80/MCS9, 1.8% DEVM, Preamble only HT40/MCS7, 3% DEVM, Preamble Only HT20/MCS0, Mask Compliance
Current Consumption	mA	240 280 290 320	250 290 300 330		CW Signal @ No RF @+20dBm @+23dBm @+26dBm
Harmonics	dBm/MHz	-35 -50			Pout = +23dBm, HT20/MCS0 2nd harmonics 3rd harmonics
Isolation	dB	-35			From ANT to either TX or RX Pin
Input Return Loss	dB		-11	-10	
Output Return Loss	dB		-11	-10	
Power Detector Output	V		0.25 0.5 0.8		@ No RF @+20dBm @+26dBm
Power Detector Variations	dB	-0.5 -1.5		0.5 1.5	Power Range from 0dBm~+26dBm Nominal Load VSWR=3:1
PA Switching Time	nS		400		
Stability (VSWR)			6:1		All non-harmonically related outputs less than -36dBm/MHz
Ruggedness (VSWR)			10:1		Pin =+10dBm, No Permanent Damage
Receive Mode					
Gain	dB	12	13	14	
Input Power of P1dB	dBm		-1 +8		LNA Active LNA Bypass
Gain Flatness	dB	-0.5		+0.5	Over any 80MHz Bandwidth
Noise Figure	dB		2.5	3.0	

Input Return Loss	dB		-15		
Output Return Loss	dB		-10		
Maximum Input Power	dBm		0 +15		LNA Active LNA Bypass
Switching Time	nS		200 800		LNA←→Bypass RX←→TX
DC Quiescent Current	mA		11 1.5	13	LNA Active LNA Bypass
Receive Bypass Mode					
Insertion Loss	dB		8		

Table 5. CONTROL LOGIC TABLE

TX_EN	LNA_EN	RX_EN	Mode of Operation
0	0	0	Shutdown Mode
1	0	0	Transmit Mode
0	1	1	Low NF Receive Mode
0	0	1	LNA Bypass Receive Mode
All Others			Unsupported (No Damage)

Note: "1" denotes high voltage state (=2.8V)
"0" denotes low voltage state (<0.3V) at Control Pins
"X" denotes the don't care state
1KΩ – 10KΩ series resistor may be required for each control line

Evaluation Board Description

The CB5712 Evaluation Board is used to test the performance of the CB5712 FEM. A suggested application schematic diagram is shown in Figure 3. A photograph of the Evaluation Board is shown in Figure 4. Table 6 provides the Bill of Materials (BOM) list for Evaluation Board components.

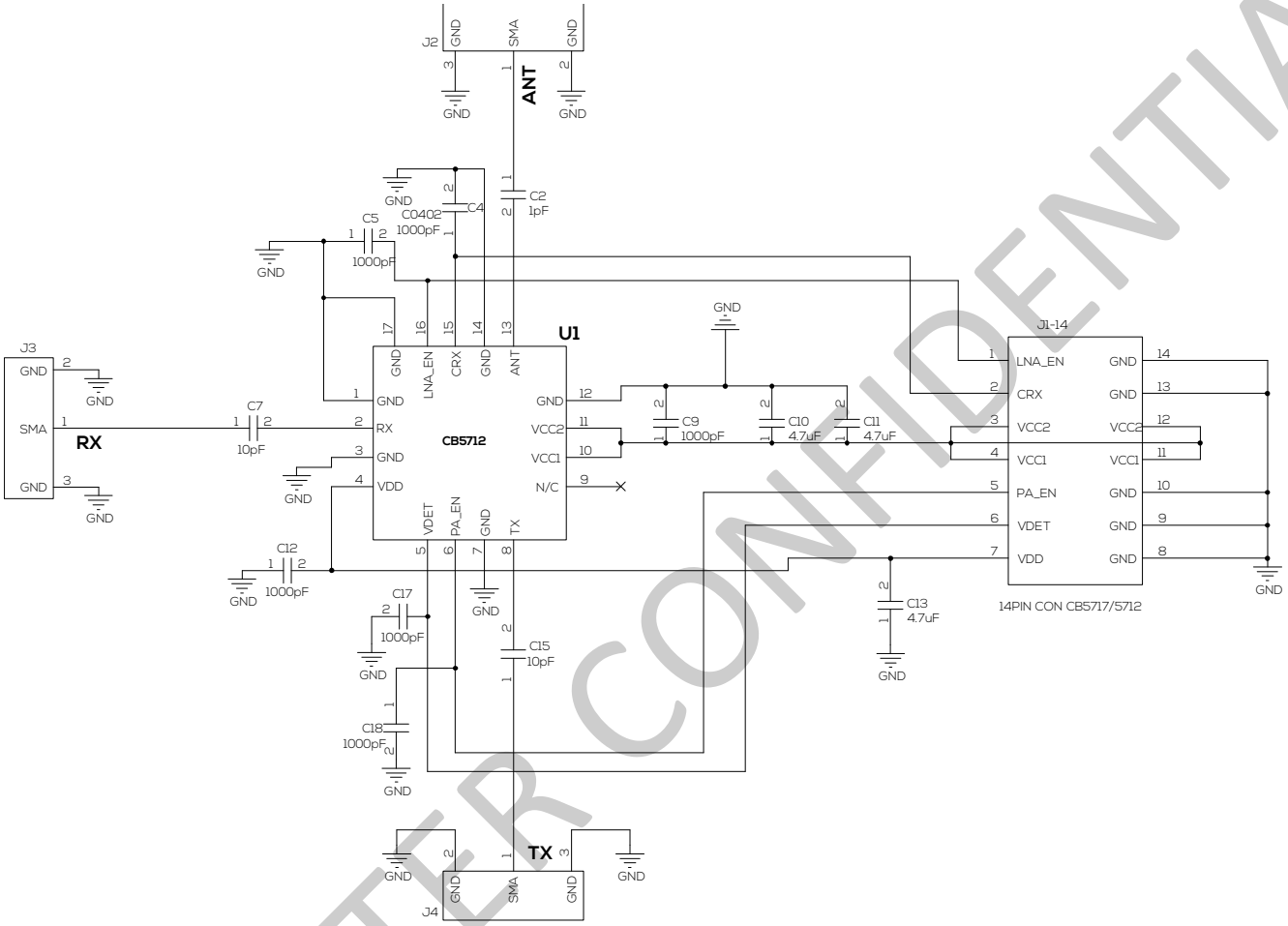


Figure 3. CB5712 Application Schematic

Table 6. CB5712 Evaluation Board Bill of Materials

Component	Value	Size	Vendor	Mfr Part Number
C2	1pF	0402	Murata	GRM1555C1H1R0BA01#
C7, C15	10pF	0402	Murata	GRM1555C1H100FA01#
C4, C5, C9, C12, C17, C18	1000pF	0402	Murata	GRM1555C1H102GA01#
C10, C11, C13	4.7uF	0805	Murata	GRM21BC71H475KE11#

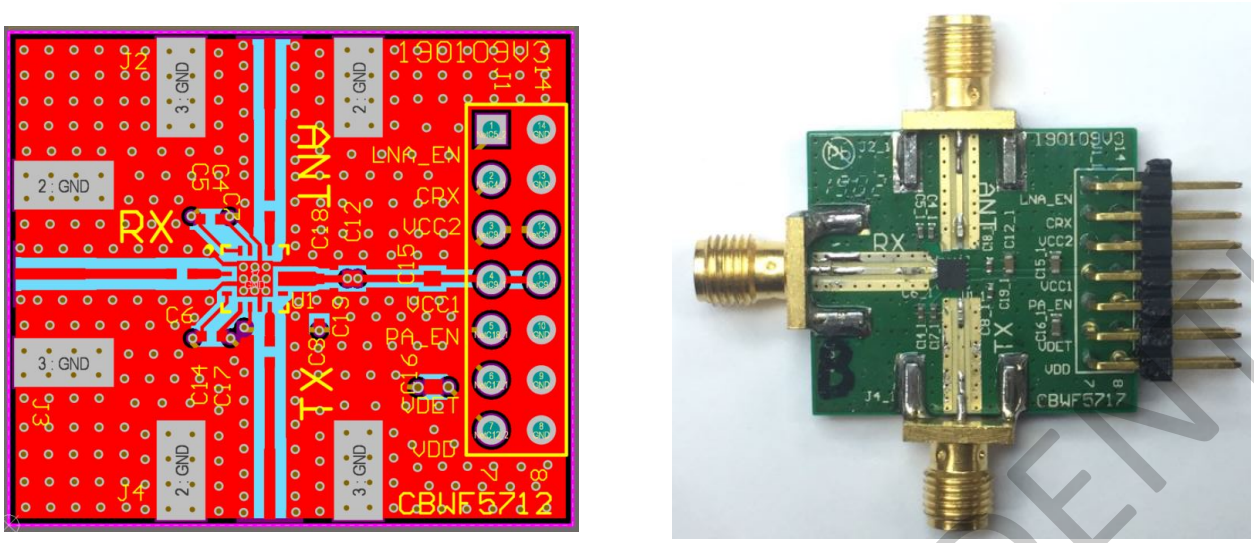


Figure 4. CB5712 Evaluation Board

Evaluation Board Setup Procedure

1. Connect system ground to GND pins of the J1-14 header.
2. Apply 4.2 V or 5 V to VCC pins of the J1-14 header.
3. Select a path according to the information in Table 5 (“0” = 0 V, “1” = 3.3 V).
4. Connect a DMM to VDET pin of the J1-14 header to monitor the power detector voltage.

Circuit Design Considerations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

Paths to ground should be made as short as possible.

The ground pad of the CB5712 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Because the circuit board acts as the heat sink, it must shunt as much heat as possible from the device.

Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board. Multiple vias to the grounding layer are required.

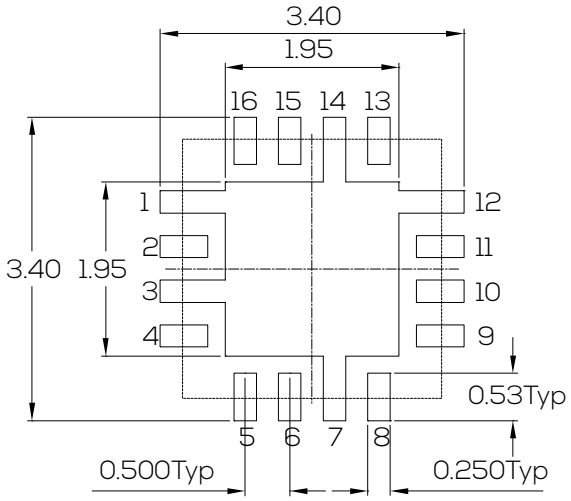
NOTE: A poor connection between the ground pad and ground increases junction temperature (TJ), which reduces the life of the device.

Place component C2, C7 and C15 close to the device.

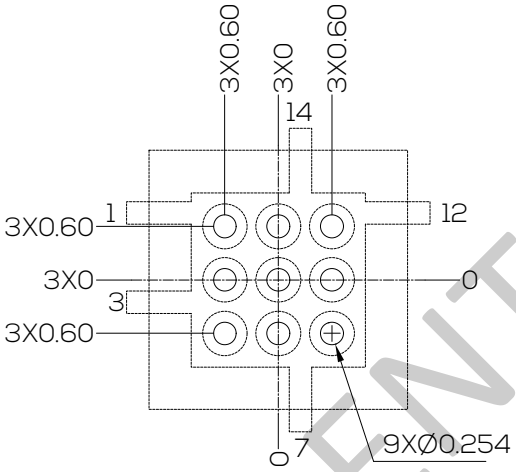
Package Dimensions

The PCB layout footprint for the CB5712 is shown in Figure 5. Typical case markings are shown in Figure 6. Package dimensions for the 16-pin QFN are shown in Figure 7, and tape and reel dimensions are provided in Figure 8.

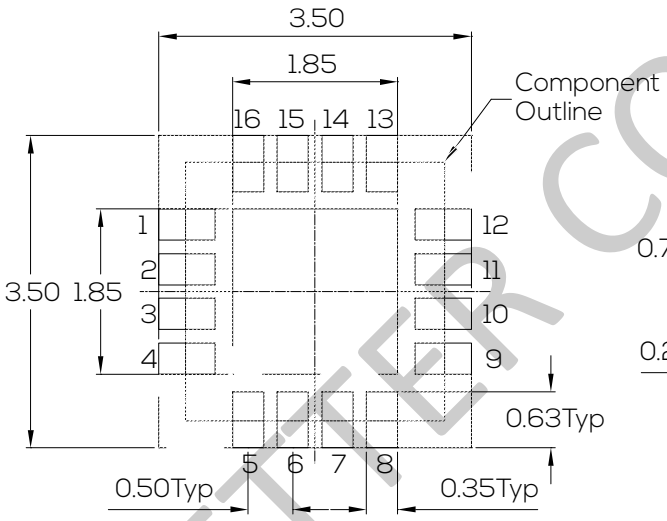
PCB LAND PATTERN



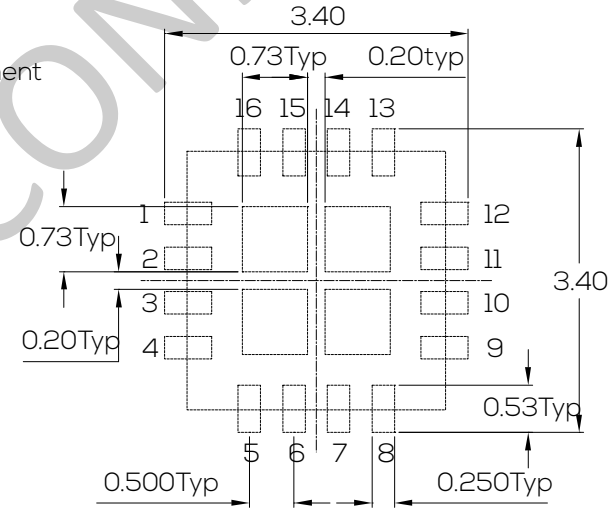
Board Metal



Via Pattern
(Note 1)



Solder Mask Pattern
(Note 2)



Stencil Pattern
(Note 3)

Notes:
1.Via hole recommendations:
0.025mm Cu via wall plating(minimum), soldermask on the far side should tent or plug via holes.
2.Solder mask recommendations:
Contact board fabricator for recommended solder mask offset and tolerance.
3.Stencil recommendations:
0.125mm stencil thickness,laser cut apertures, trapezoidal walls and rounded corners offer better paste release.

Figure 5. CB5712 PCB Layout Footprint
(Top View)

Typical Case Markings

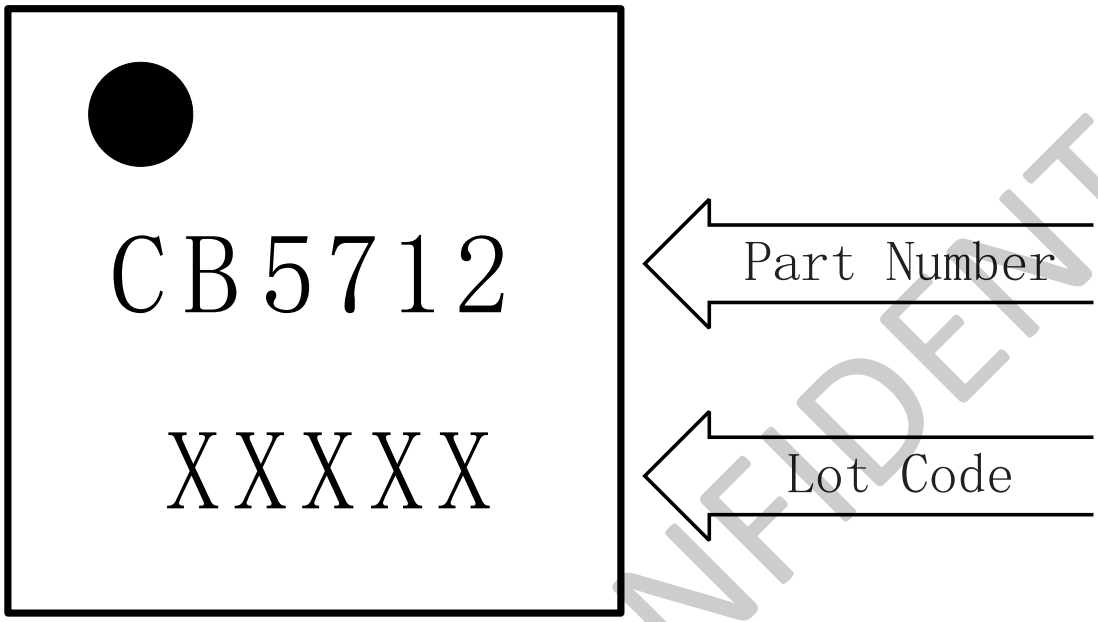
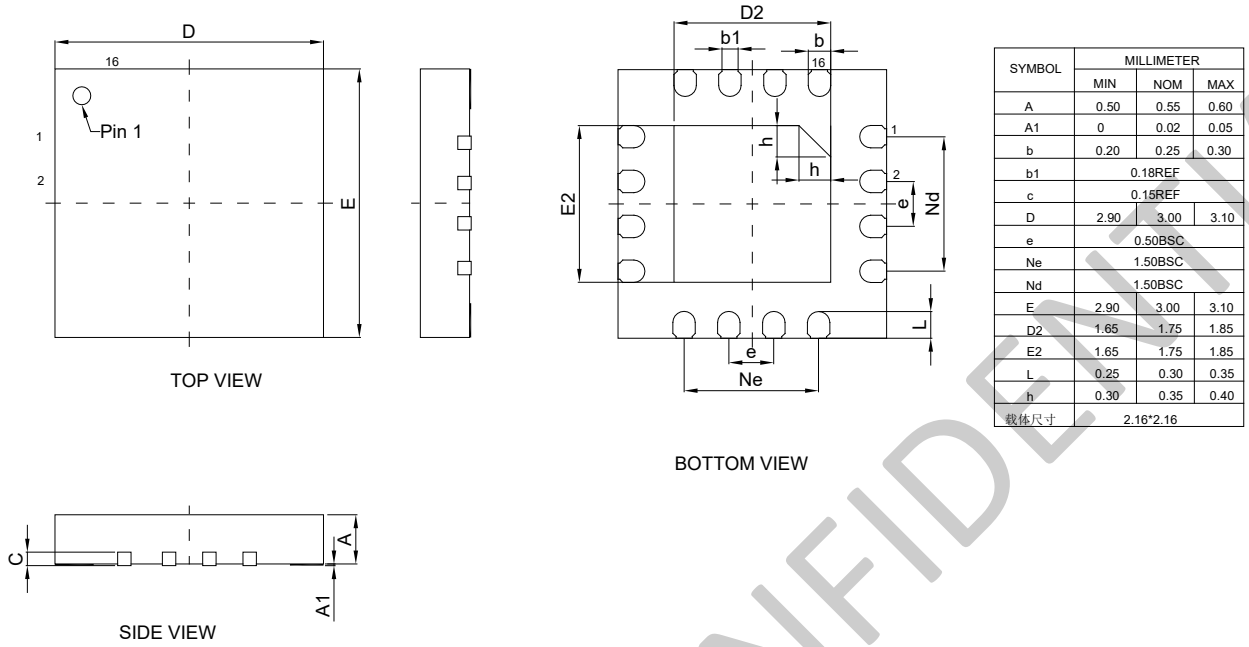


Figure 6. Typical Case Markings
(Top View)

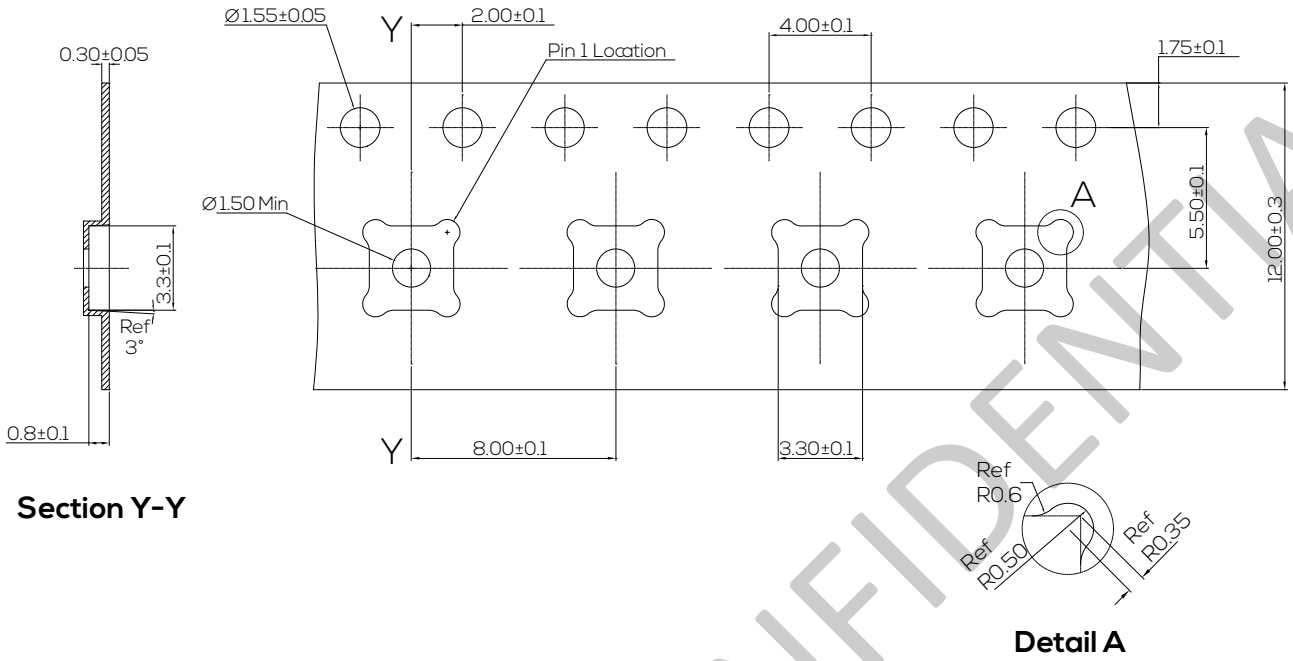
PACKAGE DIMENSIONS (All Dimensions in mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.18REF	
c		0.15REF	
D	2.90	3.00	3.10
e		0.50BSC	
Ne		1.50BSC	
Nd		1.50BSC	
E	2.90	3.00	3.10
D2	1.65	1.75	1.85
E2	1.65	1.75	1.85
L	0.25	0.30	0.35
h	0.30	0.35	0.40
载体尺寸		2.16*2.16	

Figure 7. CB5712 16-Pin QFN Package Dimensions

Tape and Reel Dimensions



Notes:
1. Measured from center line of sprocket hole to center line of pocket.
2. Cumulative toelrance of 10 sprocket holes is ±0.20mm.
3. Other material available.
4. Typical ESD surface resistivity is from 10^5 to 10^{11} Ohms/square per EIA,JEDEC tape and reel specification

All measurements are in millimeters.

Figure 8. CB5712 Tape and Reel Dimensions

Revision History

Doc No.	Revision	Date	Description
CBDS2019001EN	A0	Jan 28, 2019	Initial Release
CBDS2019003EN	A1	Feb 28, 2019	Added Application Schematic
CBDS2019015EN	A2	Aug 8, 2020	Modify electrical parameters
CBDS2020018EN	A3	May 12, 2020	Modify layout
CBDS2020018EN	A3.5	Dec 11, 2020	Updated POD