DCP01 系列 1W、1000V_{RMS} 隔离式非稳压直流/直流转换器模块

1 特性

- 1kV 隔离（工作）：1 秒测试
- 在隔离层中施加连续电压：60VDC/42.5VAC
- UL1950 认证组件
- EN55022 B 类 EMC 性能
- 7 引脚 PDIP 和 7 引脚 SOP 封装
- 输入电压：5V、15V 或 24V
- 输出电压：±5V、±6.5V、±12V 或 ±15V
- 器件间同步
- 过热保护
- 短路保护
- 高效率

2 应用

- 信号路径隔离
- 消除接地环路
- 数据采集
- 工业控制和仪表
- 测试设备

3 说明

DCP01B 系列是 1W 隔离式非稳压直流/直流转换器模块。DCP01B 系列器件具有片上器件保护，只需要很少的外部元件即可提供额外的功能，例如输出禁用和开关频率同步。

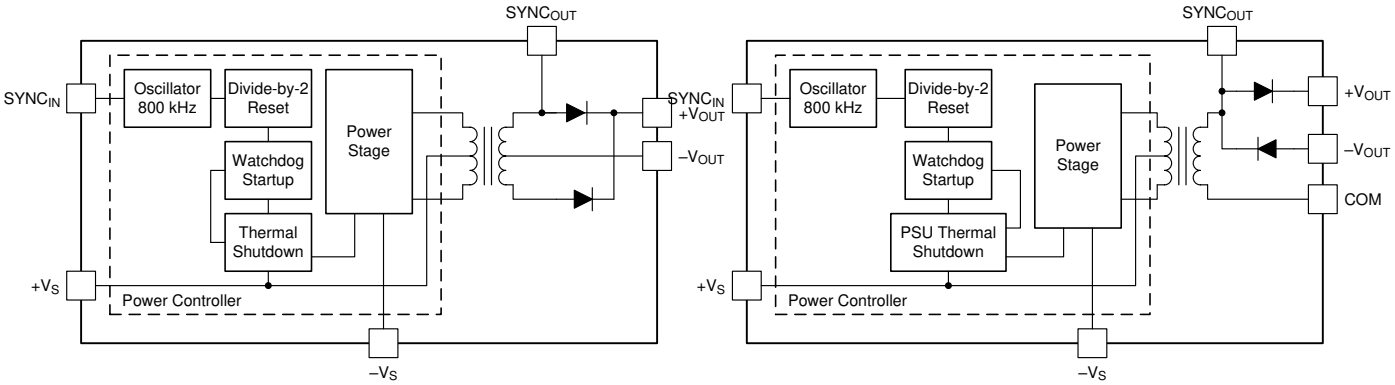
DCP01B 系列器件集这些特性和较小的尺寸于一体，非常适合用于各种应用，并且对需要信号路径隔离的应用来说，它是一个易于使用的解决方案。

警告：此产品具有运行隔离功能，仅可用于信号隔离。不可作为需要增强型隔离的安全隔离电路的一部分使用。请参阅*特性说明*中的定义。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
DCP01xxxxB	PDIP (7)	19.18mm × 10.60mm
	SOP (7)	

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。



单路输出方框图　　双路输出方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (May 2019) to Revision I (April 2020)	Page
• 更新了整个文档的表、图和交叉参考的编号格式。	1
• 添加了链接至 *节 2*	1

Changes from Revision G (February 2017) to Revision H (May 2019)	Page
• Added *节 7.3.6*	14
• Added *节 7.3.7*	14
• Added *节 7.3.10*	15

Changes from Revision F (October 2015) to Revision G (February 2017)	Page
• Adjusted Operating temperature specification to "ambient temperature range, T_A" in *节 6.3*	5

Changes from Revision E (December 2000) to Revision F (Octobert 2015)	Page
• 添加了 图 3-1	1
• Renamed pin "**0V**" to "**COM**" (output side common pin) in *节 Pin Functions*	4
• Renamed pin "$\mathbf{V_S}$ " to "$\mathbf{+V_S}$ " (input voltage pin) in *节 Pin Functions*	4
• Renamed pin "**0V**" to " – $\mathbf{V_S}$ " (input side common pin) in *节 Pin Functions*	4
• Added *节 6.3*	5
• Added *节 6.4*	5
• Added information to the ISOLATION section of *节 6.5*	6
• Added *节 7.3.1* to *节 7.3*	13
• Added a typical application design to *节 8.1*	18
• Added *节 9*	23

Device Comparison Table

at T_A = 25°C, +V_S = nominal, C_{IN} = 2.2 µF, C_{OUT} = 0.1 µF, (unless otherwise noted)

DEVICE NUMBER	INPUT VOLTAGE V_S (V)			OUTPUT VOLTAGE V_{NOM} AT V_S (TYP) (V) 75% LOAD			DEVICE OUTPUT CURRENT (mA) (3)	LOAD REGULATION 10% TO 100% LOAD (1)		NO LOAD CURRENT I_Q (mA) 0% LOAD	EFFICIENCY (%) 100% LOAD	BARRIER CAPACITANCE C_{ISO} (pF) V_{ISO} = 750Vrms
	MIN	TYP	MAX	MIN	TYP	MAX	MAX	TYP	MAX	TYP	TYP	TYP
DCP010505BP DCP010505BP-U	4.5	5	5.5	4.75	5	5.25	200	19	31	20	80	3.6
DCP010505DBP DCP010505DBP-U				±4.25	±5	±5.75	200(2)	18	32	22	81	3.8
DCP010507DBP DCP010507DBP-U				±5.75	±6.5	±7.25	153(2)	21	35	38	81	3.0
DCP010512BP DCP010512BP-U				11.4	12	12.6	83	21	38	29	85	5.1
DCP010512DBP DCP010512DBP-U				±11.4	±12	±12.6	83(2)	19	37	40	82	4.0
DCP010515BP DCP010515BP-U				14.25	15	15.75	66	26	42	34	82	3.8
DCP010515DBP DCP010515DBP-U				±14.25	±15	±15.75	66(2)	19	41	42	85	4.7
DCP011512DBP DCP011512DBP-U	13.5	15	16.5	±11.4	±12	±12.6	83	11	39	19	78	2.5
DCP011515DBP DCP011515DBP-U				±14.25	±15	±15.75	66(2)	12	39	20	80	2.5
DCP012405BP DCP012405BP-U	21.6	24	26.4	4.75	5	5.25	200	13	23	14	77	2.5
DCP012415DBP DCP012415DBP-U				±14.25	±15	±15.75	66(2)	10	35	17	76	3.8

(1) Load regulation = (V_{OUT} at 10% load – V_{OUT} at 100%)/V_{OUT} at 75% load

(2) I_{OUT1} + I_{OUT2}

(3) $P_{OUT(max)}$ = 1 W

5 Pin Configuration and Functions

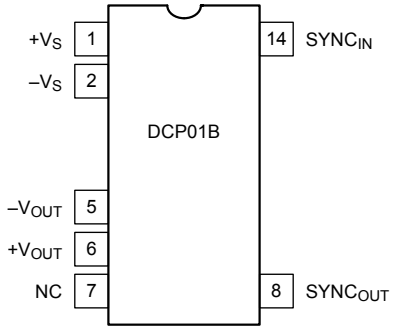


图 5-1. 7-Pin PDIP and SOP (Single Output) NVA and DUA Package (Top View)

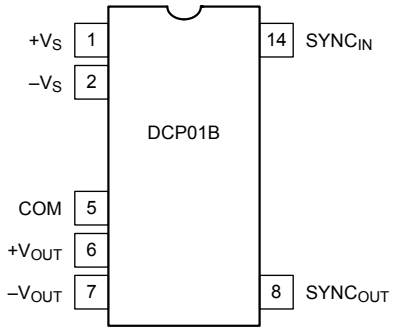


图 5-2. 7-Pin PDIP and SOP (Dual Output) NVA and DUA Package (Top View)

Pin Functions

PIN NAME	PIN NUMBER		I/O (1)	DESCRIPTION
	SINGLE-OUTPUT	DUAL-OUTPUT		
COM	—	5	O	Output side common
NC	7	—	—	No connection
$SYNC_{IN}$	14	14	I	Synchronization. Synchronize multiple devices by connecting the SYNC pins of each. Pulling this pin low disables the internal oscillator.
$SYNC_{OUT}$	8	8	O	Synchronization output. Unrectified transformer output
$+V_{OUT}$	6	6	O	Positive output voltage
$+V_S$	1	1	I	Input voltage
$-V_{OUT}$	5	7	O	Negative output voltage
$-V_S$	2	2	I	Input side common

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	5-V input devices		7	V
	15-V input devices		18	
	24-V input devices		29	
Lead temperature (soldering, 10 s)			270	°C
Storage temperature, T_{stg}		–60	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	5-V input devices	4.5	5	5.5	V
	15-V input devices	13.5	15	16.5	
	24-V input devices	21.6	24	26.4	
Operating ambient temperature range, T_A		–40		100	°C

6.4 Thermal Information

THERMAL METRIC (1)		DCP01B NVA (PDIP) 7 PINS	DCP01B DUA (SOP) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61	61	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24	24	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7	7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24	24	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_A = 25°C, $+V_S$ = nominal, C_{IN} = 2.2 µF, C_{OUT} = 0.1 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
P_{OUT}	Output power	I_{LOAD} = 100% (full load)				1	W
V_{RIPPLE}	Output voltage ripple	C_{OUT} = 1 µF, I_{LOAD} = 50%			20		mV_{PP}
	Voltage vs. Temperature	–40°C ≤ T_A ≤ 25°C			0.046		%/°C
		25°C ≤ T_A ≤ 100°C			0.016		%/°C
INPUT							
V_S	Input voltage range			–10%		10%	
ISOLATION							
V_{ISO}	Isolation	1-second flash test	Voltage	1			kVrms
			dV/dt			500	V/s
			Leakage current			30	µA
		Continuous working voltage across isolation barrier	DC			60	VDC
			AC			42.5	VAC
LINE REGULATION							
V_{OUT}	Output voltage	I_{OUT} ≥ 10% load current and constant, V_S (min) to V_S (typ)			1%	15%	
		I_{OUT} ≥ 10% load current and constant, V_S (typ) to V_S (max)			1%	15%	
RELIABILITY							
	Demonstrated	T_A = 55°C			55		FITS
THERMAL SHUTDOWN							
T_{SD}	Die temperature at shutdown				150		°C
I_{SD}	Shutdown current				3		mA

6.6 Switching Characteristics

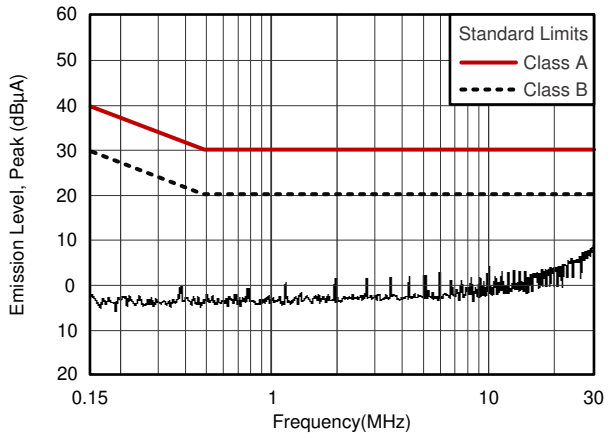
at T_A = +25°C, $+V_S$ = nominal, C_{IN} = 2.2 µF, C_{OUT} = 0.1 µF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC}	Oscillator frequency	f_{SW} = f_{OSC}/2		800		kHz
V_{IL}	Low-level input voltage, SYNC		0		0.4	V
I_{SYNC}	Input current, SYNC	V_{SYNC} = 2 V		75		µA
$t_{DISABLE}$	Disable time			2		µs
C_{SYNC}	Capacitance loading on SYNC pin (1)	External			3	pF

(1) The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* (SBAA035) describes this configuration.

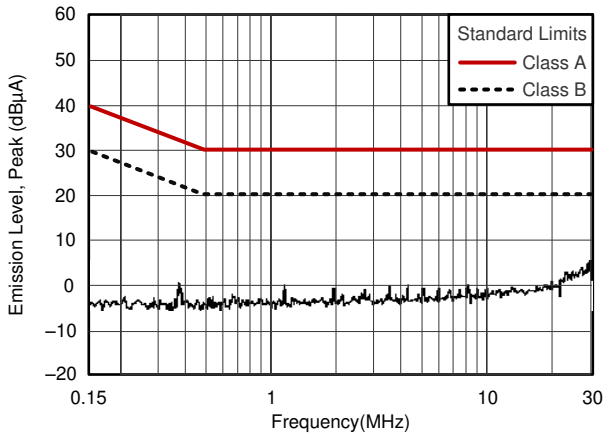
6.7 Typical Characteristics

At T_A = 25°C, V_{+VS} = nominal, (unless otherwise noted)



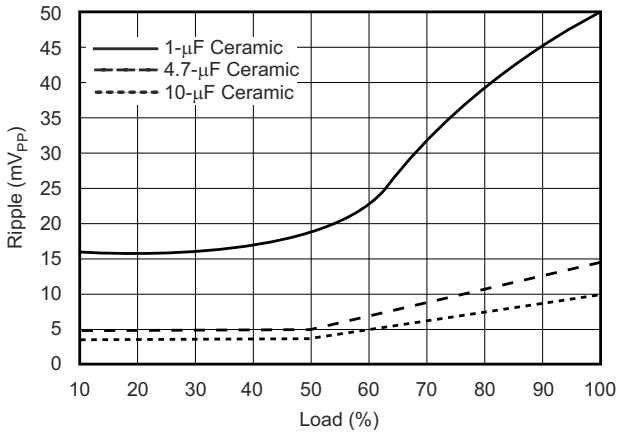
DCP010505B 125% Load

图 6-1. Conducted Emissions



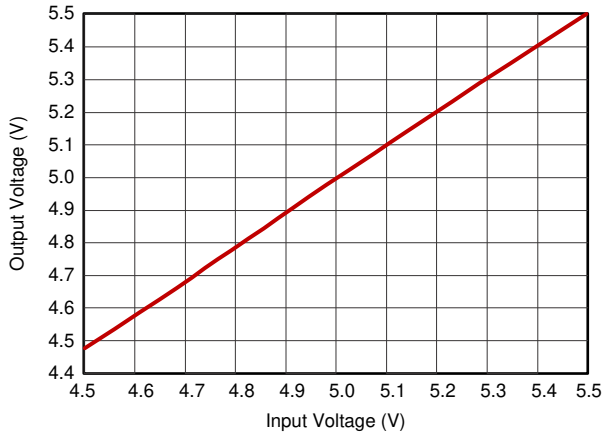
DCP010505B 8% Load

图 6-2. Conducted Emissions



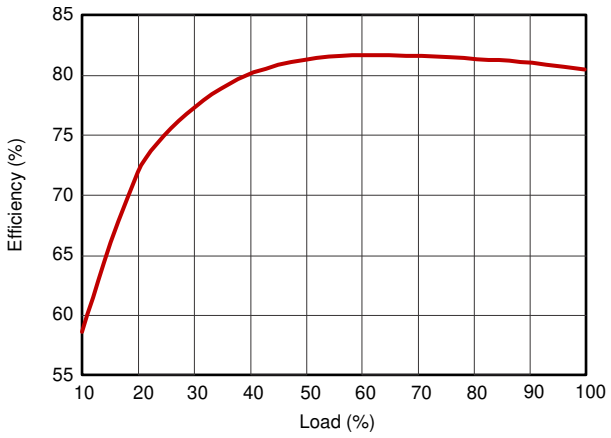
DCP010505B 20-MHz BW

图 6-3. Output Ripple versus Load



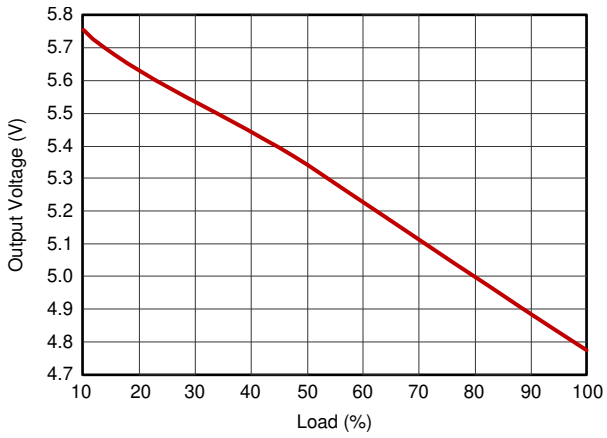
DCP010505B

图 6-4. Line Regulation



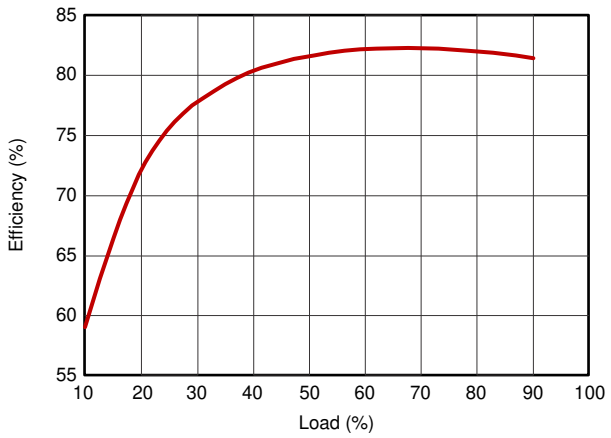
DCP010505B

图 6-5. Efficiency versus Load



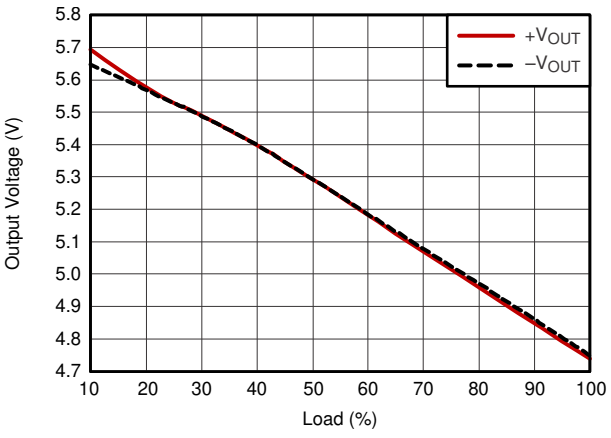
DCP010505B **Note:** Operations under 10% Load

图 6-6. Load Regulation



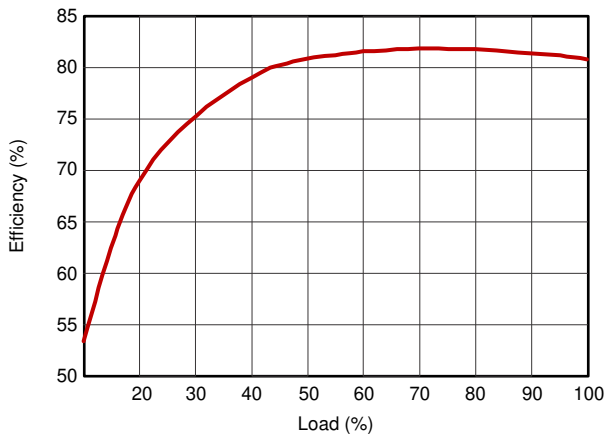
DCP010505DB

图 6-7. Efficiency versus Load



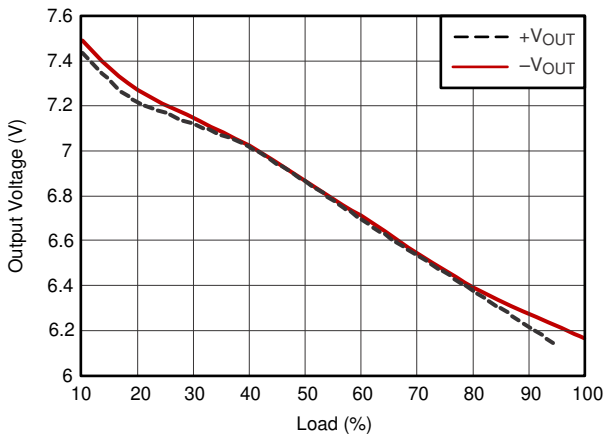
DCP010505DB **Note:** Operations under 10% Load

图 6-8. Load Regulation



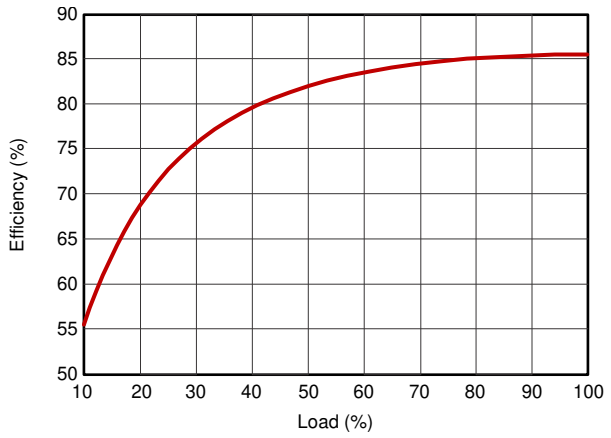
DCP010507DB

图 6-9. Efficiency versus Load



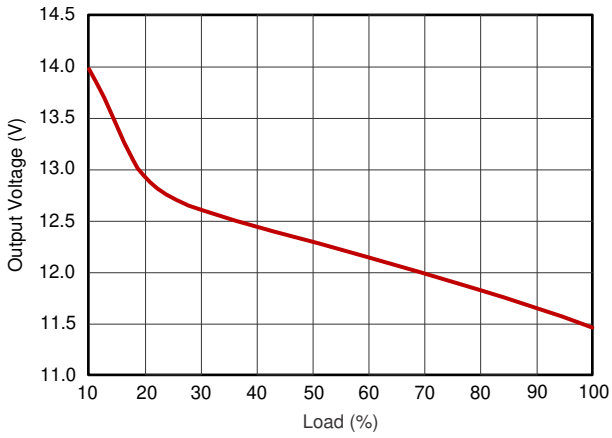
DCP010507DB **Note:** Operations under 10% Load

图 6-10. Load Regulation



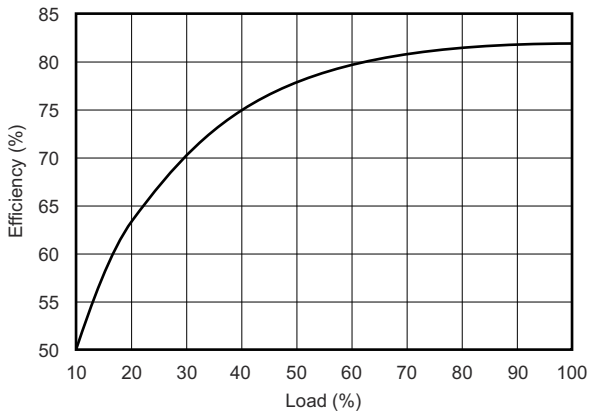
DCP010512B

图 6-11. Efficiency versus Load



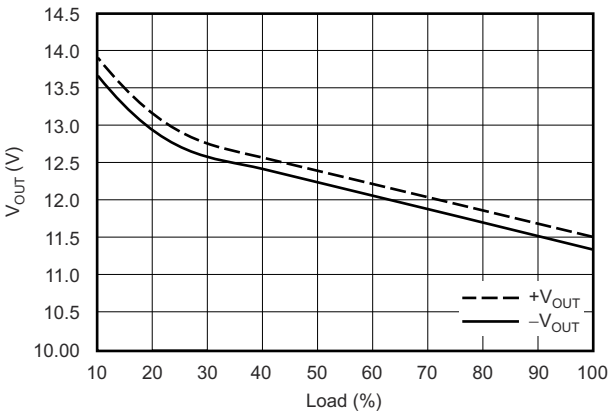
DCP010512B **Note:** Operations under 10% Load

图 6-12. Load Regulation



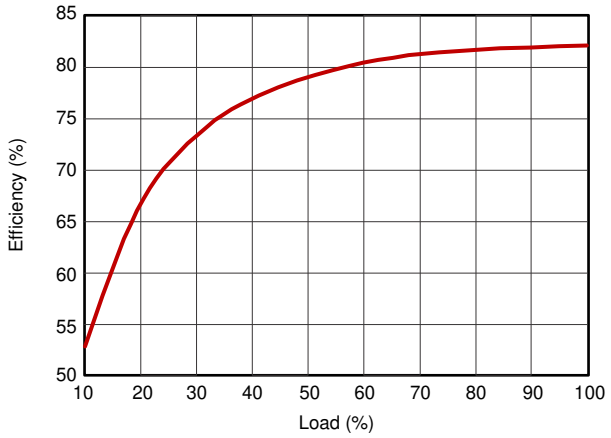
DCP010512DB

图 6-13. Efficiency versus Load



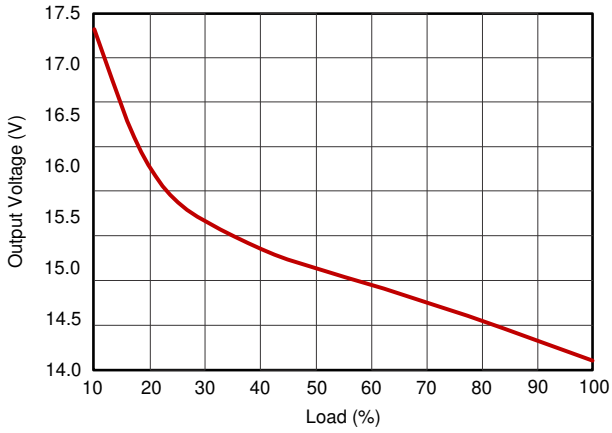
DCP010512DB **Note:** Operations under 10% Load

图 6-14. Load Regulation



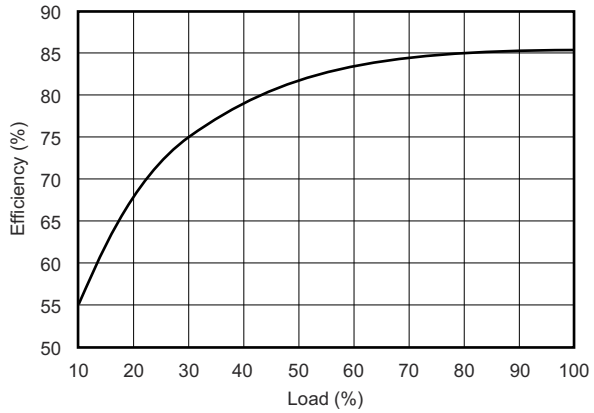
DCP010515B

图 6-15. Efficiency versus Load



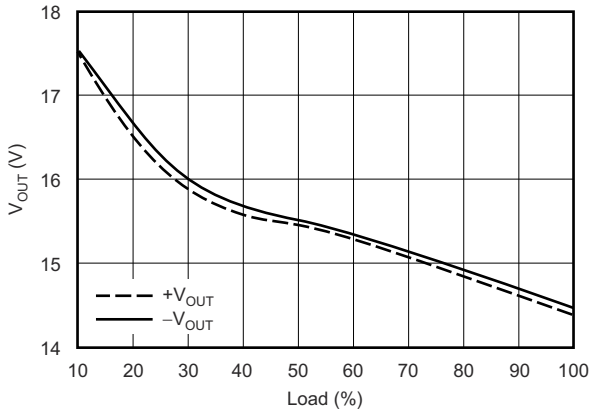
DCP010515B **Note:** Operations under 10% Load

图 6-16. Load Regulation



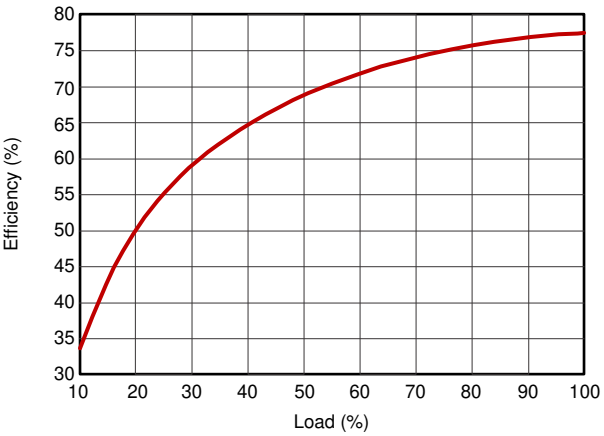
DCP010515DB

图 6-17. Efficiency versus Load



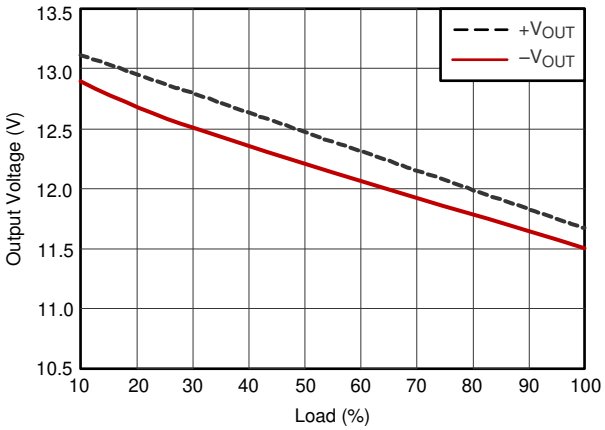
DCP010515DB **Note:** Operations under 10% Load

图 6-18. Load Regulation



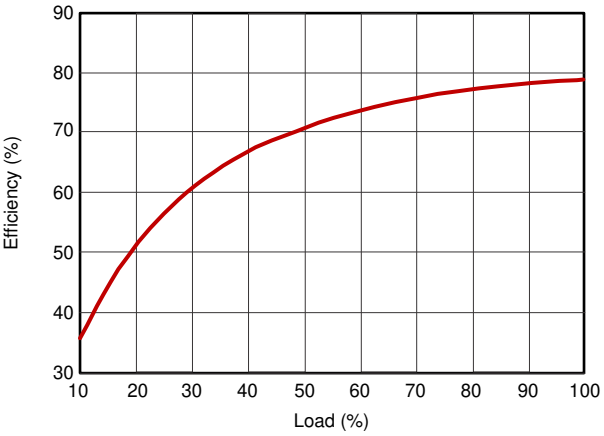
DCP011512DB

图 6-19. Efficiency versus Load



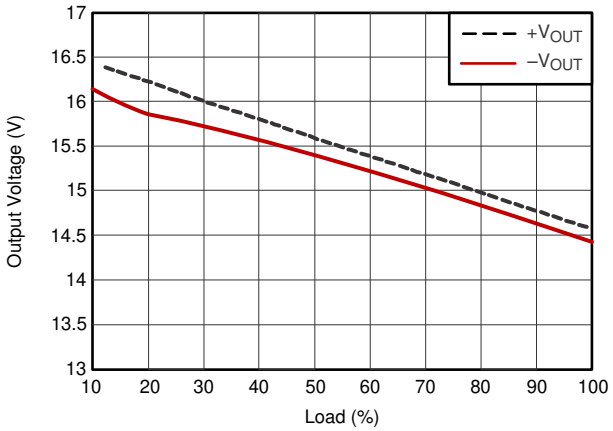
DCP011512DB **Note:** Operations under 10% Load

图 6-20. Load Regulation



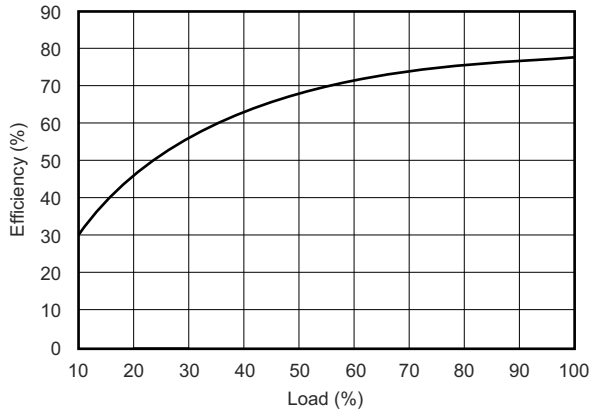
DCP011515DB

图 6-21. Efficiency versus Load



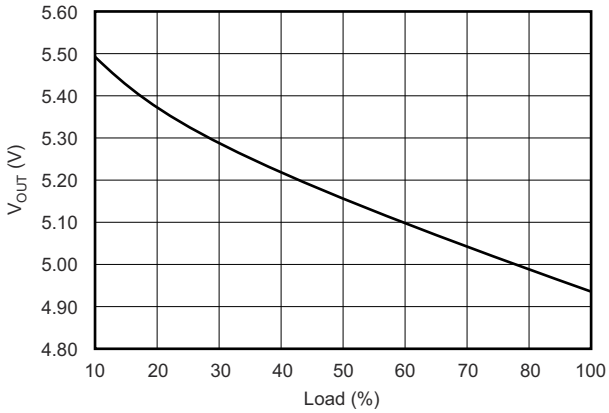
DCP011515DB **Note:** Operations under 10% Load

图 6-22. Load Regulation



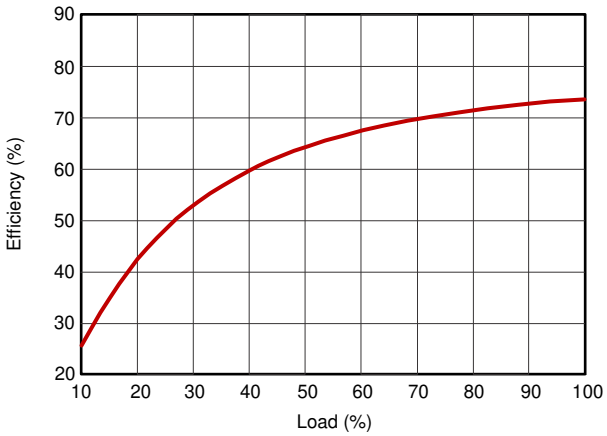
DCP012405B

图 6-23. Efficiency versus Load



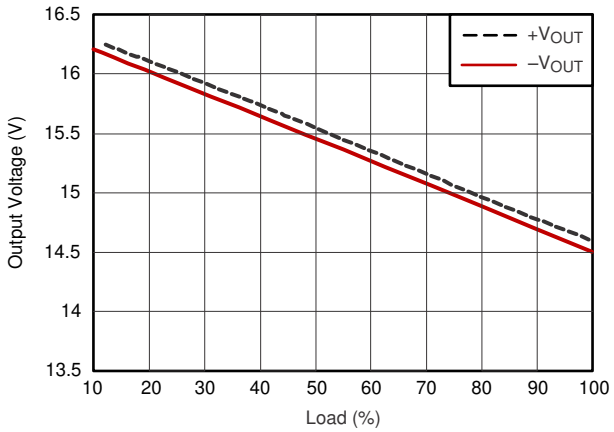
DCP012405B **Note:** Operations under 10% Load

图 6-24. Load Regulation



DCP012415DB

图 6-25. Efficiency versus Load



DCP012415DB **Note:** Operations under 10% Load

图 6-26. Load Regulation

7 Detailed Description

7.1 Overview

The DCP01B offers up to 1 W of isolated, unregulated output power from a 5-V, 15-V, or 24-V input source with a typical efficiency of up to 85%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control device. The DCP01B devices are specified for operational isolation only. The circuit design uses an advanced BiCMOS and DMOS process.

7.2 Functional Block Diagrams

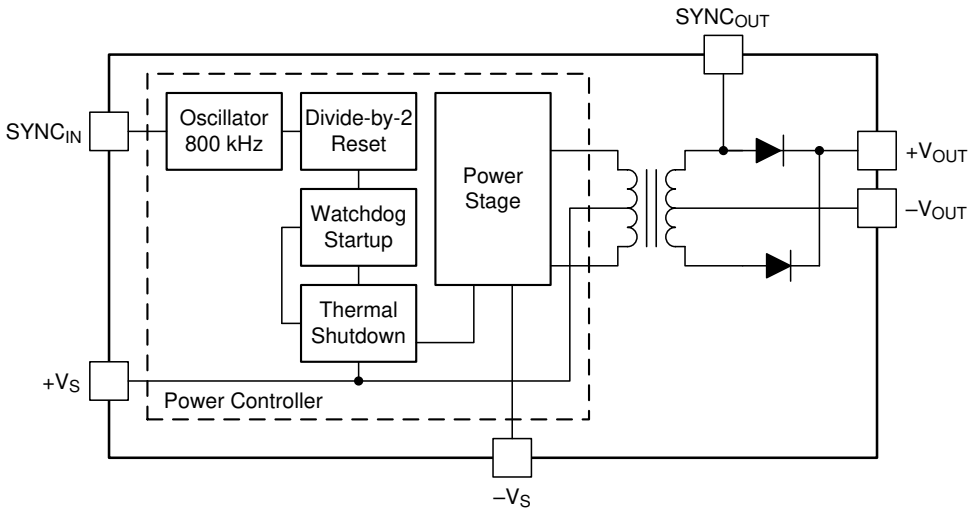


图 7-1. Single Output Device

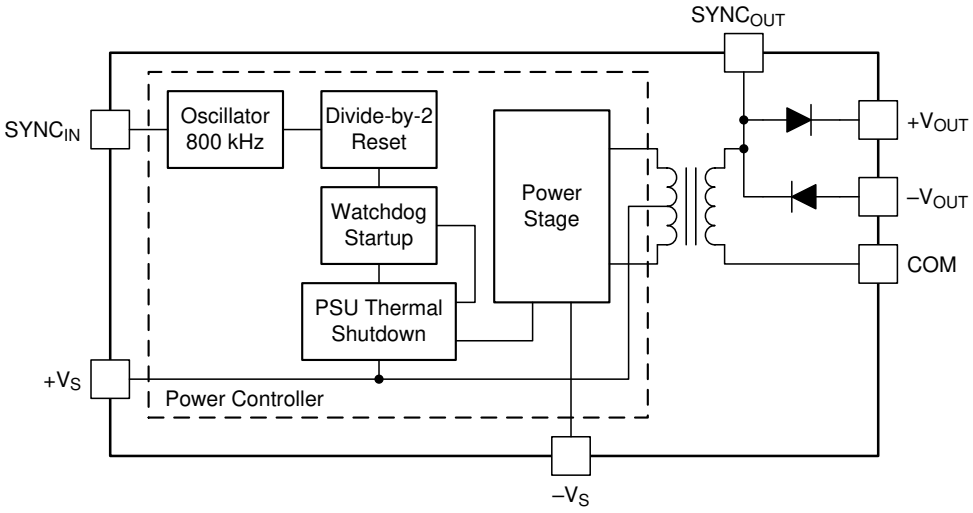


图 7-2. Dual Output Device

7.3 Feature Description

7.3.1 Isolation

Underwriters Laboratories, UL™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42.5 V peak or 60 V_{DC} for more than one second.

7.3.1.1 Operation or Functional Isolation

Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation must never be used as an element in a safety-isolation system.

7.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

7.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.5 V_{RMS}, or 60 V_{DC}. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

WARNING

Do not use the device as an element of a safety isolation system that exceeds the SELV limit.

If the device is expected to function correctly with more than 42.5 V_{RMS} or 60 V_{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage, and further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

7.3.1.4 Isolation Voltage

The terms *Hipot test*, *flash-tested*, *withstand voltage*, *proof voltage*, *dielectric withstand voltage*, and *isolation test voltage* all describe a similar idea. They describe a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI’s DCP01B series of DC/DC converters are all 100% production tested at 1.0 kV_{AC} for one second.

7.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCP01B series of DC/DC converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of one second per test.

7.3.2 Power Stage

The DCP01B series of devices uses a push-pull, center-tapped topology. The DCP01B devices switch at 400 kHz (divide-by-2 from an 800-kHz oscillator).

7.3.3 Oscillator And Watchdog Circuit

The onboard, 800-kHz oscillator generates the switching frequency by a divide-by-2 circuit. The oscillator can be synchronized to other DCP01B series device circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be disabled by pulling the $SYNC_{IN}$ pin low. When the $SYNC_{IN}$ pin goes low, the output pins transition into tri-state mode, which occurs within 2 μs.

7.3.4 Thermal Shutdown

The DCP01B series of devices are protected by a thermal-shutdown circuit.

If the on-chip temperature rises above 150°C, the device shuts down. Normal operation resumes as soon as the temperature falls below 150°C. While the over temperature condition continues, operation randomly cycles on and off. This cycling continues until the temperature is reduced.

7.3.5 Synchronization

When more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCP01B series of devices overcomes this interference by allowing devices to synchronize to one another. Synchronize up to eight devices by connecting the SYNC pins of each device, taking care to minimize the capacitance of tracking. Stray capacitance (greater than 3 pF) reduces the switching frequency, or can sometimes stop the oscillator circuit. The maximum recommended voltage applied to the SYNC pin is 3.0 V.

For an application that uses more than eight synchronized devices, use an external device to drive the SYNC pins. The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* describes this configuration.

Note

During the start-up period, all synchronized devices draw maximum current from the input simultaneously. If the input voltage falls below approximately 4 V, the devices may not start up. A 2.2-μF capacitor should be connected close to each device input pin.

7.3.6 Light Load Operation (< 10%)

Operation below 10% load can cause the output voltage to increase up to double the typical output voltage. For applications that operate less than 10% of rated output current, it is recommended to add a minimum load to ensure the output voltage of the device is within the load regulation range. For example, connect a 250-Ω pre-load resistor to meet the 10% minimum load condition for the DCP010505BP.

7.3.7 Load Regulation (10% to 100%)

The load regulation of the DCP01B series of devices is specified at 10% to 100% load. Placing a minimum 10% load will ensure the output voltage is within the range specified in 节 *6.5*. For more information regarding operation below 10% load, see 节 *7.3.6*.

7.3.8 Construction

The basic construction of the DCP01B series of devices is the same as standard integrated circuits. The molded package contains no substrate. The DCP01B series of devices are constructed using an IC, rectifier diodes, and a wound magnetic toroid on a lead frame. Because the package contains no solder, the devices do not require

any special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

7.3.9 Thermal Management

Due to the high power density of these devices, it is advisable to provide ground planes on the input and output rails.

7.3.10 Power-Up Characteristics

The DCP01B series of devices do not include a soft-start feature. Therefore, a high in-rush current during power up is expected. Refer to the DCPA1 series of devices for a 1-W, isolated, unregulated DC/DC converter module with soft start included. 图 7-3 shows the typical start-up waveform for a DCP010505BP, operating from a 5-V input with no load on the output. 图 7-4 shows the start-up waveform for a DCP010505BP starting up into a 10% load. 图 7-5 shows the start-up waveform starting up into a full (100%) load.

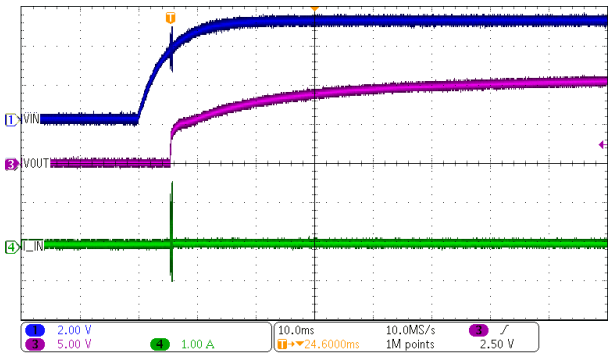


图 7-3. DCP010505BP Start-Up at No Load

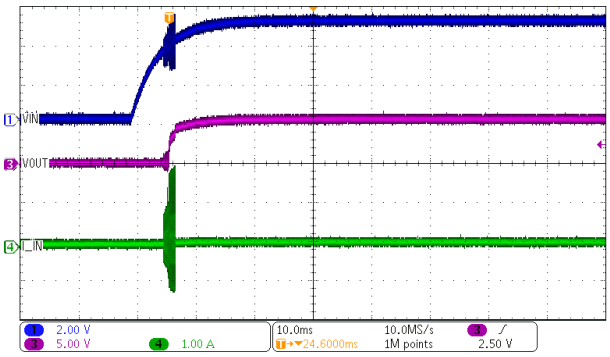


图 7-4. DCP010505BP Start-Up at 10% Load

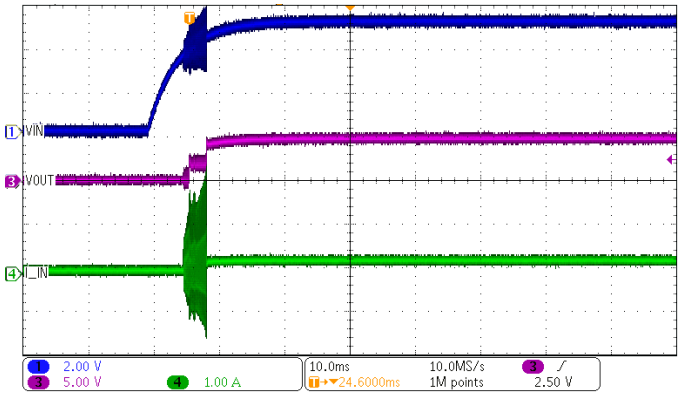


图 7-5. DCP010505BP Start-Up at 100% Load

7.4 Device Functional Modes

7.4.1 Disable and Enable ($SYNC_{IN}$ Pin)

Each of the DCP01B series devices can be disabled or enabled by driving the $SYNC_{IN}$ pin using an open-drain CMOS gate. If the $SYNC_{IN}$ pin is pulled low, the DCP01B becomes disabled. The disable time depends upon the external loading. The internal disable function is implemented within 2 μs. Removal of the pulldown causes the DCP01B to be enabled.

Capacitive loading on the $SYNC_{IN}$ pin must be minimized (≤ 3 pF) to prevent a reduction in the oscillator frequency. The application report *External Synchronization of the DCP01/02 Series of DC/DC Converters* describes disable and enable control circuitry.

7.4.2 Decoupling

7.4.2.1 Ripple Reduction

The high switching frequency of 400 kHz allows simple filtering. To reduce ripple, it is recommended that a minimum of 1-μF capacitor be used on the $+V_{OUT}$ pin. For dual output devices, decouple both of the outputs to the COM pin. The required 2.2-μF, low ESR ceramic input capacitor also helps reduce ripple and noise, (24-V input voltage versions require only 0.47 μF of input capacitance). See application report *DC-to-DC Converter Noise Reduction*.

7.4.2.2 Connecting the DCP01B in Series

Multiple DCP01B isolated 1-W DC/DC converters can be connected in series to provide non-standard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCP01.

Connect the $+V_{OUT}$ from one DCP01B to the $-V_{OUT}$ of another (see 图 7-6). If the $SYNC_{IN}$ pins are tied together, the self-synchronization feature of the DCP01B prevents beat frequencies on the voltage rails. The synchronization feature of the DCP01B allows easy series connection without external filtering, thus minimizing cost.

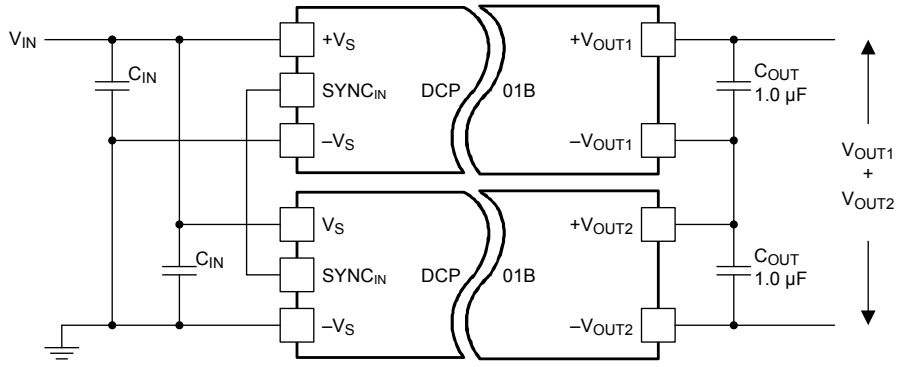


图 7-6. Multiple DCP01B Devices Connected in Series

The outputs of a dual-output DCP01B can also be connected in series to provide two times the magnitude of $+V_{OUT}$, as shown in 图 7-7. For example, connect a dual-output, 15-V, DCP012415DB device to provide a 30-V rail.

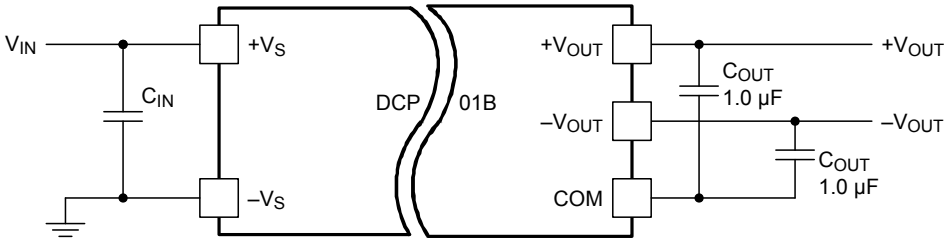


图 7-7. Dual Output Devices Connected in Series

7.4.2.3 Connecting the DCP01B in Parallel

If the output power from one DCP01B is not sufficient, it is possible to parallel the outputs of multiple DCP01Bs, as shown in 图 7-8 (applies to single output devices only). The synchronization feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

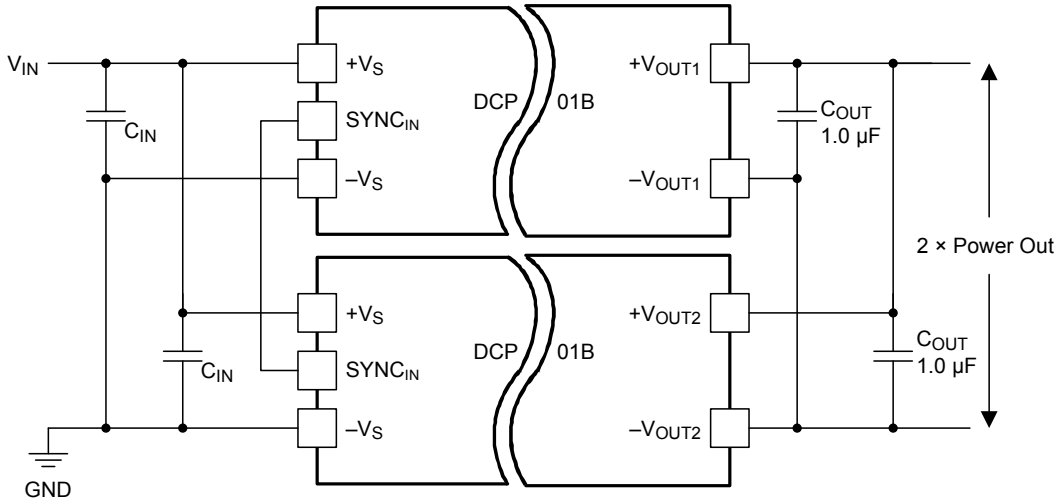


图 7-8. Multiple DCP01B Devices Connected in Parallel

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

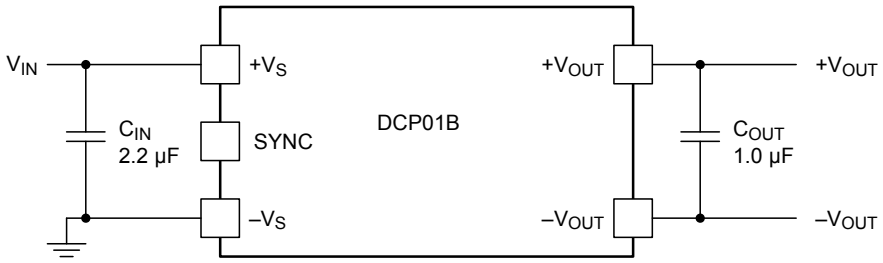


图 8-1. Typical DCP010505 Application

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 and follow the design procedures shown in the *节 8.2.2*.

表 8-1. Design Example Parameters

PARAMETER		VALUE	UNIT
$V_{(+VS)}$	Input voltage	5	V
$V_{(+VOUT)}$	Output voltage	5	V
I_{OUT}	Output current rating	200	mA
f_{SW}	Operating frequency	400	kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

For all 5-V and 15-V input voltage designs, select a 2.2-µF low-ESR ceramic input capacitor to ensure a good startup performance. 24-V input applications require only 0.47-µF of input capacitance.

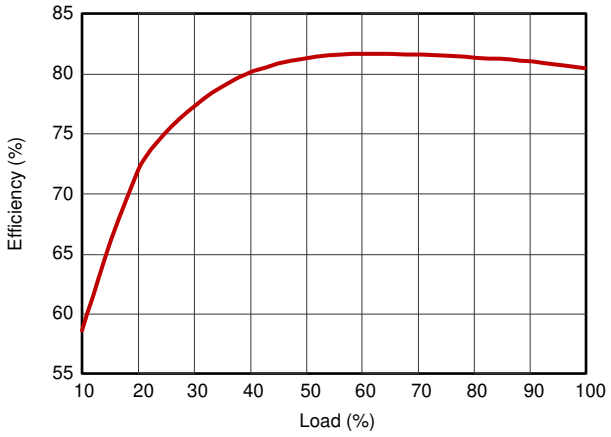
8.2.2.2 Output Capacitor

For any DCP01B design, select a 1.0-µF low-ESR ceramic output capacitor to reduce output ripple.

8.2.2.3 $SYNC_{IN}$ Pin

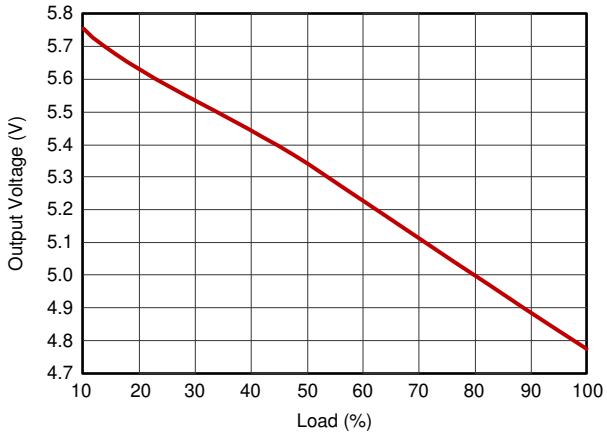
In a stand-alone application, leave the $SYNC_{IN}$ pin floating.

8.2.3 DCP010505 Application Curves



DCP010505B

图 8-2. Efficiency versus Load



DCP010505B **Note:** Operations under 10% Load

图 8-3. Load Regulation

8.2.4 PCB Design

The copper losses (resistance and inductance) can be minimized by the use of mutual ground and power planes (tracks) where possible. If that is not possible, use wide tracks to reduce the losses. If several devices are being powered from a common power source, a star-connected system for the track must be deployed. Do not connect the devices in series, because that type of connection cascades the resistive losses. The position of the decoupling capacitors is important. They must be as close to the devices as possible in order to reduce losses. See *节 10* for more details.

8.2.5 Decoupling Ceramic Capacitors

All capacitors have losses because of internal equivalent series resistance (ESR), and to a lesser degree, equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of frequency versus capacitor impedance. These graphs typically show the capacitor impedance falling as frequency is increased (as shown in 图 8-4). In 图 8-4, X_C is the reactance due to the capacitance, X_L is the reactance due to the ESL, and f_0 is the resonant frequency. As the frequency increases, the impedance stops decreasing and begins to rise. The point of minimum impedance indicates the resonant frequency of the capacitor. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.

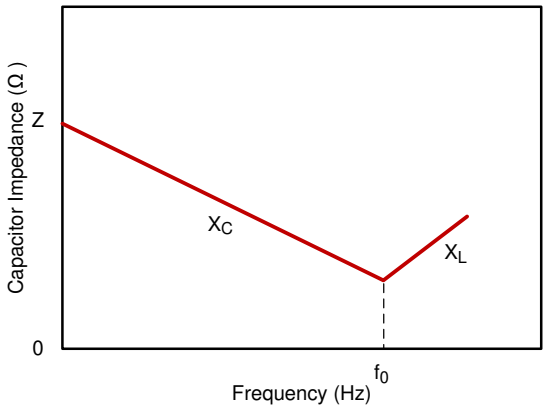


图 8-4. Capacitor Impedance versus Frequency

However, there is a 180° phase difference resulting in cancellation of the imaginary component. The resulting effect is that the impedance at the resonant point is the real part of the complex impedance, namely, the value of the ESR. The output capacitor's resonant frequency must be higher than the default switching frequency (800 kHz) of the device to properly decouple noise at and below the switching frequency.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current, as shown in 方程式 1.

$$V_{IN} = V_{PK} - (ESR \times I_{TR}) \quad (1)$$

where

- V_{IN} is the voltage at the device input
- V_{PK} is the maximum value of the voltage on the capacitor during charge
- I_{TR} is the transient load current

The other factor that affects the performance is the value of the capacitance. However, for the input and the full wave outputs (single-output voltage devices), ESR is the dominant factor.

8.2.6 Input Capacitor and the Effects of ESR

If the input decoupling capacitor is not ceramic (and has an ESR greater than 20 mΩ), then at the instant the power transistors switch on, the voltage at the input pins falls momentarily. If the voltage falls below approximately 4 V, the device detects an undervoltage condition and switches the internal drive circuits to a momentary off state. This detection is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. A slow-down or stoppage results in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value, at which time the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process repeats until the input capacitor charges sufficiently to start the device correctly.

Normal start-up should occur in approximately 1 ms after power is applied to the device. If a considerably longer start-up duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5-V to 15-V input devices, a 2.2-μF, low-ESR ceramic capacitor ensures good startup performance. For 24-V input voltage devices, 0.47-μF ceramic capacitors are recommended. Tantalum capacitors are not recommended, since most do not have low-ESR values and will degrade performance. If tantalum capacitors must be used, close attention must be paid to both the ESR and voltage as derated by the vendor.

Note

During the start-up period, these devices may draw maximum current from the input supply. If the input voltage falls below approximately 4 V, the devices may not start up. Connect a 2.2-μF ceramic capacitor close to the input pins.

8.2.7 Ripple and Noise

A good quality, low-ESR ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensures a smooth start-up.

A good quality, low-ESR ceramic capacitor placed as close as practical across the rectifier output terminal and output ground gives the best ripple and noise performance. See application report *DC-to-DC Converter Noise Reduction* for more information on noise rejection.

8.2.7.1 Output Ripple Calculation Example

The following example shows that increasing the capacitance has a much smaller effect on the output ripple voltage than does reducing the value of the ESR for the filter capacitor.

To calculate the output ripple for a DCP010505 device:

- V_{OUT} = 5 V

- I_{OUT} = 0.2 A
- At full output power, the load resistor is 25 Ω
- Ceramic output capacitor of 1 μF, ESR of 0.1 Ω
- Capacitor discharge time 1% of 800 kHz (ripple frequency)

t_{DIS} = 0.0125 μs

$\tau = C \times R_{LOAD}$

$\tau = 1 \times 10^{-6} \times 12.5 = 12.5$ μs

$V_{DIS} = V_O(1 - EXP(-t_{DIS} / \tau))$

V_{DIS} = 5 mV

By contrast, the voltage dropped because of ESR:

$V_{ESR} = I_{LOAD} \times ESR$

V_{ESR} = 20 mV

Ripple voltage = 25 mV

8.2.8 Dual DCP01B Output Voltage

The voltage output for dual DCP01B devices is half wave rectified; therefore, the discharge time is 1.25 μs. Repeating the above calculations using the 100% load resistance of 50 Ω (0.1 A per output), the results are:

τ = 25 μs

t_{DIS} = 1.25 μs

V_{DIS} = 244 mV

V_{ESR} = 10 mV

Ripple Voltage = 133 mV

This time, it is the capacitor discharging that contributes to the largest component of ripple. Changing the output filter to 10 μF, and repeating the calculations, the result is:

Ripple voltage = 25 mV

This value is composed of almost equal components.

The previous calculations are offered as a guideline only. Capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

8.2.9 Optimizing Performance

Optimum performance can only be achieved if the device is correctly supported. The very nature of a switching converter requires power to be instantly available when it switches on. If the converter has DMOS switching transistors, the fast edges will create a high current demand on the input supply. This transient load placed on the input is supplied by the external input decoupling capacitor, thus maintaining the input voltage. Therefore, the input supply does not see this transient (this is an analogy to high-speed digital circuits). The positioning of the capacitor is critical and must be placed as close as possible to the input pins and connected via a low-impedance path.

The optimum performance primarily depends on two factors:

- Connection of the input and output circuits for minimal loss.
- The ability of the decoupling capacitors to maintain the input and output voltages at a constant level.

9 Power Supply Recommendations

The DCP01B is a switching power supply, and as such can place high peak current demands on the input supply. To avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCP01 device. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

10 Layout

10.1 Layout Guidelines

Due to the high power density of these devices, provide ground planes on the input and output rails.

图 10-1 and 图 10-2 show the schematic for the two DIP through-hole packages, and two SOP surface-mount packages for the DCP family of products which include DCP01B, DCP02, DCV01, DCR01, and DCR02. 图 10-3 and 图 10-4 illustrate a printed circuit board (PCB) layout for the schematics.

Including input power and ground planes provides a low-impedance path for the input power. For the output, the COM signal connects via a ground plane, while the connections for the positive and negative voltage outputs conduct via wide traces in order to minimize losses.

The output should be taken from the device using ground and power planes, thereby ensuring minimum losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

Allow the unused SYNC pin, to remain configured as a floating pad. It is advisable to place a guard ring (connected to input ground) or annulus connected around this pin to avoid any noise pick up. When connecting a SYNC pin to one or more SYNC design the linking trace to be short and narrow to avoid stray capacitance. Ensure that no other trace is in close proximity to this trace SYNC trace to decrease the stray capacitance on this pin. The stray capacitance affects the performance of the oscillator.

10.2 Layout Example

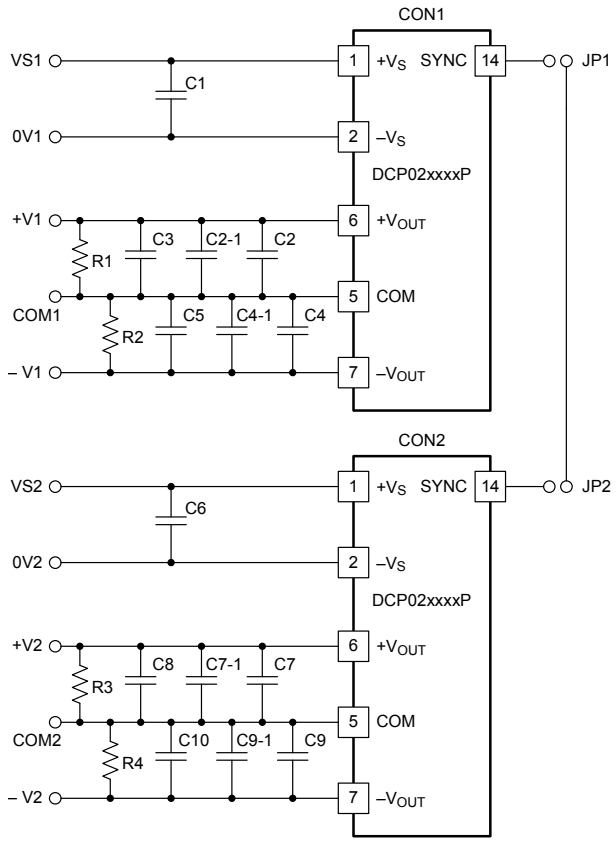


图 10-1. PCB Schematic, P Package

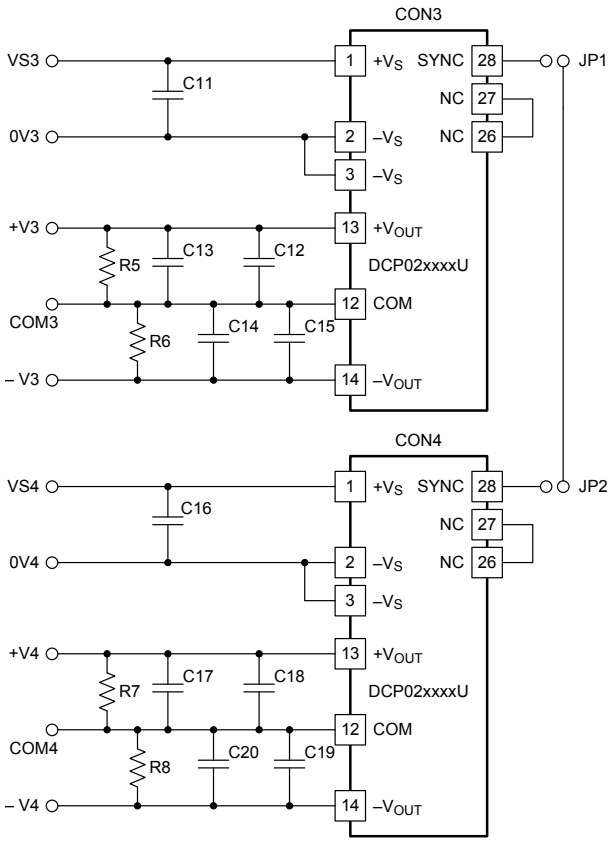


图 10-2. PCB Schematic, U Package

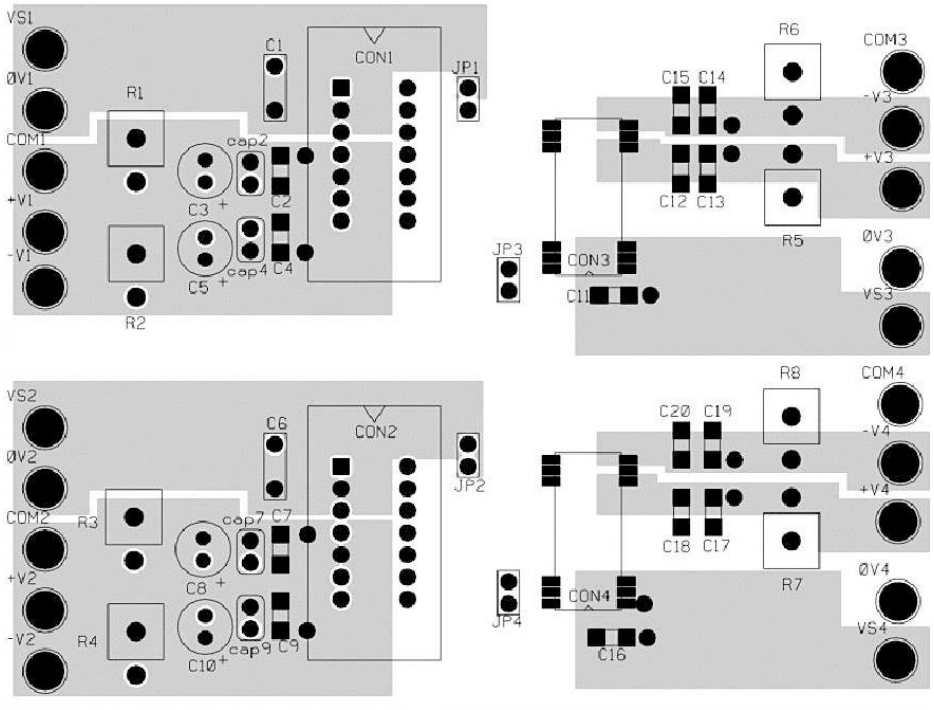


图 10-3. PCB Layout Example, Component-Side View

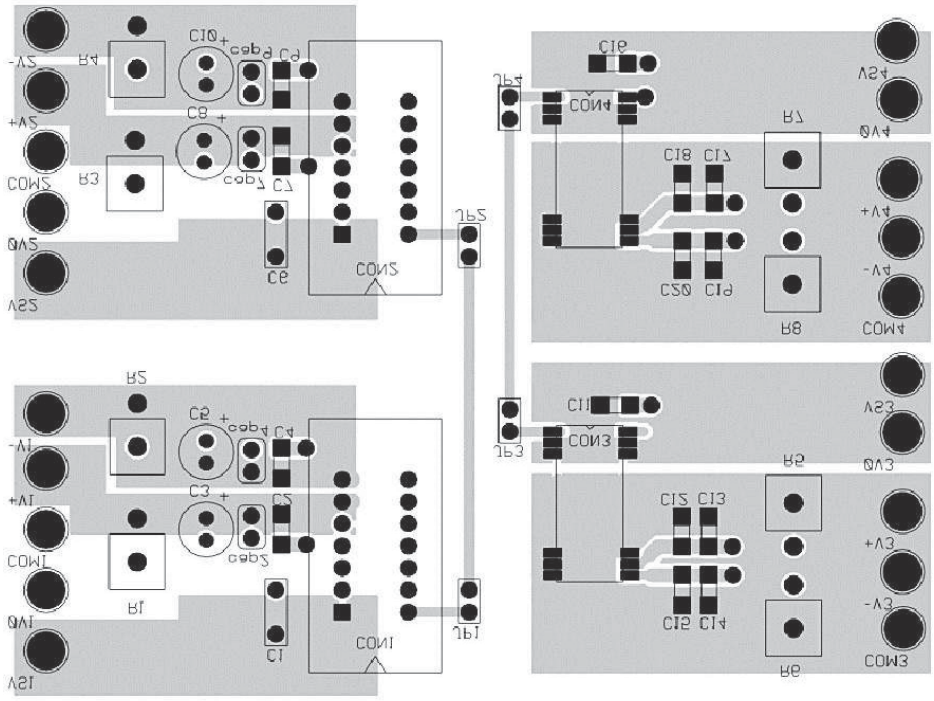


图 10-4. PCB Layout Example, Non-Component-Side View

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

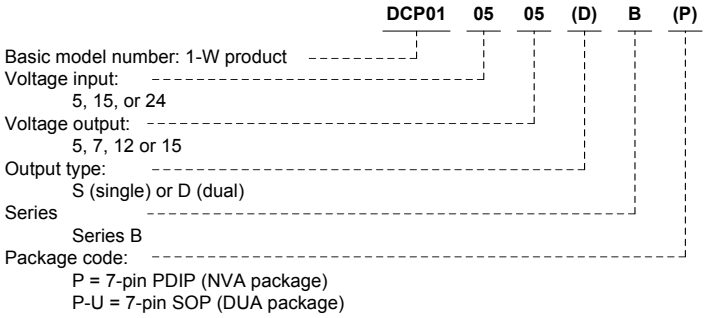


图 11-1. Supplemental Ordering Information

11.2 Documentation Support

11.2.1 Related Documentation

- *DC-to-DC Converter Noise Reduction*
- *External Synchronization of the DCP01/02 Series of DC/DC Converters*
- *Optimizing Performance of the DCP01/02 Series of DC/DC Converters*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP010505BP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010505BP	Samples
DCP010505BP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010505BP-U	Samples
DCP010505BP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010505BP-U	Samples
DCP010505BP-U/7E4	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010505BP-U	Samples
DCP010505BP-UE4	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010505BP-U	Samples
DCP010505DBP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010505DBP	Samples
DCP010505DBP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010505DBP-U	Samples
DCP010505DBP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010505DBP-U	Samples
DCP010505DBP-U/7E4	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010505DBP-U	Samples
DCP010507DBP-U/7E4	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010507DBP-U	Samples
DCP010507DBP-UE4	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010507DBP-U	Samples
DCP010507DBPE4	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010507DBP	Samples
DCP010512BP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010512BP	Samples
DCP010512BP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010512BP-U	Samples
DCP010512BP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010512BP-U	Samples
DCP010512DBP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010512DBP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP010512DBP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010512DBP-U	Samples
DCP010512DBP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010512DBP-U	Samples
DCP010512DBPE4	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010512DBP	Samples
DCP010515BP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010515BP	Samples
DCP010515BP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010515BP-U	Samples
DCP010515BP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010515BP-U	Samples
DCP010515DBP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP010515DBP	Samples
DCP010515DBP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010515DBP-U	Samples
DCP010515DBP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP010515DBP-U	Samples
DCP011512DBP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP011512DBP	Samples
DCP011512DBP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP011512DBP-U	Samples
DCP011515DBP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP011515DBP	Samples
DCP011515DBP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP011515DBP-U	Samples
DCP011515DBP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP011515DBP-U	Samples
DCP012405BP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP012405BP	Samples
DCP012405BP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP012405BP-U	Samples
DCP012415DBP	ACTIVE	PDIP	NVA	7	25	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 100	DCP012415DBP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DCP012415DBP-U	ACTIVE	SOP	DUA	7	25	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP012415DBP-U	Samples
DCP012415DBP-U/700	ACTIVE	SOP	DUA	7	700	RoHS & Non-Green	NIPDAU	Level-3-260C-168 HR	-40 to 100	DCP012415DBP-U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

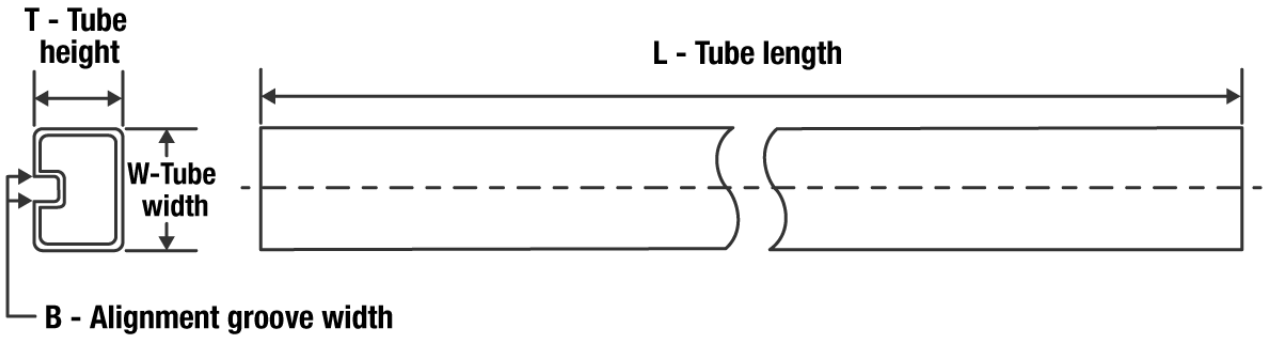
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

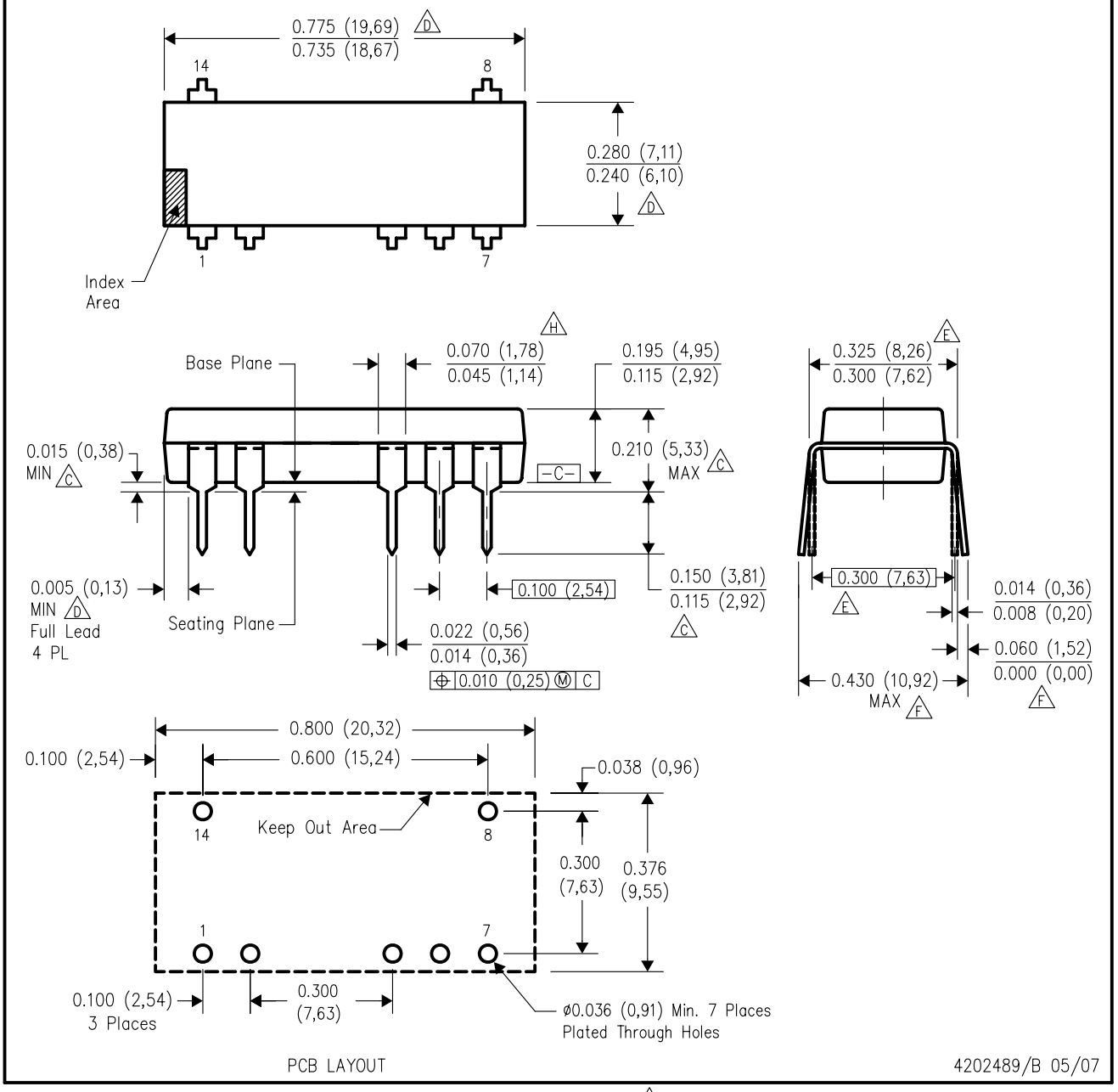
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DCP010505BP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP010505DBP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP010507DBPE4	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP010512BP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP010512DBP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP010512DBPE4	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP010515BP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP010515DBP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP011512DBP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP011515DBP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP011515DBP-U	DUA	SOP	7	25	532.13	13.51	7.36	6.91
DCP012405BP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07
DCP012415DBP	NVA	PDIP	7	25	533.4	14.33	13.03	8.07

NVA (R–PDIP–T7/14) PLASTIC DUAL–IN–LINE

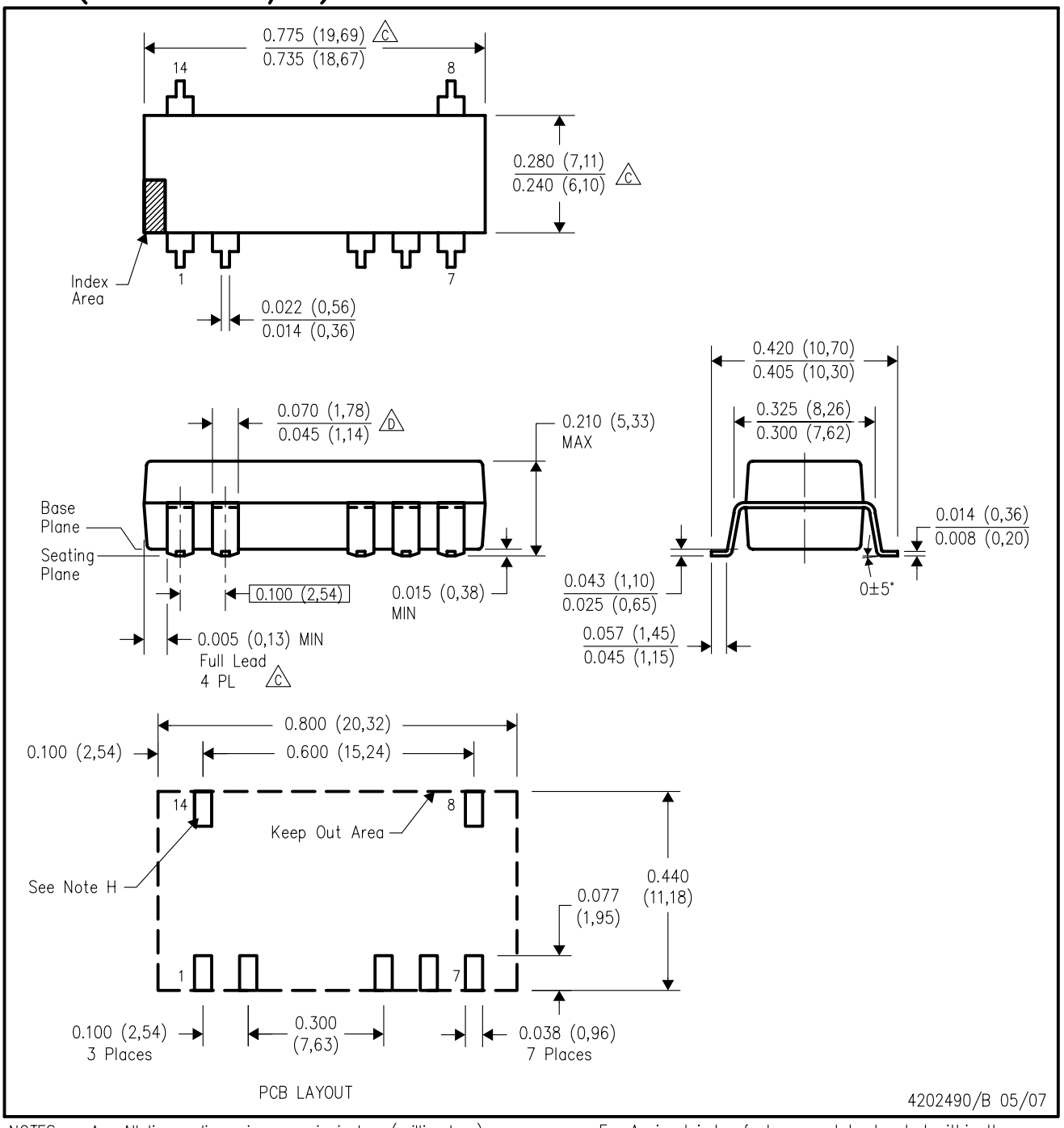


PCB LAYOUT

4202489/B 05/07

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS–3.
- D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- E. Dimensions measured with the leads constrained to be perpendicular to Datum C.
- F. Dimensions are measured at the lead tips with the leads unconstrained.
- G. Pointed or rounded lead tips are preferred to ease insertion.
- H. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).
- I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- J. A visual index feature must be located within the cross–hatched area.
- K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- L. Falls within JEDEC MS–001–AA.

DUA (R–PDSO–G7/14) PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).
- D. Lead shoulder maximum dimension does not include dambar protrusions. Dambar protrusions shall not exceed exceed 0.010 (0,25).
- E. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.
- F. A visual index feature must be located within the cross–hatched area.
- G. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
- H. Power pin connections should be two or more vias per input, ground and output pin.

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