

## 0.6A, 60V, 1.0MHz Step-Down Converter in a TSOT23-6

### DESCRIPTION

The CS5523R is a monolithic, step-down, switch mode converter with a built-in power MOSFET. It achieves a 0.6A peak-output current over a wide input supply range with excellent load and line regulation. Current-mode operation provides a fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown. The CS5523R requires a minimal number of readily-available external components. The CS5523R is available in SOT23-6L package.

### FEATURES

- 0.6A Peak Output Current
- 700mΩ Internal Power MOSFET
- Capable to Start Up with Big Output Capacitor
- Stable with Low-ESR Ceramic Output Capacitors
- Up to 90% Efficiency
- Fixed 1.0MHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over-Current Protection
- Wide 4.5V-to-60V Operating Input Range
- 100% Duty Cycle Low Dropout Operation

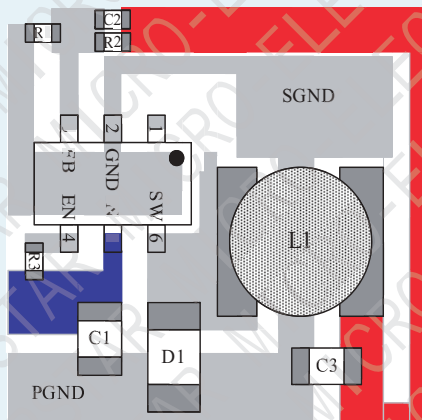
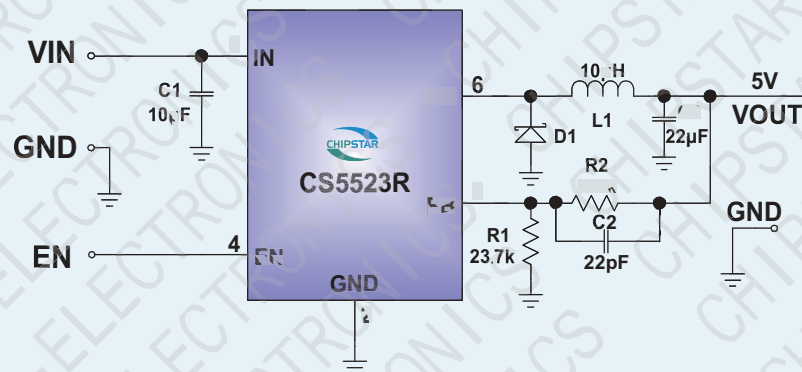
### Package

- SOT23-6L

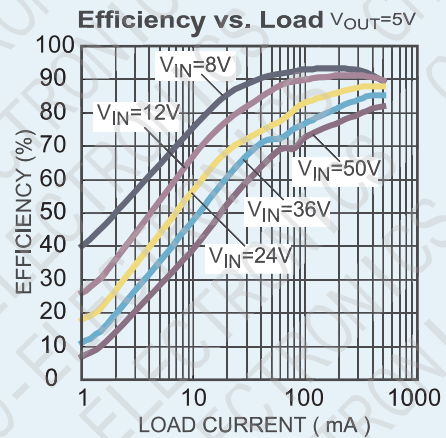
### APPLICATIONS

- Power Meters
- Battery Chargers
- Distributed Power Systems
- WLED Drivers
- Pre-Regulator for Linear Regulators

### TYPICAL APPLICATION CIRCUIT

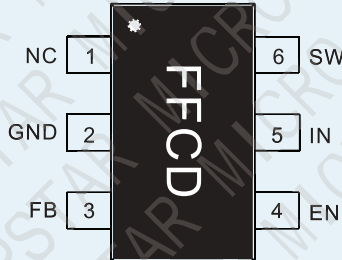


PCB Layout



**PIN CONFIGURATION**

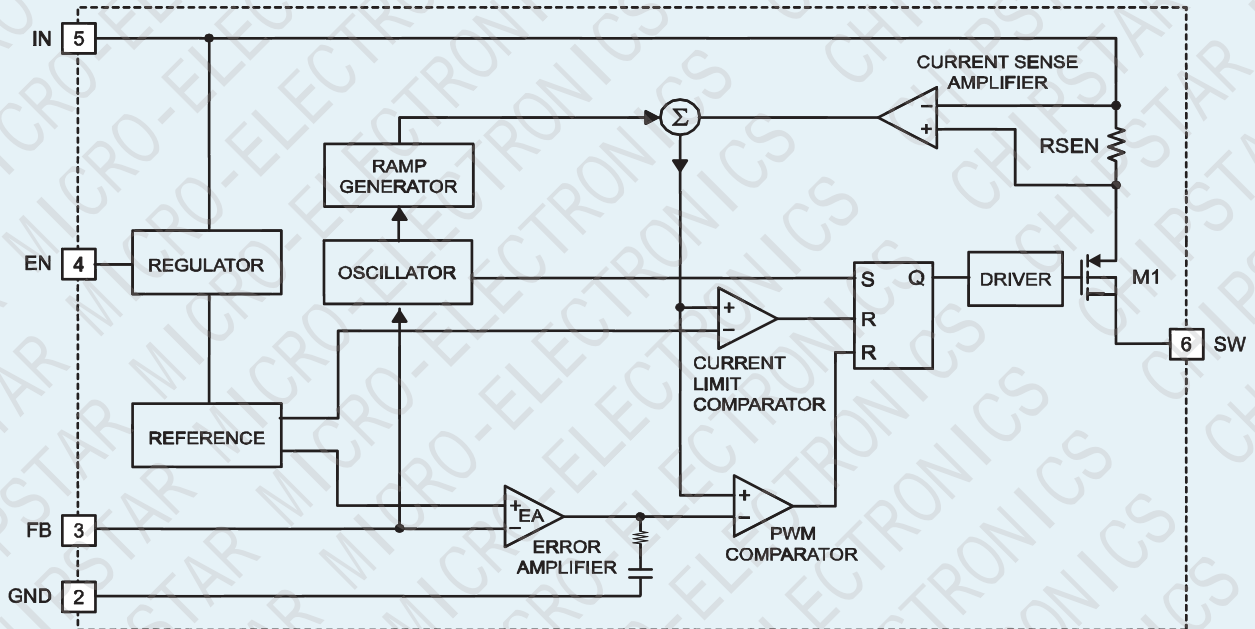
SOT23-6L CS5523R(TOP VIEW)



**PIN FUNCTIONS**

Pin #	Name	Description
1	NC	Not connect
2	GND	Ground. Voltage reference for the regulated output voltage. Requires special layout considerations. Isolate this node from the D1 to C1 ground path to prevent switching current spikes from inducing.
3	FB	Feedback. Sets the output voltage. Connect to the tap of an external resistor divider from the output to GND.
4	EN	On/Off.
5	IN	Supply Voltage.
6	SW	Switch Output.

**FUNCTION DIAGRAM**



Functional Block Diagram


**Absolute Maximum Ratings**

Supply Voltage $V_{IN}$	-----	-0.3V to 65V
$V_{SW}$	-----	-0.3V to $V_{IN}+0.3V$
All Other Pins	-----	-0.3V to +6V
$\theta_{JA}$	-----	180°C/W
$\theta_{JC}$	-----	90°C/W
Mayction Temperature Range	-----	125°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-55°C to 150°C
Mayction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C
ESD HBM(Human Body Mode)	-----	2KV
ESD MM(Machine Mode)	-----	200V

**Recommended Operating Conditions**

Supply Voltage $V_{IN}$	-----	4.5V to 60V
-------------------------	-------	-------------

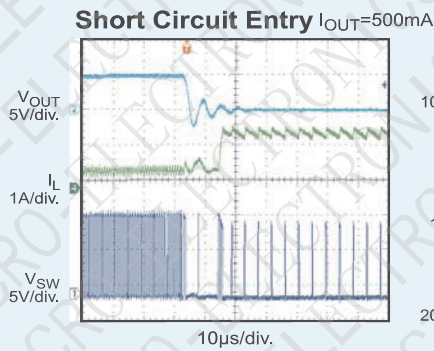
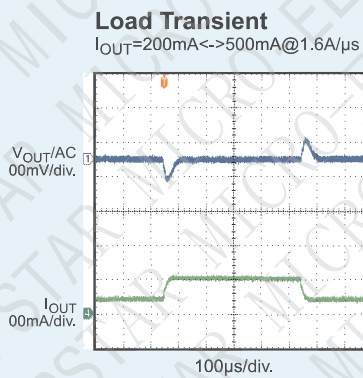
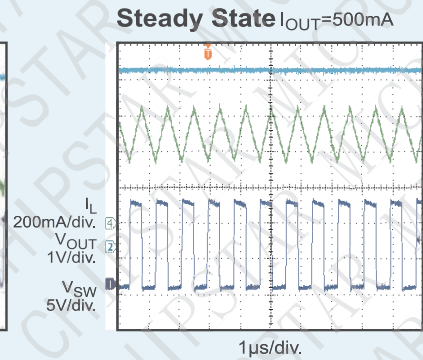
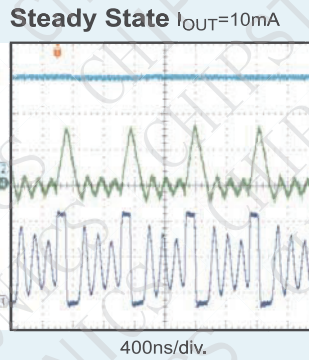
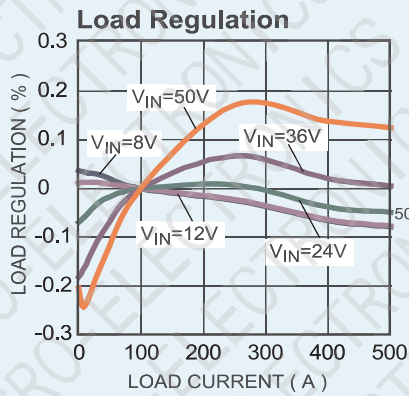
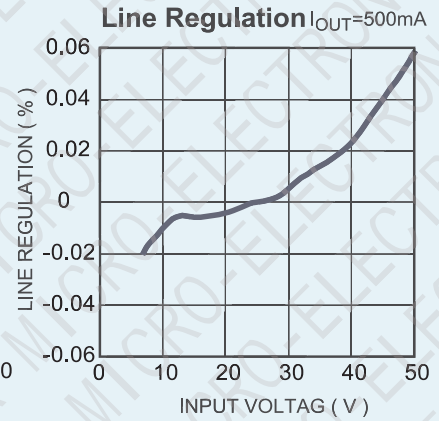
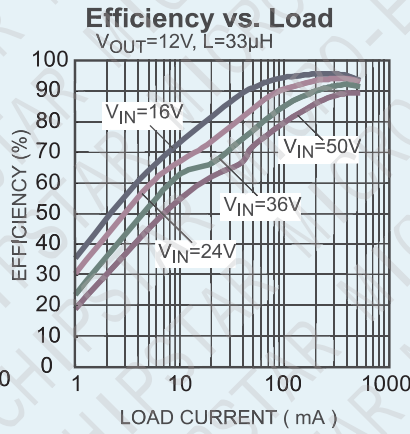
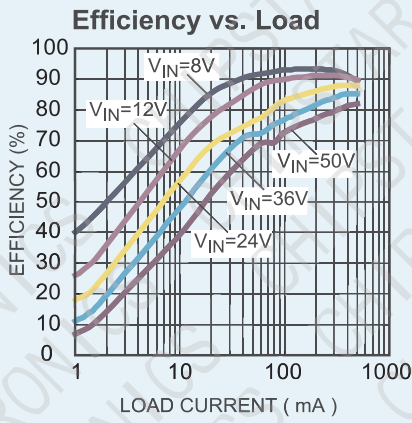
**Order Information**

Device	Package	Making	Reel Size	Tape Width	Quantity
CS5523R	SOT23-6L		7"	8mm	3000

**ELECTRICAL CHARACTERISTICS  $V_{IN} = 12V, T_A = +25^\circ C$ , unless otherwise noted.**

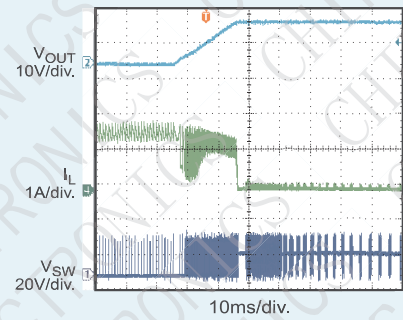
Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	$V_{FB}$	4.5V to 60V	0.792	0.812	0.832	V
Feedback Current	$I_{FB}$	$V_{FB} = 0.85V$			0.1	$\mu A$
Switch-On Resistance R	$DS(ON)$			0.7		$\Omega$
Switch Leakage	$I_{SW\_LKG}$	$V_{EN} = 0V, V_{SW} = 0V$			1	$\mu A$
Current Limit I	$I_{LIM}$			1.0		A
Oscillator Frequency	$f_{SW}$	$V_{FB} = 0.6V$		1.0		MHz
Foldback Frequency	$f_{SW\_F}$	$V_{FB} = 0V$		200		kHz
Maximum Duty Cycle	$D_{MAX}$	$V_{FB} = 0.6V$			100	%
Minimum ON-Time	$\tau_{ON}$			100		ns
Under-Voltage Lockout Threshold, Rising	$V_{UVLO\_R}$			3.65		V
Under-Voltage Lockout Threshold, Falling	$V_{UVLO\_F}$			3.5		V
Under-Voltage Lockout Threshold, Hysteresis	$V_{UVLO\_HYS}$			150		mV
Supply Current (Shutdown)	$I_S$	$V_{EN} = 0V$		2	5	$\mu A$
Supply Current (Quiescent)	$I_Q$	$V_{EN} = 2V, V_{FB} = 1V$		90		$\mu A$
Thermal Shutdown	$SD$			175		$^\circ C$
Thermal Shutdown Hysteresis	$SD\_HYS$			20		$^\circ C$

**TYPICAL PERFORMANCE CHARACTERISTICS**  $V_{IN}=12V, V_{OUT}=5V, L=10\mu H, T_A=25^\circ C$ , unless otherwise noted.



**Short Circuit Recovery**

$V_{IN}=16V, V_{OUT}=12V,$   
 $C_{OUT}=2200\mu F, I_{OUT}=500mA$



## OPERATION

The CS5523R is a current mode buck regulator. That is, the EA output voltage is proportional to the peak inductor current. At the beginning of a cycle, M1 is off. The EA output voltage is higher than the current sense amplifier output, and the current comparator's output is low. The rising edge of the 1.0MHz CLK signal sets the RS Flip-Flop. Its output turns on M1 thus connecting the SW pin and inductor to the input supply.

The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to the Current Sense Amplifier output and compared to the Error Amplifier output by the PWM Comparator. When the sum of the Current Sense Amplifier output and the Ramp Compensation signal exceeds the EA output voltage, the RS Flip-Flop is reset and M1 is turned off. The external Schottky rectifier diode (D1) conducts the inductor current.

If the sum of the Current Sense Amplifier output and the Ramp Compensation signal does not exceed the EA output for a whole cycle, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.81V bandgap reference. The polarity is such that lower than 0.81V FB pin voltage increases the EA output voltage. Since the EA output voltage is proportional to the peak inductor current, an increase in its voltage also increases current delivered to the output.

The CS5523R has 0.6ms internal soft-start. Softstart prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuit generates a soft-start voltage (SS) ramping up with fixed rising rate. When it is less than the internal reference(REF), SS overrides REF so the error amplifier uses SS as the reference. When SS exceeds REF, REF regains control.

When there is extreme big capacitor at output (e.g. 2200uF or even bigger), output voltage would rise slower than SS because the current that needed to charge up the big output capacitor is higher than chip's max output current ability. Current limit would be kicked in the whole startup period until Vo rises to its regulated value.

### Setting Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic). Table 1 lists resistors for common output voltages. The feedback resistor (R2) also sets the feedback loop bandwidth with the internal compensation network. R1 is:

$$R1 = \frac{R2}{\frac{V_{OUT}}{0.812V} - 1}$$

Table 1: Resistor Selection for Common Output Voltages

V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)
1.8	102 (1%)	124 (1%)
2.5	59 (1%)	124 (1%)
3.3	40.2 (1%)	124 (1%)
5	23.7 (1%)	124 (1%)
12	8.2 (1%)	113 (1%)

### Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input supply and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing through the input. Use ceramic capacitors with X5R or X7R dielectrics for their low ESRs and small temperature coefficients. For most applications, a 10μF capacitor will sufficient.

### Selecting the Output Capacitor

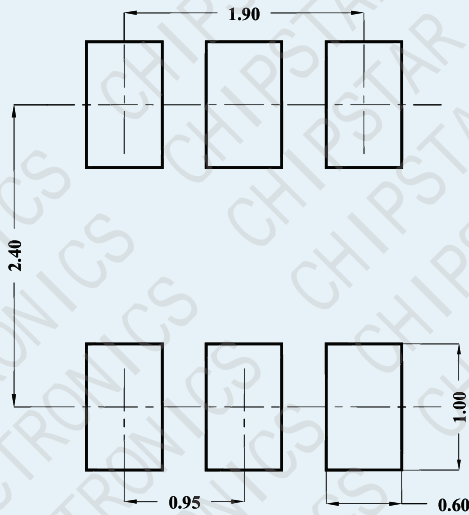
The output capacitor keeps the output voltage ripple small and ensures feedback loop stability. The output capacitor impedance should be low at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics for their low ESR characteristics. For most applications, a 22μF ceramic capacitor will sufficient.

### PCB Layout Guide

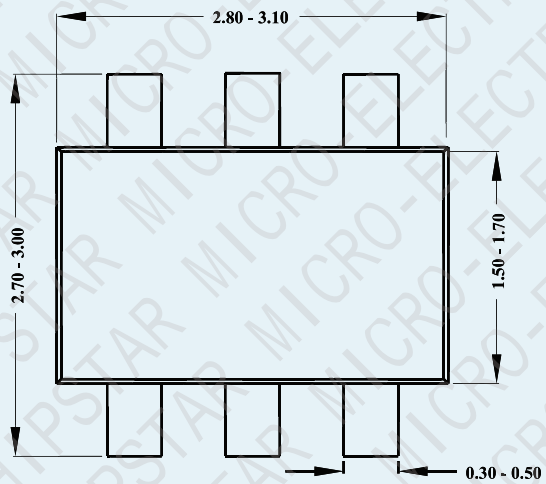
PCB layout is very important to stability. Please follow these guidelines and use Figure 2 as reference.

- 1) Keep the path of switching current short and minimize the loop area formed by the input capacitor, high-side MOSFET, and Schottky diode.
- 2) Keep the connection from the power ground→Schottky diode→SW pin as short and wide as possible.
- 3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
- 4) Route SW away from sensitive analog areas such as FB.
- 5) Connect IN, SW, and especially GND to large copper areas to cool the chip for improved thermal performance and longterm reliability. For single layer PCBs, avoid soldering the exposed pad.

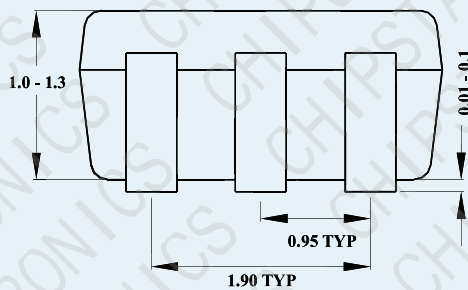
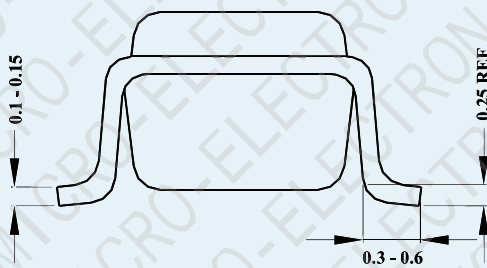
**Package Information**  
 SOT23-6L Package Outline & PCB Layout



**Recommended Pad Layout**



**Top View**



**Notes: All dimension in MM**  
**All dimension don't include mold flash & metal burr**